TWO WAY POWER FLOW USING GTO THYRISTORS

MOHAMAD HUSSEIN TAHA

Doctor of Philosophy

THE UNIVERSITY OF ASTON IN BIRMINGHAM

August 1992

ACKNOWLEDGEMENTS

I would like to express my sincere thanks to my supervisor the late Mr. B. James and to my adviser Mr. L. Babad for all their advice, suggestions and help. I would also like to thank Professor W. T. Norris who has recently assisted with the supervision of the project.

I am grateful to Mr. B. Harrison and Mr. L. Radford for all their help with the laboratory work.

A special mention must go to my sponsors the Hariri Foundation who are entirely responsible for the funding of this project.

I would like to express my thanks and love to my wife Sonia for her help, encouragement and support. My love and thanks also to my children Sophia, Miriam and Hussein. Finally, my thanks and love to all my family in Lebanon for their moral support throughout my studies.

LIST OF CONTENTS.

LIST OF SYMBOLS

α, β	Rectifier firing angles.
α(pnp),(αnpn)	Transistor current amplifications.
CSI	Current source inverter.
C_S	Snubber capacitor
D_F	Free-wheeling diode.
D_S	Snubber diode.
E_d	Centre tap inverter input voltage.
I_A	GTO anode current.
I_{DC}	Rectifier output current.
I_{FG}	GTO forward gate current.
I_{GQ}	GTO reverse gate current.
$I_{G(on)}$	GTO on-state gate current.
I_L	Mean load current.
I_T	GTO on-state current
I_{TAIL}	GTO tail current.
f	Frequency.
L_x	Stray inductance.
P.F.	Power factor.
P_{mean}	Mean power.
P.S U.	Power supply unit.
R_S	Snubber resistor.
Q_{GQ}	GTO turn-off gate charge.
V_{AK}	GTO anode-cathode voltage.
V_D	GTO continuous direct off-state voltage.
V_{DC}	Rectifier output voltage.
V_{DM}	GTO turn-off voltage.
V/F	Voltage to frequency converter.
V_m	AC maximum voltage.
V_{DP}	GTO peak forward transient voltage.

V_{RG}	GTO reverse gate voltage.
W_S	Snubber energy.
t_d	Delay time.
t_{gf}	Fall time
t_{gs}	Storage time
t_r	Rise time.
T,TR	Transistor.
t_q	Thyristor turn-off time.
μ	Operational amplifier gain.
η	Efficiency.
01	Zero level of the oscilloscope Channel 1.
02	Zero level of the oscilloscope Channel 2.
03	Zero level of the oscilloscope Channel 3.
04	Zero level of the oscilloscope Channel 4.
01,2	Common zero of the oscilloscope Channels 1 and 2.
03,4	Common zero of the oscilloscope Channels 3 and 4.

CHAPTER ONE

LITERATURE SURVEY AND RESEARCH LAYOUT

1-1 INTRODUCTION.

There are many industrial applications that require bidirectional power transfer between two systems and there are a number of methods by which this is currently performed. Before starting with a survey of these methods, it is important to give a simple explanation of reversal of power flow within the power electronics area.

The simplest system to demonstrate the idea of bidirectional power flow is perhaps the single phase fully controlled line commutated thyristor converter. This type of converter has the advantage that its power control switching devices can be commutated by its own voltage supply without any additional external circuit or commutation function (1). Figure (1-1-a) shows a single phase fully controlled thyristor converter with a highly inductive load. The converter also contains a voltage source (E) which may be reversed, depending upon the required operation of the converter.

The DC output voltage equals:

$$V_{dc} = \frac{1}{\pi} \int_{\alpha}^{\alpha+\pi} V_m \sin\omega t \, d(\omega t) \qquad (1\text{-}1)$$

Where α is the firing-angle of the thyristor, measured from the natural commutation point. For a single phase system, α measured from the zero crossing of each half cycle of the input supply voltage. The firing angle α can be varied from a small value to almost 180 degrees. Up to a delay of 90 degrees, the voltage source is connected in the direction of the full arrow (refer to figure (1-1), the converter operates in rectification mode and the power flows from the supply to the load. The DC output voltage and current are positive. If the firing angle increases beyond 90 degrees and

the voltage source is reversed as shown by the dotted arrow, the DC output voltage will be negative but the current remains positive. There will be a reverse power flow from the load to the supply and the converter will operate in the inversion mode (1-8).

If a DC machine is used as the load element, it acts as a motor while the converter is rectifying. When the firing angle increases beyond 90 degrees, the DC machine acts as a generator, but since the current direction cannot reverse, the machine can only generate by having its armature or field connections reversed (2).

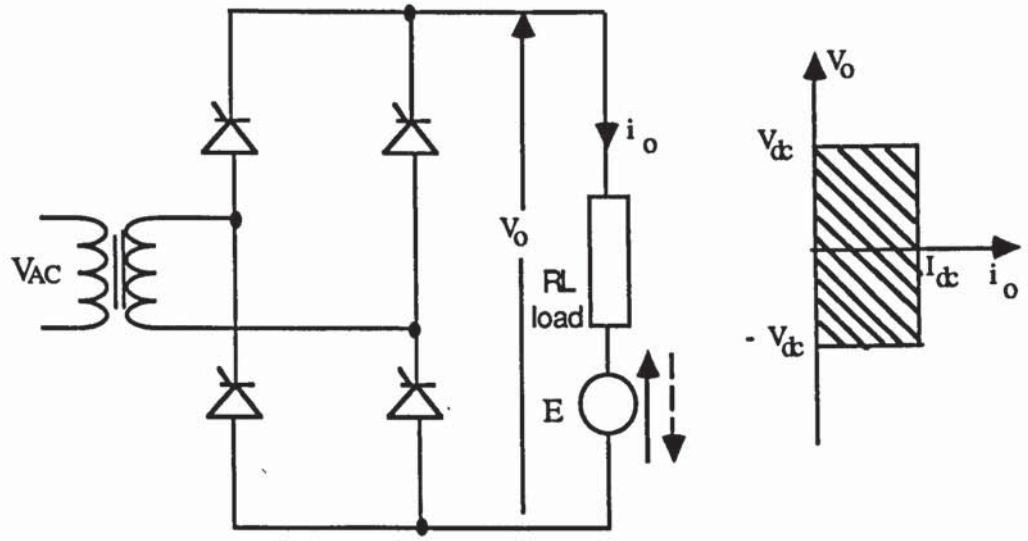
If two full converter bridges are connected back to back as shown in figure (1-1-b), the output voltage and current can be reversed. The system will provide four-quadrant operation and is called a dual (3) or double (4) converter. The firing angles are controlled so that one converter operates as a rectifier and the other operates as an inverter. Dual converters are normally used in high power variable drives and in HVDC.

There are several problems in the use of this type of converter (1,9-12):

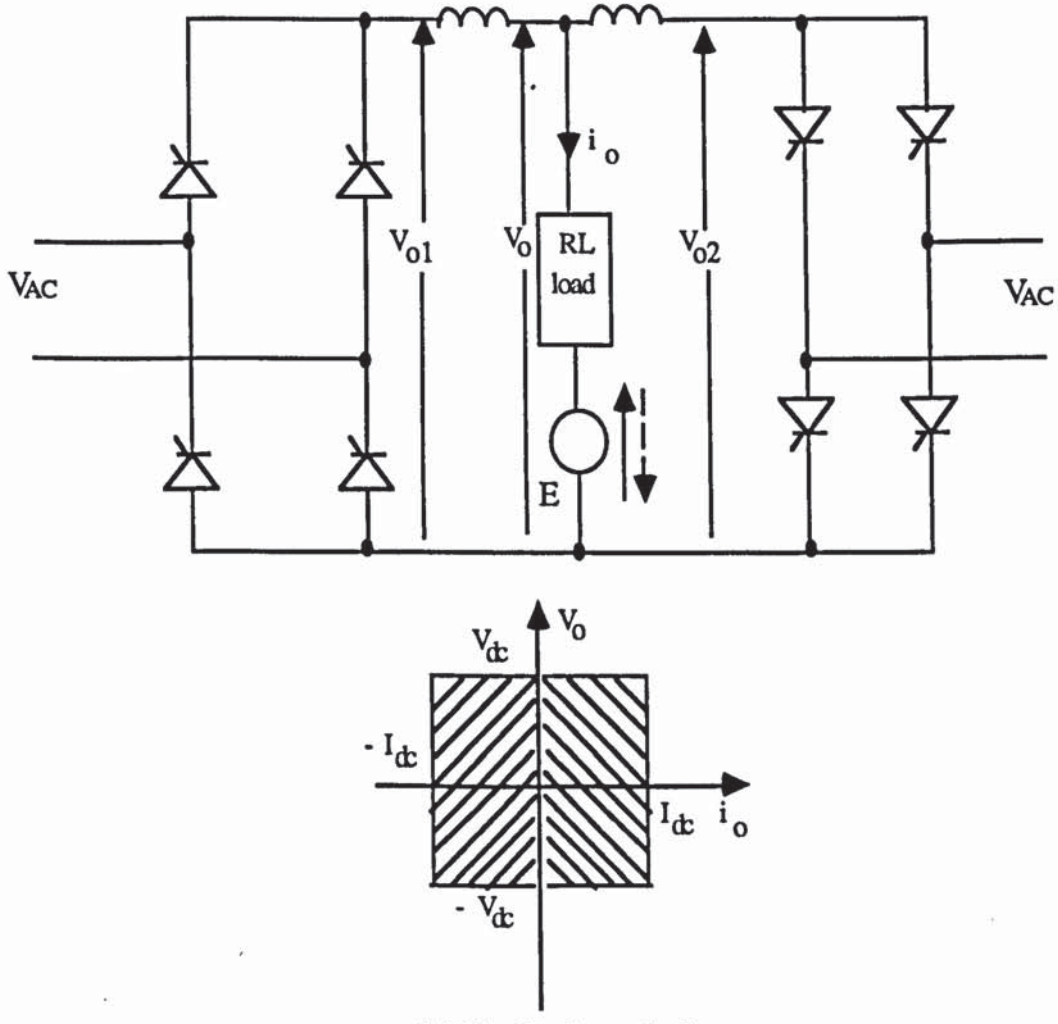
a) The power factor decreases as the firing angle increases.

b) The harmonics of the line current are relatively high.

In this chapter some of the published work for tackling the above problems is discussed. The advantages and layout of the author's research is presented at the end of the chapter.



(a) Single phase converter.



(b) Single phase dual converter.

Figure (1-1)Fully controlled bridge converters.

1-2 A BI-DIRECTIONAL AC-DC POWER CONVERTER.

A forced commutated AC-DC converter is able to draw nearly sinusoidal current at unity power factor and power exchange between the AC line and DC load or vice-versa by reversal of the direct current (10-13).

Recent evolution of power devices with high frequency switching such as the bipolar transistor, MOSFET and GTO have made possible the use of PWM to serve the above purposes. A number of papers on the three-phase controlled current PWM rectifier have reported on its capability for fast power reversal while feeding near sinusoidal input current with unity power factor (14,15).

In the past decade, great progress has been made in switching mode converters (16,17). Among these, the conventional and most widely used is perhaps the sinusoidal PWM switching mode converter (16). This converter is simple in construction, but has the disadvantage of having high voltage switching transients and losses (18).

Recently, converters based on the current forced switching control technique have been developed (19,20), in which the device can be operated with a sinusoidal line current, unity power factor and a regulated busbar voltage in the converter mode. In references (10) and (11-13) respectively, single-phase and three-phase converters have been presented. PWM is employed for rectification and inversion modes. Figure (1-2) shows a single phase GTO converter; between the mains and the input of the converter there is an inductor. The fundamental component of the AC voltage waveform developed by the converter (E_C) is adjustable in magnitude and phase with respect to the AC mains (V_S) (10). The direction of the power flow is dependent on the magnitude and phase between the two voltages (13). The detail of the control circuit is not explained here, however the above references reported that with PWM control techniques for rectification and inversion modes, reversal of power flow

between AC and DC side can be achieved with unity power factor and a sinusoidal input current.

In references (18-21), a current-forced hystereris switching control technique with a forced commutated converter has been used. The configuration is similar to figure (1-2). In the rectifier mode of operation, the input AC current is forced to track a sinusoidal reference waveform. When the input current is less than the reference current, the magnetic energy in the inductor must increase and this can be achieved by circulating the input current between a diode and a controlled device. When the input current is higher than the reference current, the incremental magnetic energy stored in the inductor is released to the load via the antiparallel diodes. The reference current is synchronised with the utility voltage source and this always gives a unity power factor. In the case of inverter operation, the devices will operate differently to the rectifier mode. Thus a sinusoidal output voltage waveform can be obtained. The above references reported reversal of power flow between the AC mains and DC load with unity power factor.

In reference (22), simulation of a three phase bi-directional power flow system using GTOs has also been reported. The authors of the paper concentrated their study on the system harmonics. Reference (22) reports that the use of a forced commutated converter creates a harmonic spectrum better than the line commutated one.

In references (23) and (24), a three phase PWM AC to DC converter using thyristors as switching devices has been discussed. The main disadvantage of this system is the requirement of a commutation circuit for each thyristor.

However the main disadvantage of the work described in the above references is that, it is difficult to control the power factor in cases when the system needs to operate at leading or lagging power factors.

1-3 BI-DIRECTIONAL AC-AC POWER FLOW.

In any AC-AC system, static power converters constitute an interface between the mains and the load, usually an induction machine is used as the load element. The static power converters adapt and control the energy flow to provide AC power at the input of the machine. The conversion of AC-AC could be passed through two stages AC-DC and DC-AC converters (AC/DC/AC) or one stage AC-AC converter, some applications of these types of conversions are presented in the following sections.

The rectifier stage of the AC/DC/AC converters, consists of an uncontrolled diode bridge or, less frequently, of a phase controlled thyristor converter. This results in a high harmonic content in the input AC line current and gives an input power factor which is dependent on the phase angle of the rectifier. The other disadvantage of this type of converter is that when the motor is regenerating, the stored energy is being returned to the DC link. This raises the DC link voltage by increasing the charge on the DC link capacitor. Unless this energy can be returned to the fixed frequency source using a converter in the inverting mode, regeneration is very limited. The energy can be dissipated in a braking resistor placed across the DC link and this is a form of dynamic braking (2). These two methods of braking are illustrated in figure (1-3). The disadvantage of the regenerative inverter configuration is that three different converters with two different units are needed. In the case of the braking resistor, there is wasted energy especially with high power induction motors.

Different techniques for AC-AC bi-directional power flow have been used. References (26-29) used a configuration called a matrix converter which is shown in figure (1-4). The nine switches in this circuit are arranged in a "matrix", and are switched sequentially and cyclically, such that any phase of the three-phase input can be connected to any phase of three-phase output, with either polarity of the voltage input or current output. The switches are assumed to have bi-directional voltage blocking ability as well as bi-directional current conduction and turn-off capability (25). A conventional bipolar junction transistor inside a bridge diode, or an inverse

parallel connection of transistors could be used as a switch element of the system of figure (1-4). It has been shown by Venturini (27-29) that with the proper switching algorithm, the matrix converter is capable of operating at lagging, unity, or even leading power factor at a variable frequency. Four-quadrant operation can be obtained with this type of converter, i.e., motor or generating operation with either leading or lagging current.

The distinguishing feature of this converter is the complete absence of a DC link. No energy capacitor or inductor is needed to support the link voltage or current. However, relatively small capacitors will generally be needed to isolate the converter from the inevitable inductance of the supply.

The main disadvantages (25) of this converter are:

a) The high device losses and the device cost have so far prevented this converter from having much of an impact on the converter market.

b) The output voltage is limited to 1/2 the input voltage.

c) The switching instants must be carefully controlled; since current spikes could occur in the switch currents if overlap exists between gating signals, while a voltage spike could occur across the switch if a gap exists between switch gating signals.

Another technique used in references (30-32), is a DC link current converter utilizing PWM technique for both the input and output bridges. The configuration is shown in figure (1-5). The implementation of the PWM techniques requires gate turn-off switching devices such as bipolar transistors, MOSFETs or GTOs to be used as unilateral switches (33). This configuration comprises a converter section to convert the constant frequency AC power from the commercial power source to DC power, a reactor to smooth the DC current and an inverter section to convert the DC power to the variable voltage variable frequency AC power (30). The capacitors are connected to both input and output sides to absorb the overvoltages which occur when the switch current cuts off. Sinusoidal current can be derived at both the input and

output lines and four-quadrant operation is readily obtained by simply reversing the polarity of the DC link voltage. This type of converter is used with a medium power (several hundred horse power) level but is not generally favoured because of the expensive and bulky passive components (33).

The three-phase current-controlled PWM rectifier/inverter DC voltage link shown in figure (1-6) has been reported in references (34-35). The current-controlled PWM converter merits attention due to its ability to deliver near sinusoidal currents at unity power factor. In addition the converter permits bidirectional DC current flow without the need for dual converters. In this configuration, both the rectifier and the inverter are identical. The current in each phase tracks a reference current waveform. Under the rectification mode of operation, the current path is preponderantly through the diodes, and under the inverter operation the current flows preponderantly through the forced commutated devices. Reference (36) used the same control technique but with a single phase system which can be useful to drive an AC traction motor from a single phase supply. Although a reversal of power flow with unity power factor was achieved with this type of converter, the main disadvantage is that, it is difficult to control the power factor in case the system needed to operate at leading or lagging power factors.

It is also possible to utilize a dual PWM converter for a resonant AC/DC link converter to achieve a reversal of power flow with unity power factor as has been mentioned and discussed in references (37-42). The advantage of these converters compared with the conventional DC voltage or current link converters is that the devices can operate without snubbers and with very little heat sinking. This is due to the zero voltage switching.However, the size and cost of the link inductor and capacitor are major inhibiting factors.

1-4 RESEARCH LAYOUT.

The previous sections outlined the many techniques which are used to reverse power flow between AC and DC or AC and AC systems. Nearly all the references used an antiparallel diode with a forced commutated device for each converter arm. It was mentioned that the main disadvantage of the schemes of these references is the difficulty of controlling the power factor in case the system is needed to operate at leading or lagging power factor. However a new system using GTOs thyristor was built and studied for reversing the power flow in both directions. The main difference with the new system is that two antiparallel GTOs are used instead of a diode and a GTO. The advantages and disadvantages of the system is discussed at the end of this section.

Originally the idea of the project was to build a three-phase system containing two GTOs converters connected in series, with each converter containing 12 antiparallel GTOs. However, due to lack of time and practical difficulties such as late delivery of components, the project was modified to a single-phase system as shown in the block diagram of figure (1-7). Two single phase converters are connected in series. Each converter contains 8 antiparallel GTOs. When power flows from side (A) to side (B), S_1 closes and the AC mains supplies converter (A). This operates as a rectifier, by switching $GTOs_{(A2)}$ on as controlled devices and switching $GTOs_{(A1)}$ off. The output of rectifier (A) supplies the input of converter (B), which operates as an inverter. This can be achieved by switching $GTOs(B_2)$ continuously on, thus operating them as diodes and switching $GTOs(B_1)$ on to carry the inverter current. S_2 must turn-off, to disconnect the supply from converter (B). The power from inverter (B) is fed to the load. When power flows from side (B) to side (A), converter (B) operates as a rectifier and converter (A) operates as an inverter. There is a switch at the input of each converter, since there is no synchronization between the system and the mains. This was due to the shortage of time which prevented synchronization the output of each converter with the mains.

The main objectives of the project were to study and investigate the reversal of the power flow between the two converters under steady-state and transient conditions and to investigate and control the rectifier power factor.

A brief outline of the various stages of the work is presented below.

a) An amount of time was spent to design and study a GTO drive circuit. Later some time was spent learning the technique for designing a PCB for the GTO gate drive. The work was done in the university laboratory using a computer software package called a 'Smartwork PCB draughting software'. The design, diagrams and explanations of the gate drive circuit and the switching behaviour of the GTO used in this research are shown in Chapter 2.

b) A small system of about 100 W rating was designed and built to study and investigate the reversal of power flow between two units. The design and results of the system are presented in Chapter 3.

c) As mentioned at the beginning of this chapter, one of the objectives of the system was to control the rectifier power factor. The author designed a rectifier control circuit which gave the choice of operating the system with either leading or lagging power factor. The full details of this circuit and the system control circuit are presented in Chapter 4.

d) The complete system was assembled in a single framework which was designed in the department and photographs of this are shown in Chapter 4.

e) Before testing and reaching the final stage of the project, some problems were encountered, such as inrush current into the filter capacitor and transient voltages at the input to each converter. These problems, together with the experimental results are discussed in Chapter 5.

The advantages of this configuration are:]

a) The rectifier power factor can be controlled.

b) The power flow can easily be reversed; it has been found that the GTO can easily be transferred from a controlled device to a diode (always on).

The main disadvantage of this configuration is the switching losses of the devices. As shown in figure (1-7) there is a diode in series with each GTO, due to the fact that this type of GTO has a very low reverse voltage blocking capability and the need for series diodes stemmed from the non-availability of symmetrical GTOs .

The system can be operated in four-quadrants and can be used for a variable speed drive or to link two systems with different frequencies.

Finally, there is further work to be done on this research topic and this is discussed in the conclusions in Chapter 6.

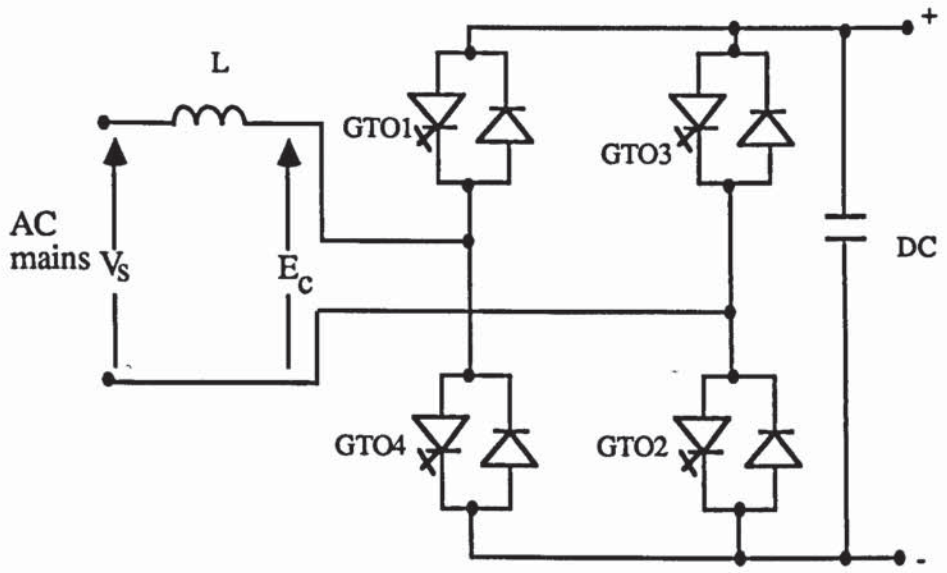


Figure (1-2) Single phase converter circuit

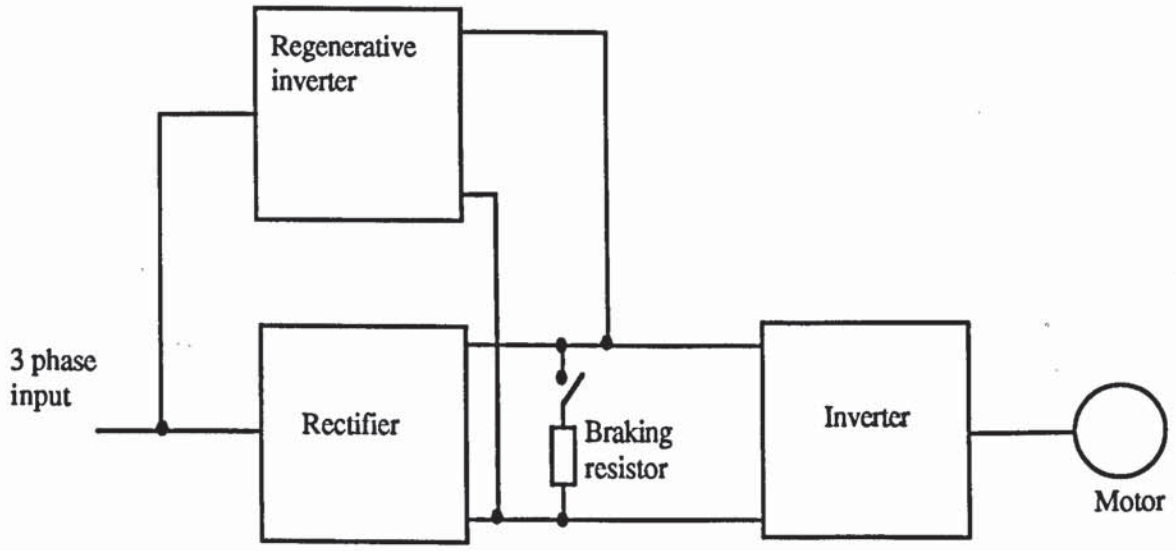


Figure (1-3) Induction motor regenerative braking.

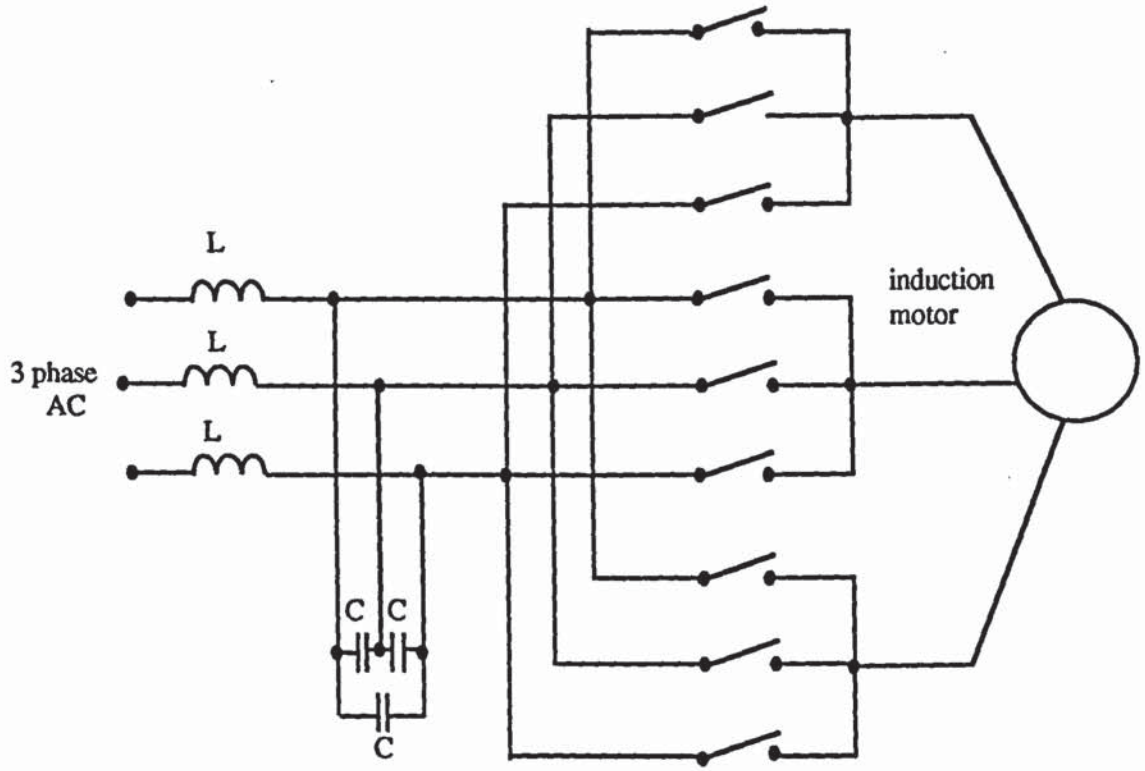


Figure (1-4) Matrix converter.

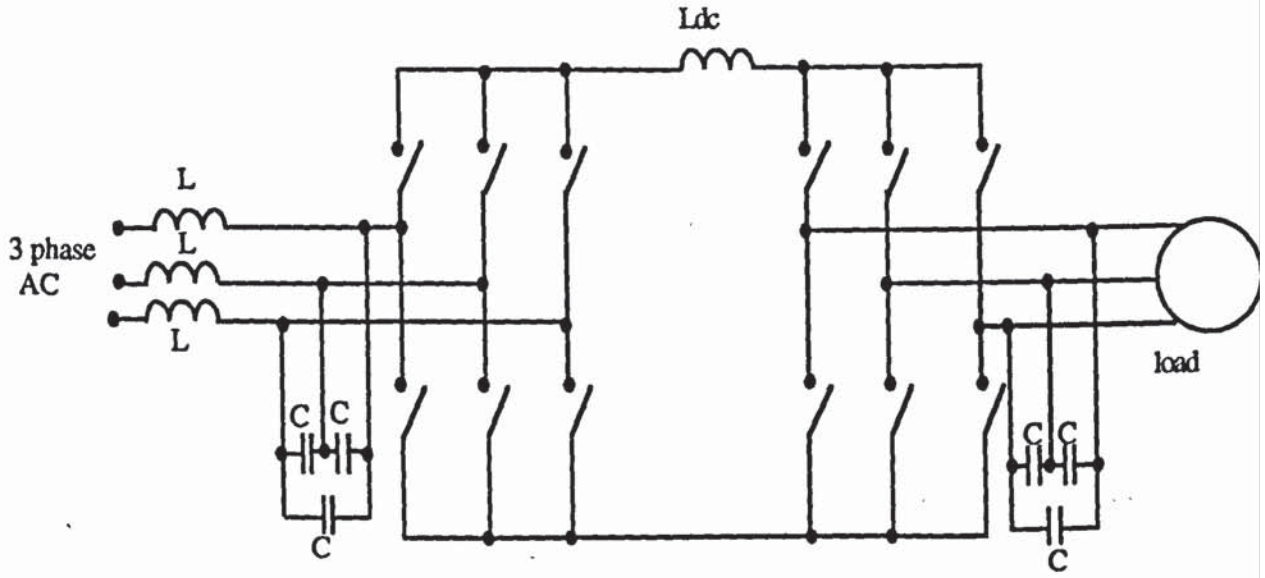


Figure (1-5) PWM current source inverter.

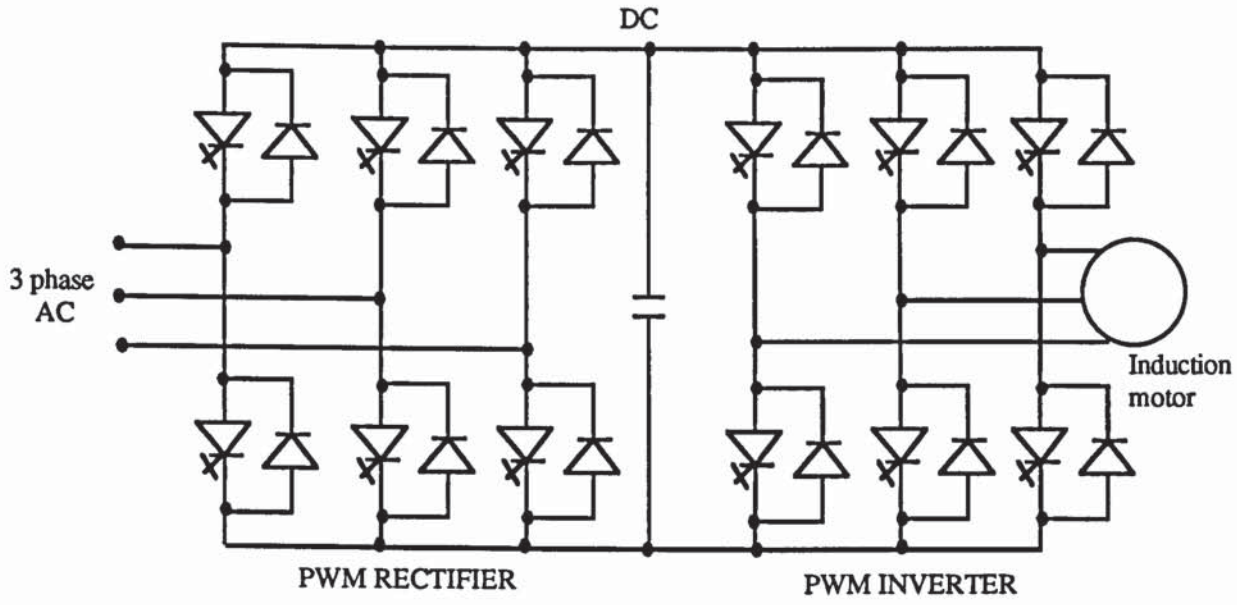


Figure (1-6) PWM-rectifier-PWM-inverter drive of an AC machine.

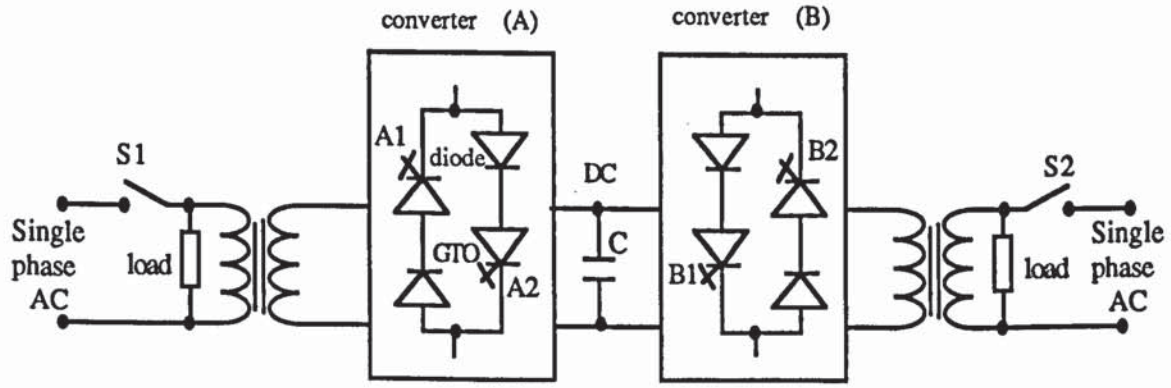


Figure (1-7) AC-AC converters using GTOs.

CHAPTER TWO

THE GTO THYRISTOR

2-1 INTRODUCTION.

Recent developments in power semiconductor devices have yielded new and efficient controllable switches like the gate turn off thyristor (GTO) which is able to handle a higher blocking voltage compared with a power transistor and has the additional advantage of gate turn-off capability, eliminating the need for commutation circuits which are used with conventional thyristors.

The construction of a GTO is similar to that of a conventional thyristor. It has a three terminal, four layer pnpn structure, which can be explained in terms of a two transistor model as shown in figure (2-1-a). This is a regenerative arrangement, in which the collector current of one transistor supplies the base drive for the other transistor (43,44). Once the thyristor is turned on, it cannot be turned-off. Thus the off-state cannot be restored by the gate signal.

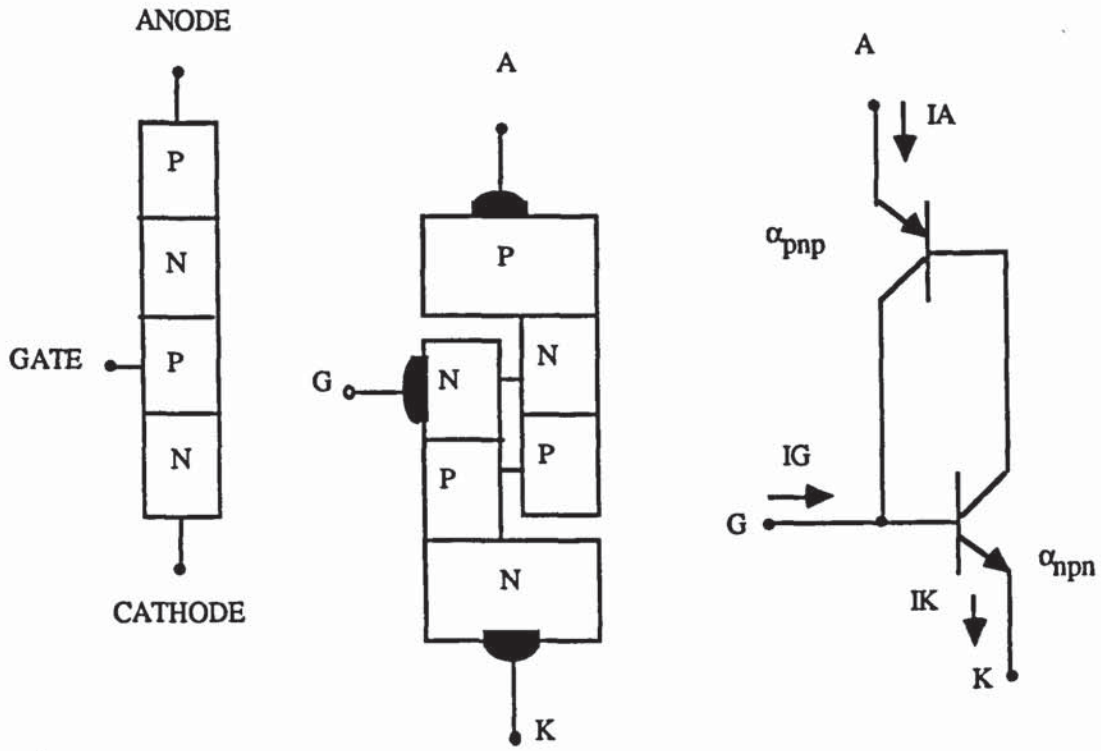
The GTO thyristor can be turned-off by extracting sufficient current from the gate to cause the loop gain to fall to a point where the regenerative action ceases. This can be obtained by making α(npn) relatively large and α(pnp) small. The current amplification factor α(pnp) of a GTO is lower than that of a conventional thyristor. Two methods are used to control α(pnp); the diffusion of heavy metal as a life time killer and an anode-emitter short-circuit.These are shown in figure (2-1-b-c). In the heavy metal doping technique, the n_1 region is doped with metal, such as gold, in order to reduce the lifetime of minority carriers (43,45,47).

The anode emitter shorting technique results in a device with a very low reverse voltage blocking capability. As can be seen in figure (2-1-c), the only junction capable of blocking reverse voltage is junction J_3, since J_1 has been shorted out. A

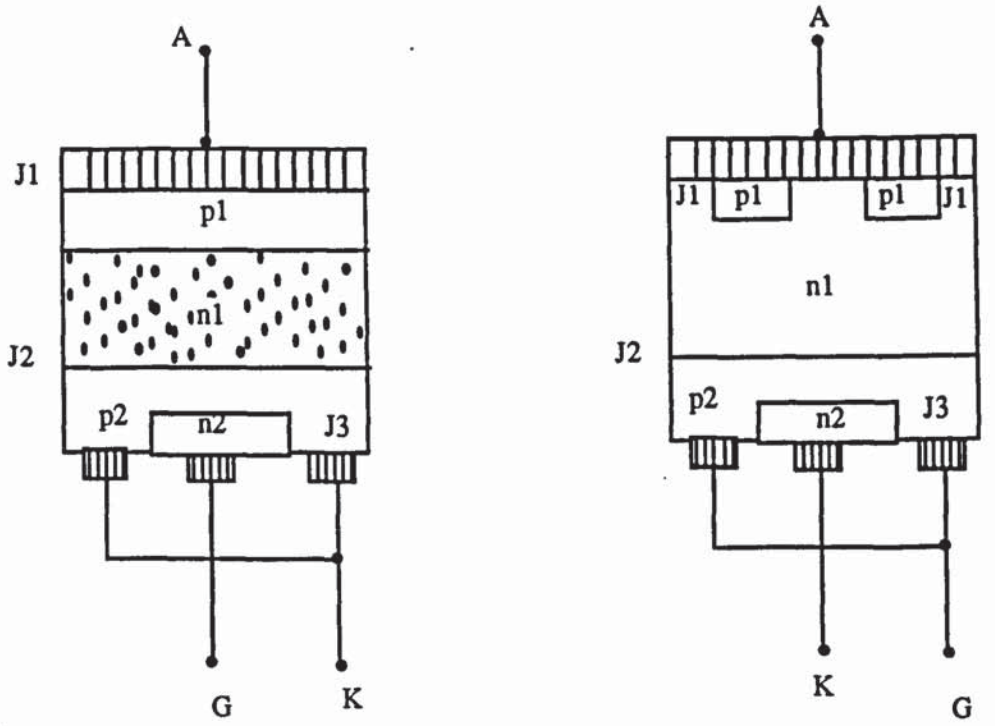
GTO with heavy-metal doping for minority carrier lifetime control has an on-state forward voltage drop of 10-15% greater than that obtained with a GTO using anode emitter shorting. However, its reverse voltage blocking capability is much greater since junction J_1 is available to block reverse voltage as shown in figure (2-1-b) (45).

The Marconi GT224K GTO, was chosen for the research for the following reasons. Firstly a full data sheet for the device was provided by MEDEL and secondly, the device was offered to the department at a very reasonable cost. The data sheet of the GTO is given in appendix (A).

This chapter will improve the understanding of the switching behaviour of a GTO thyristor and the operation and design of both snubber and gate drive circuits. An inverter circuit as illustrated in section (2-6) of this chapter was used for this purpose.



Two Transistor model (a)



(b) Heavy Metal Doping

(c) Anode Emitter Shorts

Figure (2-1) GTO Construction.

2 -2 TURN-ON CHARACTERISTICS.

A GTO thyristor is a latching device. Once the anode current reaches a certain latching value, the device will go into full conduction (50-53). The total turn-on time is the sum of the delay time (t_d) and the rise time (t_r) as defined in figure (2-2) . Table (2-1) shows the terms and definitions for each symbol of the GTO switching waveforms. The turn-on time depends on the characteristics of the device as well as the rate of rise and the amplitude of the gate current .

To accomplish fast turn-on, a steep rise and a large value of gate current are required. The values depend on the size and the rating of the device and are usually specified by the manufacturer.

The power loss is comparatively low during the delay time because the anode current at this stage is still low. Maximum turn-on power losses are incurred during the rise time when the load is resistive with no di/dt limiting inductance in the circuit (50-55).

2-3 TURN-OFF CHARACTERISTICS.

The on-state anode current can be turned-off by applying a negative gate bias to the gate-cathode junction of the GTO (50,53). The turn-off time is defined as the sum of the storage time (t_{gs}), the fall time (t_{gf}) and the tail time (45,53,56) as defined in figure (2-2).

The initiation of a negative gate voltage causes negative gate current to start to flow. The rate of rise of this current is controlled by the value of the turn-off voltage and the gate circuit inductance (51,57).

During the storage period, anode current (I_A) and device voltage (V_{AK}) remain constant. The switching power losses in this period are comparatively small. The duration of the storage time depends on how rapidly the excess charge (Q_{GQ}) is removed from the P-base of the GTO. The termination of the storage time usually occurs when the gate current reaches a maximum value (53,57).

When the excess charge is removed, the centre junction of the GTO comes out of saturation. The anode current starts to fall rapidly and the anode voltage rises to V_{DP}. The anode voltage continues to rise at a linear rate until it reaches V_{DM}. There is further explanation about V_{DP} and V_{DM} in section (2-4).

After the fall time the anode current goes to a low value I_{TAIL}, which decays more slowly, the duration of this time depends upon the characteristics of the device (53,48). The tail time is an important factor for switching power losses since the anode voltage is high at this time.

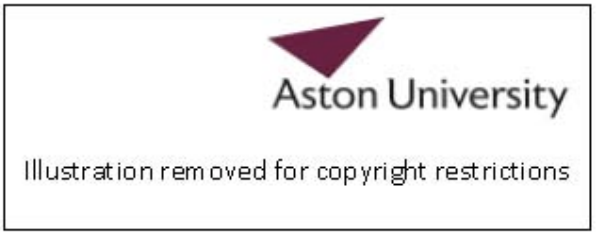


Figure (2-2) GTO general switching waveforms.

(waveforms taken from MEDL data)

Symbol	Term	Definitions
dV/dt	Critical rate of rise of off-state voltage	The minimun value of rate of rise of off-state voltage to cause switching from off-state to on-state.
I_{FG}	Forward gate current	The peak value of forward gate current at turn -on.
I_{Gon}	On-state gate current	The value of the gate current during on-state conduction.
I_{Tav}	On-state current	The maximum value of mean on-state current.
Q_{GQ}	Turn-off gate charge	The charge supplied to the gate during reverse bias that causes the on-state current to fall to 90% of its initial value.
t_d	Delay time	The time interval between the gate current reaching 10% of its final value and the off state voltage falling to 90% of its initial value
t_{gf}	Fall time	The time interval for the on-state current to fall from 90% of its initial value and the beginning of tail time.
t_{gq}	Gate controlled turn-off time	The time interval between the reverse gate current reaching 10% of its final value and the beginning of tail time.
t_{gs}	Storage time	The time interval between the reverse gate current reaching 10% of its final value and the on-state current falling to 90% of its initial value.
t_r	Rise time	The time interval for the on-state voltage to fall from 90% to 10% of its initial value
V_D	Continuous (direct) off-state voltage.	The maximum value of applied direct off state voltage
V_{DM}	Turn-off voltage	The peak value of direct off-state voltage at turn-off.
V_{DP}	Peak forward transient voltage.	The peak value of forward transient voltage appearing across the anode and cathode of the GTO during the fall time.
V_{RG}	Reverse gate voltage	The value of negative gate-cathode voltage.
I_{GQ}	Reverse gate current	The value of reverse current at switch off

Table (2-1) GTO terms, symbols and definitions.

2-4 SNUBBER CIRCUIT.

It is necessary to connect a snubber circuit across a GTO to limit the rate of rise of voltage during GTO turn-off and to limit the peak power dissipated by providing an alternative path for the anode current when the GTO turns-off (51,59.61). Figure (2-3) shows the connection of a snubber circuit across a GTO chopper circuit. The snubber circuit consists of a capacitor, a resistor and a diode.

After the expiry of the storage time, the GTO anode current collapses with a fall time which produces a very high rate of rise of current in the snubber circuit. The transient responses of the snubber network produce a voltage spike V_{DP} which appears at the anode of the GTO. This voltage depends on the inductance of the snubber capacitor, the inductance of the circuit wiring and the transient turn-on impedance of the snubber diode (61,62). The value of V_{DP} must be kept below the rated value of the GTO to avoid excessive turn-off power dissipation.

The capacitor voltage rises at a linear rate given by:

$$\frac{dV_C}{dt} = \frac{I_A}{C_S} \qquad (2\text{-}1)$$

Where I_A is the anode current.

The capacitor voltage continues to rise until it reaches the DC supply voltage, at which instant, point (A) shown in figure (2-3) becomes effectively clamped to the DC supply. The capacitor voltage then overshoots and reaches V_{DM}. The overshoot amount will be governed by the value of the snubber capacitor and the stray inductance.

The peak overshoot may be determined by simply considering the energy transfer in the circuit as follows. The total energy change in the system equals the energy stored in the inductance L plus the energy absorbed by the capacitor from the supply, where L is the total leakage inductance ($L_{X1} + L_{X2}$) of the circuit.

Therefore:

$$\frac{1}{2} C_S(V_{DM}^2 - V_{DC}^2) = \frac{1}{2} LI_A^2 + V_{DC}\int idt \qquad (2\text{-}2)$$

Where:

V_{DM} is the peak capacitor voltage reached.

V_{DC} is the supply voltage.

$$i = C_S \frac{dV_C}{dt}$$

Therefore.

$$\frac{1}{2} C_S(V_{DM}^2 - V_{DC}^2) = \frac{1}{2} LI_A^2 + V_{DC}\int_{D_{DC}}^{V_{DM}} C_S\, dV_C \qquad (2\text{-}3)$$

$$\frac{1}{2} C_S(V_{DM}^2 - V_{DC}^2) = \frac{1}{2} LI_A^2 + C_S V_{DC}(V_{DM} - V_{DC}) \qquad (2\text{-}4)$$

Which gives:

$$V_{DM} = V_{DC} + I_A\sqrt{\frac{L}{C_S}} \qquad (2\text{-}5)$$

After the voltage overshoots, the capacitor discharges through R_S and D_F, eventually settling to the DC supply voltage. The current in the snubber circuit approaches zero and a reverse current flows through the snubber diode maintained by the stored charge. D_S cannot regain its reverse blocking capability until most of the stored charge is removed by the reverse extraction process and internal recombination of the charge carriers. This snap off of reverse current will produce via external circuit inductance, a negative voltage spike which then recovers rapidly to the steady-state positive voltage level (45,48,49,64). Since the magnitude of this voltage excursion depends on the diode turn-off speed, the snapiness can be reduced to a certain degree by using a soft recovery diode.

The greater part of the energy stored in C_S during turn off is dissipated in R_S. The required power rating of R_S is given by:

$$W_S = \frac{1}{2} C_S V_C^2 f \qquad (2\text{-}6)$$

Where f is the switching frequency and V_C is the snubber capacitor voltage.

(Note that, in the above equation, V_{DM} is used to calculate the rating of the snubber resistor. Although the time during which V_C equals V_{DM} is only a fraction of a cycle, by basing on V_{DM} rather than V_{DC}, this gives a safety margin for the resistor rating).

The ohmic value of R_S is chosen to enable C_S to discharge almost completely during the shortest period for which the GTO is conducting. Otherwise any residual charge left on C_S will add to the voltage spike V_{DP} at turn-off. The discharge time is governed by the time constant $R_S C_S$. It is well known that for a RC circuit, the capacitor needs at minimum 5 times the time constant to be almost discharged. MEDL data sheet recommended that (57):

$$C_S R_S < t_{on}/5. \qquad (2\text{-}7)$$

Where t_{on} is the conduction time of the GTO. On the other hand, the value of the snubber resistor R_S must be high enough to limit to a safe value the capacitor discharging current which flows through the GTO at turn on (45).

2-5 GTO GATE DRIVE CIRCUIT.

The gate drive circuit has a direct influence on the switching performance of a GTO thyristor. As was mentioned in section (2-3) the storage time is affected by the rate of rise of gate current and the peak gate current. In designing a gate drive circuit, care must be taken to ensure that the rate of rise of gate current meets the manufacturer's specification, and this can be controlled by varying the value of the gate inductance and the turn-off voltage (53,54).

The GTO drive circuit represented by the block diagram of figure (2-4) is comprised the following blocks.

a) The input signal which handles the incoming control signal and the driver stages.

b) The initial turn-on current which contains a circuit to handle the peak value of forward current (I_{FG}) at turn-on.

c) The third one contains a circuit to carry the back porch current which is the value of the gate current during on-state conduction.

d) Finally the turn-off circuit and this carries the turn-off current (I_{GQ}) (this is the value of reverse gate current at turn-off).

Figure (2-5) shows the circuit details for the turn-on and turn-off parts and figure (2-6) shows the waveform of the initial turn-on and the back porch current. The initial turn-on current consists of a high current pulse (About 15 A magnitude for 12μs) which can be obtained by discharging the capacitor C_{on} through 1 Ω resistor and power MOSFET1. The back porch current (about 1A) is obtained by switching the 5V supply to the gate through the 5 Ω resistor and power MOSFET2. To avoid any gap between the initial and the back porch current, MOSFET1 and MOSFET2 must turn-on simultaneously. According to the data sheet of the device, the initial pulse should have an amplitude of at least 10 A whilst the back porch current should be 1 A at 25 °C.

Turn-off is achieved by discharging capacitor C_{off} through the GTO gate and the two power MOSFETs3,4 in parallel to handle the reverse current of the GTO at turn-off. Note that MOSFETs1,2 are P channel enhancement and MOSFETs3,4 are N channel enhancement types. To turn-on the P channel the input voltage should be more negative than the threshold voltage(-2 V) and for N channel the input voltage should be more positive than the threshold voltage (3V).

The gate circuits in turn are driven from turn-on and turn-off stages as shown in figure (2-7). To understand the operation of the drive stage circuit, the circuit has been divided into simple sections and each section is explained individually. As shown in figure (2-7) an opto-isolator is connected at the input of the drive stage, this is used to isolate each drive circuit from the input signal. The device is ideal for

isolating high speed logic interfaces, eliminating ground loops and implementing isolated line receivers in high noise environments.

The GTO thyristor is a latching device and a single narrow pulse or a pulse train to its gate is usually sufficient to turn it on. Due to the characteristics and application of the present gate drive circuit, wide-width pulses are used to drive the GTO. This means a continuous pulse supplies the gate throughout the whole conduction period of the GTO. When the input pulse of the gate circuit driving stages is high, the GTO will turn-on and when the input pulse is low, the GTO will turn-off.

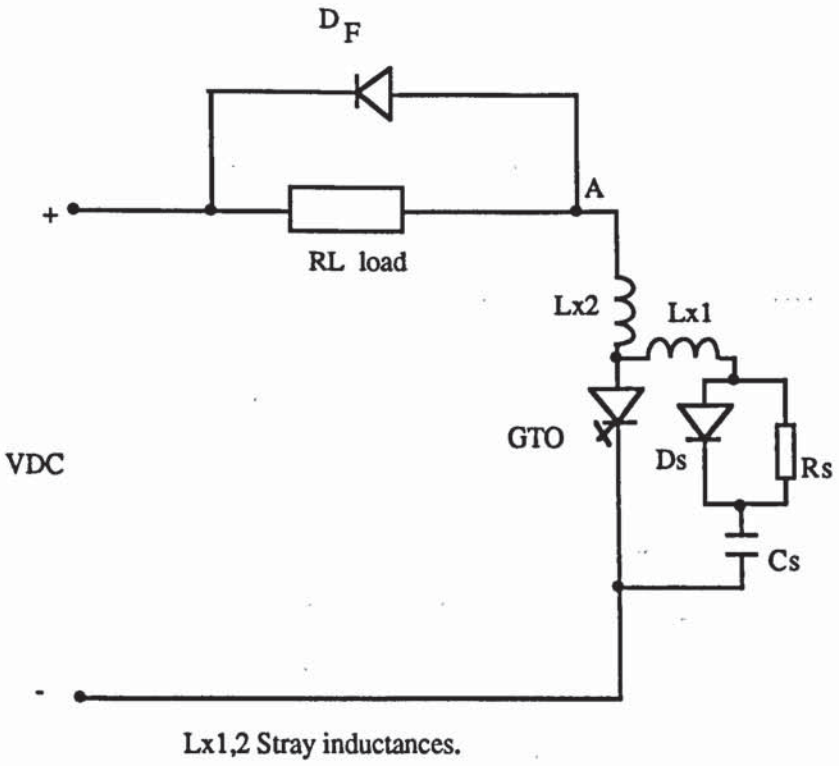


Figure (2-3) Snubber circuit.

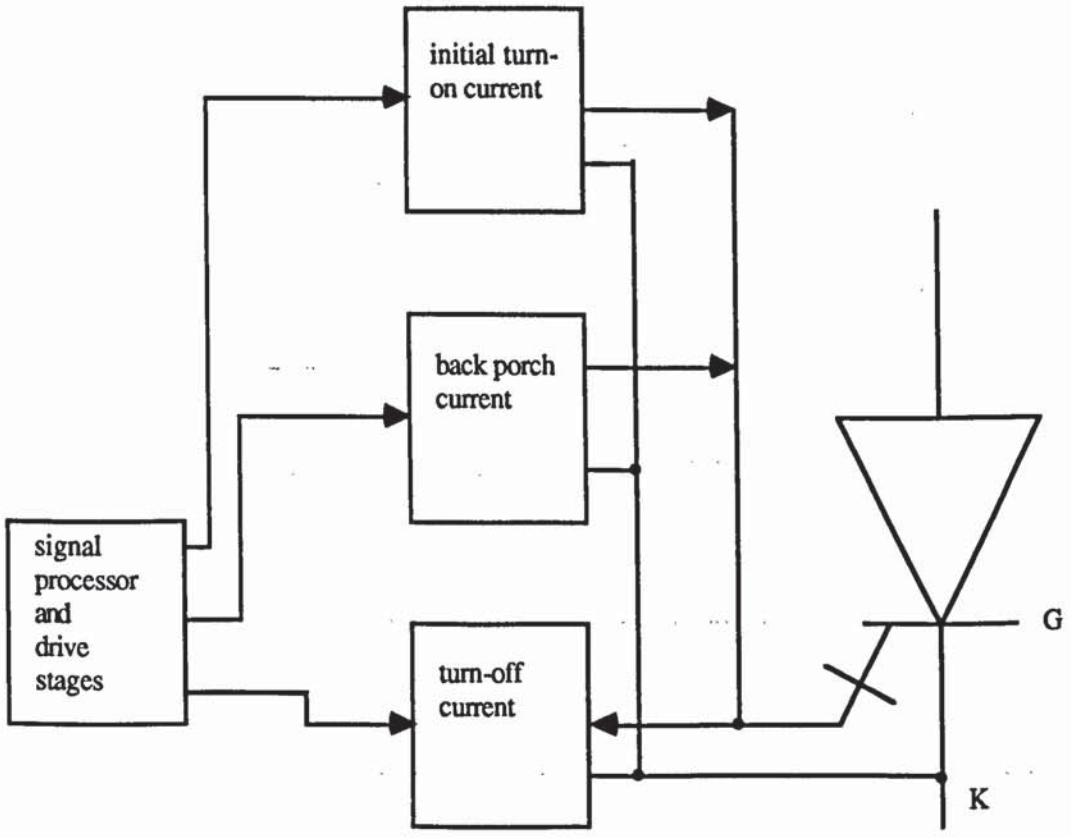


Figure (2-4) Gate drive block diagram.

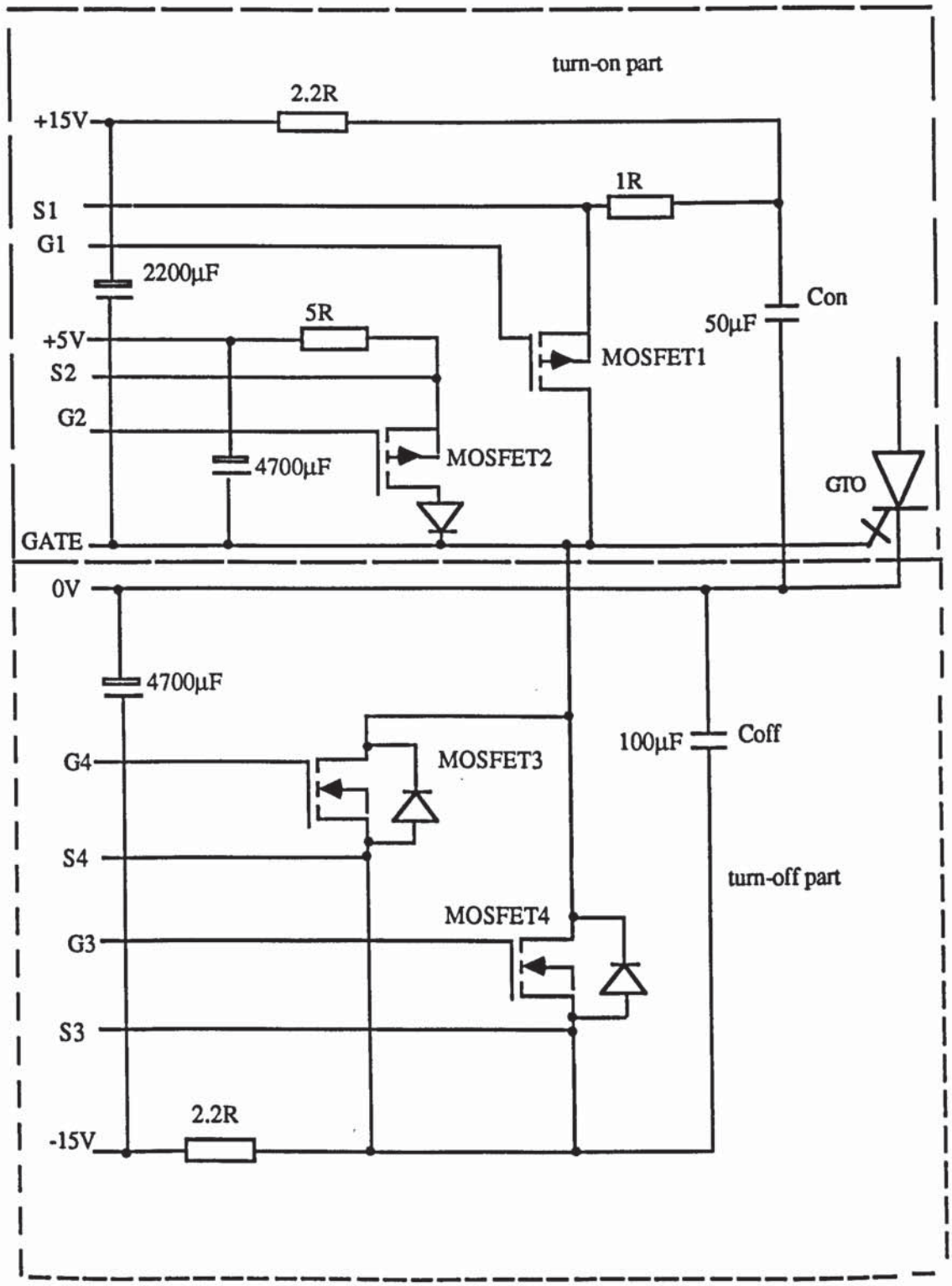


Figure (2-5) GTO Drive circuit.

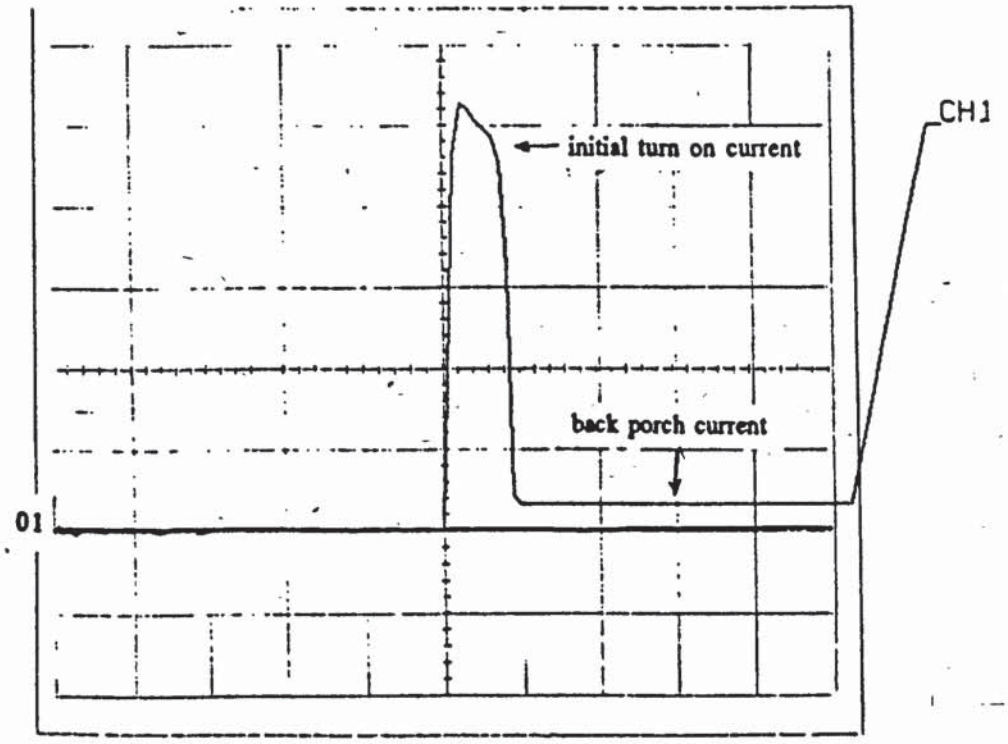


Figure (2-6) Initial turn on and back porch current.
CH2: 3 A/div.
Initial on current: 16 A.
Back porch current: 1 A.
Time: 15 µs/div.

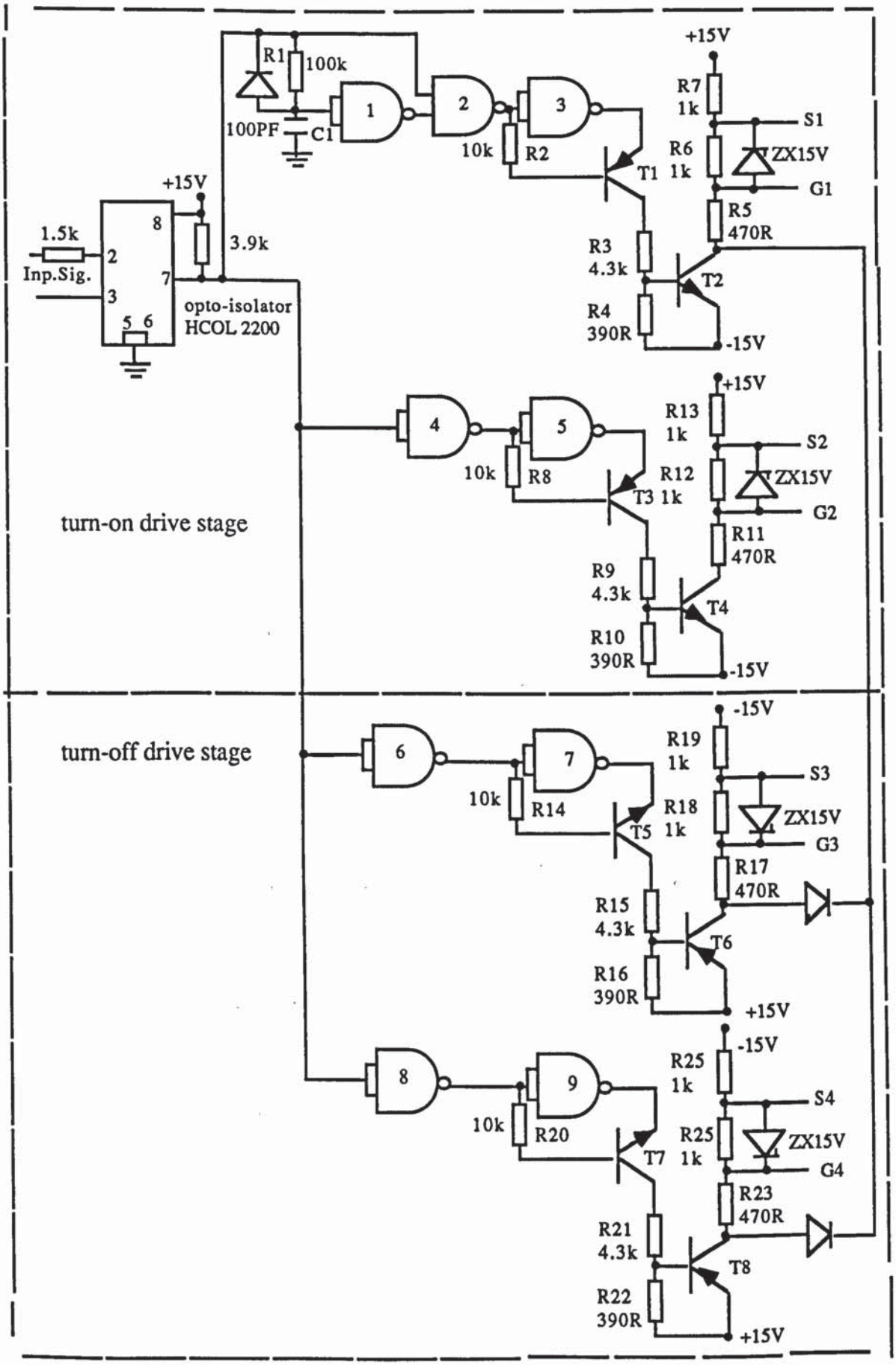


Figure (2-7) Gate circuit drive stages.

2-5-1 DELAY CIRCUIT.

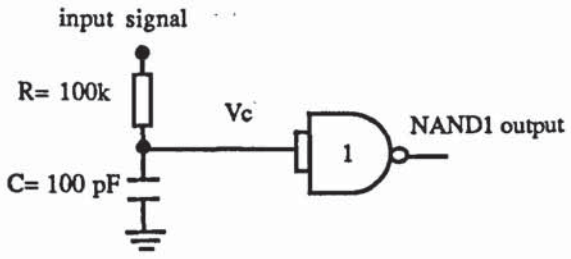
A 12 μs signal is used to feed the driving stage of MOSFET1 in order to carry the initial turn-on current pulse. This signal is generated by a delay circuit comprising three NAND gates and an RC circuit as shown in figure (2-9). This kind of NAND gate (CMOS 4093 2-input NAND Schmitt trigger) switches at different voltage levels for positive and negative going edges. For a positive-going edge, the gate switches when the input voltage reaches 70% of its peak value and for a negative-going edge, the gate switches when the input voltage drops to 30% of its peak value. The peak value of the input voltage is 15 V, therefore the output of the NAND gate changes state when its input reaches 10.5 V or when its input drops to 4.5 V.

To get a 12 μs wide signal, the input of the delay circuit must rise exponentially and reaches 70% of its peak voltage in 12 μs. By feeding the input signal to an RC circuit, the capacitor voltage will reach 70% of the peak input when t = 1.2RC as illustrated in equation (2-8)

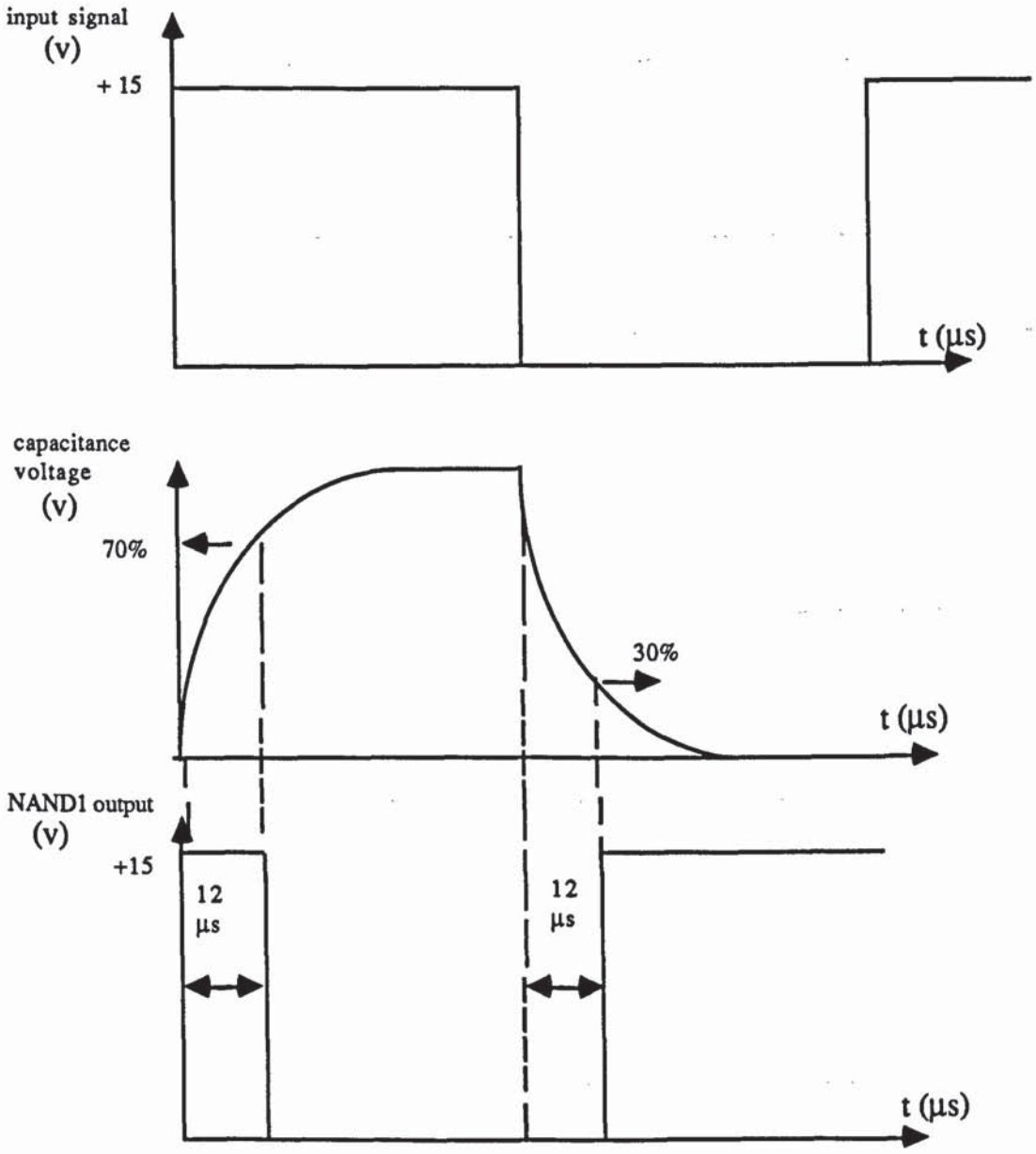
$$V_C = V_{inp}\left(1 - e^{\frac{-t}{RC}}\right) \qquad (2\text{-}8)$$

Figure (2-8) shows the connections of the input signals to the RC circuit and the effect of NAND1. R = 100 k Ω, C = 100 pF, 1.2RC = 12 μs

Refer again to figure (2-9), the output of NAND1 supplies one input of the NAND2 and the input signal supplies the other input. The output of NAND2 is inverted using NAND3, which gives a 12 μs pulse at the beginning of the input signal. Figure (2-10) shows the oscillograms of the input signal and the output of the delay circuit (output of NAND3).

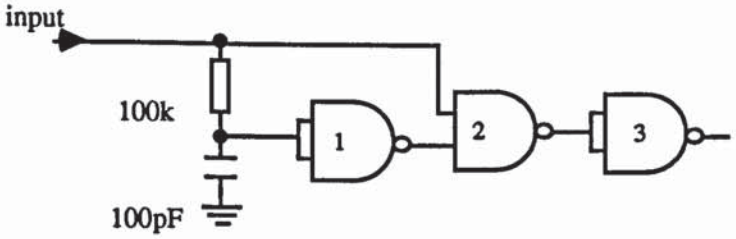


(a) Circuit connections.

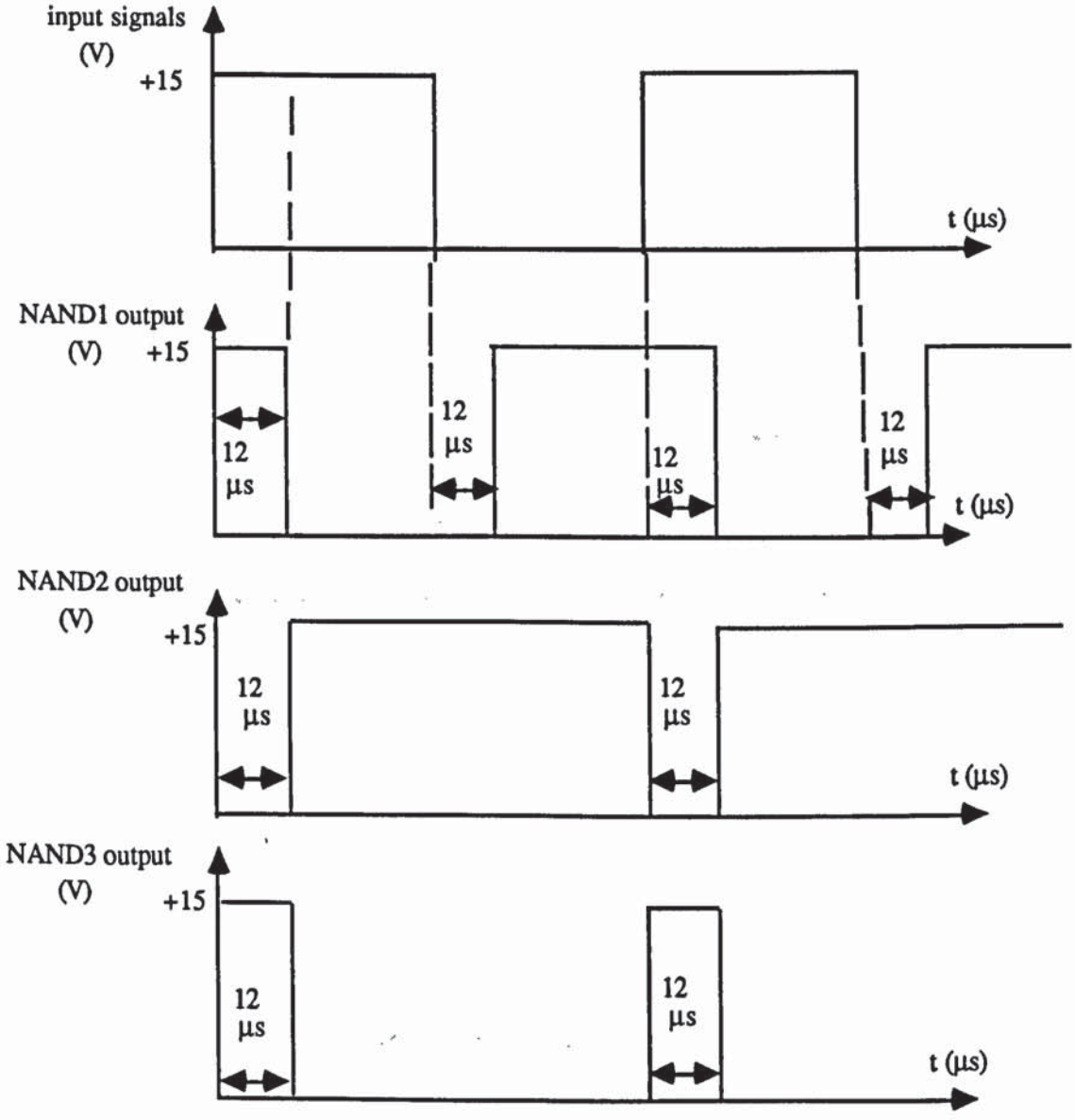


(b) Circuit waveforms.

Figure (2-8) RC circuit connections and waveforms.



(a) Circuit connections.



(b) Circuit waveforms.

Figure (2-9) Delay circuit connections and waveforms.

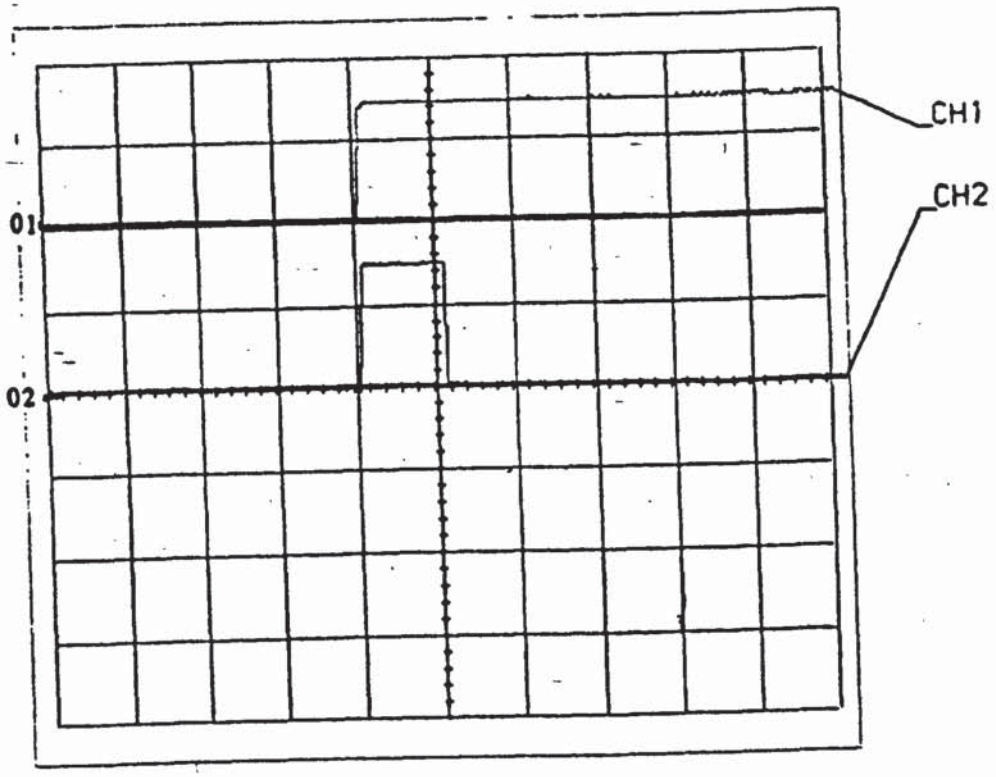


Figure (2-10) Output of the delay circuit.
CH1: 15 V/div. (input signal).
CH2: 15 V/div. (delay circuit output).
Time: 10 μs/div.

2-5-2 MOSFET1 DRIVE STAGE.

Figure (2-11) shows the MOSFET1 drive stage. Each time the input signal changes from low to high state, the output of NAND2 will be zero for a 12 μs duration. The output of NAND2 feeds the base of transistor T1 to switch it on. The emitter of T1 is connected to the output of NAND3 which inverts the state of NAND2 output. When T1 turns-on, current flows through its emitter, collector and the resistors (R3 and R4). These resistors operate as a voltage divider to feed the base of T2. When transistor T2 turns-on, a current flows from the +15 V rail through R7, R6, R5, and T2 to the -15 V rail. This current produces a voltage at the gate of MOSFET1, with a magnitude of:

$$V_{G1S1} = \frac{30}{R_7+R_6+R_5} R_6 = \frac{30}{1+1+0.47} = 12.1 \text{ V}$$

This voltage is negative with respect to the source and less than the threshold voltage thus MOSFET1 will turn-on to carry the initial pulse current.

After the 12 μS duration, the output of NAND2 changes state to a high level (+15 V), T1 turns-off and the base of T2 is connected to -15 V rail. Hence T2 turns-off and the current through R6 cuts-off. The gate-source voltage is zero which is higher than the threshold voltage and this turns MOSFET1 off. Figure (2-12) shows the oscillograms of the drive stage.

2-5-3 MOSFET2 DRIVE STAGE.

Figure (2-13) shows the MOSFET2 drive stage. The input signal is inverted by NAND4 to feed the base of transistor T3 via R8, whilst the emitter of T3 is connected to the output of NAND5 which has the same state as the input signal. When the input signal is high, the base of T3 is low, A current flows through its emitter, collector and the resistors (R9,R10), this current supplies the base of transistor T4 to turn it on. When T4 turns-on, a current flows from the +5 V rail through R13, R12, R11

and T4 to the -15 V rail. This current produces a gate voltage across R12 with a magnitude of:

$$V_{G2S2} = \frac{20}{R_{11}+R_{12}+R_{13}} R_{12} = \frac{20}{1+1+0.47} = 8 \text{ V}$$

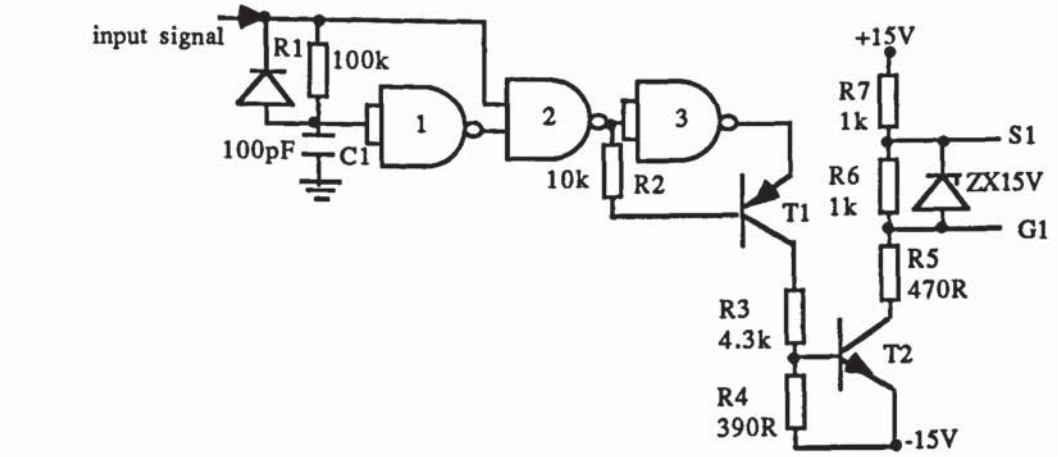
This gate voltage is negative with respect to the source of MOSFET2 and less than the threshold voltage, hence MOSFET2 turns-on to carry the back porch current of the GTO gate drive circuit. When the input signal is low, T3 turns-off. Transistor T4 also turns-off. Since there is no current flow from the +5 V rail, the voltage across R12 is zero and MOSFET2 switches off. Figure (2-15) shows the oscillograms of the drive stage.

2-5-4 MOSFET3 DRIVE STAGES.

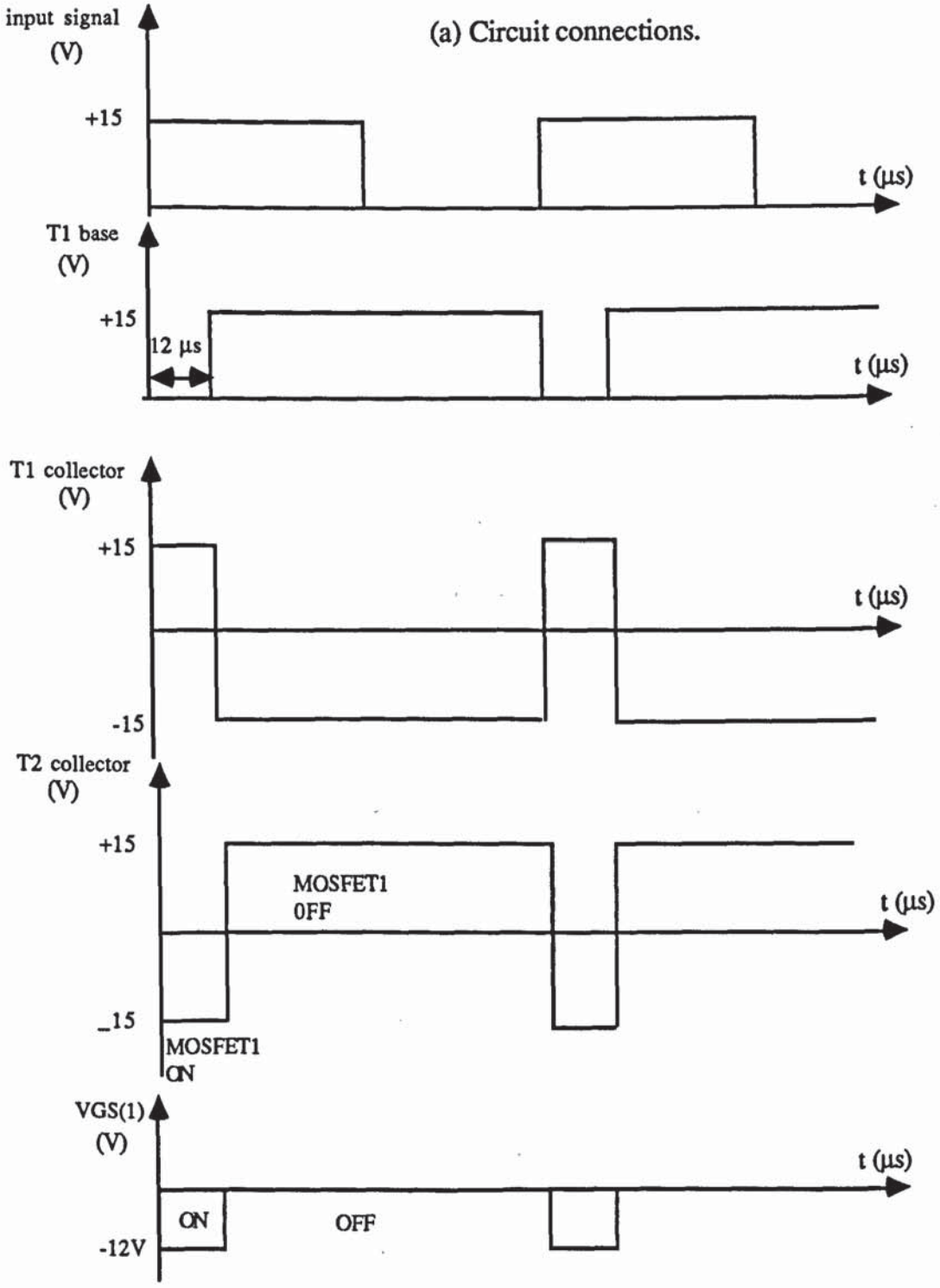
Figure (2-14) shows the MOSFET3 drive stage. The input signal is inverted by NAND6 to feed the npn transistor T5. When the input signal is low the base drive of T5 is high and this turns it on. The emitter of T5 is connected to the output of NAND7 which is low. A current flows from the +15 V rail through R16, R17 and T5. By the operation of the voltage divider (R15 and R16) the base voltage level of T6 is negative with respect to the emitter. T6 will turn on and a current flows from the +15 V rail through T6, R17, R19, and R20 to the -15 V rail. This current produces a gate voltage across R18 with a magnitude of:

$$V_{G3S3} = \frac{30}{R_{17}+R_{18}+R_{19}} R_{18} = \frac{30}{1+1+0.47} = 12.1 \text{ V}$$

This gate voltage is positive with respect to the source of MOSFET3 and higher than the threshold voltage, thus MOSFET3 turns-on. When the input signal is high (+15 V), T5 turns-off which in turn switches transistor T6 off. Since there is no current flow through T6, the voltage across R18 is zero and MOSFET3 turns-off.Figure (2-16) shows the oscillograms of the drive stage. (Note that the operation of MOSFET4 driving stage is similar to that of MOSFET3).



(a) Circuit connections.



(b) Circuit waveforms.

Figure (2-11) MOSFET1 drive stage.

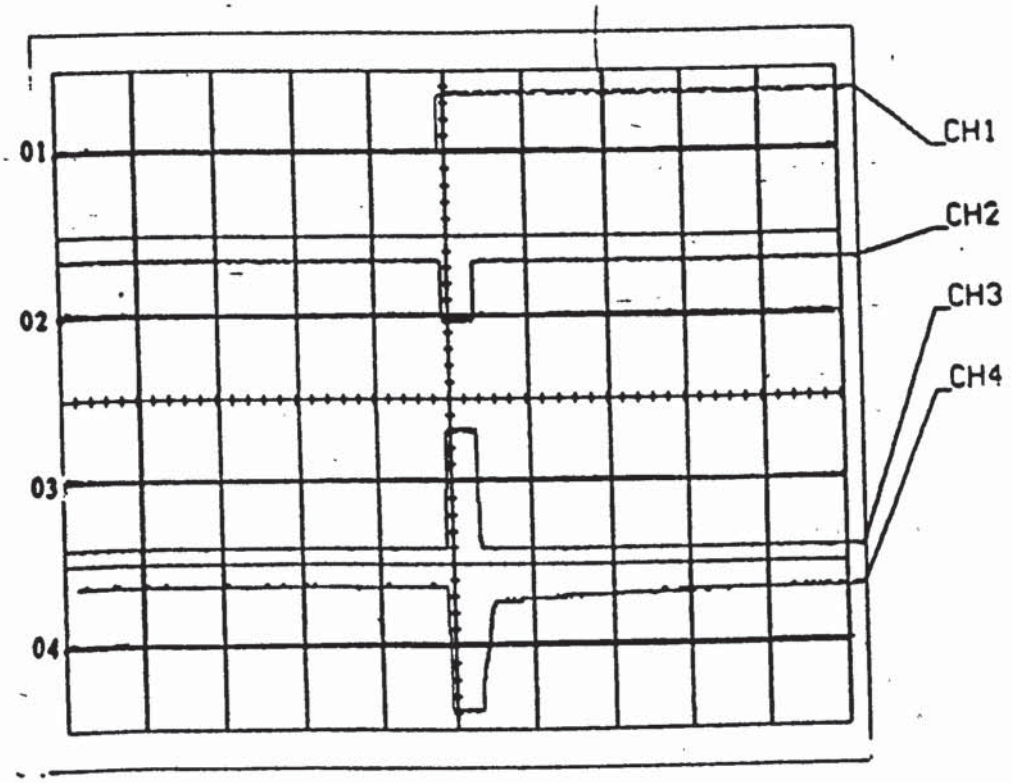
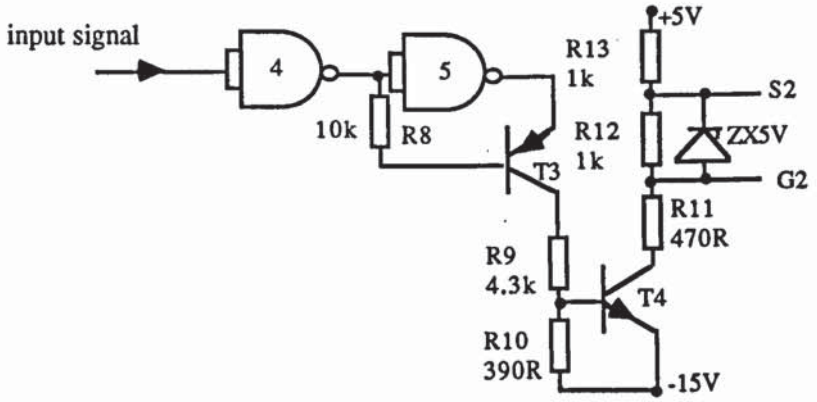
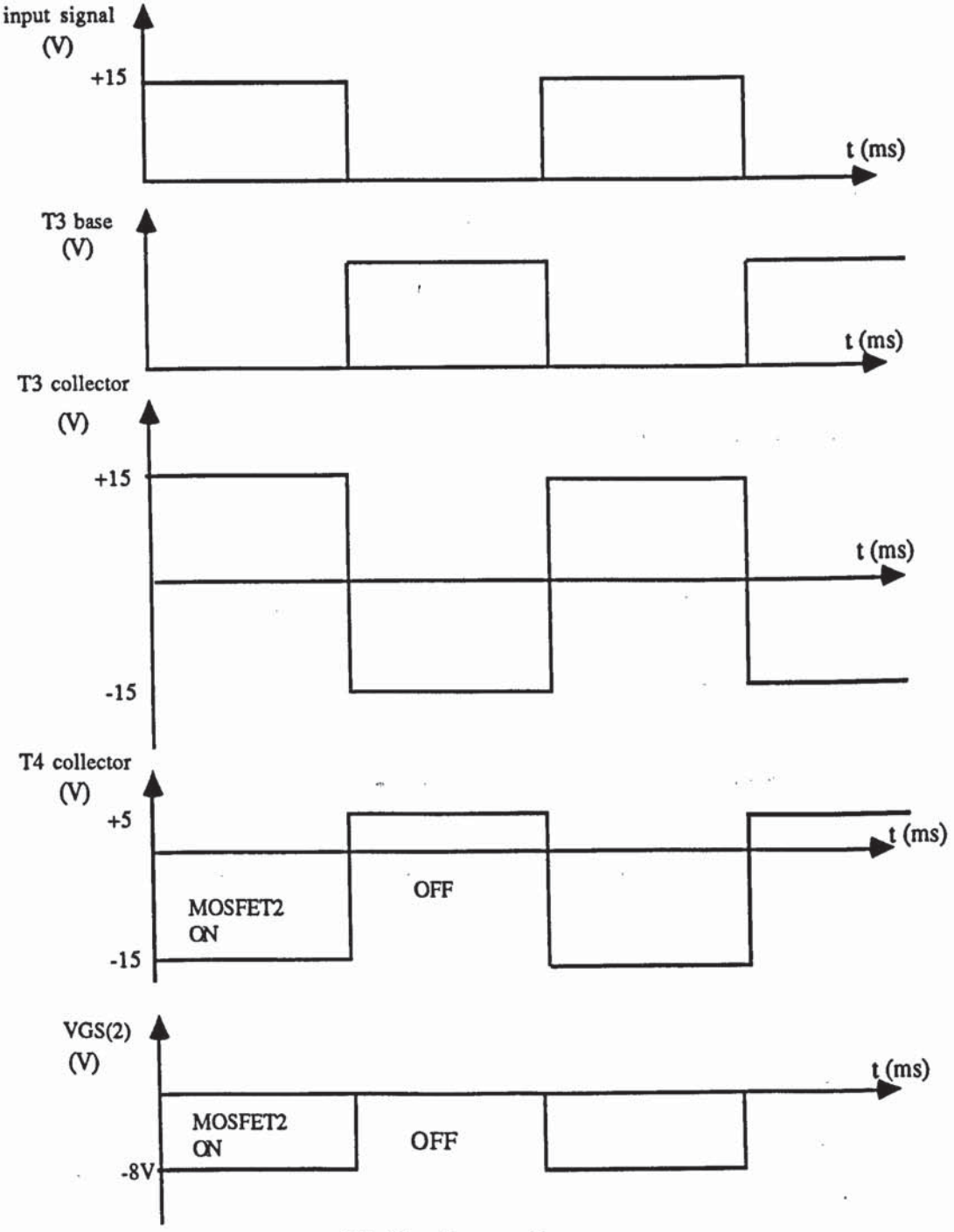


Figure (2-12) Output of MOSFET1 drive stage.
CH1: Input signal 20 V/div.
CH2: T1 base 20 V/div.
CH3: T1 collector 20 V/div.
CH4: T2 collector 20 V/div.
Time: 25 μs/div.

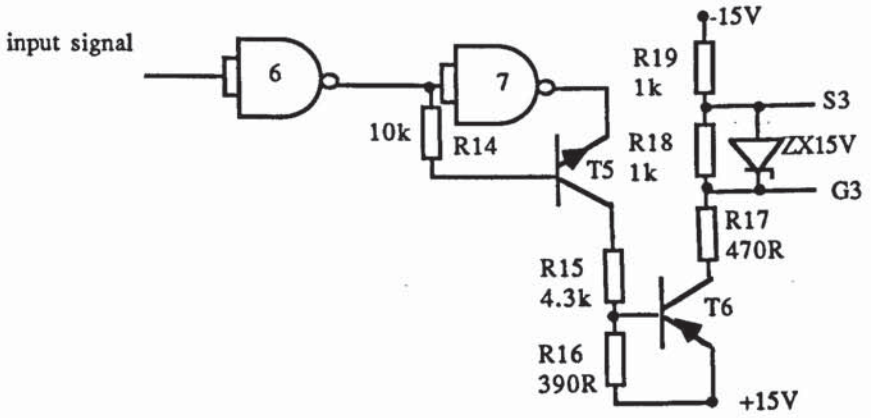


(a) Circuit Connections.

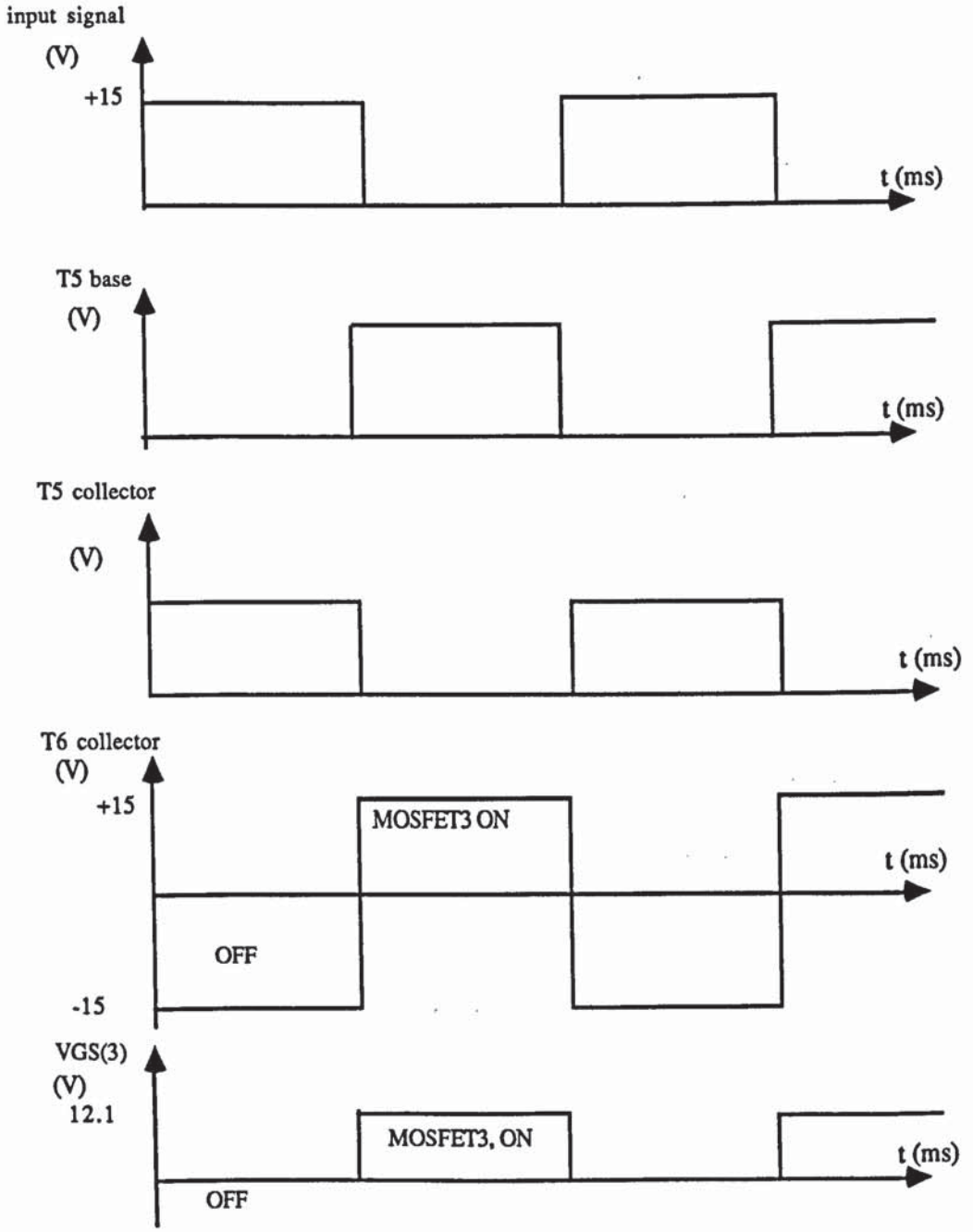


(b) Circuit waveforms.

Figure (2-13) MOSFET2 drive stage.



(a) Circuit connections.



(b) Circuit waveforms.

Figure (2-14) MOSFET3 drive stage.

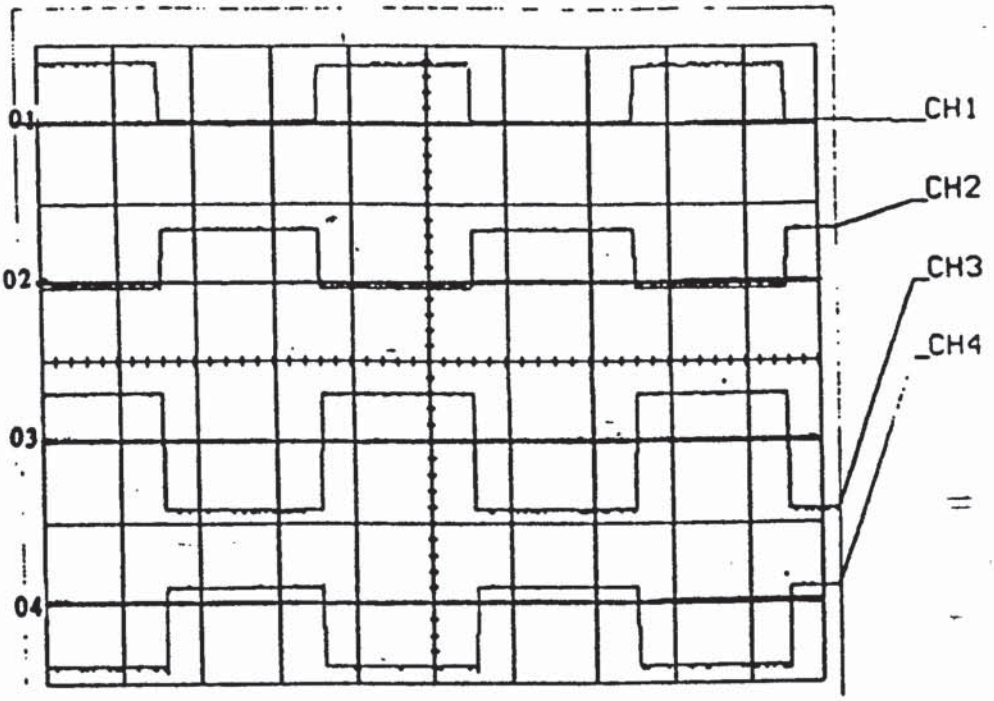


Figure (2-15) Outputs of MOSFET2 drive stage.
CH1: Input signal 20 V/div.
CH2: T3 base 20 V/div.
CH3: T3 collector 20 V/div.
CH4: T4 collector 20 V/div.
Time: 5ms/div.

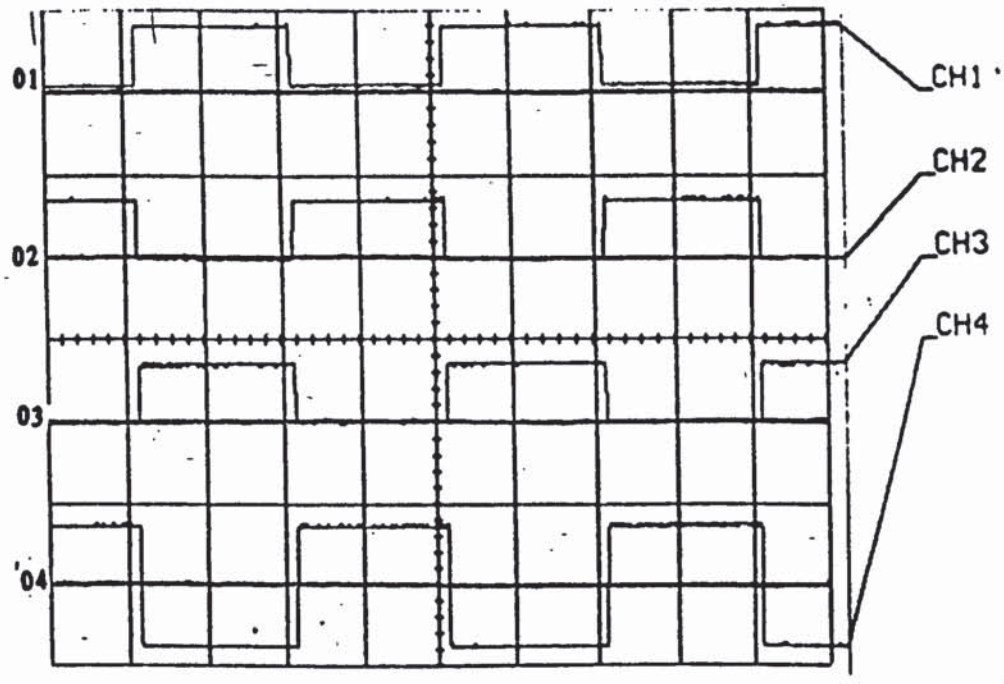


Figure (2-16) Outputs of MOSFET3 drive stage.
CH1: Input signal 20 V/div.
CH2: T5 base 20 V/div.
CH3: T5 collector 20 V/div.
CH4: T6 collector 20 V/div
Time: 5 ms/div.

2-6 GTO TESTING CIRCUIT.

The switching waveforms and the operation of the gate drive circuit of the GT224K GTO were tested using the single phase half-bridge inverter of figure (2-17). For the initial test it was decided to operate the GTO at 10 A RMS as a safety margin and a switching frequency of 1kHz was chosen since this was the chosen frequency for the PWM waveform. The voltage of the DC power supply was 100 V. To obtain the required current of 10 A RMS at the stated voltage and switching frequency, the load was arranged to have an inductance of 800 μH and virtually negligible resistance to minimize the losses.

Referring to figure (2-17), since the inverter is a half bridge, when one GTO is turned-on for a time T/2 (T = 1/f), the instantaneous voltage across the load is $V_{DC}/2$. Assume that, for the first half cycle GTO_1 is turned on to carry the load current. When GTO_1 turns-off and GTO_2 turns-on, the load voltage reverses and the load current transfers to the diode D_2, the voltage drop across D_2 reverses the biases of GTO_2. The current through D_2 starts to fall and when it reaches zero, GTO_2 becomes a forward biased and the load current flows through GTO_2. Again when GTO_2 turns-off and GTO_1 turns-on, the load current transfers first to the diode D_1 and when it reaches zero, it transfers to GTO_1.

Under-steady state condition the maximum load current passing through the GTO at the end of first half cycle equals:

$$I_{PK} = \frac{V_{DC}}{8fL} \qquad (2\text{-}9)$$

Where f is the inverter frequency and L is the load inductance. The derivation of the above formula is given in appendix (B).

With f = 1kHz, L = 800 μH and V_{DC} = 100 V, the peak current equals:

$$I_{PK} = \frac{100}{(8)(1000)(0.0008)} \tilde{=} 16\ A$$

Figure (2-18) shows that GTO_1 starts to conduct when the current through D_1 reaches zero. Since the load is purely inductive, the conduction period of the GTO is almost equal to that of the diode. I_{PK}= 16 A, and the RMS current is:

$$I_{RMS} = \frac{I_{PK}}{\sqrt{3}} = \frac{16}{\sqrt{3}} = 9.23 \text{ A}$$

Figure (2-19) shows the load voltage, load current, the voltage across GTO_1 and the voltage across GTO_2. It is clear that the voltage across the load is $V_{DC}/2$.

The value of the snubber capacitor was calculated assuming that, future research would be carried on with a 50 A peak anode current through each GTO. According to the device data sheet, the maximum permissible dV/dt is 500 V/μs and referring to the snubber section in this chapter, the value of C_S is:

$$C_S = \frac{I_A}{dV_C/dt} = 0.1 \ \mu F \qquad (2\text{-}10)$$

As mentioned above in this inverter peak anode current is much less than 50 A (I_{PK} = 16 A), when a 0.1 μF snubber capacitor was used, it was found that the snubber circuit produces a high voltage spike and overshoot voltage (V_{DP} = 100 V, V_{DM} = 200 V, $V_{overshoot}$ = 100 V). The voltage V_{DP} depends on the inductances of the snubber capacitor and the circuit wiring. The voltage V_{DM} also decreases when C_S increases.

$$V_{DM} = V_{DC} + I_A\sqrt{\frac{L}{C_S}} \qquad (2\text{-}11)$$

Where:

$$V_{overshoot} = I_A\sqrt{\frac{L}{C_S}} \qquad (2\text{-}12)$$

To reduce the values of the above voltages and to minimize the capacitor inductance, four capacitors were used in parallel for the snubber circuit (0.22 μF each capacitor) and these gave waveforms shown in figure (2-20), where:

$V_{DM} = 120$ V.

$V_{DP} = 25$ V.

$V_{overshoot} = 20$ V.

With $I_A = 16$ A and $C_S = 0.88$ μF, the total stray inductance according equation (2-12) is:

$$L = \frac{V_{overshoot}^2 C_S}{I_A^2} = 1.375\ \mu H$$

The ohmic value of R_S must be:

$$R_S < \frac{t_{on}}{5C_S} \qquad (2\text{-}13)$$

With 1 kHz switching frequency, the conduction time of the GTO is 250 μs which gives a choice for the value of the snubber resistance of 57 Ω or less, the rating of the resistor must be:

$$W_S = \frac{1}{2} C_S\ V_C^2 f \qquad (2\text{-}14)$$

Where V_C is the snubber capacitance voltage.

With $C_S = 0.88$ μF, $V_C = 120$ V and $f = 1$ kHz, the required rating is approximately 7 W. R_S should be large enough to limit the capacitor discharge current and since a 15 Ω, 7 W resistor was available, this was used for the snubber circuit. The maximum capacitor discharge current is quite low compared with the current rating of the GTO.

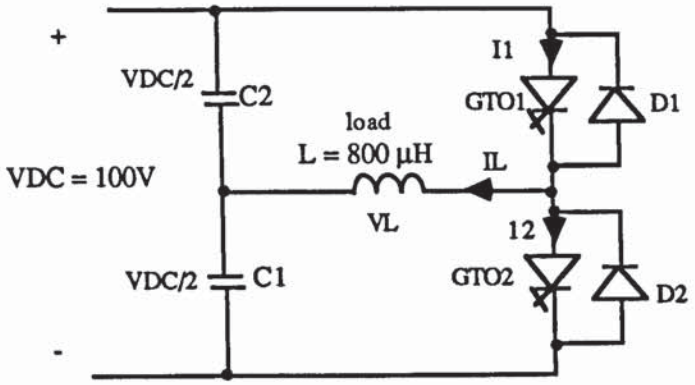
$$I_{C(Max)} = \frac{V_C}{R_S} = \frac{120}{15} = 8\ A$$

Figure (2-21) shows the GTO_1 switching waveforms. From Channel 3 it can be seen that $I_{GQM} = 13$ A (it reaches this value after 0.75 μs). Thus:

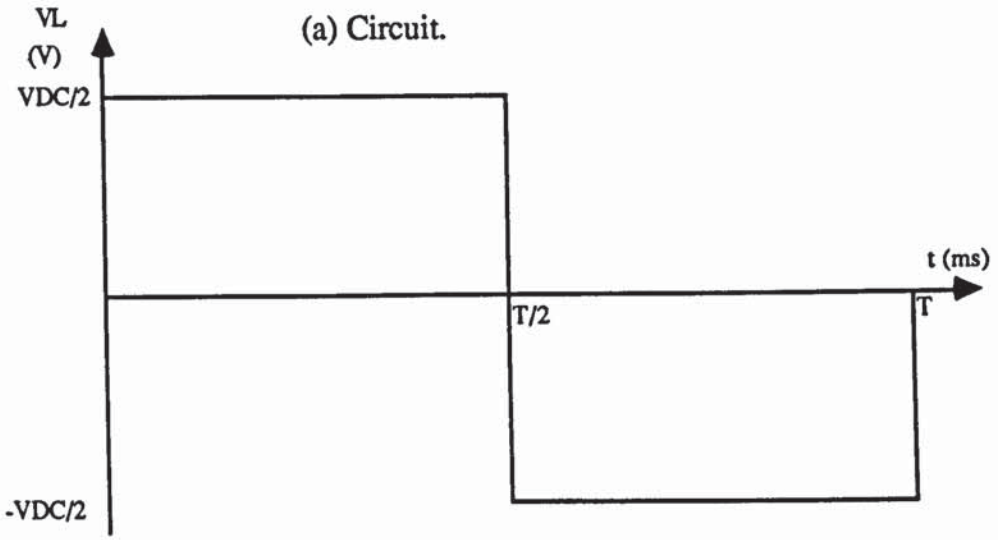
$$\frac{dI_{GQ}}{dt} = \frac{13}{0.75} = 17.33\ A/\mu s$$

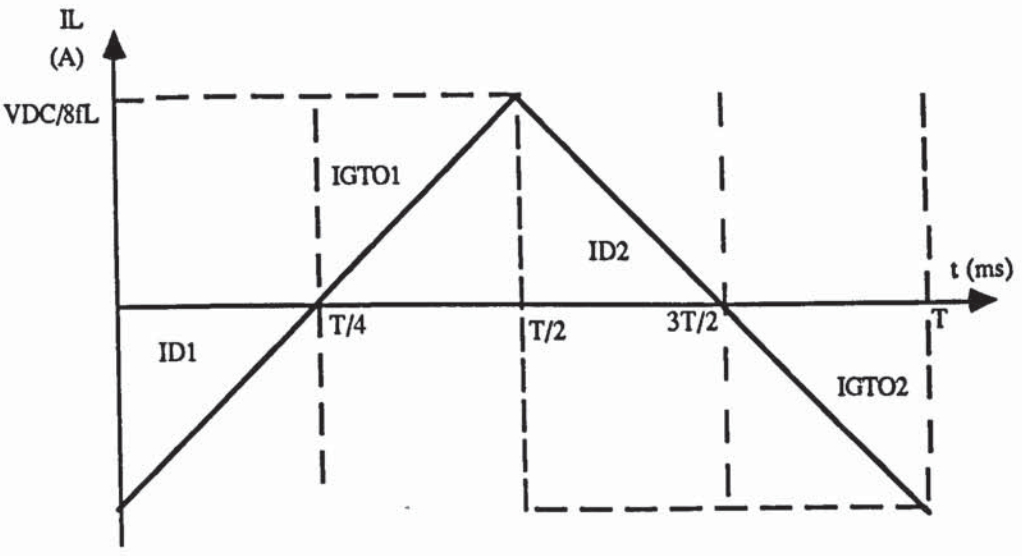
According to the device data sheet, the rate of rise of the reverse current must be between 12 and 30 A/μs.

In conclusion the above test shows that the switching characteristics and the operation of the gate drive of the GT224K meets the design and data sheet specification for the device.



(a) Circuit.





(b) Load voltage and current with an inductive load.

Figure (2-17) GTO Inverter.

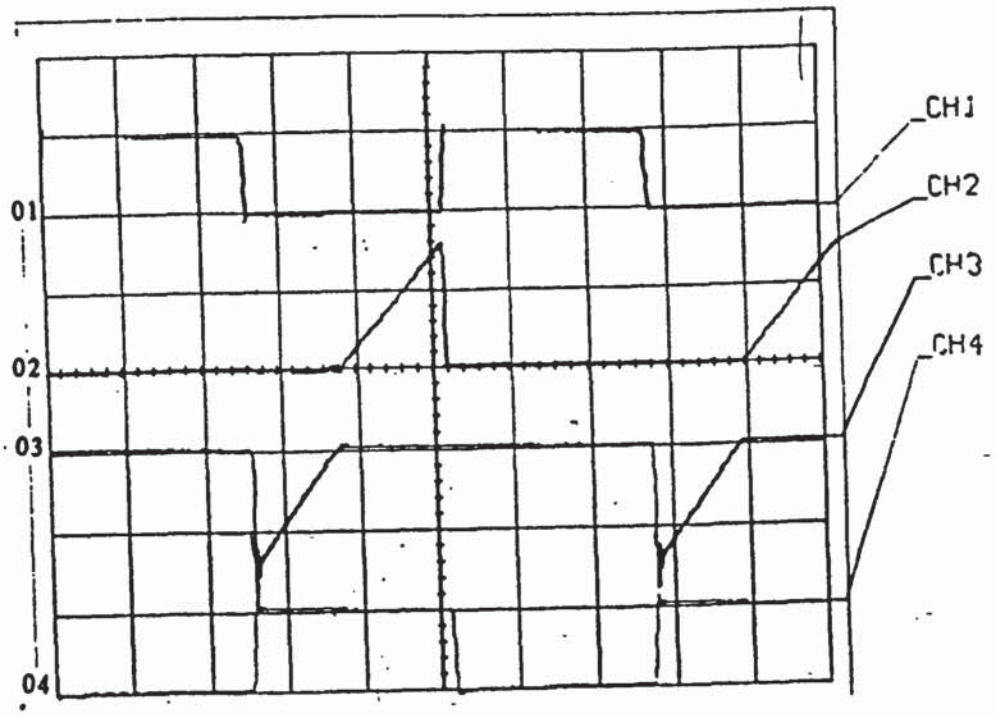


Figure (2-18) Devices Voltages and Currents
CH1: V_{AK} (GTO_1) 100V/div.
CH2: I_A (GTO_1) 10 A/div.
CH3: I_{D1} 10 A/div.
CH4: V_{AK} (GTO_2) 100V/div.
Time: 5 ms/div.

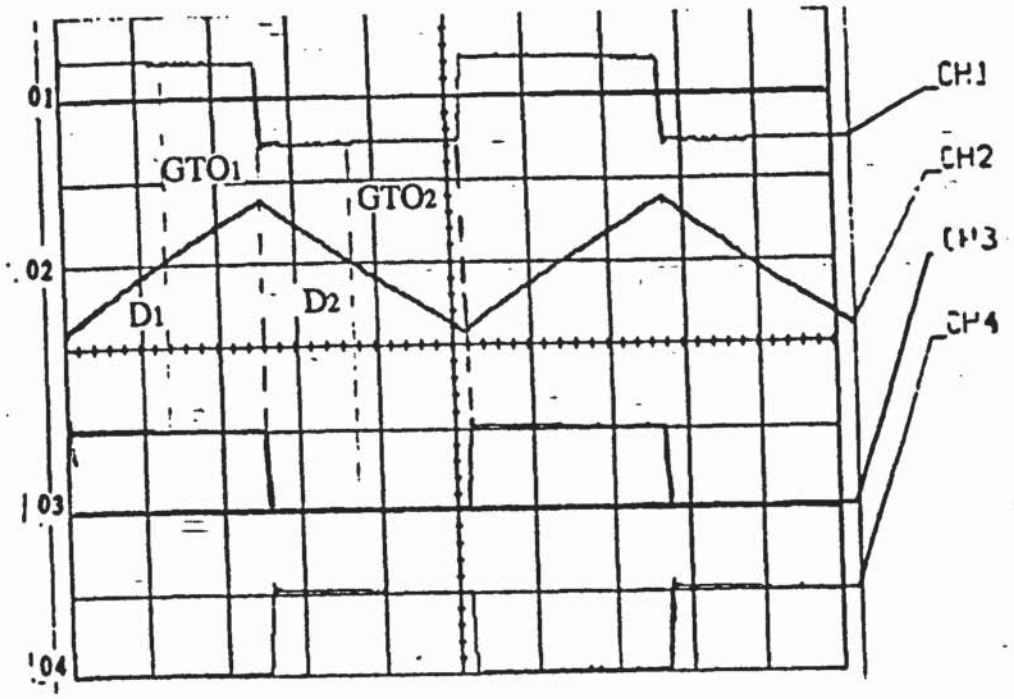


Figure (2-19) Load voltage and current.
CH1: Load voltage 100V/div.
CH2: Load current 20 A/div.
CH3: V_{AK} (GTO_2) 100V/div.
CH4: V_{AK} (GTO_1) 100V/div.
Time: 5 ms/div.

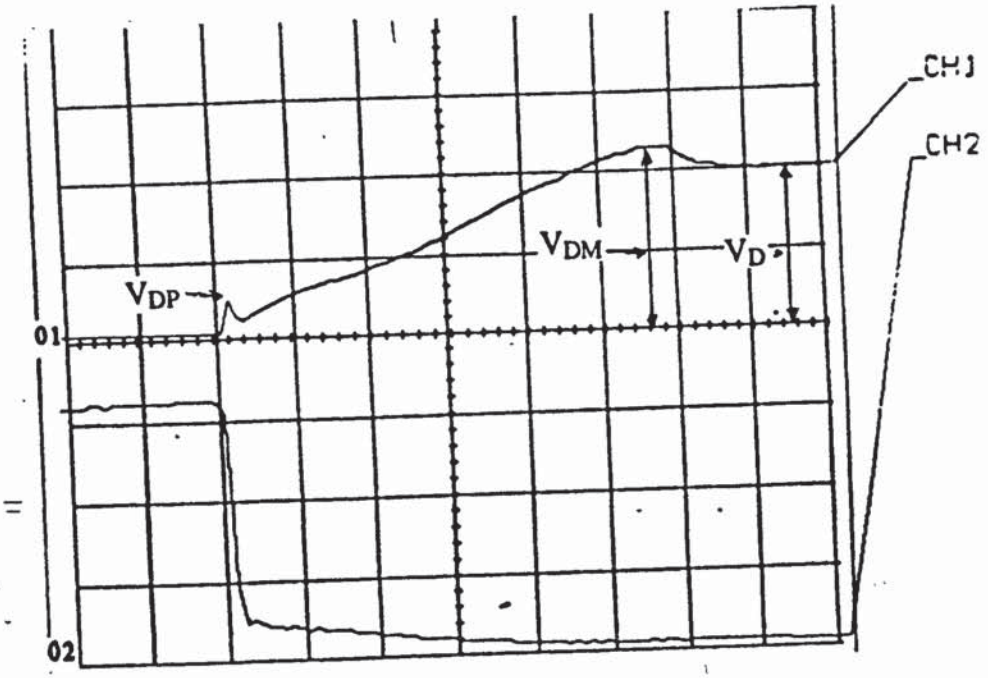


Figure (2-20) Voltage and Current when GTO1 is turning-off.
CH1: V_{AK} 50V/div.
CH2: I_A 5 A/div.
V_{DP} = 25V
V_{DM} = 120V.
Time: 2 μs/div.

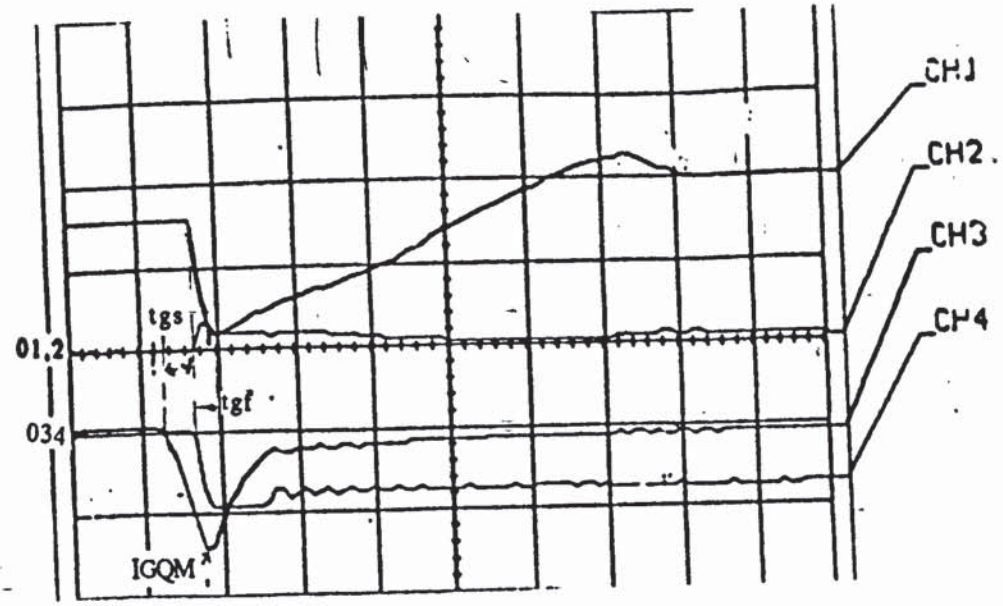


Figure (2-21) Switching waveforms of GTO1.
CH1: V_{AK} 50V/div.
CH2: I_A 10A/div.
CH3: I_{GQ} 10 A/div.
CH4: V_{GK} 20V/div.
Time: 2 μs/div. Fall time = 0.5μs. Storage time = 1μs.

CHAPTER THREE

PRELIMINARY INVESTIGATION FOR TWO WAY POWER FLOW.

3-1 INTRODUCTION.

The circuit shown in figure (3-1) was chosen for a preliminary investigation into the problems associated with two directions power flow. The circuit contains two centre-tap inverters (A_1 and B_1), a diode bridge (A_2) and a half-bridge GTO (B_2). The use of a diode bridge and a half-bridge GTO respectively in converters (A_2) and (B2) was necessitated by the lack of a sufficient quantity of gate drive circuits for the GTOs.

The configuration of figure (3-1) was decided on for preliminary investigation for the following reasons:

a) The centre tap inverters readily lend themselves to the use of low battery voltages and low power loads.

b) The power supplies were self contained and independent of the mains, thus ensuring additional safety and avoiding the need for synchronization with the mains.

This chapter presents the operation of the system , operation and testing of the centre tap inverters, system control circuit and finally a discussion of some results obtained from the system.

3-2 SYSTEM OPERATION.

When power flows from side (A) to (B) of the circuit shown in figure (3-1), (A_1) acts as an inverter, with its output feeding the diode bridge (A_2). The output of (A_2) supplies (B_2), which operates as an inverter to supply rectifier (B_1) and the battery charges via diodes $D_{1,2(B1)}$.

When power flows from side (B) to (A), (B_1) operates as an inverter, (B_2) changes from an inverter to a rectifier and the power is dissipated in the load. When (B_2) is operating as an inverter, GTO_3 and GTO_4 are continuously on and operate as diodes. The current flows through GTO_1 and C_1 during one half cycle and C_2, GTO_2 during the other. When (B_2) operates as a rectifier, GTO_1 and GTO_2 are off and GTO_3 and GTO_4 turn-on as controlled devices. In this case, the rectifier will operate via GTO_3 and D_2 or GTO_4 and D_1.

3-3 CENTRE TAP INVERTER.

There are two centre tap inverters connected to DC power supplies as shown in figure (3-1). These inverters are designed for 24 V and 5 A on the DC side and 65 V and 1.5 A RMS on the AC side. Conventional thyristors are used because the gate drive circuit for a thyristor is much cheaper and simpler than that of a GTO, while the single capacitor and inductor required for the commutation circuit of this 100 W parallel inverter are sufficiently small and cheap to justify their use in this application. When one thyristor is on, the DC source voltage appears across one half of the transformer primary, the total primary voltage is 2 V_{DC}, and the capacitor is charged to 2 V_{DC}. When the other thyristor is fired, the charged capacitor is then placed across the first thyristor turning it off.

Inverter (A_1) is used to send power only while (B_1) is used either to send or receive power. When (B_1) is sending power, its input is connected to a 24 V power supply unit and when it is receiving power it is connected to a 12 V battery which will charge via the diodes. The reason for using the 24 V power supply unit for inverter (B_1) is that the diodes are connected to an 18 V tapping as shown in figure (3-1) so the nominal voltage on the "high voltage" side would not be sufficient to produce the required charging voltage for a 24 V battery. Transistor switches are used to connect (B_1) either to the 24 V power supply unit or to the 12 V battery depending on the direction of power flow.

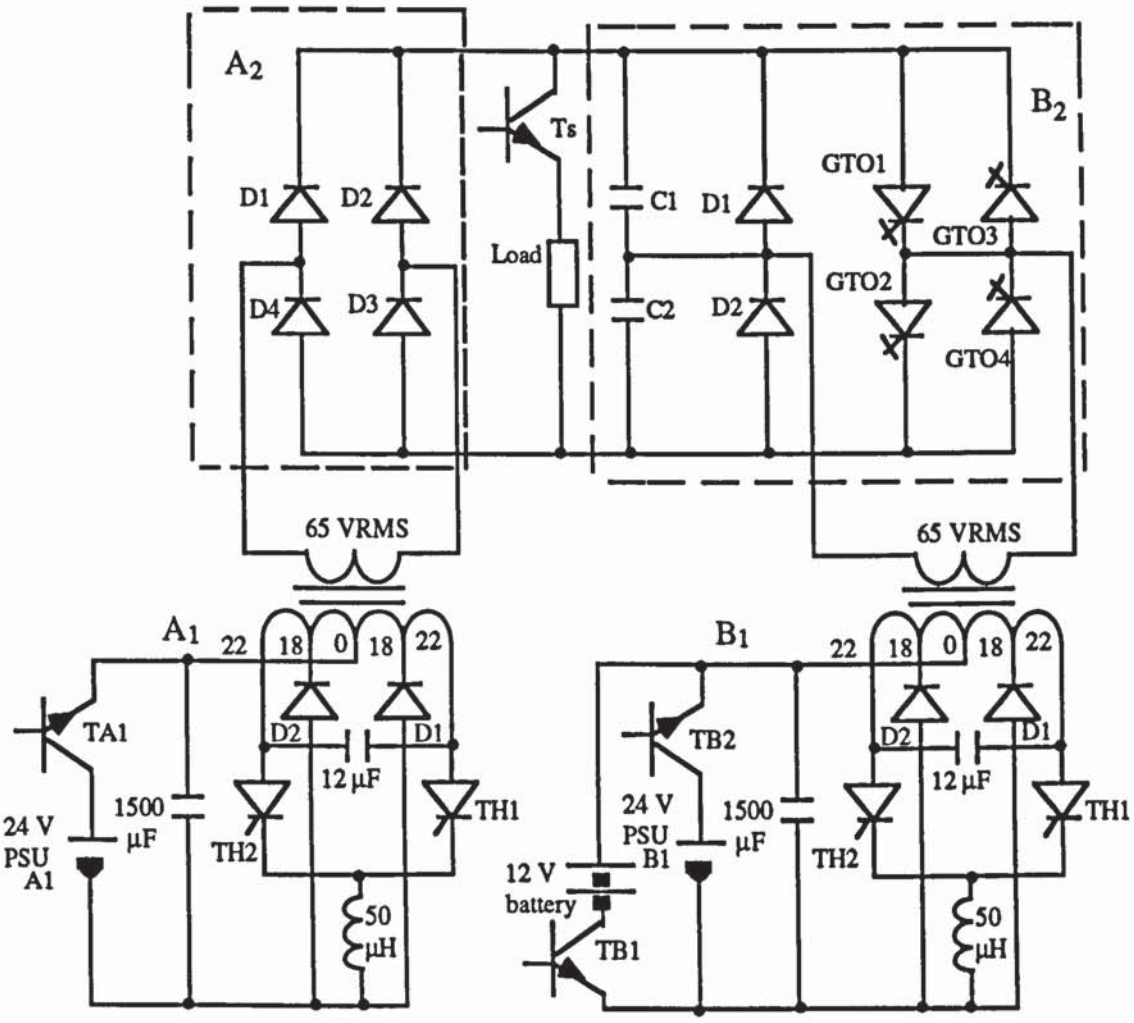


Figure (3-1) Single phase arrangement for two way power flow.

(The drive and snubber circuits of the devices have been omitted from the figure so as not to confuse the explanation)

3-3-1 THYRISTOR FIRING CIRCUIT.

Figure (3-2) shows the thyristor firing circuit for the centre tap inverter which contains an integrator, a voltage-to-frequency converter (V/F), a D type flip flop and various resistors, capacitors and logic gates. Each part of the circuit will be explained individually.

Figure (3-3-a) shows the connections for the integrator and the V/F converter. The integrator uses a 741 operational amplifier with a capacitive feed back. Its input (V_1) is connected to a DC voltage which produces a current to charge the capacitor (C_1) with a value equal to V_1/R_2.

The current flows in C_1 producing a volt drop which equals (65):

$$V_{C1} = \frac{1}{C_1}\int i dt = \frac{V_1}{R_2 C_1}\int dt \qquad (3\text{-}1)$$

The output voltage of the integrator $V_2 = -V_{C1}$. Therefore:

$$V_2 = -\frac{V_1}{C_1 R_2}\int dt \qquad (3\text{-}2)$$

The input to the integrator is negative and this gives a positive going output voltage as shown in figure (3-3-b). The integrator output is connected to the input of (V/F) which produces pulses at a frequency proportional to its applied input voltage. In the event of failure of the DC supply, the integrator would try to maintain the output voltage (input of V/F) for a few milliseconds, the output voltage falls at the same rate as the capacitor voltage. The discharging time of the capacitor dependents on the time constant of the circuit. The connections for the V/F converter are given in figure (3-3-a) and the equation for the output frequency (66) is.

$$f_{out} = \frac{V_2}{2.09}\cdot\frac{R_S}{R_L}\cdot\frac{1}{R_t C_t}\ \text{Hz} \qquad (3\text{-}3)$$

Where: V_2 is the output voltage of the integrator.

The output of the integrator and hence the frequency of V/F converter can be varied by means of the variable resistor R_1 which was set to give a frequency of 100 Hz.

The V/F converter is connected to the D type flip-flop of figure (3-2), which operates as a trigger. A 50% duty cycle is obtained by connecting the complementary output terminal of the flip-flop to its D input and its clock to the output of the V/F converter. The output of the D type flip-flop will change state (high to low or vice versa) at the positive going edge of its clock pulse. In this case, the output frequency of the flip-flop is half the frequency of the V/F converter, as shown in the waveforms of figure (3-4) giving an output of 50 Hz.

Two delay circuits are used, as shown in figure (3-2), to introduce a delay time between the outgoing thyristor and firing the incoming thyristor. Otherwise, a short circuit condition would result through the two thyristors.The value of the delay time depends on the time constants (R_6C_2 and R_7C_3). An experiment showed that the optimum delay time to be introduced is 35μS. The operation of the delay circuit is similar to the one which is given in appendix (C).

Each delay circuit output supplies a thyristor drive stage, which contains a transistor and two resistors. When the output of the delay circuit is high (+15 V), a current flows through R_8 (or R_{10}) and transistor TR_1 (or TR_2) turns-on. A current is supplied from the +15 V rail through R_9 (or R_{11}) and the emitter of TR_1 (or TR_2) to the gate of thyristor TH_1 (or TH_2) to turn it on. The thyristor gate current is approximately 120 mA which is greater than the minimum gate current of 100 mA defined in the device data sheet.

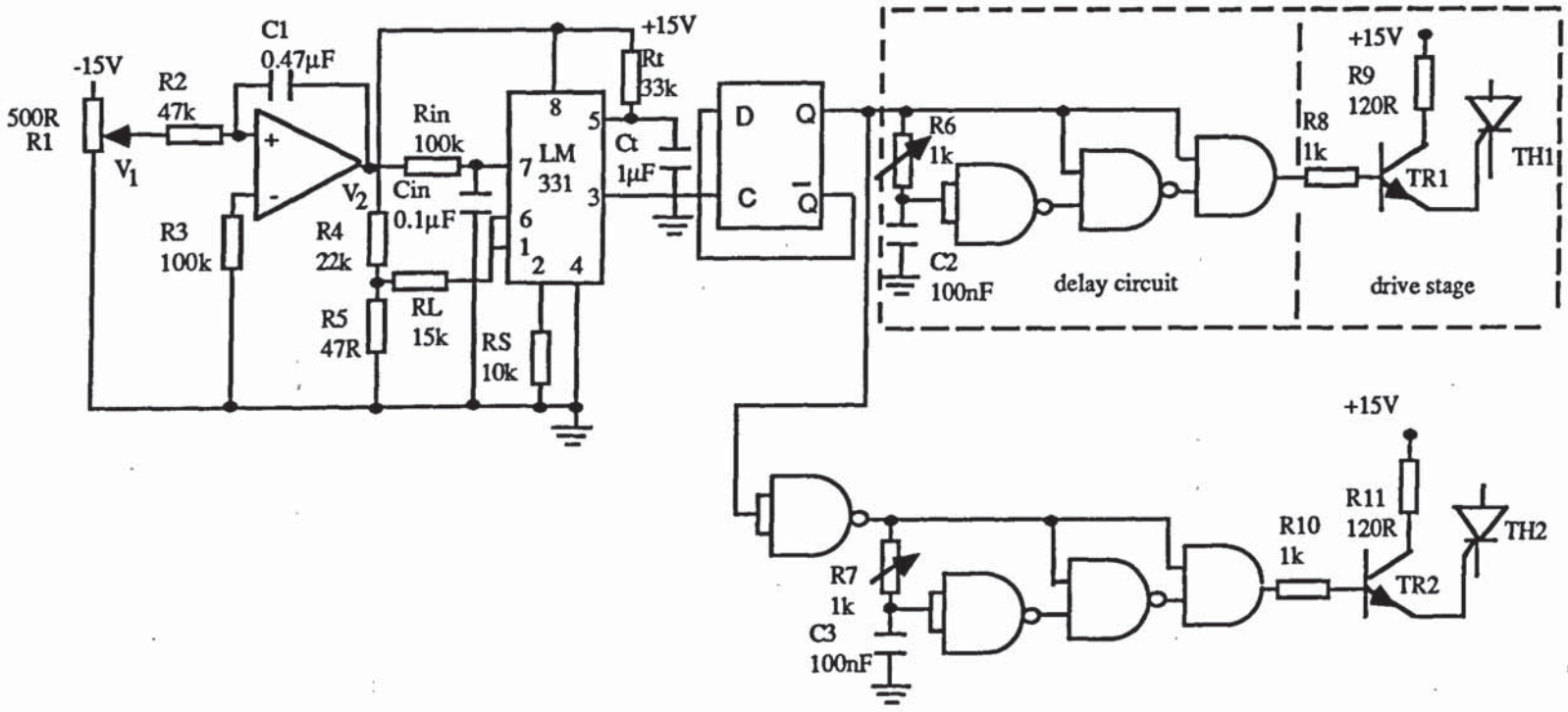
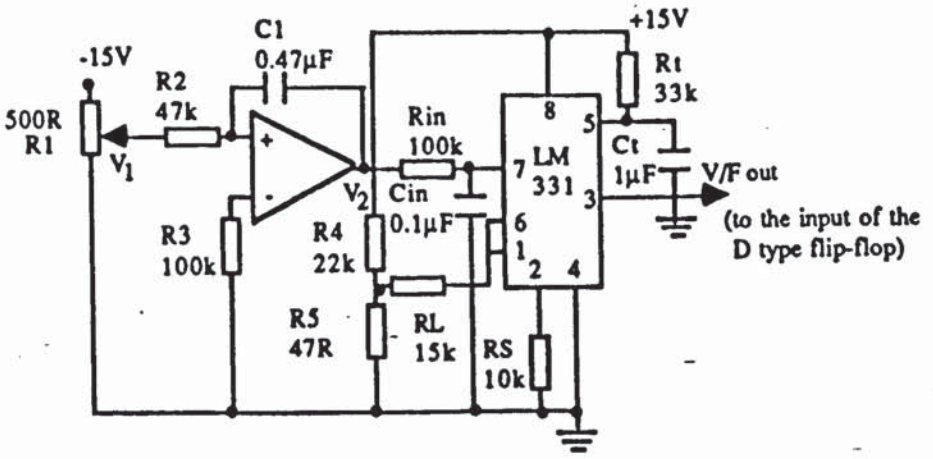
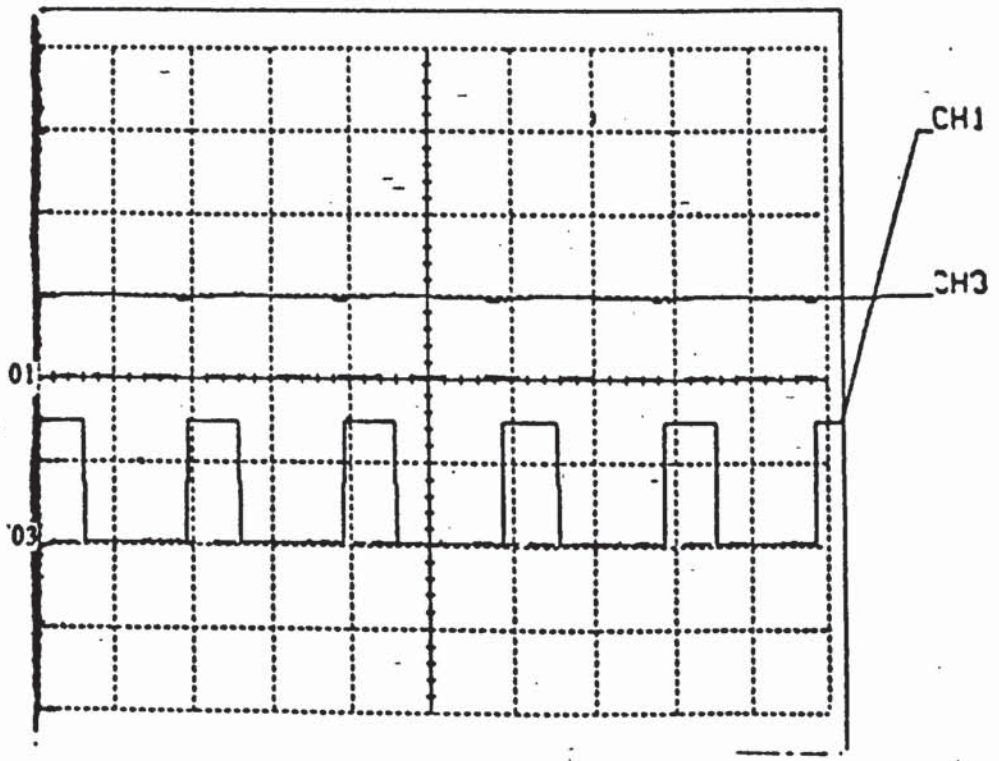


Figure (3-2) Thyristor firing circuit.



(a) Circuit connections.



(b) Circuit waveforms.

Figure (3-3) Integrator and the V/F circuit.
CH1: 10 V/div (output of the V/F).
CH3: 10 V/div (output of the integrator).
Time: 5 ms/div.

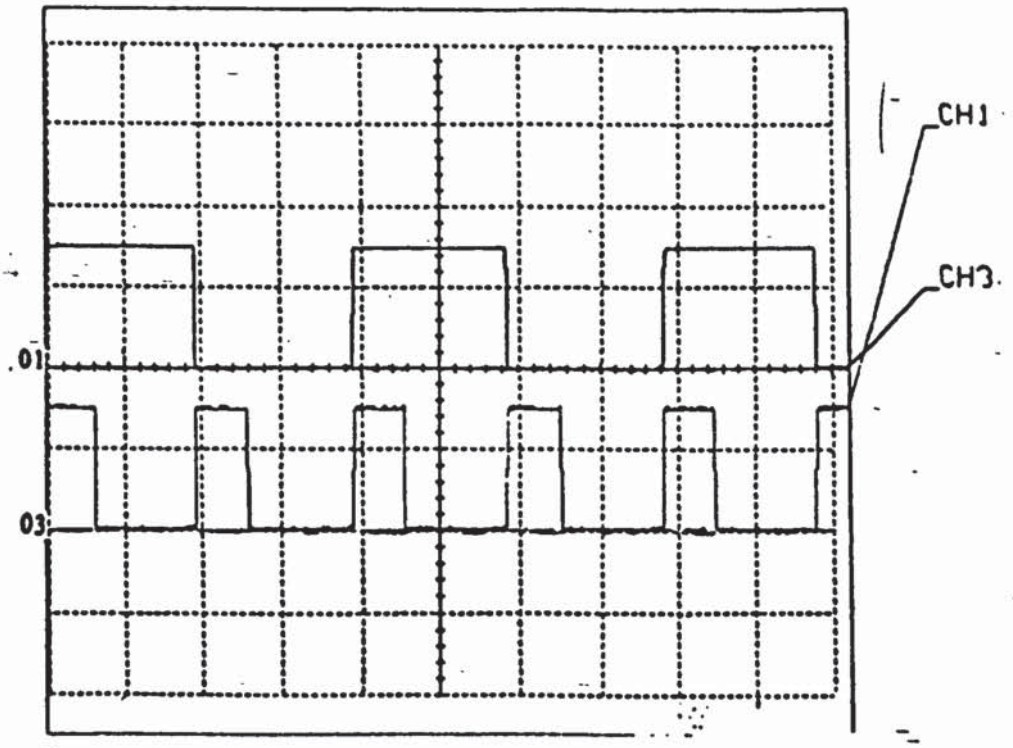


Figure (3-4) Output waveforms of the V/F and the flip-flop.
CH1: 10 V/div (V/F output).
CH3: 10 V/div (D flip flop output).
Time: 5 ms/div.

3-3-2 THYRISTOR TURN-OFF TIME.

A thyristor is turned-off by reducing its anode current to a value less than the holding current which is almost zero. The turn-off time (t_0) is the time required to regain forward blocking capability after forward current has ceased to flow.

The turn-off time of the thyristor operating in a centre tap inverter is given by (67):

$$t_0 = g(x)\sqrt{4LC} \tag{3-4}$$

where:

$$g(x) = \sin^{-1}\left[\frac{x}{\sqrt{x^2+1}}\right] - \sin^{-1}\left[\frac{x}{2\sqrt{x^2+1}}\right] \tag{3-5}$$

and

$$x = \frac{E_d}{I_{pk}}\sqrt{\frac{4C}{L}} \tag{3-6}$$

where:

E_d is the inverter input voltage,

I_{pk} is the peak thyristor current and

L and C are the commutating capacitor and inductance.

The derivation of the above expressions are given in appendix (E).

The centre tap inverters were tested on open-circuit, with a resistive load (R = 42 Ω) and an inductive load (L = 60 mH, R = 25 Ω). These values were chosen to limit the load current to the rating of the inverter (I_{LRMS} = 1.5 A). As mentioned at the beginning of the chapter, the output of the centre tap inverter is 65 V, so the RMS current for a resistive load is:

$$I_{LRMS} = \frac{V_L}{R} = \frac{65}{42} = 1.54 \text{ A}$$

For an inductive load, the load current grows exponentially given by:

$$I_L = \frac{V_L}{R}\left(1 - e^{-tR/L}\right) \qquad (3\text{-}7)$$

To choose the values of inductance and resistance, the following considerations were made. Firstly considering the exponential part of the above equation is much less than 1, the peak load current approximates to:

$$I_{Lpeak} = \frac{V_L}{R} = \frac{65}{25} = 2.6 \text{ A}$$

Secondly, assuming the load current has a triangular waveform, the RMS current is given by:

$$I_{LRMS} = \frac{I_{peak}}{\sqrt{3}} = \frac{2.6}{\sqrt{3}} = 1.5 \text{ A}$$

The turn-off time of the thyristors were investigated and compared with the theoretical results shown in table (3-1) and figures (3-5) to (3-7). It was found that the turn-off time of the two thyristors in each inverter is the same so table (3-1) shows the turn off time of one thyristor in each inverter. The oscillograms show the results for one inverter only, since there is not much difference between the waveforms of the two inverters. The inverter input DC voltage was 22 V (the DC supply is 24 V but there is a 2 V drop in the inverter).

Figure (3-5) shows the turn-off time of one thyristor in inverter (A1) with the transformer secondary open circuited. The peak current through the thyristor is 2 A, by using equations (4,5,6):

$x = 10.77$

$g(x) = 0.95$

$t_0 = 46.55\ \mu s$

Figure (3-6) shows the turn-off time of one thyristor in inverter (A1) with a resistive load. The peak current through the thyristor is 7.2 A, thus:

$x = 2.99$

$g(x) = 0.75$

$t_0 = 36.74\mu s$

Figure (3-7) shows the turn off-time of one thyristor in inverter (A_1) with an inductive load. The peak current through the thyristor is 11 A, therefore:

$x = 1.95$

$g(x) = 0.63$

$t_0 = 30.8\ \mu s$

There is a small difference in the turn-off time between the two inverters, with 5% difference for the resistive load and 7% for the inductive load. There is also a small difference between the theoretical and experimental results of about 2.5%. It is believed that these differences may be related to the losses and tolerances of the commutating capacitor and inductance.

	No load I_{pk}= 2 A	Resistive load I_{pk}= 7.2 A	Inductive load I_{pk} = 11 A
Inverter (A) (TH1, TH2) t_0 in μs	46 (46.5)	36 (36.7)	28 (30.8)
Inverter (B) (TH1, TH2) t_0 in μs	46 (46)	37 (37)	30 (33)

Table (3-1) Turn-off time of the thyristors.

(Theoretical values in brackets)

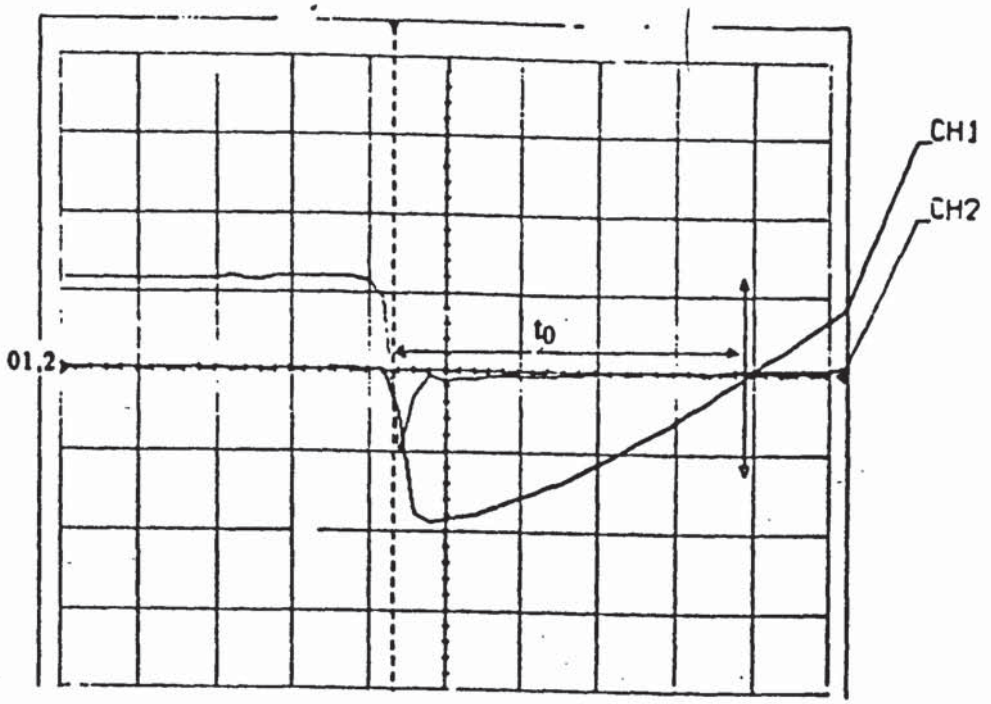


Figure (3-5) Thyristor turn off time on open circuit (A1).
CH1: V_{AK} 20 V/div.
CH2: I_{AK} 1.6 A/div.
Time: 10 μs/div.
t_0 = 46 μs

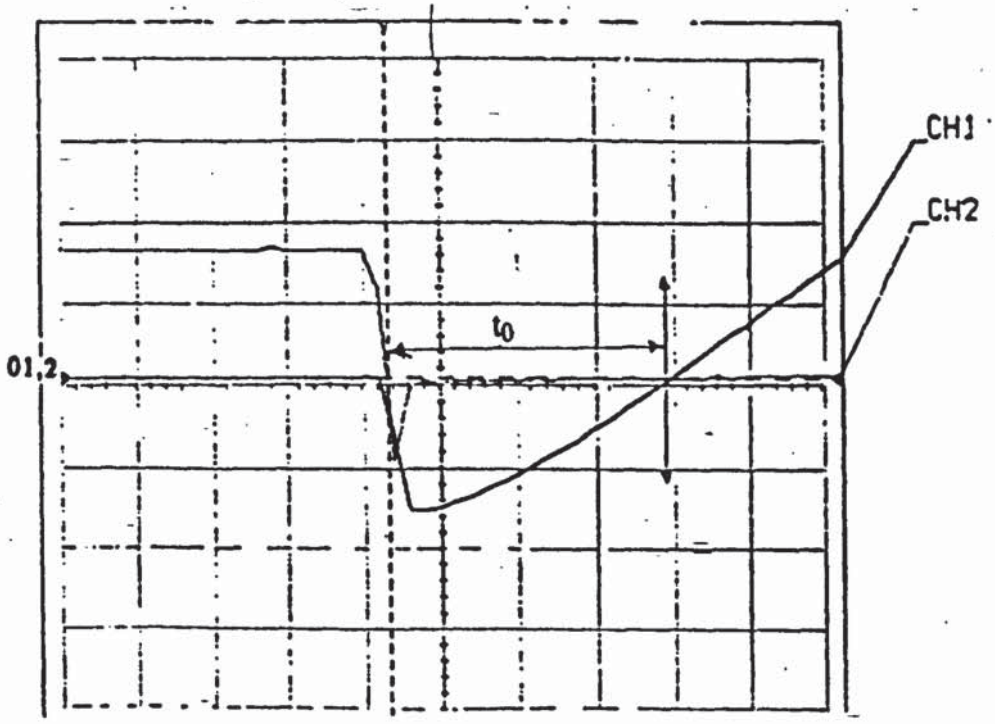


Figure (3-6) Thyristor turn off time with a resistive load (A1).
CH1: V_{AK} 20 V/div.
CH2: I_{AK} 4 A/div.
Time: 10 μs/div.
t_0 = 36 μs.

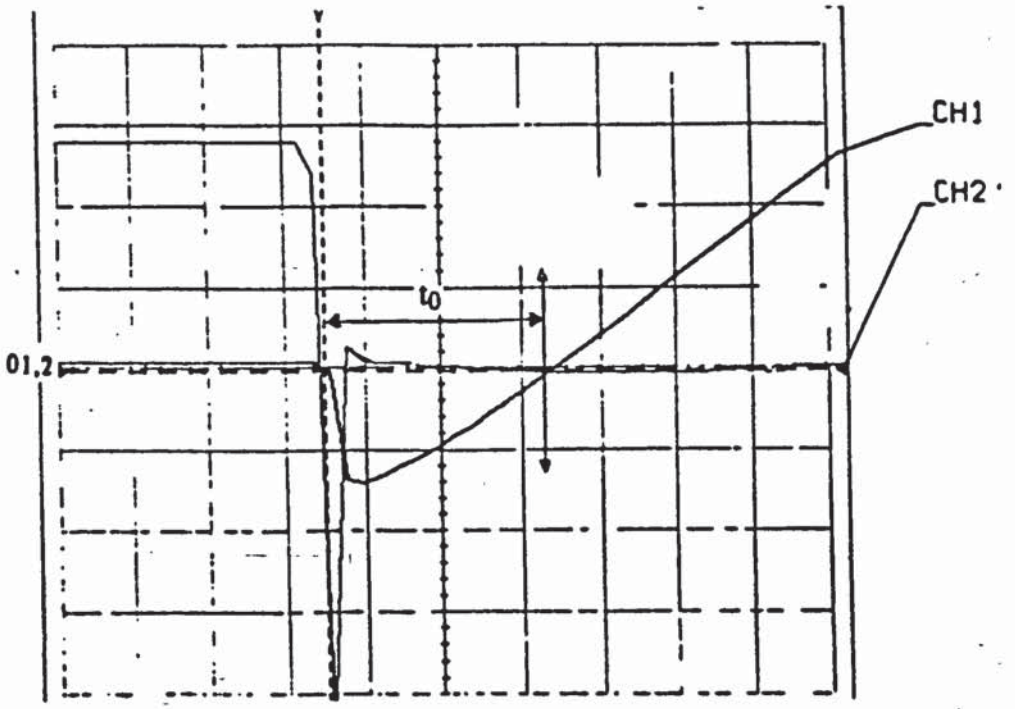


Figure (3-7) Thyristor turn off time with an inductive load (A1).

CH1: V_{AK} 20 V/div.

CH2: I_{AK} 4 A/div.

Time: 10 μs/div.

t_0 = 28 μs.

3-4 GTO INVERTER/RECTIFIER DRIVE PULSES.

The gating pulses for the GTOs in the inverter circuit (B_2) are obtained from a 4047 CMOS astable multivibrator. The outputs of the 4047 were set to give a 50 Hz frequency with a 10 ms pulse width. Figures (3-8) shows the circuit connections for the inverter drive pulses. According to reference (66), the output frequency is:

$$f = \frac{1}{4.4R_1C_1} \text{ Hz} \qquad (3\text{-}8)$$

A delay circuit is connected to each output of the 4047 to prevent the two GTOs from being on simultaneously. The operation of the delay circuit and its use with an inverter control circuit are explained in appendix (C).The delay time depends on the time constant (R_2C_2) and (R_3C_3). It was found that the optimum turn-off time for the GTO was 15 μs. This means a 15 μs time delay must be introduced to the turn-on pulse, to allow the complementary device to turn-off.

As explained previously, when (B_2) operates as a rectifier, $GTOs_{1,2}$ turn-off and $GTOs_{3,4}$ turn-on as controlled devices. In order to synchronize the rectifier drive pulses with the output of the centre tap inverter (B_1), the drive pulses are taken directly from the output of the D type flip-flop of the thyristor firing circuit. Figures (3-9) (a) and (b) respectively show the circuit connections and the waveforms for the rectifier drive pulses. (Note that,the output voltage at the secondary winding of the transformer of the centre tap inverter is shown so that its synchronization with the driving pulses can be seen).

3-5 TRANSISTOR DRIVE CIRCUIT.

When power flows from side (A) to side (B) of the circuit shown in figure (3-1),transistors T_{A1} and T_{B1} turn-on simultaneously to connect the input of inverter (A_1) to the 24 V P.S.U and (B1) to the 12 V battery. Transistors T_{B2} and Ts are turned-off to disconnect the input of inverter (B_1) from the 24 V P.S.U and the output of converter (B_2) from the load.

When power flows from side (B) to side (A) transistors T_{A1} and T_{B1} turn-off to disconnect the centre taps of the transformers (A_1) and (B_1) from the P.S.U and the battery respectively. Transistors T_{B2} turn-on, to connect the 24 V P.S.U. to the input of inverter (B_1), at the same time transistor Ts turn-on to connect the load to the output of converter (B_2) which operates as a rectifier.

Figure (3-10) shows the drive circuit for the four transistors. Since one pair of these transistors is turning-on whilst the other pair is turning-off, two delay circuits are connected to the inputs of their drive circuits to prevent the two transistor pairs ((T_{A1},T_{B1}) and (Ts,T_{B2})) being on simultaneously.

To simplify the explanation of the transistor drive circuit assume that transistor T_{A1} is turning-on. When the input signal is low (0 V), the base of the pnp transistor (T_1) is low and it turns-on. Current flows from the +15 V rail via R_{on} to turn T_{A1} on.

When the input signal is high, the pnp transistor (T_1) turns-off and the voltage drop of the diode D maintains a negative bias between the base and emitter of T_{A1}.

Opto-isolators are used to provide isolation between the control circuit and the base drives of the transistors.

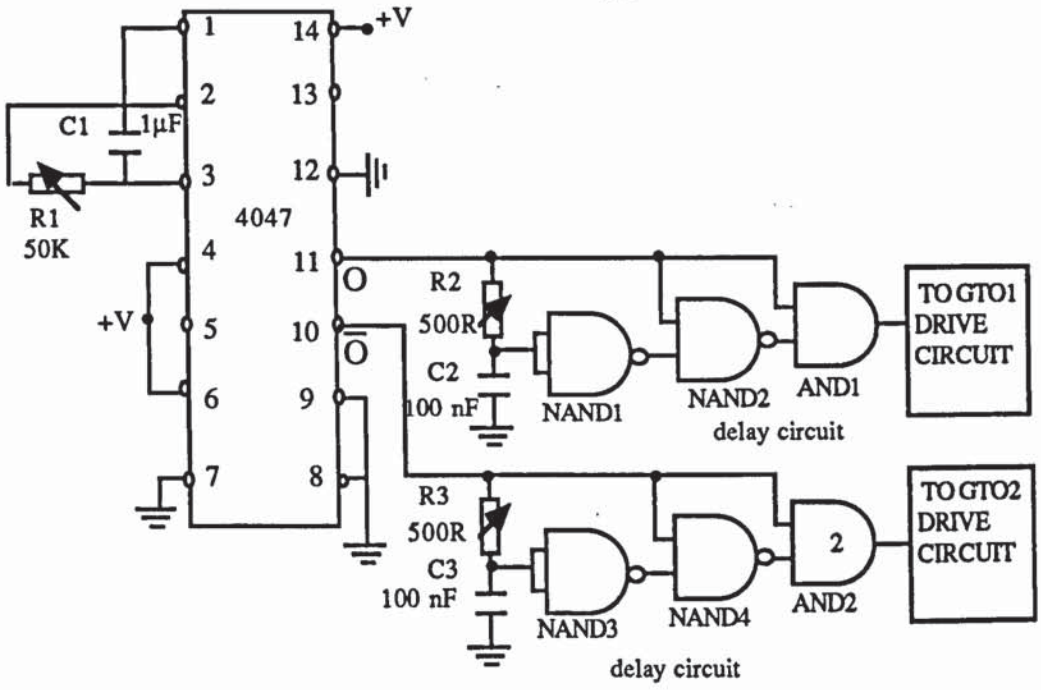
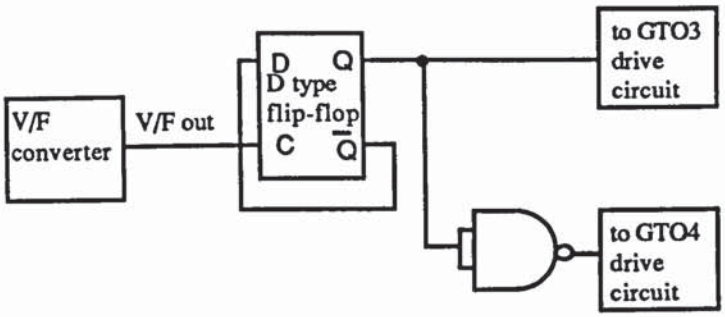
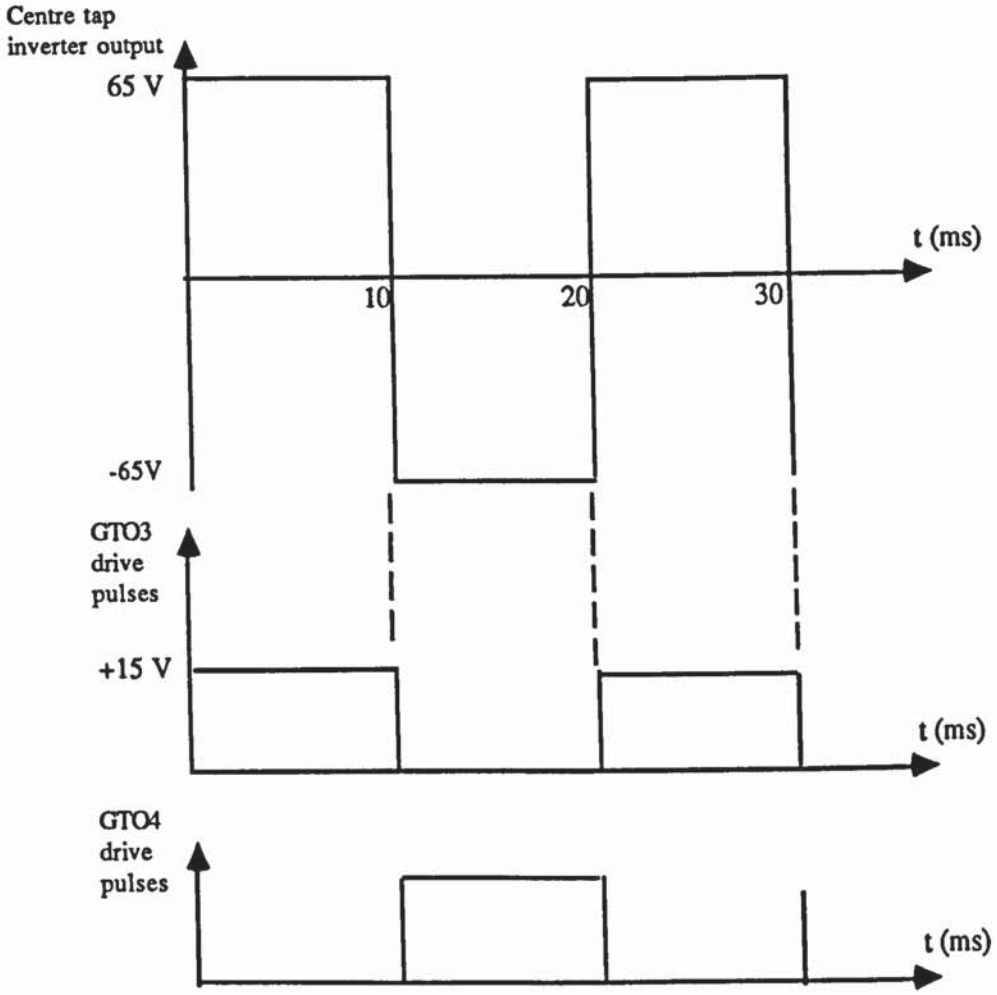


Figure (3-8) GTO inverter drive pulse circuit connections.



(a) Circuit connections.



(b) Circuit waveforms.

Figure (3-9) GTO rectifier drive pulse circuit.

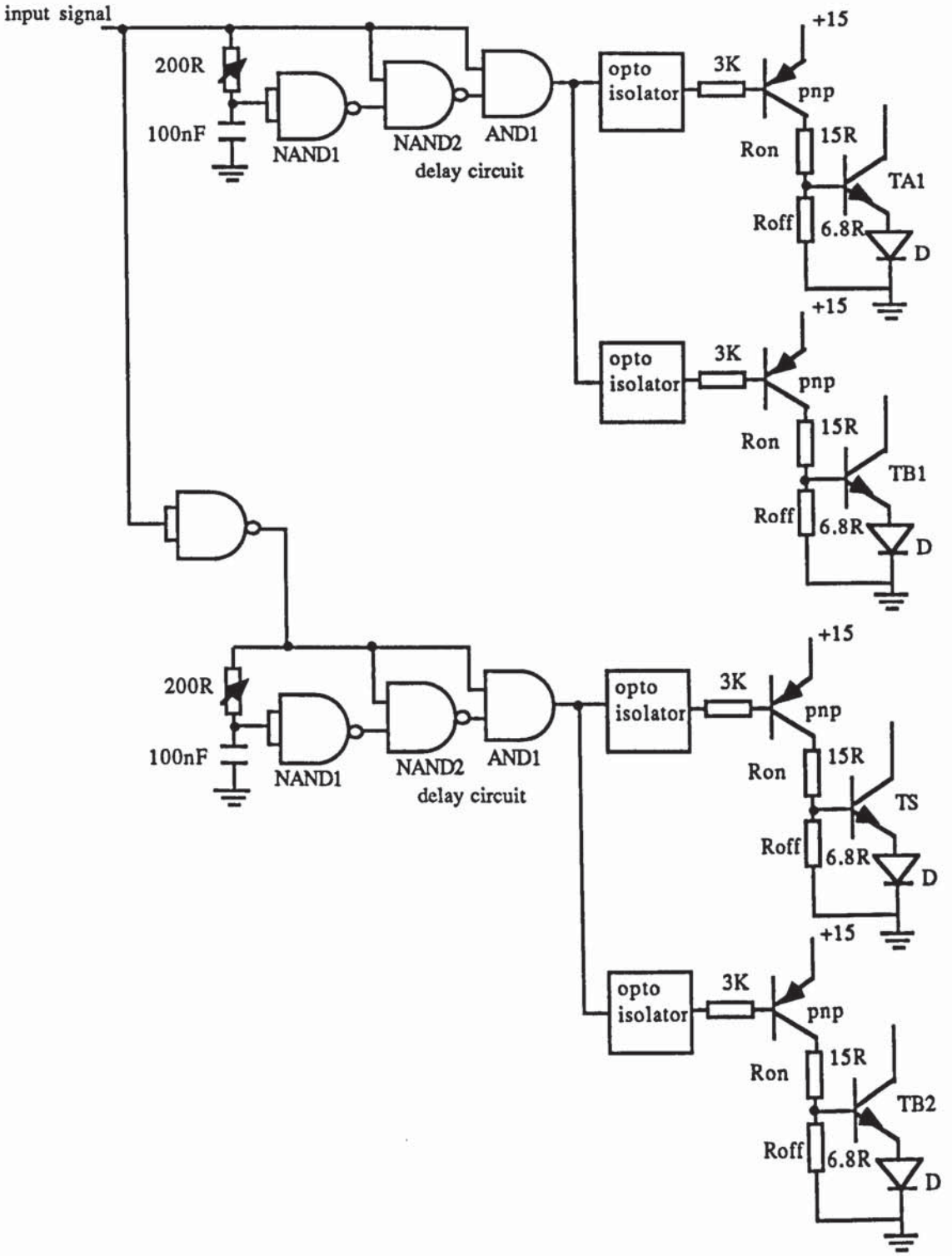


Figure (3-10) Transistor drive circuits.

3-6 CONTROL CIRCUIT.

The control circuit of the system shown in figure (3-1) was designed to provide the correct signals to drive the switching devices (transistors, thyristors and GTOs) to send power in both directions. One limitation of this particular control circuit is that it can be controlled from side (A) only. Figure (3-11) shows the connections of the system control circuit. By changing the state of the comparator output, the signals will transfer from one group of devices to another depending on the required direction of the power flow.

As can be seen from figure (3-11), one input of the comparator (V_1) is used as a fixed 7.5 V reference, the other input (V_2) can be varied by means of the variable resistor R_4. When V_2 is higher than V_1, the comparator output is low. When V_2 is lower than V_1, the comparator output changes state from low to high level (note that low level means zero and high level means 15 V).

Table (3-2) shows the switching sequences of the control circuit when power flows in both directions. Assuming that power flows from side (A) to (B). (V_2 must be higher than V_1) the comparator output is low (0 V), point (X) is high and (Y) is low. Therefore:

1) Transistor T_{A1} turns-on and P.S.U.A_1 supplies the inverter (A_1).

2) The thyristor firing circuit feeds the drive stages of thyristors $TH_{1,2A}$ and (A_1) operates as an inverter to supply the rectifier diode bridge (A_2).

3) The switch transistor T_S turns-off and the rectifier diode bridge (A_2) supplies the converter (B_2).

4) $GTO_{3,4}$ operate as diodes (always on) and $GTO_{1,2}$ turn-on, (B_2) now operates as an inverter to supply the converter (B_1).

5) Transistors T_{B1} turn-on and T_{B2} turn-off. Converter (B_2) is connected to the battery, at the same time, thyristors $TH_{1,2B}$ turn off, (B_2) operates as a rectifier and the battery charges via the diodes.

When reverse power is required, the voltage V_2 must be reduced to a value less than 7.5 V , point (X) changes to low state and (Y) changes to high state therefore:

1) Transistor T_{A1} turns-off and the P.S.U.A_1 is disconnected from inverter (A_1).

2) The thyristor firing circuit is disconnected from the drive stage of thyristors $TH_{1,2A}$ to turn them off.

3) Transistor T_{B1} turns-off and T_{B2} turns-on and converter (B_2) is connected to the (P.S.U.B_1). At the same time thyristors $TH_{1,2B}$ turn-on and (B_2) operates as an inverter to feed (B_2).

4) $GTOs_{3,4}$ turn-on to operate as controlled devices and $GTOs_{1,2}$ turn-off, B_2 operates as a rectifier to supply the load .

5) The switch transistor Ts turn-on to connect the load to the output of (B_2).

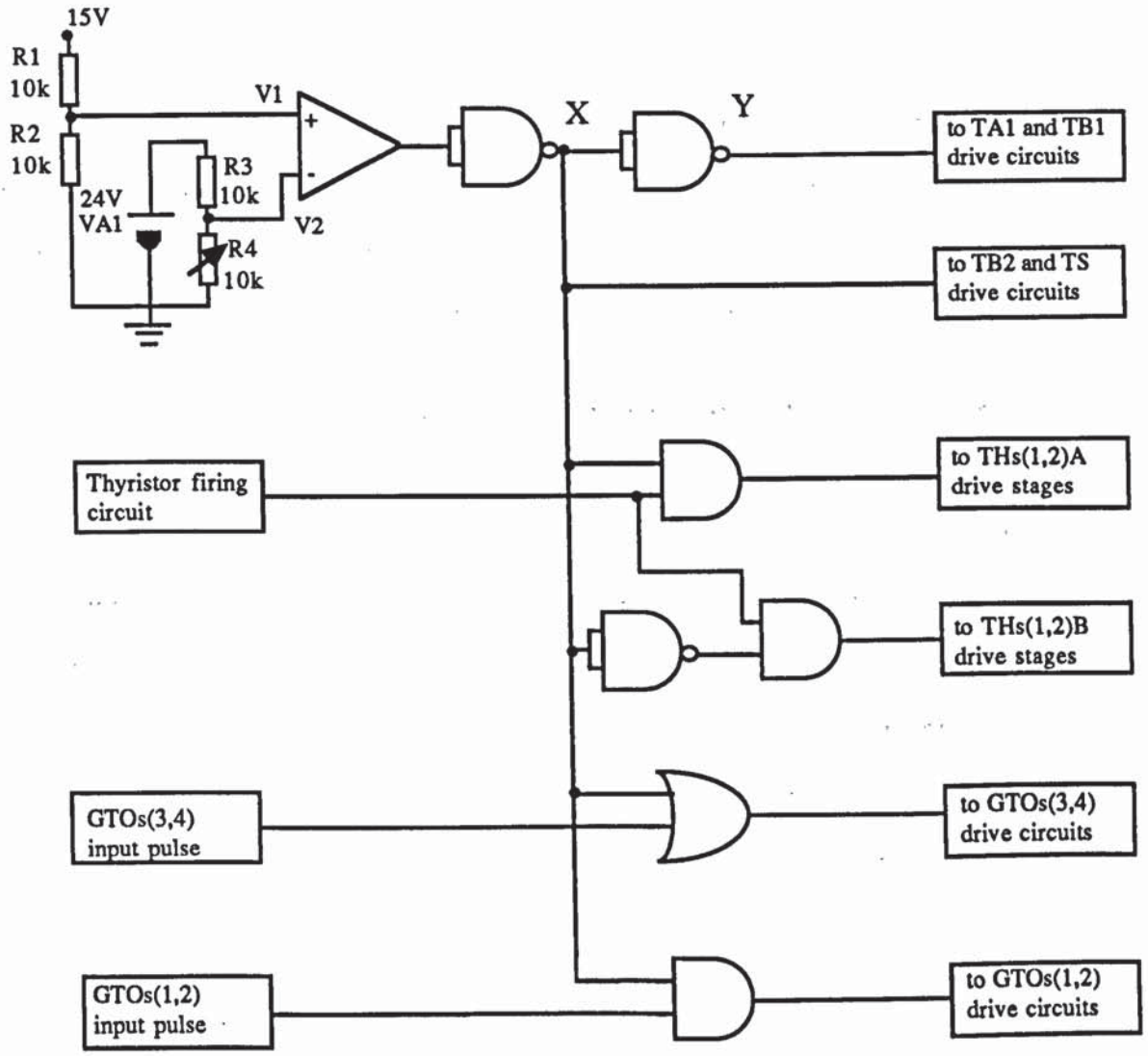


Figure (3-11) Control circuit connections.

	X	Y	TA1	TB1	TB2	TS	TH 1,2 A	TH 1,2 B	GTO 1,2	GTO 3,4
Power A TO B V2>V1	high	low	on	on	off	off	on	off	on	operate as diodes
Power B TO A V2<V1	low	high	off	off	on	on	off	on	opertate as diodes	on

Table (3-2) Switching sequences of the control circuit.

3-7 POWER FLOW IN TWO DIRECTIONS.

Referring to figure (3-1), a centre zero ammeter was connected in the rail between the load and converter B_2 to observe the direction of the power flow. Meanwhile, some problems occurred when the change over of the power flow takes place. These problems have prevented recording the voltage and current waveforms of the GTOs .

As mentioned at the beginning of this chapter when converter (B_2) operates as an inverter, the current flows through GTO_1 and C_1 during one half cycle and GTO_2 and C_2 during the other. However when converter (B_2) operates as a rectifier, the capacitors affect its input and output voltage and current waveforms. The reason is that the current charges the capacitors first and then it continues to flow through the load. It was found that the capacitor charging current is high compared with the current rating of the power supply unit. Thus the power supply unit of (B_1) ($P.S.U_{B1}$) collapses because this type of power supply is automatically limited to 5 A.

The results in figures (3-12) and (3-13) show the oscillograms of the input voltage and current of (B_2). In figure (3-12), C_1 and C_2 have been removed, it can be seen that both the output voltage and the current of the centre tap inverter (B_1) are square waves with 65 V and 1.5 A peak. In figure (3-13) ($C_1 = C_2 = 100\ \mu F$) have been connected, the capacitor currents are quite high (about 7A giving 14 A on the primary side). Also the peak output voltage is reduced to 50 V and the peak output current to 1.25 A. It has been observed that the input DC voltage of the centre tap inverter (B_1) (PS.U.B_1) has collapsed from 24 V to 20 V which means that the power supply unit is over loaded.

Since the rating of the system is very low compared with the rating of the GTOs, it was decided to proceed with the main project, to observe the transfer of the current between two GTOs when change over occurs.

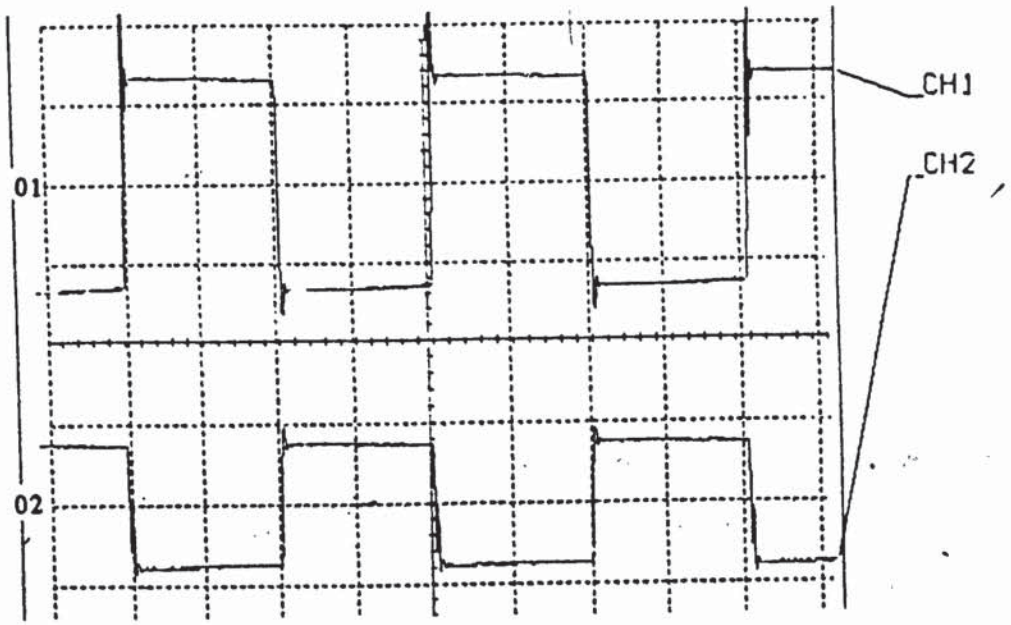


Figure (3-12) Output voltage and current of inverter B2.
($C_1 = C_2 = 0$).
CH1: Output voltage 50V/div.
CH2: output current 2A/div.
Time: 5 ms/div.

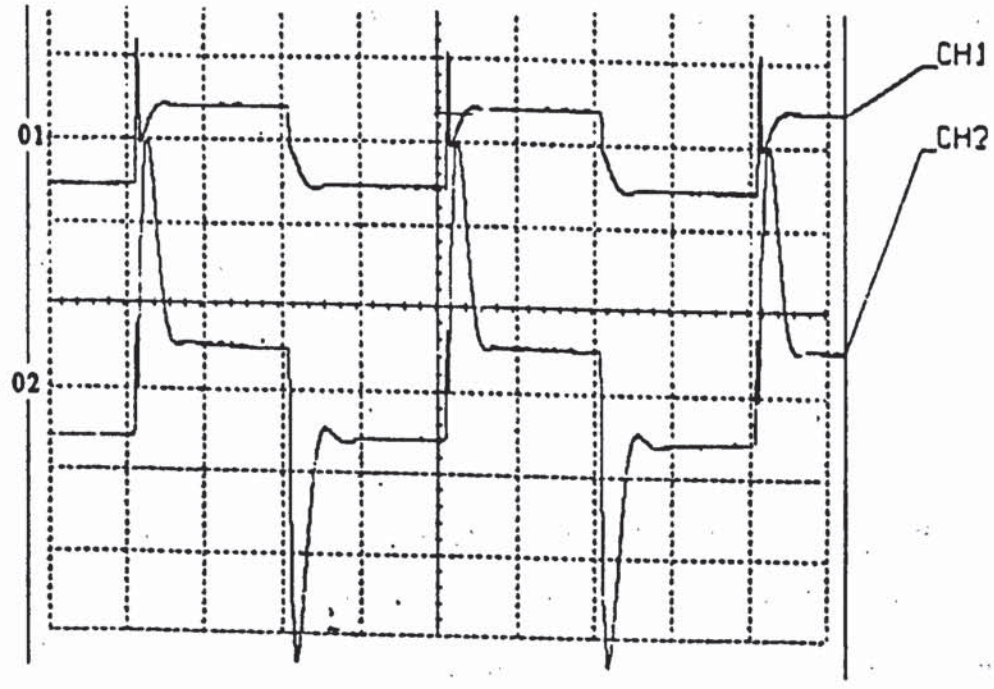


Figure (3-13) Output voltage and current of inverter B2.
($C_1 = C_2 = 100\ \mu F$).
CH1: Output voltage 100V/div.
CH2: Output current 2A/div.
Time: 5 ms/div.

CHAPTER FOUR

SINGLE PHASE TWO WAY POWER FLOW

4-1 INTRODUCTION.

It was mentioned in Chapter 1 that the original objective of the project was to build and study a three-phase system. However due to various technical difficulties and the lack of time, it eventually proved necessary to base the project on a single-phase system. The chapter deals with the operation of the system and the control circuit. The experimental results obtained from the system are presented in the next chapter.

4-2 SYSTEM OPERATION.

Figure (4-1) shows a single phase arrangement for sending power in two directions. The essential differences between this system and the one described and discussed in Chapter 3 run as follows:

a) The preliminary single-phase system has a 100 W rating whereas this system has 1 kW rating.

b) The first system contains a half bridge GTO converter while this system contains two full GTO converter bridges which are connected in series.

When power flows from side (A) to (B), transistor TR_A turns-on to connect the AC mains to the input of converter (A) which operates as a rectifier. This can be achieved by turning $GTOs_{(2,6,4,8)A}$ on as controlled devices and turning $GTOs_{(1,5,3,7)A}$ off. The output of rectifier (A) feeds the input of converter (B). (B) operates as an inverter, by turning $GTOs_{(2,4,6,8)B}$ on as diodes and turning $GTOs_{(1,5,3,7)}$ on to carry the inverter current. Transistor TR_B is turned-off to disconnect converter B from the AC mains and the power from (B) is dissipated in

the load. The load is connected permanently, in order to absorb the transient. Table (4-1) shows the switching sequence of the devices.

When reverse power is required, transistor TR_A is turned-off to disconnect converter (A) from the AC mains. Transistor TR_B is turned-on to connect converter (B) to the mains. (B) transfers from inverter to rectifier operation by turning $GTOs_{(1,7,3,5)B}$ off and $GTOs_{(2,8,4,6)B}$ on as controlled devices. The output of (B) feeds converter (A) which transfers from rectifier to inverter operation by turning $GTOs_{(2,8,4,6)A}$ on as diodes and $GTOs_{(1,7,3,5)A}$ on to carry the inverter current. The output of inverter (A) is connected to the load to dissipate the power.

The reason for using a transistor switch at the output of each converter is that the system is not synchronized with the mains as mentioned in Chapter 1.

The GTO gate drive circuits were assembled on printed circuit boards (PCBs). To prevent any interference between the gate drive circuits, a separate ready made DC power supply was used for each circuit. Each power supply unit has three DC output voltages, (+15 V, -15 V and +5 V) and it was placed directly on the gate drive PCB and this was mounted close to the GTO to reduce the length of the wire connections. Each GTO has been fitted with a suitable heat sink to provide cooling for the device (the calculation of the heat sink is given in appendix F). Figure (4-2) shows the system block diagram. The whole system was assembled in a single rack and figure (4-3) to (4-7) show some photographs for different parts of the system.

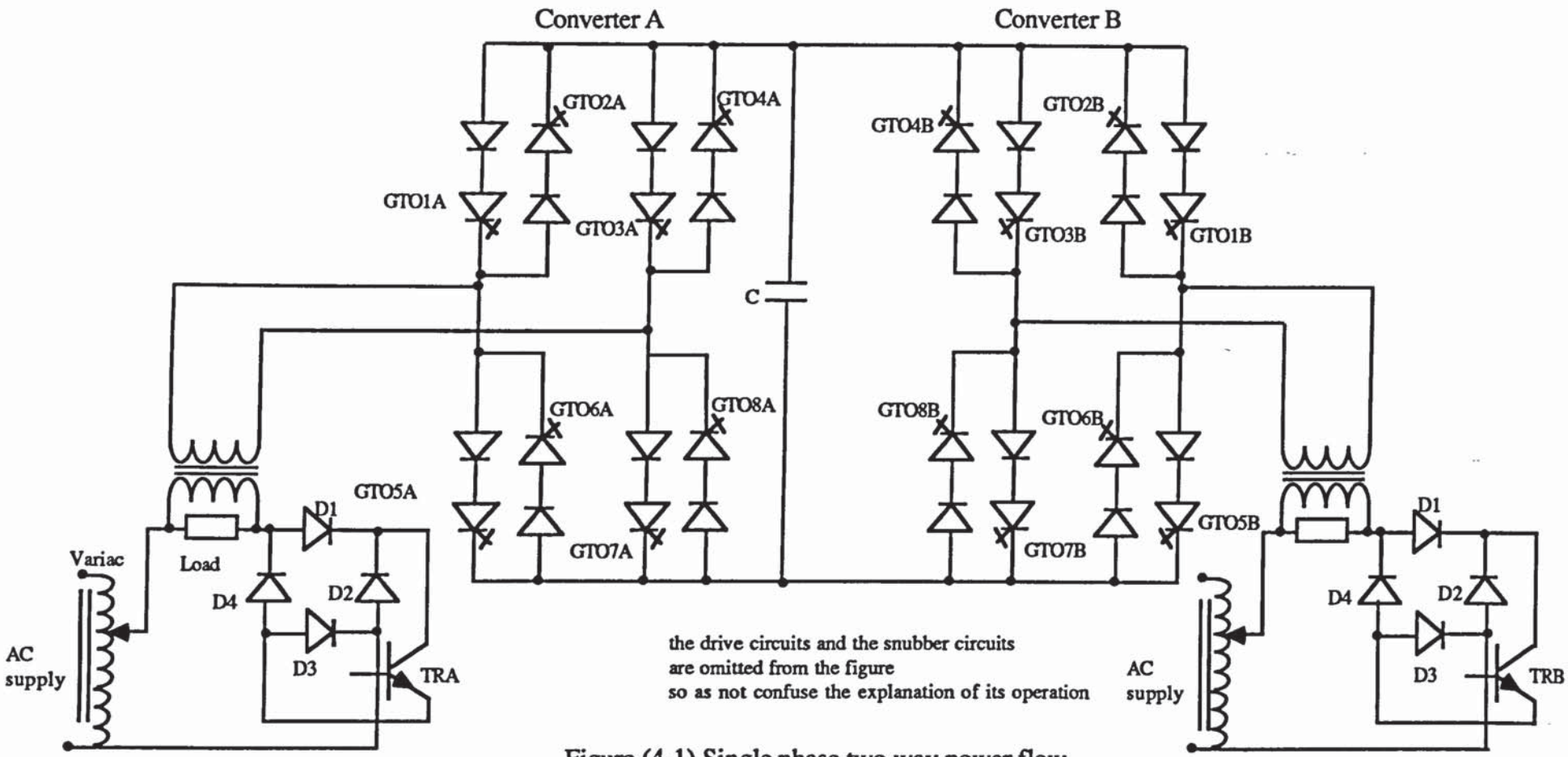


Figure (4-1) Single phase two way power flow.

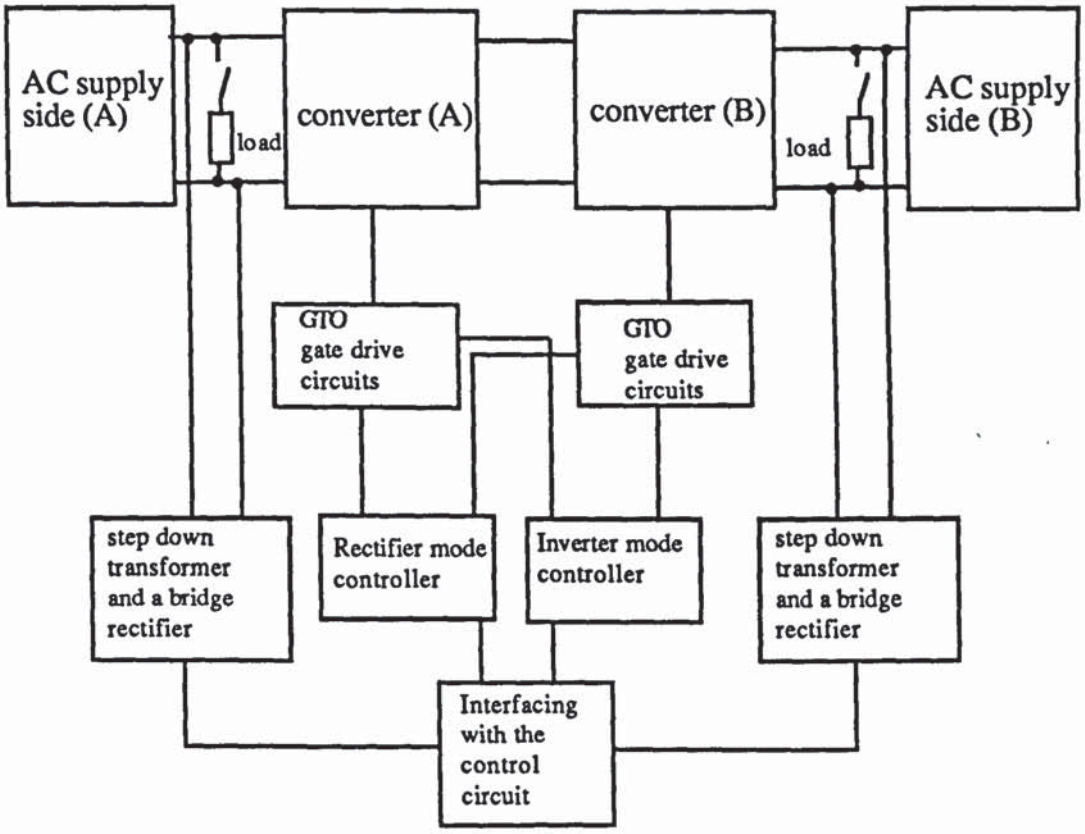


Figure (4-2) System block diagram.

	GTOs (2,8,4,6) A	GTOs (1,7,3,5) A	Transistor TRA	GTOs (2,8,4,6) B	GTOs (1,7,3,5) B	Transistor TRB
Power from A to B	on A operates as a rectifier	off	on	on GTOs operate as diodes	on B operates as an inverter	off
Power from B to A	on GTOs operate as diodes	on A operates as an inverter	off	on B operates as a rectifier	off	on

Table (4-1) Switching sequence of the devices.

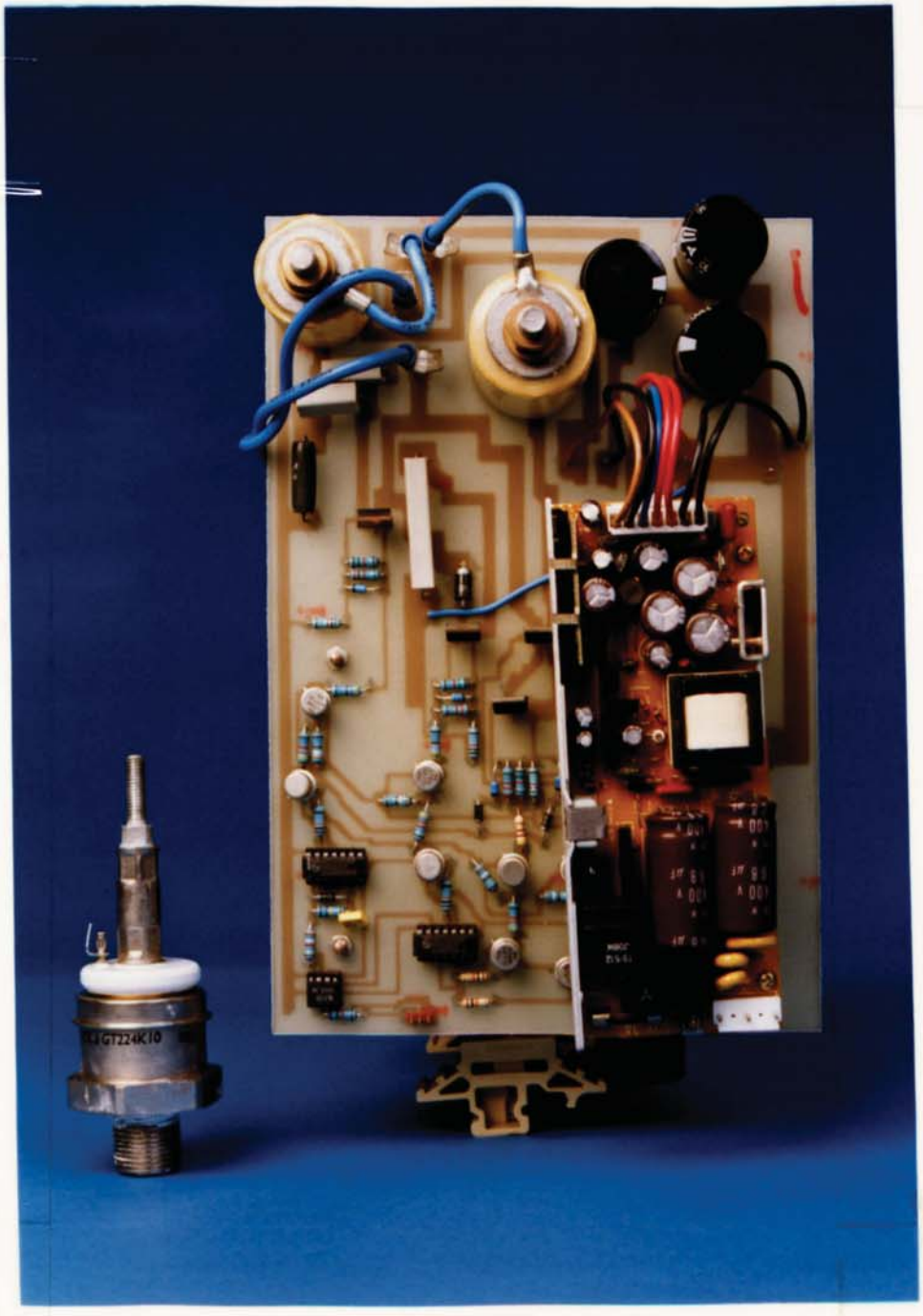


Figure (4-3) Photograph of the GTO and its gate drive circuit.

(The PSU appears in the right corner of the photograph)

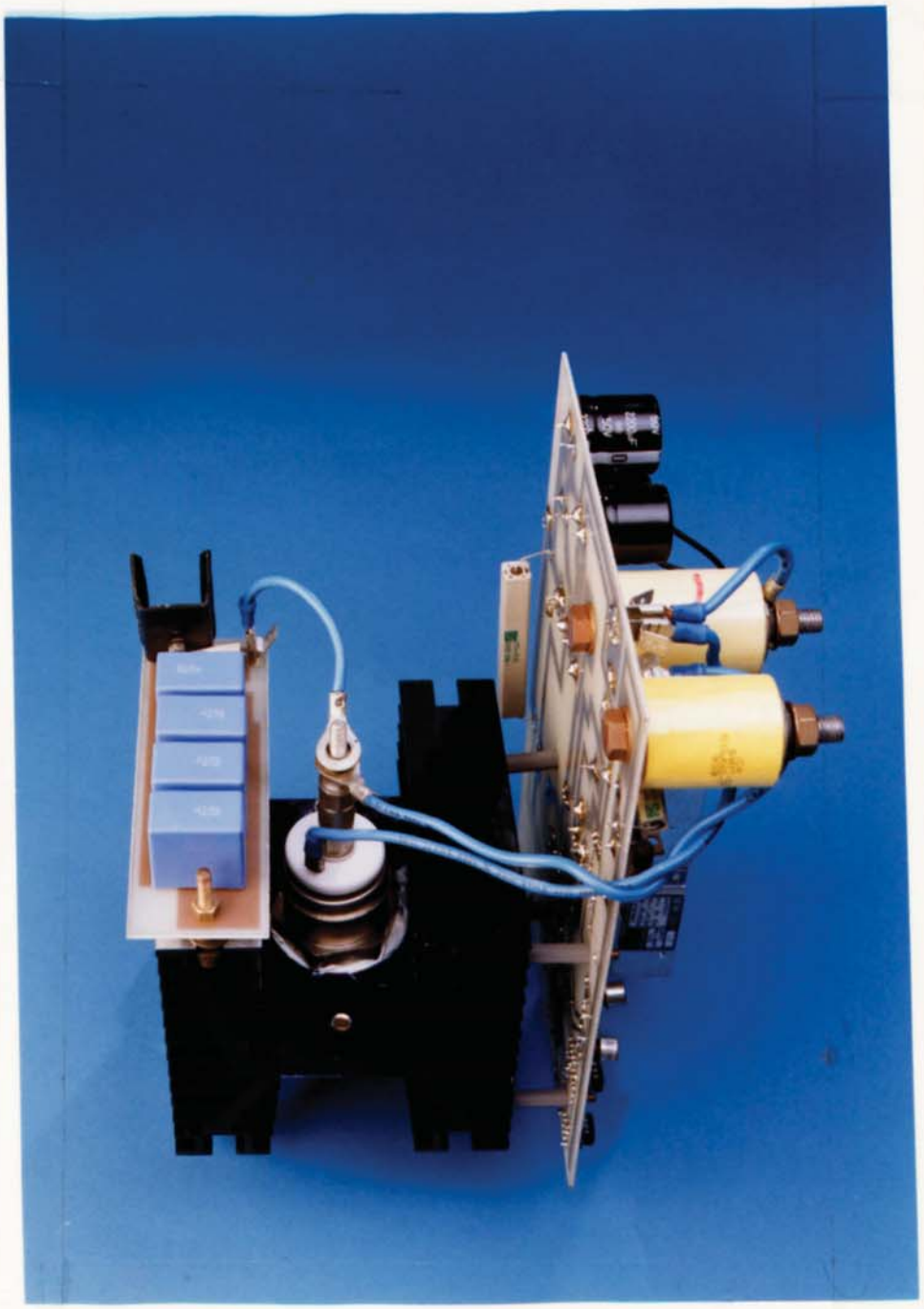


Figure (4-4) Photograph showing the GTO mounted on the heat sink, the snubber circuit and the connections from the gate drive circuit.
(The snubber circuit appears on the left hand side of the heat sink)

Figure (4-5) Photograph showing converter (A) of the single phase system. the resistors on the left hand side represent the load.

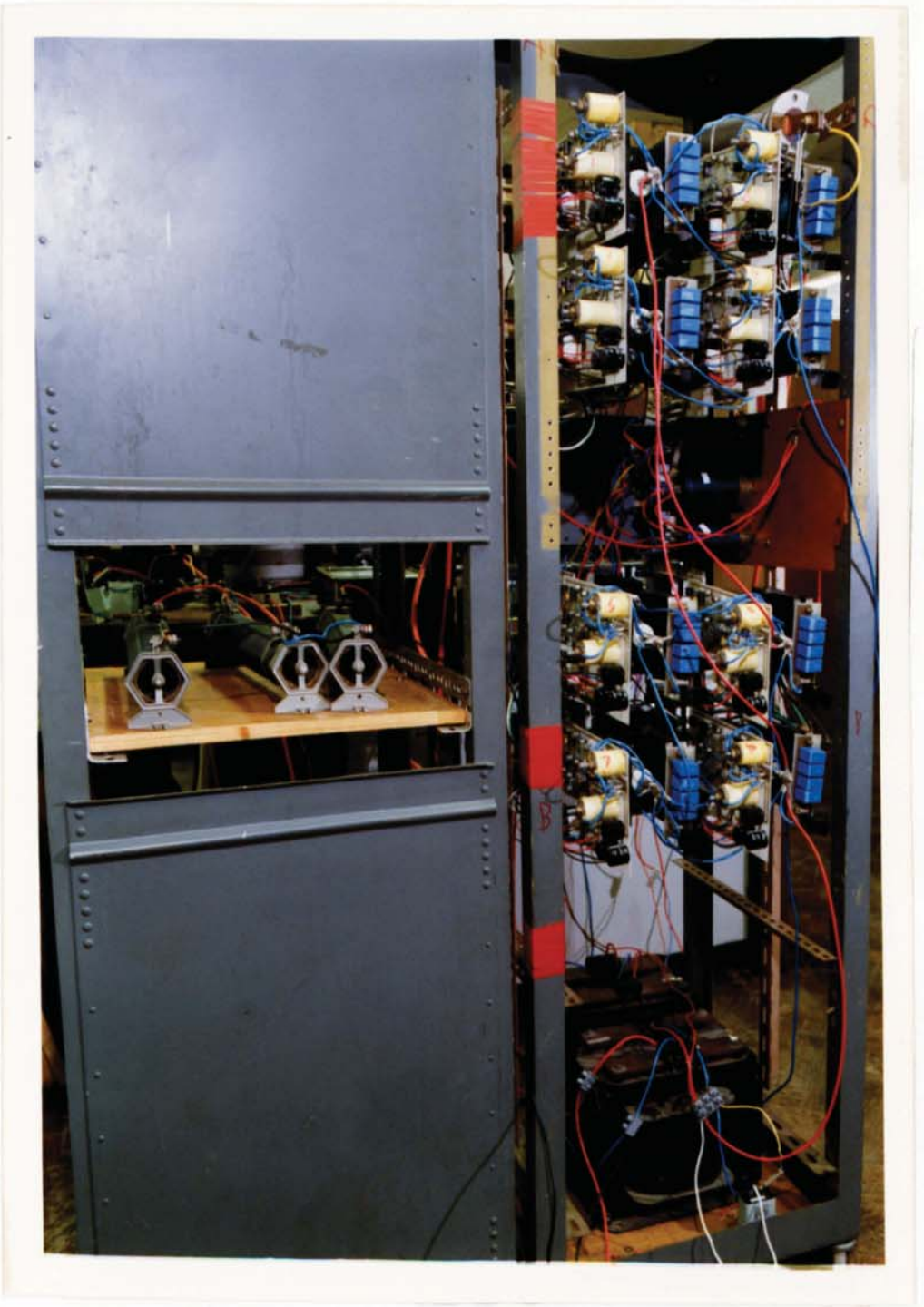


Figure (4-6) Photograph showing converter (B) of the single phase system.

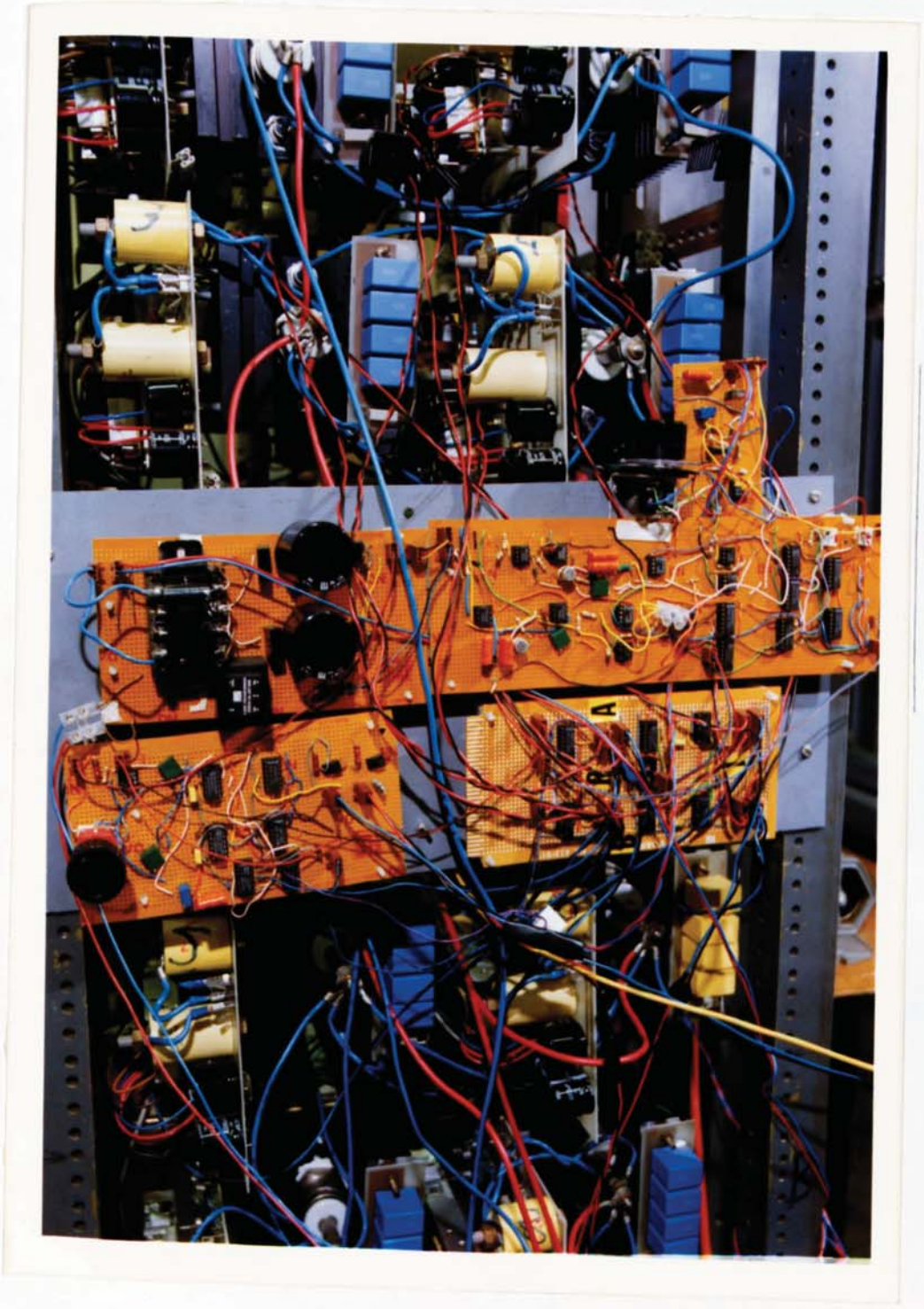


Figure (4-7) Photograph showing different parts of the system control circuit.

4-3 SYSTEM CONTROL CIRCUIT.

It was mentioned in the previous section that both converters may be operated either as a rectifier or an inverter, depending on the direction of power flow. The control circuit designed to operate each converter in the required mode. The control circuit itself comprises several parts which will be discussed and explained individually; these are:

a) Rectifier control circuit.

b) Inverter drive pulse generator.

c) Transistor drive circuit.

4-4 RECTIFIER CONTROL CIRCUIT.

The most commonly used circuit for varying the load voltage and current of a controlled rectifier is the phase angle control (47) which controls the firing delay angle α. The angle α is measured from the natural commutation point which in the single phase is the same point of the zero crossing for each half cycle.A new circuit was designed to control the load voltage and current from both ends of each half cycle, the advantage of this scheme is discussed in the next chapter. The control angle from the beginning of a half cycle is defined as α while that from the end of the half cycle is β. To control these angles, a ramp wave is compared with an adjustable DC voltage. The operation and design of the circuits which generate these angles are explained individually. Figures (4-8) and (4-9) show respectively the block diagram and the circuit connections for the rectifier control circuit.

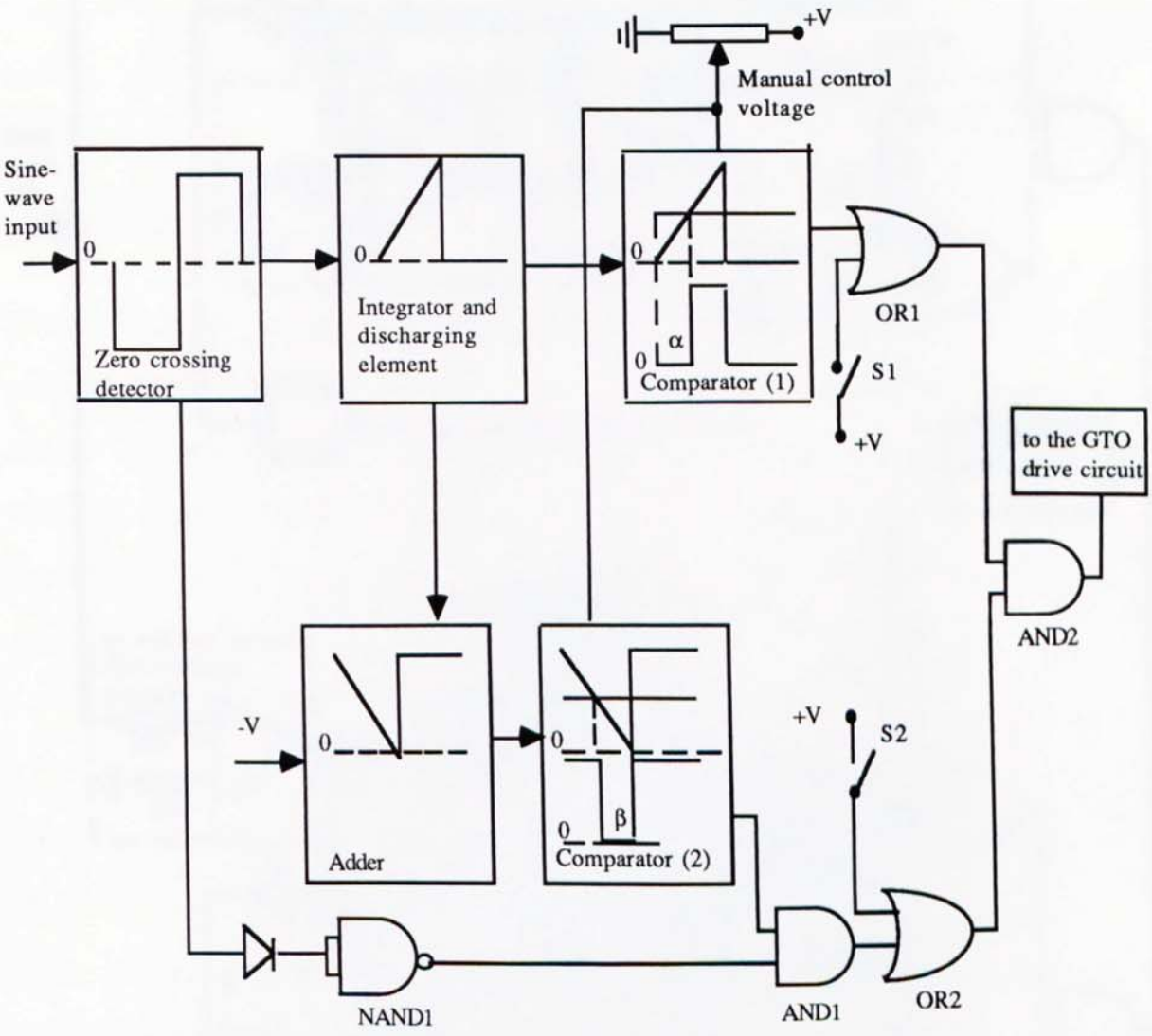


Figure (4-8) Rectifier control circuit block diagram.

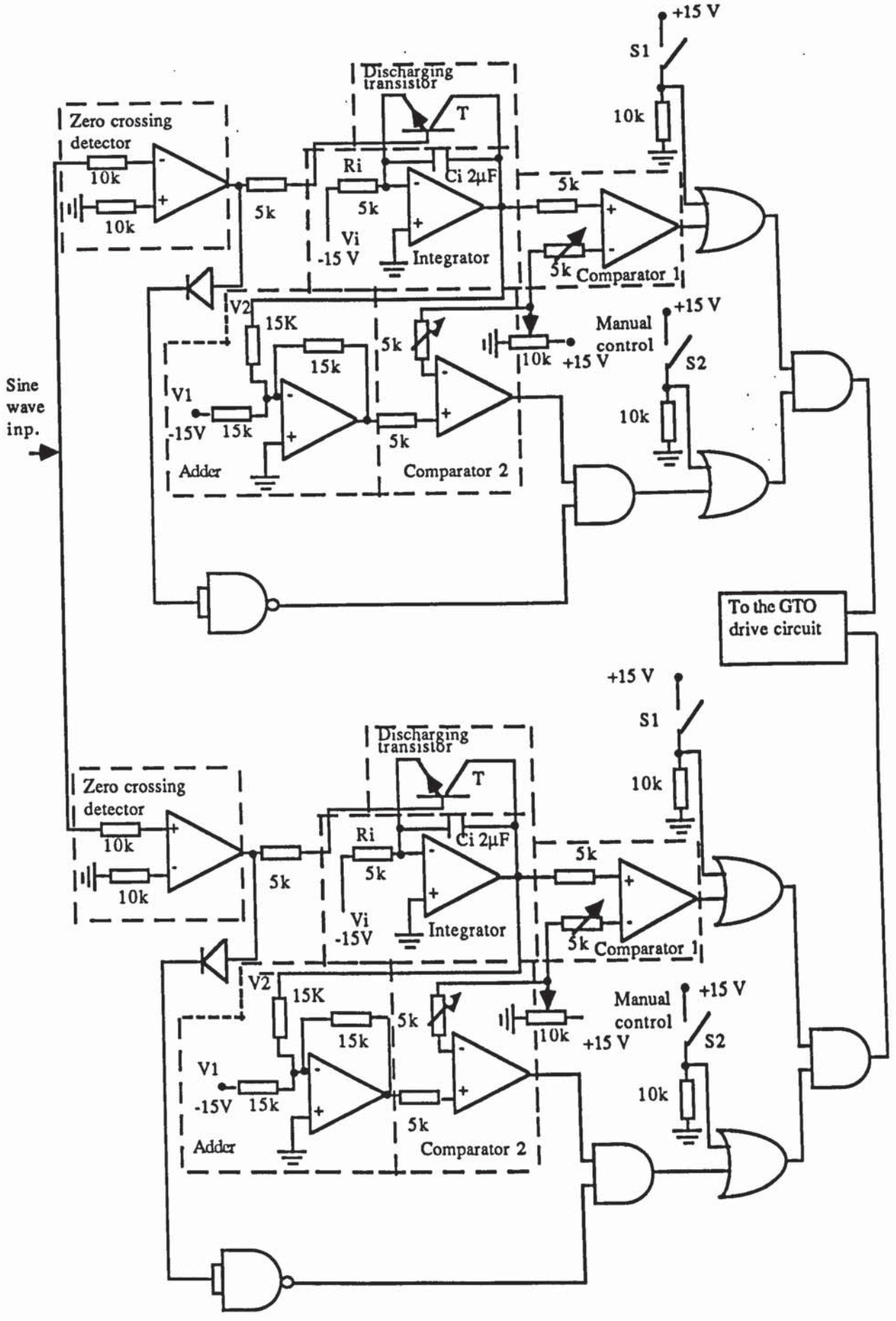


Figure (4-9) Connections of the rectifier control circuit.
The upper part is for a positive half cycle and the lower one for a negative half cycle.

4-4-1 ZERO CROSSING DETECTOR.

The zero crossing detector (ZCD) provides synchronization of the rectifier control circuit with the AC mains. It operates as a squarer which transforms the sinusoidal input waveform to a square wave. The squarer input is obtained from the 15 V secondary winding of a single phase transformer whose primary is connected to the mains. When the input signal is positive, the output of the squarer saturates to the positive supply and when the input is negative,the output saturates to the negative supply.

4-4-2 INTEGRATOR.

The integrator uses a 741 operational amplifier with a capacitive feed back, the input is connected to the negative voltage rail (-V). A transistor T is connected in parallel with the capacitor as shown in figure (4-9) with its base connected to the output of the ZCD. When the output of the ZCD is negative, T is turned-off and a current flows through Ri to charge the capacitor, such that the integrator gives a ramp function (65):

$$V_{out} = \frac{-1}{R_i C_i} \int V_i \, dt \qquad (4\text{-}1)$$

When the input signal is positive, transistor T turns-on and the capacitor discharges via T. The output of the integrator is reset to the voltage drop across the transistor which is assumed to be zero. Figure (4-10) shows the input and output voltage waveforms of the zero crossing detector and the integrator output.

4-4-3 CONTROLLING ANGLES α and β.

Refer to figures (4-8) and (4-9), the output ramp from the integrator is compared with an adjustable DC voltage. When the DC voltage is larger than the ramp voltage, the output of the comparator is zero, and when the DC voltage is lower than the ramp voltage, the output is high (+15 V). The angle α is varied by changing the level of

the DC voltage using a variable resistor. Figure (4-11) shows the waveforms for controlling angle α. The comparator output, together with other signals from other parts of the control circuit supply the gate drive circuit of a group of GTOs when the rectification mode is required.

To control the angle β, the integrator output is inverted and compared with the same DC voltage used to control angle α. This can be achieved by an operational amplifier used as an adder. The integrator output is added to a constant negative voltage as shown in figure (4-12). The output of the adder is calculated in the following way (65):

The input current I equals:

$$I = \frac{V_1}{R_1} + \frac{V_2}{R_2} \qquad (4\text{-}6)$$

The adder output voltage equals:

$$V_{out} = -IR_3 \qquad (4\text{-}7)$$

Substitute equation (6) into (7) and let $R_1 = R_2 = R_3$:

$$V_{out} = -(V_1 + V_2) \qquad (4\text{-}8)$$

Figure (4-13) shows the method for controlling angle β, which is varied by altering the DC level at the input of the comparator. As shown in figure (4-13), the comparator output goes to a high state (+15V) after an angle β but in fact this must be low until the beginning of the following cycle, so an AND gate is used to eliminate the unwanted part from the output signal of the comparator.

When angle α is used to control the load voltage and current, the rectifier operates as a natural commutation converter. The GTO then automatically turns-off when its current goes through a natural zero, and a reverse voltage appears across the GTO. When angle β is used to control the load voltage and current, the rectifier operates as

a forced commutated converter and the GTO turns-off by applying a negative gate-cathode voltage.

Figure (4-14) shows the method for controlling angles α and β which could be achieved by changing the state of the manual switches S_1 and S_2.

1) When S_1 is open and S_2 closed, the output of OR_1 is the same as the output of circuit(1) and the output of OR_2 is high. The output of the AND gate is the same as the output of circuit(1) and this gives α control.

2) When S_1 is closed and S_2 open, the output of OR_2 is the same as the output of circuit(2) and the output of OR_1 is high. The output of the AND gate is the same as the output of circuit(2) and gives control for angle β only.

3) When S_1 and S_2 are both open, control of angles α and β can be achieved simultaneously. Table (4-2) shows the state of each step for figure (4-15)

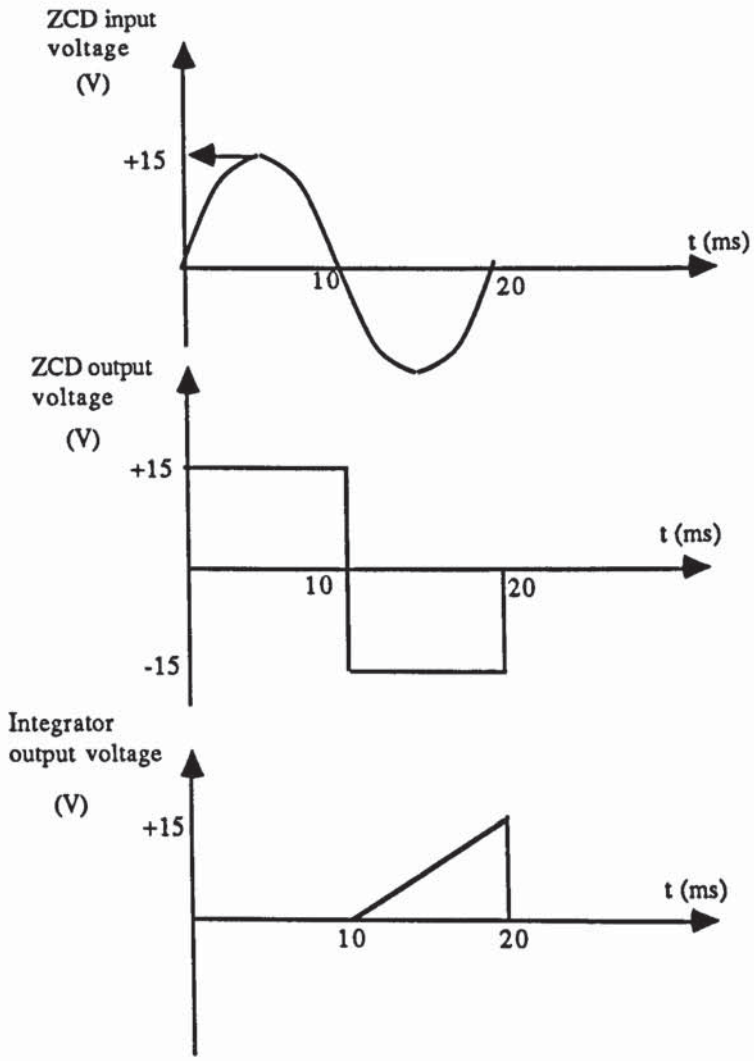


Figure (4-10) Input and output voltage waveforms of the zero crossing detector and the integrator.

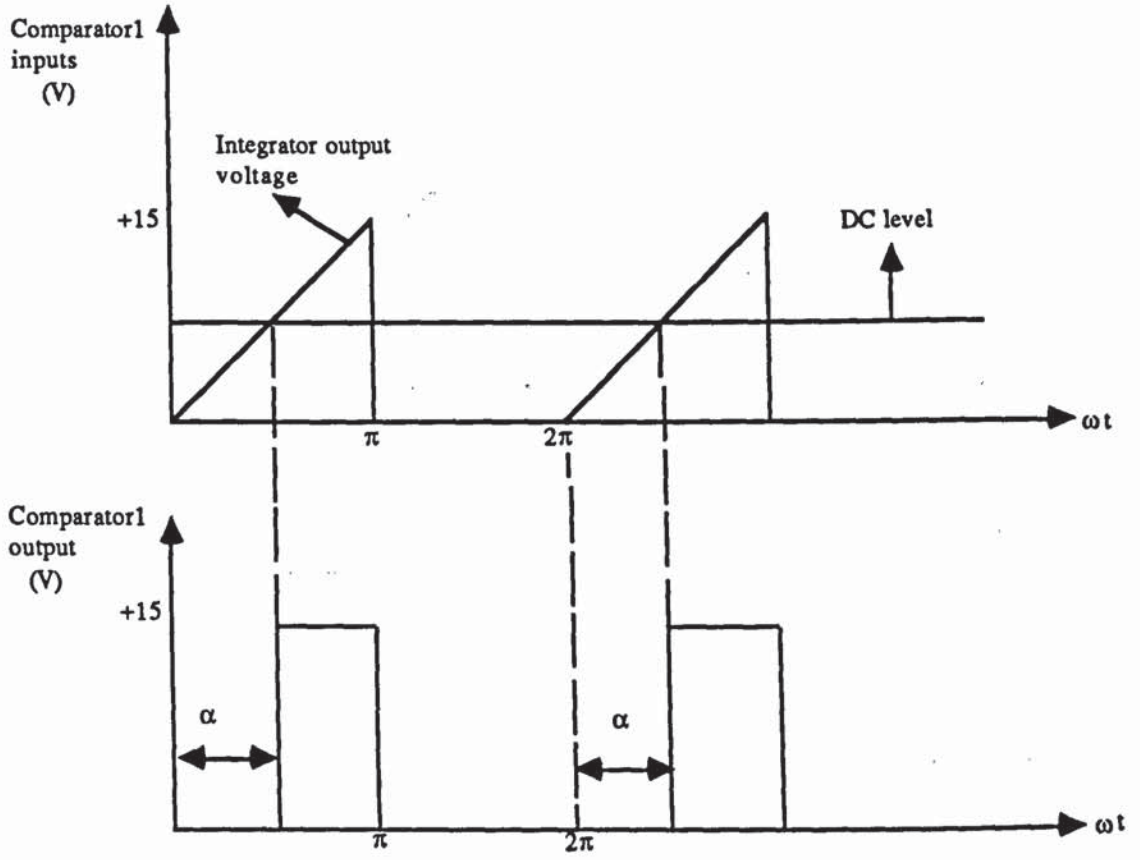
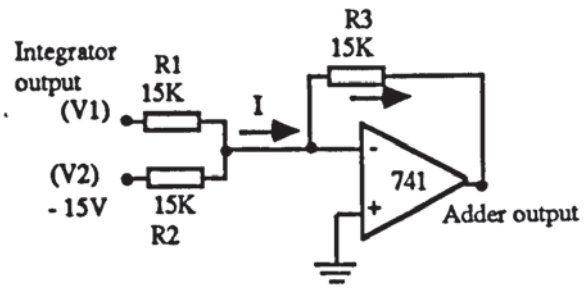
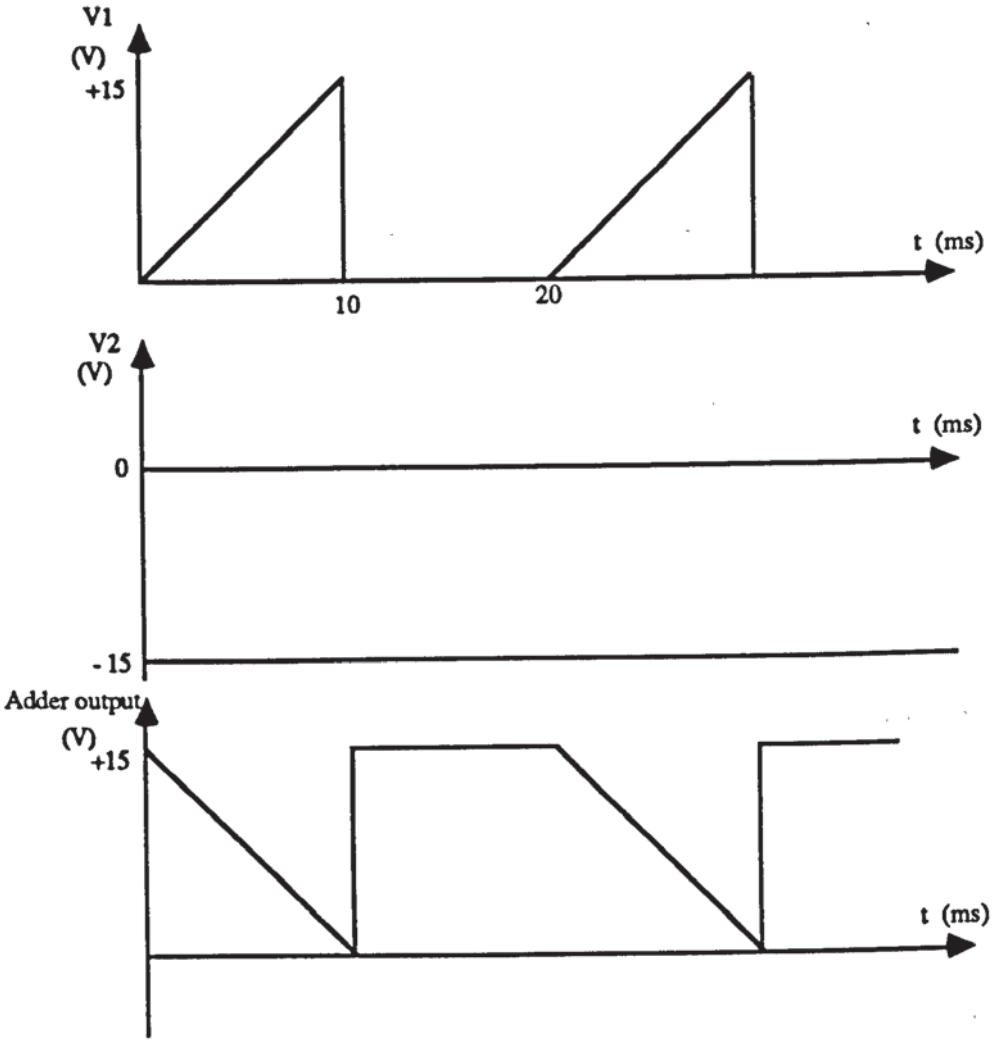


Figure (4-11) Controlling angle α.

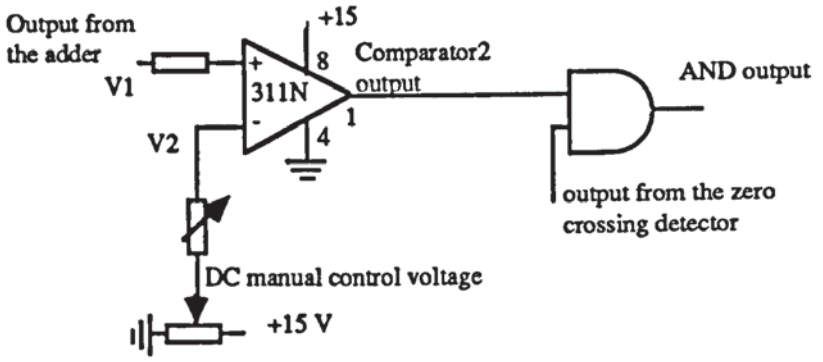


(a) Circuit connections.

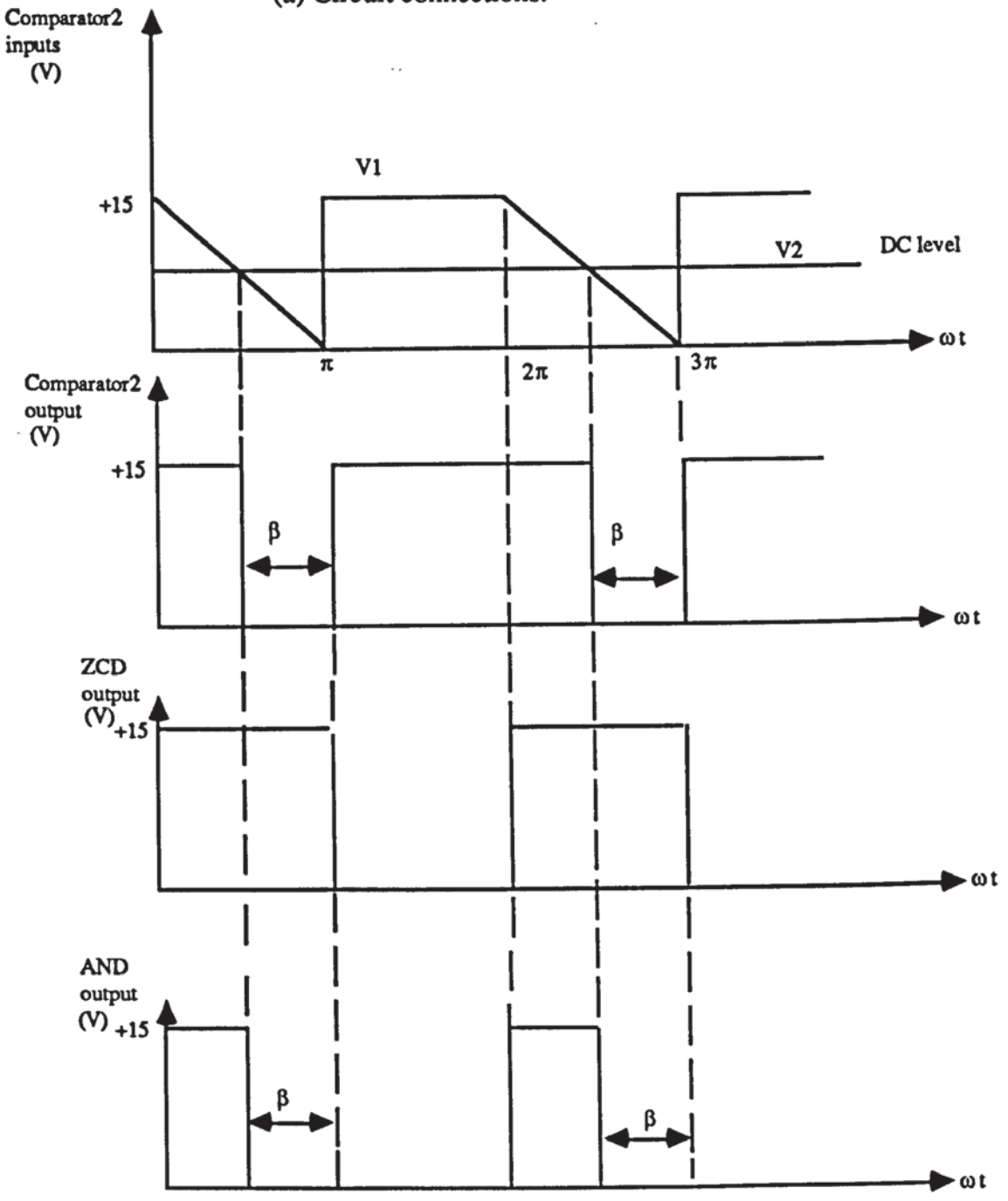


Circuit waveforms.

Figure (4-12) Adder connections.



(a) Circuit connections.



(b) Circuit waveforms.

Figure (4-13) Controlling angle β.

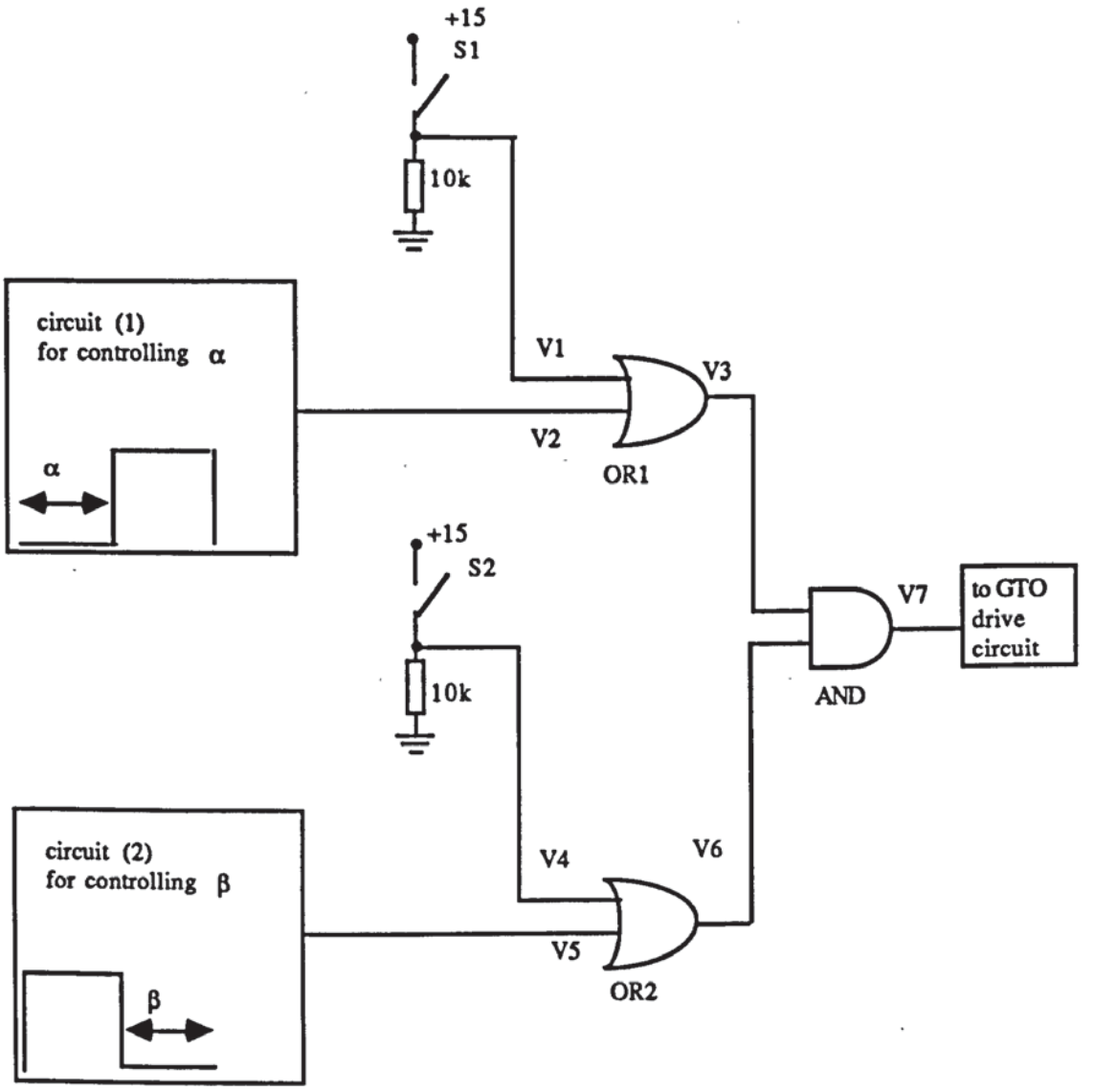


Figure (4-14) Controlling angles α and β.
(For the connections of circuits (1) and (2) refer to figure (4-9))

	V1	V2	V3	V4	V5	V6	V7
S1 open S2 closed control for α only	LOW	α	α	HIGH	β	HIGH	α
S1 closed S2 open control for β only	HIGH	α	HIGH	LOW	β	β	β
S1 open S2 open control for both α and β	LOW	α	α	LOW	β	β	α β

Table (4-2) Switching sequences of figure (4-14).

4-5 INVERTER DRIVE SIGNALS.

A 4047 CMOS multivibrator is used to generate the gate drive signals to the GTOs in the inverter circuits (A) or (B).The monostable is positive edge triggered using the output of the squarer from the rectifier control circuit as shown in figure (4-15).

The width of the monostable pulses were set at 10 ms with a period of (66):

$$T = 4.4\ R_1C_1 \qquad (4\text{-}5)$$

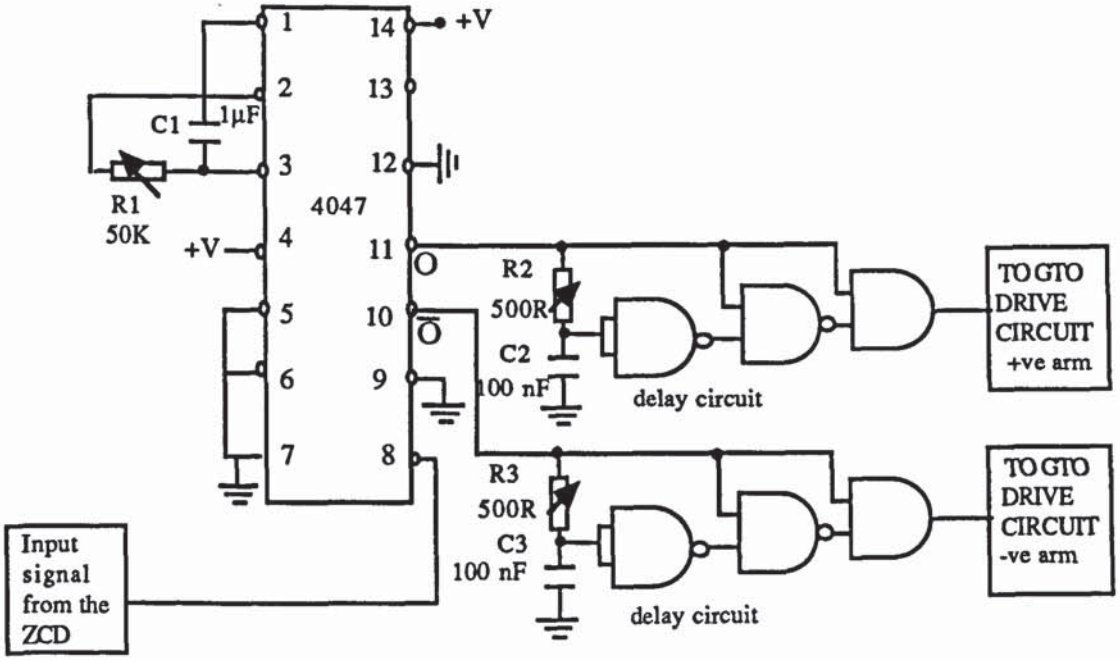
The monostable outputs are applied to two 15 μs delay circuits, to prevent both inverter arms being on simultaneously. The operation of the delay circuit is given in appendix (C).

4-6 TRANSISTOR BASE DRIVES.

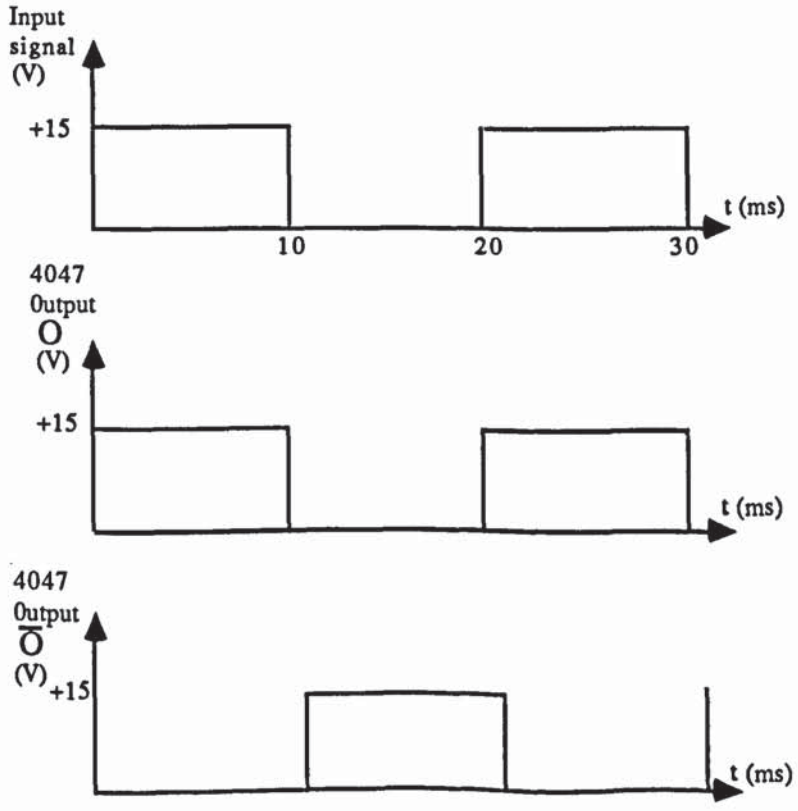
Figure (4-16) shows the two identical base drive circuits for transistors TR_A and TR_B. According to the data sheet of this type of transistor, a negative voltage (-1.5 V) must applied between the base and emitter to turn the transistor off.

Assume transistor TR_A is turning-on, When the input signal is high, the base of the pnp transistor T_1 is low and this turns it on. A current flows through R_{on} to turn transistor TR_A on. When the input signal is low, T_1 turns-off, a negative voltage (-1.5 V) appears between the base and the emitter of transistor TR_A to turn it off.

Two delay circuits are used to prevent both transistors being on simultaneously. Referring to figure (4-16), when the input signal changes state to turn TR_A off and turn TR_B on, the 15 μS delay ensures that TR_A is completely off before TR_B turns on . A similar situation arises when TR_B is turning off and TR_A is turning on.

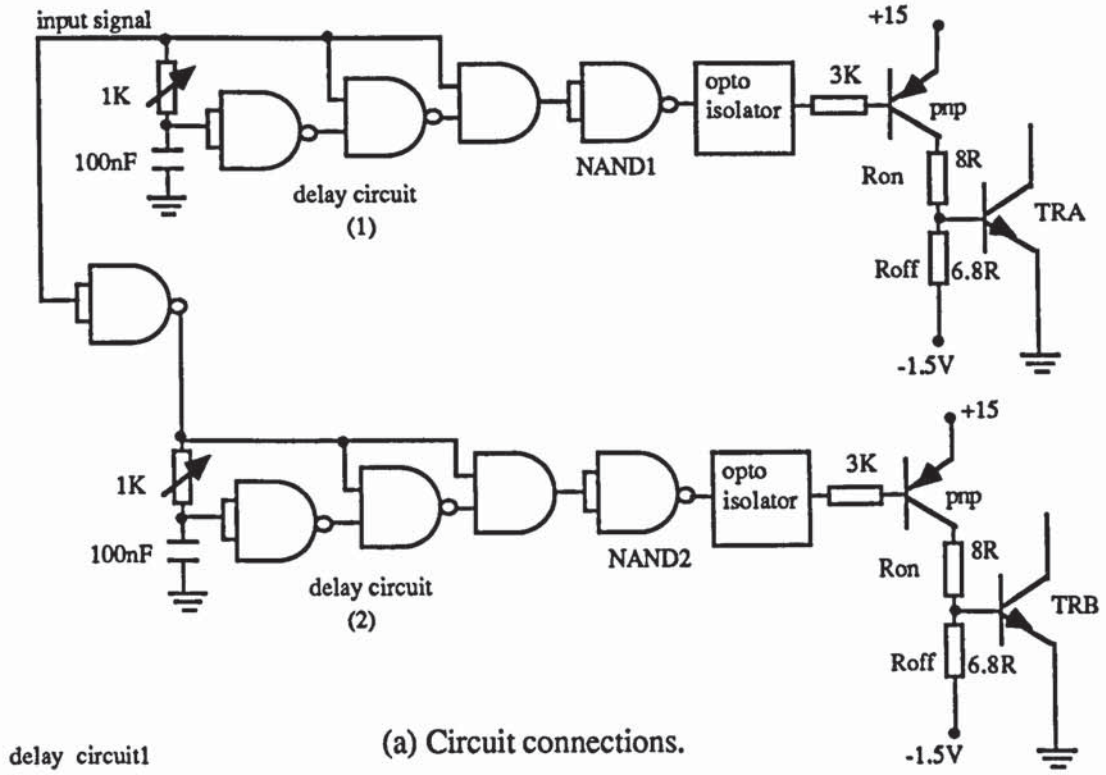


(a) Circuit connections.

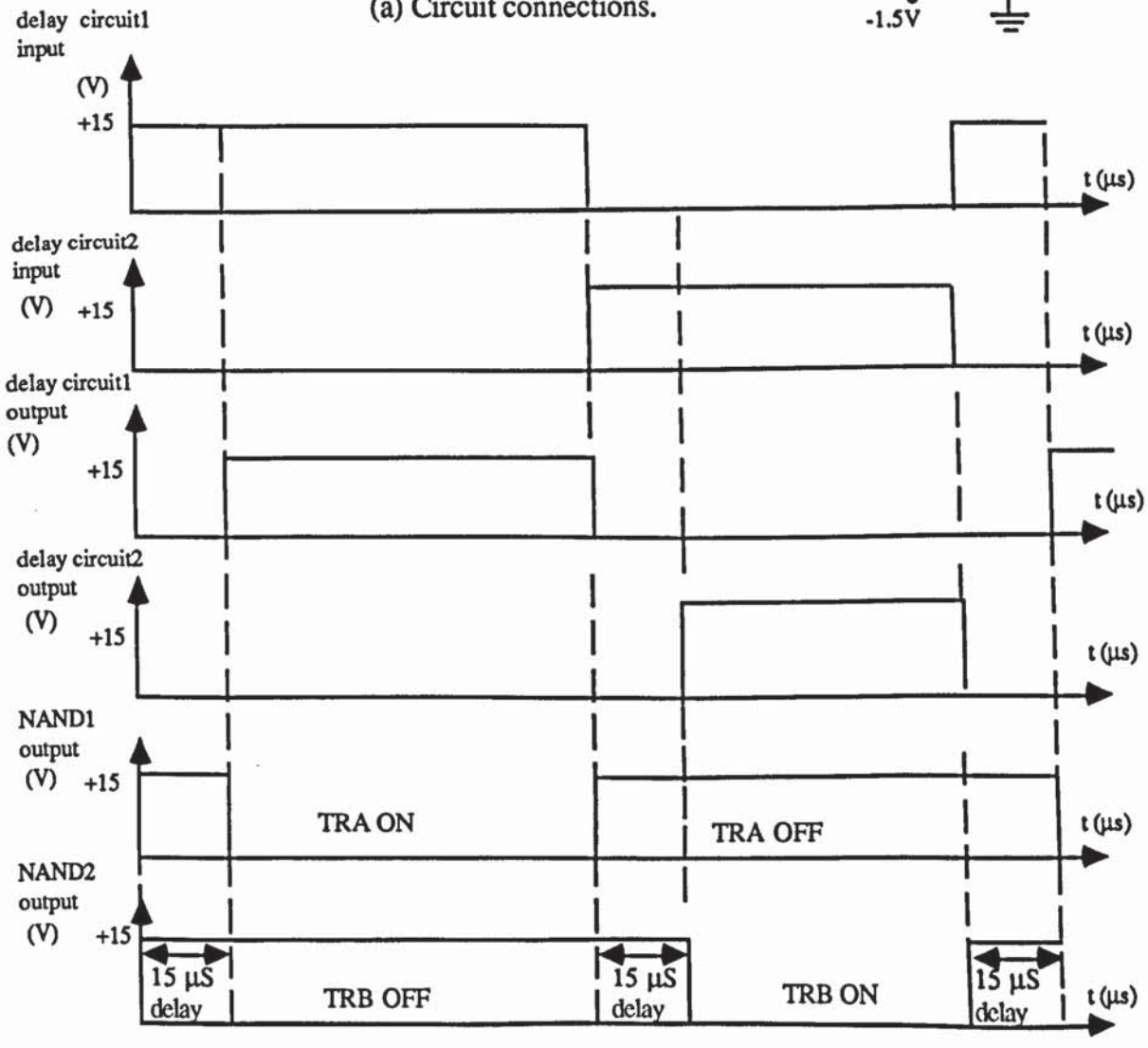


(b) Circuit waveforms.

Figure (4-15) Inverter drive pulses.



(a) Circuit connections.



(b) Circuit waveforms.

Figure (4-16) Transistor base drives.

4-7 OVERALL OPERATION OF THE SYSTEM.

When reversal of power flow is required, converters (A) and (B) change state from rectifier to inverter and vice versa and to achieve this, the scheme shown in figure (4-17) is used. When the comparator output changes state, the driving pulses transfer from one group of devices to another depending on the required direction of the power flow.

Two step-down transformers are used; one connected to the AC supply of converter (A), and the other to converter (B). Each transformer supplies a bridge rectifier smoothing capacitor circuit which produces approximately 14 V and is loaded by variable resistor which enables the output level to be changed. When $V_1 > V_2$, the output of the comparator is high (+15 V). The state of the comparator changes from high to low by increasing V_2 or reducing V_1 until V_2 is less than V_1. This can be achieved by the means of the variable resistors R_1 and R_2.

Referring to figures (4-1) and (4-17), and assuming that the power flows from side (A) to (B), the output of the comparator must be set to the high state ($V_1 > V_2$) such that:

The output of $NAND_1$ is low (0 V) and the output of $NAND_2$ is high (+15 V). The output of $NAND_2$ feeds the base drive of transistor TR_A to turn it on. The AC mains is connected to the input of converter (A). The rectifier drive pulses and the output of $NAND_1$ are applied to the inputs of $OR_{1,2}$ and these feed the drive circuits of $GTOs_{(2,4,6,8)A}$ to turn them on as controlled devices. The output of $NAND_1$ feeds the input of (delay circuit)$_1$ which has a low output state at this stage. This circuit and the inverter drive pulses are applied to the inputs of $AND_{1,2}$ which feed the drive circuits of $GTOs_{(1,7,3,5)A}$ to turn them off. (A) is operated as a rectifier supplying converter (B).

inverter drive pulses and the output of (delay circuit)2 are applied to the inputs of AND3,4 and these feed the drive circuits of GTOs(1,7,3,5)B to turn them on. (B) operates as an inverter. The output of NAND1 feeds the base drive of transistor TRB to turn it off and the output of inverter (B) is connected to the load to dissipate the power.

When power reversal is required, the state of the comparator output must be changed from high to low ($V_1<V_2$). Converter (A) changes from the rectifier to the inverter mode, its output is disconnected from the AC supply and connected to the load. Converter (B) changes from the inverter to the rectifier mode and its input is connected to the AC supply. Table (4-3) shows the switching sequence of the complete control circuit for power flow in both directions.

The delay circuits shown in figure (4-17) ensure that when converter (A) or (B) operates as an inverter GTOs(2,8,4,6) are on as diodes before the current starts to flow in each inverter arm. Otherwise a current or a voltage spike could occur at the instant of the switching if an overlap exists between the gating signals, figure (4-18) shows the waveforms of the delay circuit (1) at the instant of the switching. Assume that converter (B) is operating as a rectifier and at instant (X) it changes to inverter operation. Before the change over takes place, the output of NAND2 is low and converter (B) operates as a rectifier. When the output of the comparator changes state at instant (X), GTOs(2,8,4,6)B turn-on as diodes and after a 150 μs delay time GTOs(1,7,3,5)B turn-on to carry the inverter current. The same procedure will happen in delay circuit (2) when converter (A) transfers from a rectifier to an inverter.

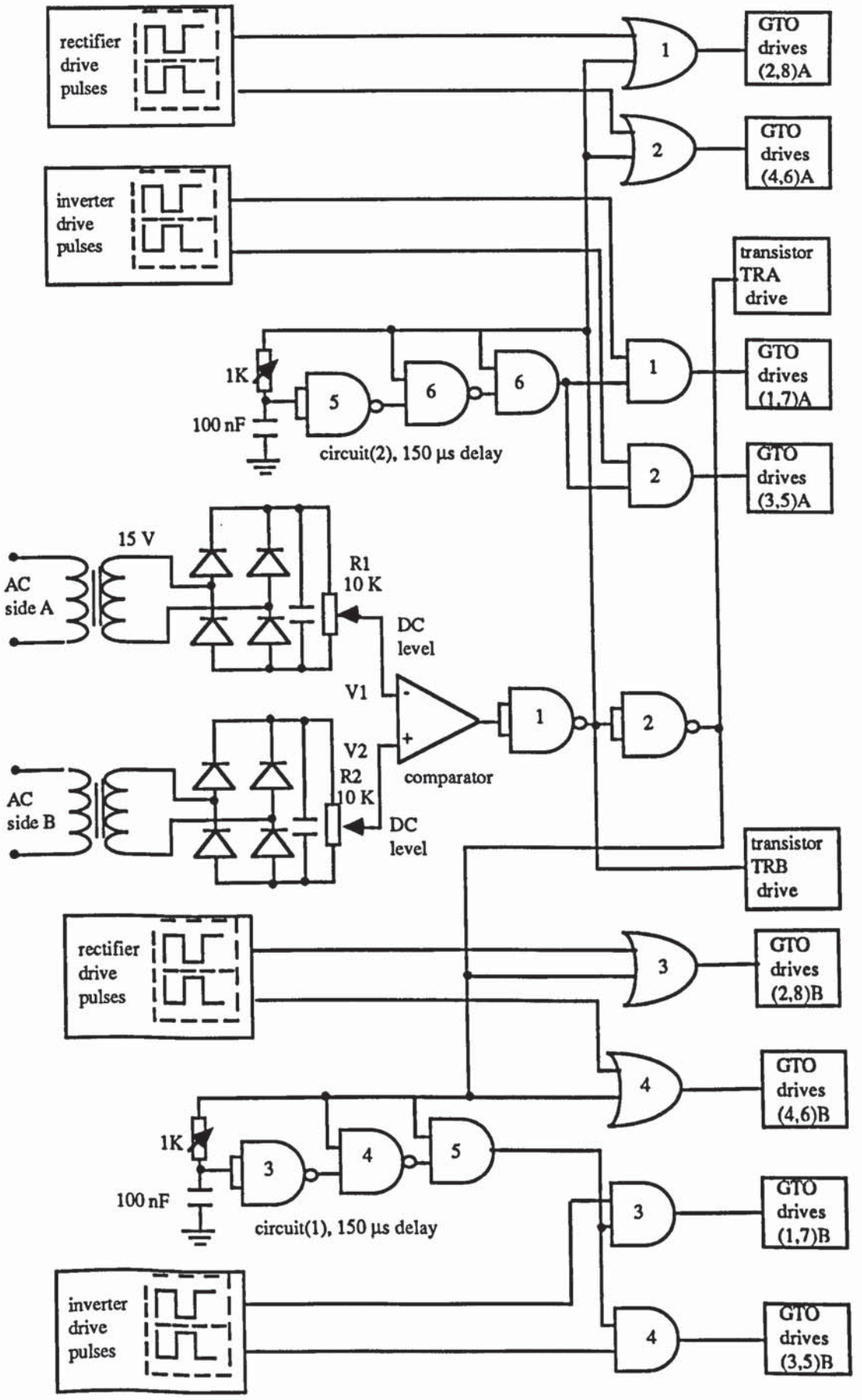


Figure (4-17) System control circuit.

							converter (A)					converter (B)		
	rectifier drive pulses	inverter drive pulses	NAND (1)	NAND (2)	OR (1,2)	AND (1,2)	gate drives of GTOs (2,4, 6,8)	base drive of TRA	gate drives of GTOs (1,3, 5,7)	OR (3,4)	AND (3,4)	gate drives of GTOs (2,4, 6,8)	gate drives of GTOs (1,3, 5,7)	base drive of TRB
power flows from A to B V1>V2			LOW	HIGH		LOW	 (A) operates as a rect	HIGH TRA is on	LOW GTOs are off	HIGH		HIGH GTOs operate as diodes	 (B) operates as an inv	LOW TRB is off
power flows from B to A V1<V2			HIGH	LOW	HIGH		HIGH GTOS operate as diodes	LOW TRA is off	 (A) operates as an inv		LOW	 (B) operates as a rect	LOW GTOs are off	HIGH TRB is on

Table (4-3) Switching sequence of the system control circuit.

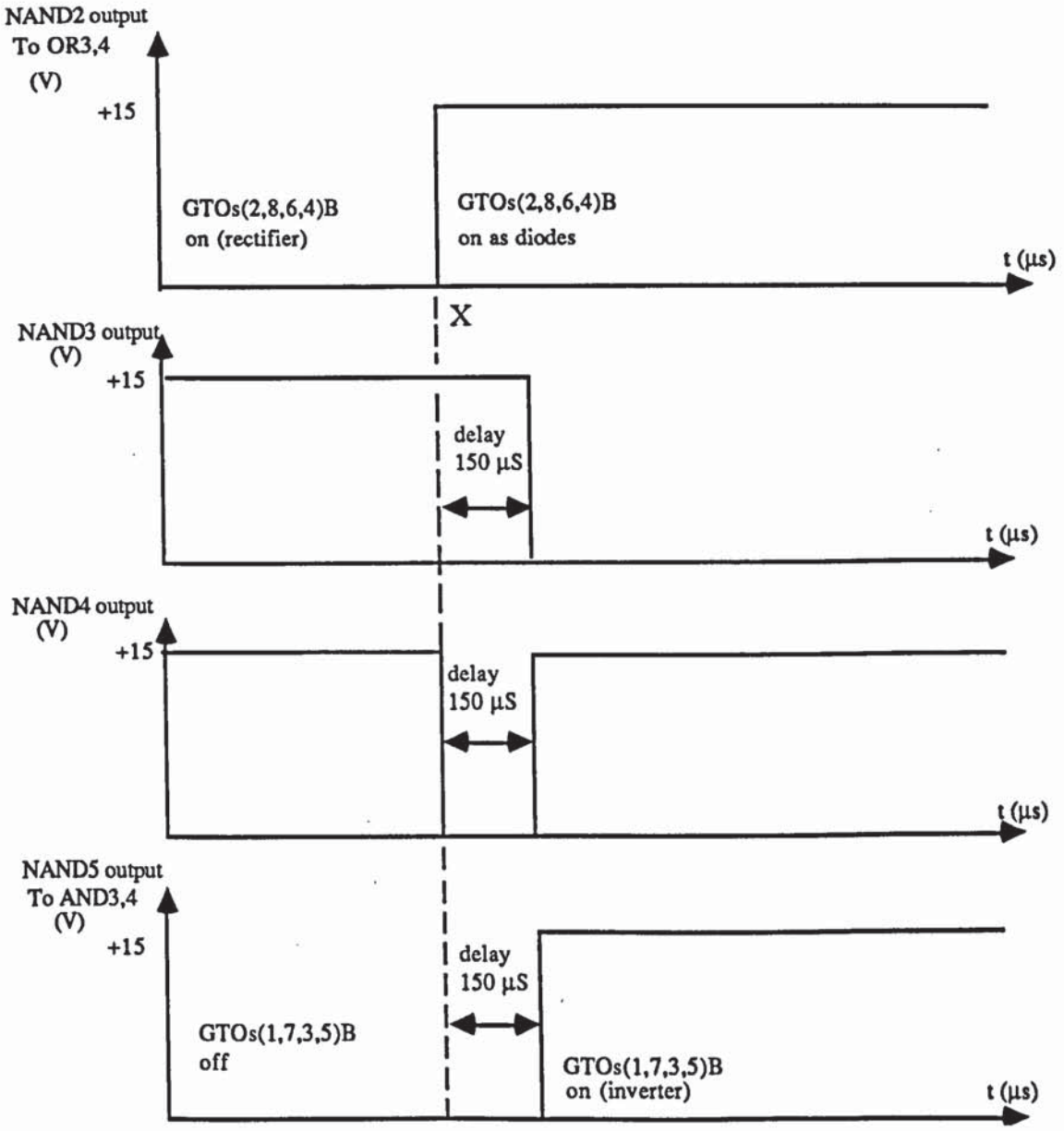


Figure (4-18) Delay circuit (1) waveforms.

CHAPTER FIVE

EXPERIMENTAL RESULTS

5-1 INTRODUCTION.

This chapter presents experimental results for the single phase system explained in Chapter 4. Since the construction and performance of the two converters are similar, all the results were obtained from converter (A). Figure (5-1) shows the location in the system of the measuring equipment used to record the results. The waveforms were recorded by using a four channel digital oscilloscope which has a print-out facility. Two major problems occurred during the commissioning of the system and these related to the transient voltage of the switching transistor and the inrush current into the filter capacitor. Before proceeding with the results, the effect and explanation of the two problems are presented.

5-2 VOLTAGE TRANSIENT OF THE SWITCHING TRANSISTOR.

Figure (5-1) shows that each side of the system is connected to the AC mains via two 2.3:1 step-down transformers. The high voltage sides are connected to the AC supplies while the low voltage sides are connected to the input of converters (A) and (B). A variac supplies each transformer to provide a variable operating voltage. On the high voltage side of each transformer a transistor and a bridge rectifier is operated as a static switch, to connect the input/output of the converter to the mains or to the load.

The transistor is a TCD 30-800 power NPN Darlington having the following rating:

Collector-emitter voltage (V_{CEX}): 800 V.

Collector-emitter sustaining voltage ($V_{CE(SUS)}$): 500 V.

Continuous collector current ($I_{C(cont)}$): 50 A.

Peak collector current: ($I_{C(pk)}$): 70 A.

Fall time (t_f): 2 μs

A polarized snubber circuit is connected across each transistor as shown in figure (5-2), with the values of snubber capacitor C and snubber resistor R calculated using the Thomson-CSF analytically derived relationships (69).

$$C \geq \frac{I_M \cdot t_f}{V_{CE(SUS)}} \tag{5-1}$$

$$R \geq \frac{V_M}{I_{CM} - I_M - I_{RR}} \tag{5-2}$$

Where:

I_{CM} is the maximum value of the collector current ($I_{C(PK)}$).

I_M is the current through the transistor during turn on.

I_{RR} is the recovery current in the snubber diode.

$V_{CE(SUS)}$ is the sustaining voltage.

V_M is the voltage across the capacitor during turn off.

t_f is the fall time of the transistor.

When calculating the snubber components, the following assumptions were made:

a) The current I_{RR} is assumed to be very low compared with I_{CM} and I_M and consequently was ignored.

b) It has assumed that the maximum capacitor voltage at turn off does not exceed the collector emitter voltage $V_{(CEX)}$.

c) The current IM was assumed to be the same as the continuous collector current of the transistor.

Making these assumptions it was found that $C \geq 0.2$ μF, and $R \geq 40$ Ω and value of $C = 0.22$ μF and $R = 40$ Ω were chosen. Many transistors failed during turn-off even though the output to the variac did not exceed 100 V. It was found that two

factors increased the transient voltage across the transistor; the leakage inductance of the variac and the transformer and the values of the snubber capacitor.

The transient voltage was minimized by using a much higher value of snubber capacitor and by connecting an RC snubber across the variac. These values are based on the following consideration. (Note that, to allow for an adequate safety margin, it has been suggested to limit the voltage transient to 650 V).

The following equation was used to determine the value of a suitable capacitor to be connected across the transformer to reduce the transient voltage (70).

$$C = \frac{VA}{31.f.(V_{pk})^2}\ \mu F \qquad (5\text{-}3)$$

Where:

VA = volt- ampere rating of transformer. (VA)

f = supply frequency. (Hz)

V_{pk} = peak voltage rating of the semiconductor device. (V)

Since the 4 kVA variac has only one winding , equation (5-3) must be divided by 2, giving a capacitor value:

$$C = \frac{4000}{2.31.50.800^2} = 2\ \mu F$$

It is worth mentioning that the maximum voltage transient occurs when the transistor turns-off at a maximum collector current and it increases sharply with this current. To determine an optimum value for the snubber capacitor across the transistor, the input voltage of the variac was fixed at 60 VRMS (85 Vpk) and the transistor peak collector current set at 6 A by varying the resistive load. The transient voltages were measured for different values of C. Figure (5-3) shows the voltage transient against the value of the snubber capacitor which is used for the transistor. From this curve, the value of 2 μF was selected for the snubber circuit. The transient voltage at this value equals 200 V.

The 4 k Ω resistor shown in parallel with the transistor in figure (5-2) provides a discharging path for the capacitor voltage. Figure (5-4) shows variation of the peak voltage transient with the RMS output voltage of the variac and the transistor peak collector current. For this test, the component values shown in figure (5-2) were used.

Figure (5-5) shows the voltage transient and the peak collector current waveforms when the switching occurs at maximum current. For these conditions, the output voltage of the variac was 160 V RMS (226 V peak) and the load was purely resistive. The DC current and voltage at the output of converter (A) were respectively 11.5 A and 85 V and the voltage transient is 620 V.

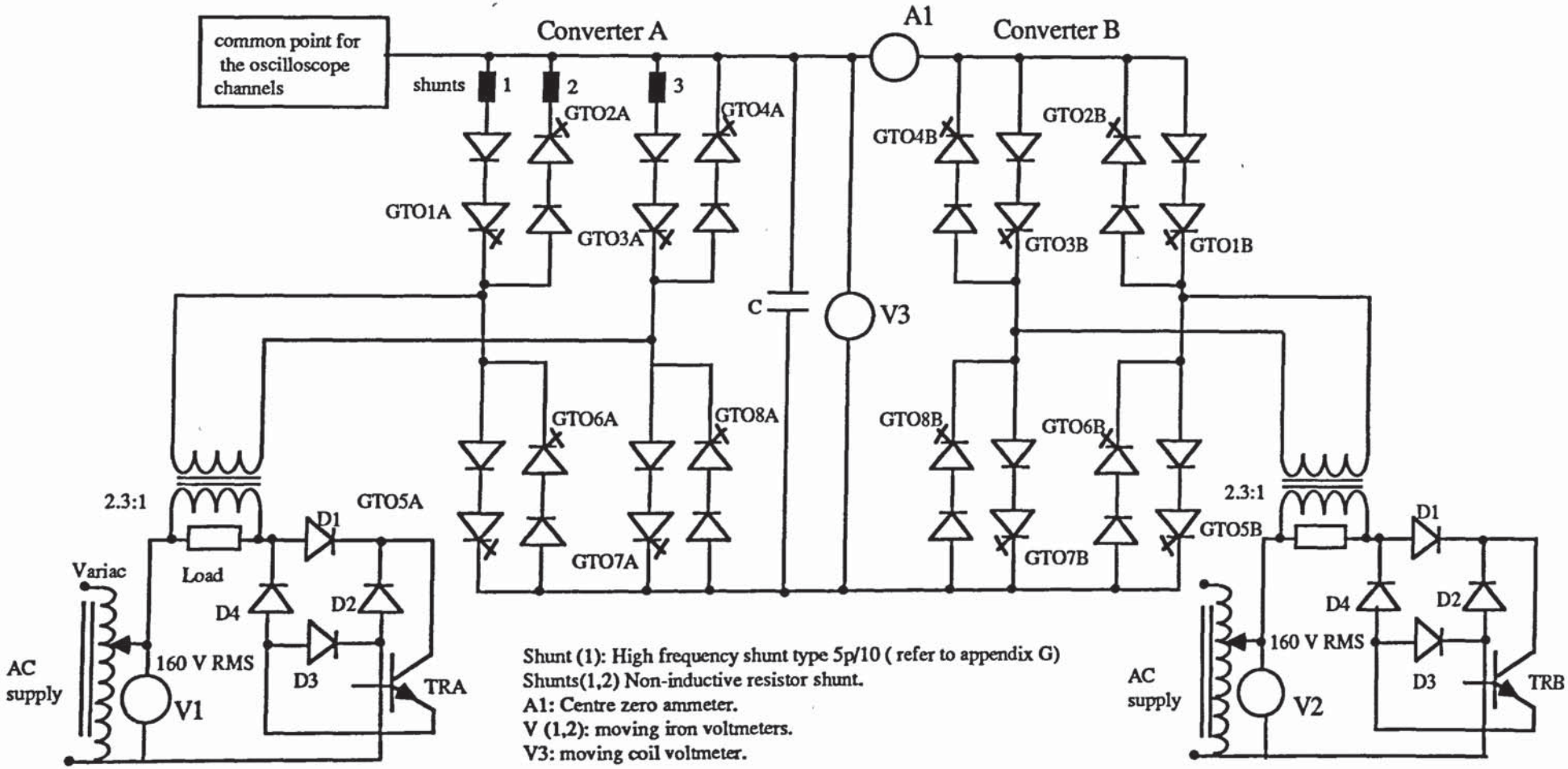


Figure (5-1) Single phase two way power flow.

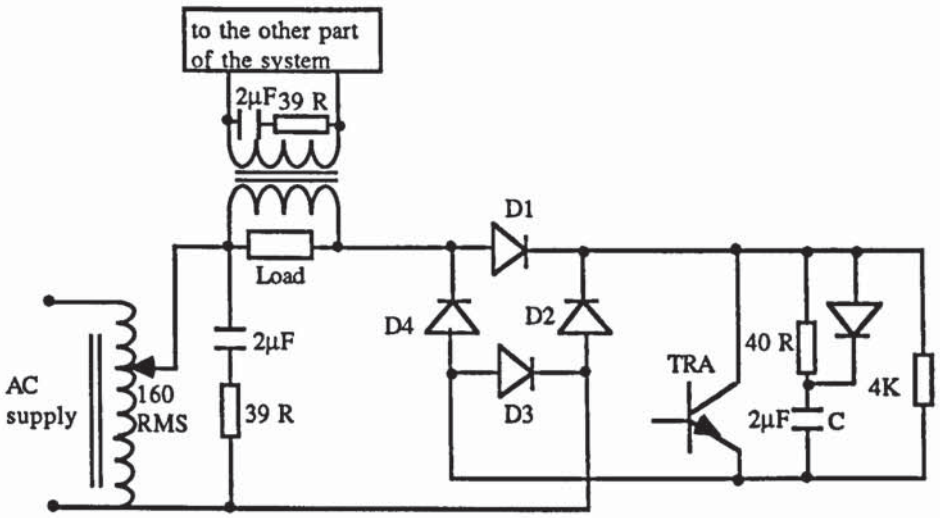


Figure (5-2) Switching transistor protection.

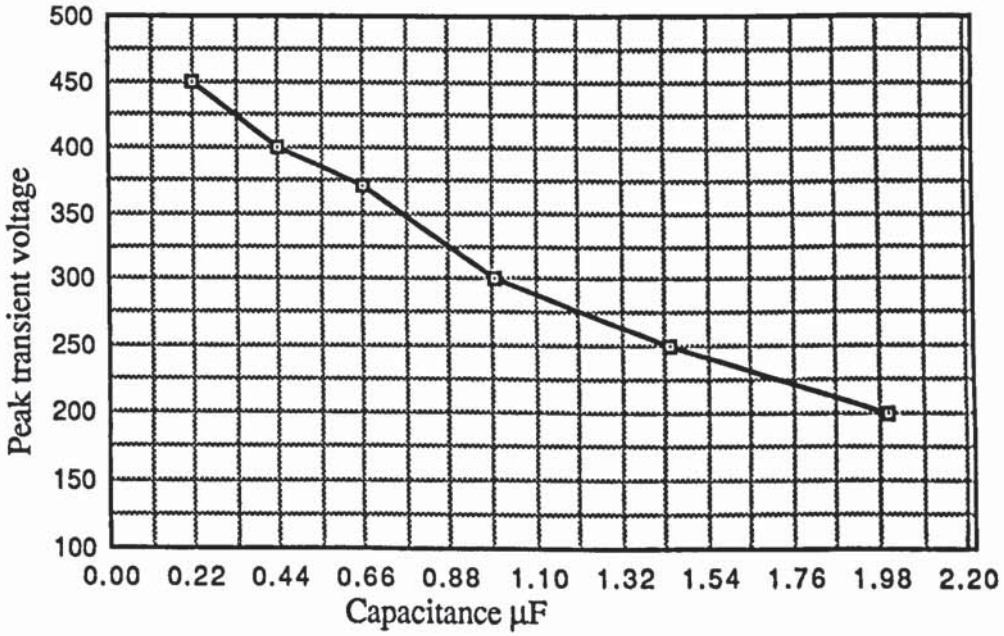


Figure (5-3) Peak voltage transient against snubber capacitance.
(Input voltage = 60 VRMS: Transistor peak current = 6 A)

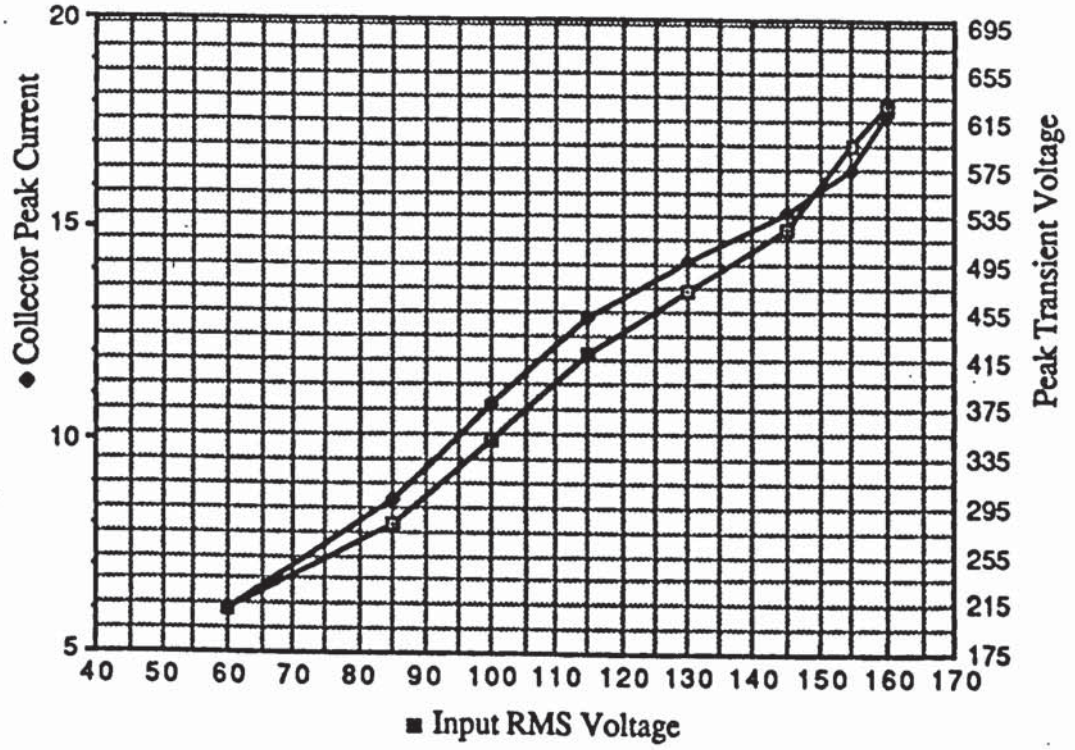


Figure (5-4) Peak voltage transient against RMS input voltage and transistor peak current.

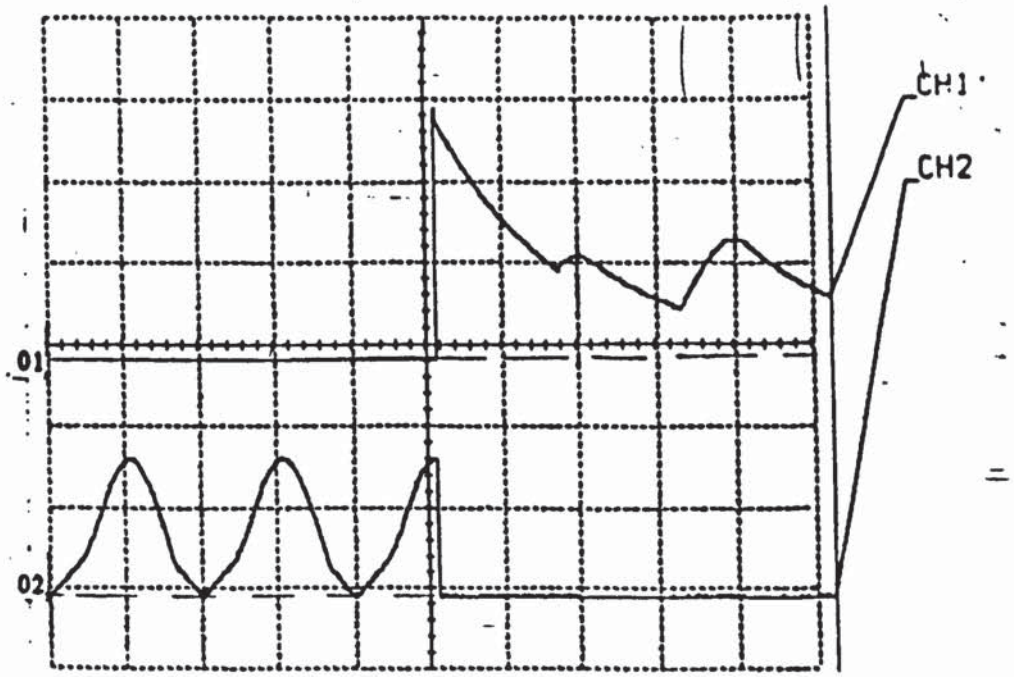


Figure (5-5) Switching transistor voltage and current.
CH1: Collector-emitter voltage 200 V/div
CH2: Collector current 10 A/div
Time: 5 ms/div.

5-3 REDUCTION OF THE CAPACITOR INRUSH CURRENT.

It is well known that when the output of a rectifier has a filter capacitor, the inrush current will be high. This current is dependent on the value of the capacitor and the rate of rise of the DC voltage.

Many diodes failed due to the high inrush current into the filter capacitor. Since the peak current rating of the diode used in the system is 70 A, adequate safety margin was allowed for and the inrush current was reduced to 60 A. At this value, the system worked without any further diode failures.

The capacitor inrush current is given by:

$$i_C = C\frac{dv}{dt} \qquad (5\text{-}4)$$

Where dv/dt is the rate of rise of the DC voltage from the rectifier output and C is the filter capacitor. The rate of rise of DC voltage was controlled using a ramp-up circuit, which delayed the firing angle of the GTOs at the instant of switching. The firing angle moved from 180 degrees to zero as the capacitor charged to full voltage. To simplify the operation of the ramp-up circuit, it is assumed that angle $\beta = 0°$ and angle α will be changed. As mentioned in the previous chapter, angle α may be varied by comparing a ramp waveform with an adjustable DC voltage. When the DC voltage is greater than the ramp wave, α is 180°, and when the DC voltage is zero, $\alpha = 0°$.

Figure (5-6) shows the connections for the ramp-up circuit. The first comparator shown in the figure is the system control circuit comparator which was explained in the previous chapter. When the values of V_1 and V_2 change ($V_1 < V_2$ or $V_1 > V_2$), the output of this comparator changes state to transfer the pulses from one group of devices to another, depending on the required direction of power flow. (For more details refer to Chapter 4). Referring to figure (5-6), assume that the comparator output changes state from low to high at instant (C). The output of $NAND_1$ will give a 50 μs delay, which is determined by the R_1C_1 network. The EXCLUSIVE-NOR

gate turns-on transistor T_1, to charge the capacitor (C_2). After the delay time, T_1 turns-off while the output of NAND2 turns transistor T_2 on. The capacitor (C_2) discharges via T_2 and R_3. The capacitor voltage (V_Y) and the adjustable voltage (V_X) are connected to a subtractor which is an operational amplifier giving an output voltage:

$$V_{out} = (V_Y - V_X) \tag{5-5}$$

At the instant of switching, (V_X) is zero and the output of the subtractor is (V_Y) which discharges slowly until it becomes almost zero, the discharging time is determined by the R_3C_2 network. The output of the subtractor is connected to the comparator which is used to control the firing angle α. The firing angle α will be reduced until the filter capacitor is fully charged. Figure (5-7) shows the waveforms of the subtractor output, ramp voltage and controlling angle α over positive and negative half-cycles. α is reduced slowly and when the subtractor output is zero, $\alpha = 0°$.

After (V_Y) becomes zero, the output of the subtractor is ($+V_X$) due to the negative sign of equation (5-5), so again angle α will be changed by varying the level of (V_X). When the state of the first comparator changes again (see instant D in figure (5-6)), the same procedure occurs.

Figure (5-8) shows the waveforms of the DC voltage and current at the instant of the switching with a resistive load. The current reaches 58 A when the DC voltage is 43 V. Theoretically, the DC voltage reached 43 V in approximately 2.5 ms. The value of the filter capacitor is 3400 μF, so:

$$I_C = C\frac{dV}{dt} = 3400\text{x}10^{-6}\frac{43}{2.5\text{x}10^{-3}} = 58.4\ \text{A}$$

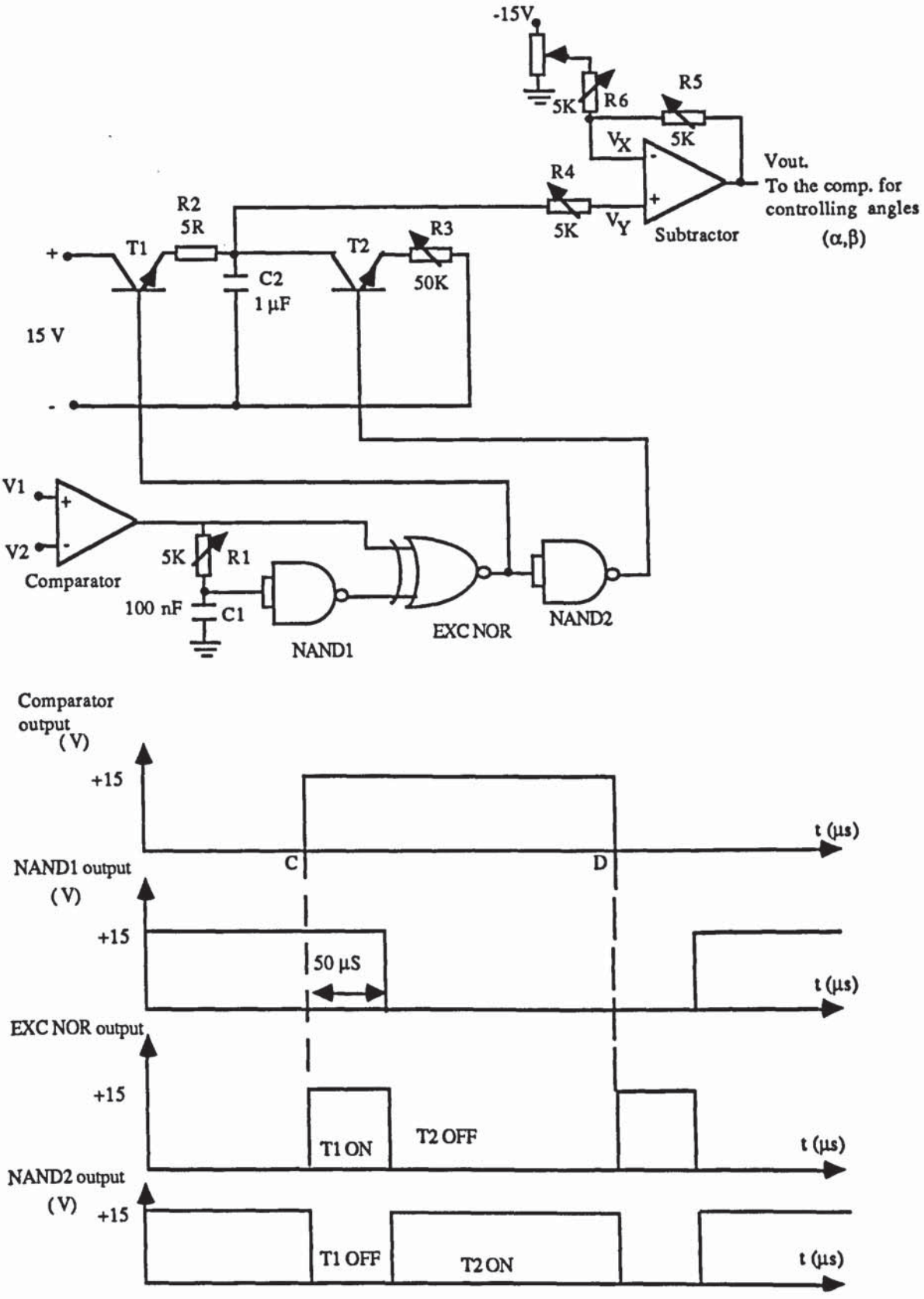


Figure (5-6) Connections of the ramp-up circuit.

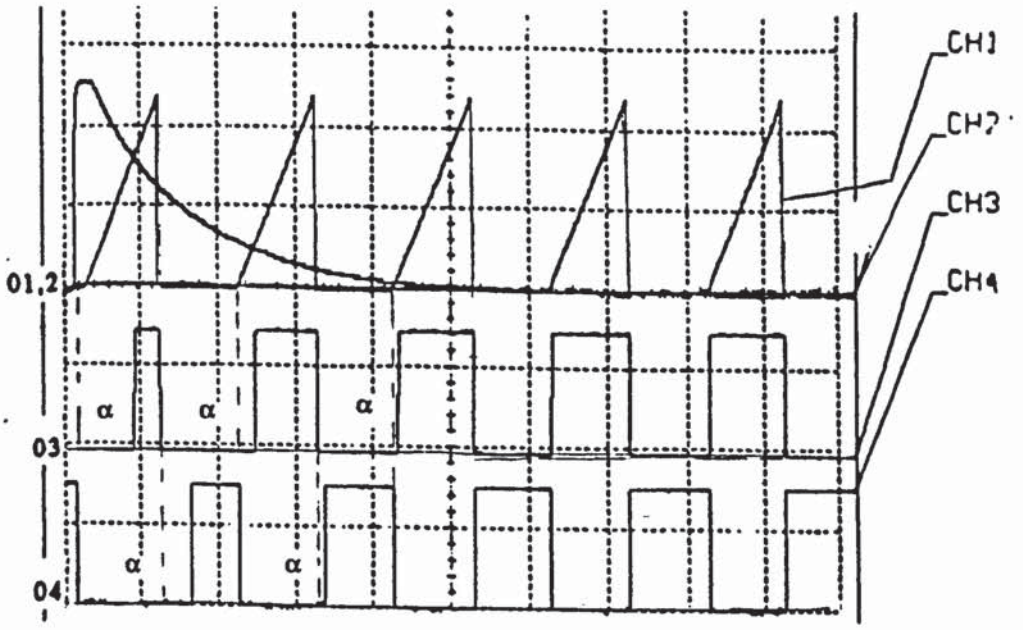


Figure (5-7) Effect of the ramp-up circuit.
CH1: Ramp voltage 5 V/div.
CH2: Subtractor output 5 V/div.
CH3: Pulses over positive half-cycle 10 V/div.
CH4: Pulses over negative half-cycle 10 V/div.
Time: 10 ms/div

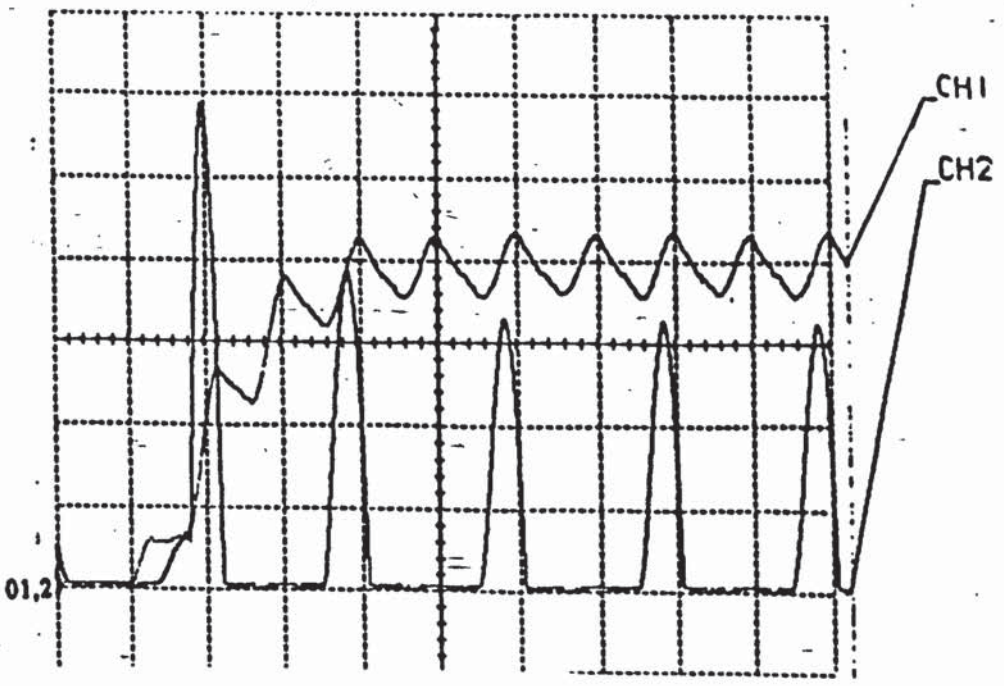


Figure (5-8) Capacitor inrush current and DC rectifier voltage (resistive load).
CH1 : DC voltage 20 V/div.
CH2 : Inrush current 10 A/div.
Time : 10 ms/div

5-4 EXPERIMENTAL RESULTS WITH A RESISTIVE LOAD.

The system of figure (5-1) was tested initially using a resistive load, R = 35 Ω. The input to the variac was adjusted to 160 V RMS (226 Peak) and the direction of the current was observed using a centre zero ammeter connected between the two converters.

Two shunts were connected to GTO1A and GTO2A, to observe the transfer of current when power flow changes direction. At steady-state conditions and when converter (A) operates as a rectifier and converter (B) operates as an inverter, the readings from the voltmeter and the ammeter on the DC side at ($\alpha = \beta = 0°$) were respectively 85 V and 11.5 A. By transforming all the parameters of the system to the low voltage side of the transformers (transformer ratio = 2.3/1), the system operated with the following parameters:

Peak input voltage of the converter (A) = 226/2.3 = 98 V.

Load resistance = 35/5.23 = 6.6 Ω.

Referring to figure (5-1), the capacitor charges to the peak of the AC supply voltage, and then discharges exponentially into the load resistance at a rate dependent on the time constant RC. The GTOs start to conduct once the anode voltage exceeds that of the smoothing capacitor and the conduction ceases when the anode voltage falls below that of the capacitor. Under these conditions, the conduction occurs over a part of each half cycle only. Ideally, the capacitor must be charged to 98 V, but as shown in figure (5-1) for each half cycle four devices in series will be on (two GTOs and two diodes). Hence the capacitor will charge to the peak input voltage minus the voltage drop of the four devices. Figure (5-9) shows the waveforms for steady-state conditions when converter (A) operates as a rectifier, the peak capacitor voltage is 92 V. Therefore, the voltage drop of the four devices together is 6 V. Referring to the current waveform through GTO2 (Channel 2) and its gate driving pulse (Channel 4), GTO2 starts to conduct at 54°and ceases conduction at 162°,this is due to the filter

capacitor.Figure (5-10) shows the steady state condition when converter (A) operates as an inverter with a purely resistive load. Reffering to Channel 3, the maximum current through GTO_1 is 12 A approximately.

The efficiency of the system was measured and calculated for both rectification and inversion, converter (A) operated as a rectifier and converter (B) operated as an inverter. The power was measured at the input of rectifier (A), the DC side of rectifier (A) and the output of inverter (B).

$$\text{efficiency} = \eta = \frac{\text{output power}}{\text{input power}} \tag{5-6}$$

a) The efficiency of rectifier (A) equals the DC output power divided by the AC input power of rectifier (A).

b) The efficiency of inverter (B) equals inverter output power divided by the DC power from rectifier (A).

c) The overall system efficiency equals the output power of inverter (B) divided by the AC input power of rectifier (A).

Table (5-1) shows both the practical and the theoretical efficiency of the system. Practical measurements were obtained using an AC power analyser PM1000.

Theoretically, the input power, DC power of rectifier (A) and AC power of inverter (B) were calculated as follows:

Input power of rectifier (A) = (input RMS Voltage).(input RMS current)

The input voltage of rectifier (A) was 69 VRMS. The RMS current was calculated by refer to figure (5-9).

$$I_{RMS} = \sqrt{\frac{1}{\pi}\int_a^b \left(I_{pk}\sin\omega t\right)^2 d\omega t} \tag{5-7}$$

Therefore:

$$I_{RMS} = I_{pk}\sqrt{\frac{1}{2\pi}\left(b - a - \frac{\sin 2b}{2} + \frac{\sin 2a}{2}\right)} \qquad (5\text{-}8)$$

Where (a) is the angle at which the GTO starts to conduct and (b) is the angle at which it ceases to conduct. Referring to figure (5-9) GTO_1 conducts for 100°, and the peak current equals 27 A. The input AC current has the same shape for each half cycle. If it is assumed that GTO_1 starts to conduct at zero and ceases at 100° (100° = 1.7 rad.), then by reference to equation (5-10) the input RMS current is:

$$I_{RMS} = 27\sqrt{\frac{1}{2\pi}\left(1.7 - \frac{\sin 2(1.7)}{2}\right)} = 14.9 \text{ A}$$

The input AC power of rectifier (A) = (69).(14.9) = 1028 W.

The power of rectifier (A) on the DC side = (85).(11.5) = 977.5 W.

The efficiency of rectifier (A), μ = 977.5/1028 = 0.95.

If the same voltage drop is considered on rectifier (A) is also considered on converter (B), therefore the current through the load resistor will be: 85-6/6.6 = 11.9 A. The AC output power of inverter (B) equals:

Output power of inverter (B) = $I^2.R = 11.9^2.6.6 = 934.6$ W.

Therefore.

The efficiency of inverter (B) = 934.6/977.5 = 0.956.

The overall system efficiency equals the AC output power of inverter (B) divided by the input power of rectifier (A) and this gives:

The overall system efficiency = 934.5/1028 = 0.90.

Figure (5-11) shows the waveforms when converter (A) transfers from rectifier to inverter operation ($\alpha = \beta = 0°$). The switching happened at approximately maximum current. The current is transferred from GTO_2 to GTO_1. GTO_2 changes from being a

controlled device to a diode (always on) and this is observed in the drive signals which are always at a high state (see Channel 4). The DC voltage is slightly reduced, since the capacitor discharges via inverter (A) and at 50 V approximately, the capacitor charges again via rectifier (B).

Figure(5-12) shows the waveforms when converter (A) transfers from inverter to rectifier operation ($\alpha = \beta = 0°$). As the current transfers from GTO_1 to GTO_2, the inrush current is quite small, because the capacitor is still partly charged. Referring to Channel 4, the drive signals are decreasing until the firing angle becomes zero.

Since the ground reference for the rectifier control circuit is different from that of the system, another two channel oscilloscope was used to display the firing angles α and β of the GTOs. Figures (5-13) and (5-14) respectively show the values of $\alpha = 90°$ and $\beta = 72°$ over a positive half-cycle, compared with a reference sine-wave. These values were used in the experimental results for reversing the power flow between converters (A) and (B) and vice versa.

Figure (5-15) shows the waveforms when converter (A) transfers from rectifier to inverter operation at $\alpha = 90°$ and $\beta = 0°$; for a DC current of 6.8 A. Figure (5-16) shows the waveforms when converter (A) transfers from inverter to rectifier operation at $\alpha = 90°$ and $\beta = 0°$. In both cases, the DC voltage took a longer time to regain its maximum value compared with $\alpha = \beta = 0°$. Figures (5-17) and (5-18) show the waveforms when converter (A) transfers from rectifier to inverter operation and vice-versa with $\beta = 72°$ and $\alpha = 0°$. Since the switching point is random, the switching occurs after approximately 36° and the current transferred from GTO_2 to GTO_3 without transient. The DC current was 6.7 A.

(Note that, there are some blips appearing on Channel 3. After some investigation it was concluded that these were due to interference between the current shunts shown in figure (5-1). Although the connections between the shunts are very short, the interference between them could not be avoided and these blips occurred in almost every waveform)

	Practical	Theoretical
AC input power of rectifier (A)	990 W	1028 W
DC output power of rectifier (A)	940 W	977.5 W
AC output power of inverter (B)	880 W	934 W
Efficiency of rectifier (A)	0.94	0.95
Efficiency of inverter (B)	0.94	O.956
Overall system efficiency	0.89	0.90

Table (5-1) Efficiency of the system.

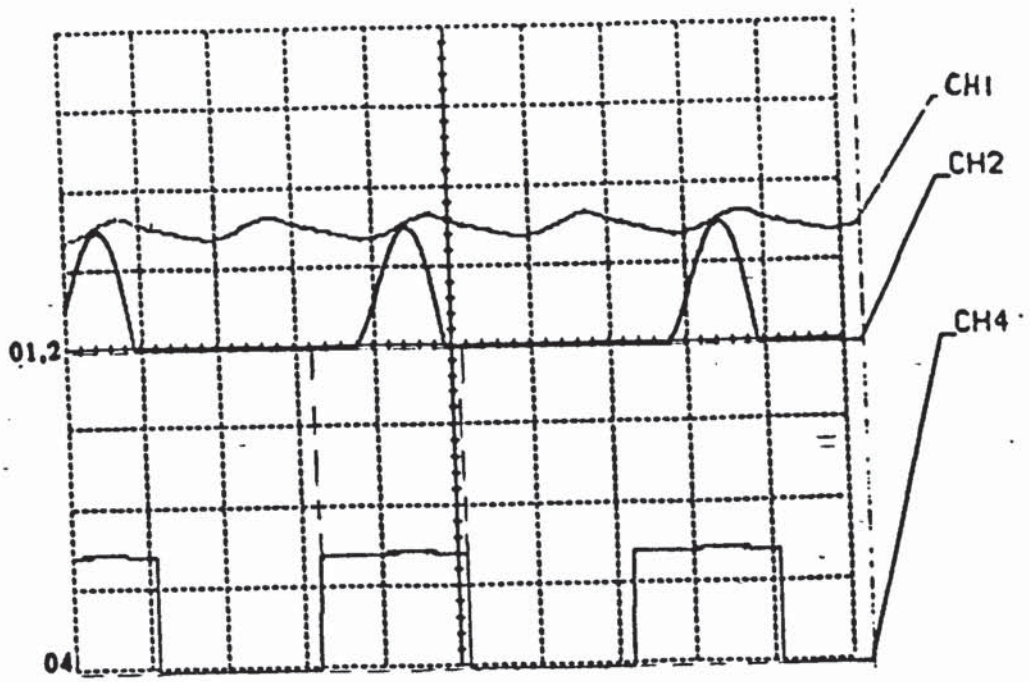


Figure (5-9) Steady-state condition when converter (A) operates as a rectifier (resistive load).
CH1: DC output voltage 50 V/div.
CH2: GTO_2 anode current 20 A/div.
CH4: GTO_2 gate signal 10 V/div.
Time: 5 ms/div.

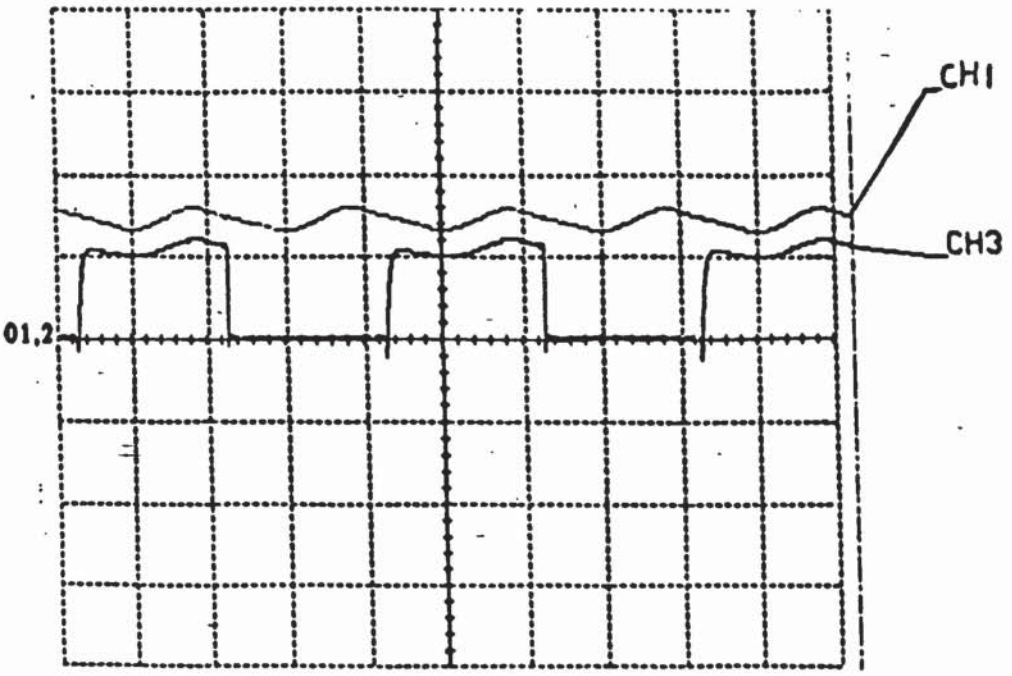


Figure (5-10) Steady-state condition converter when (A) operates as an inverter (resistive load).
CH1: DC output voltage 50 V/div.
CH2: GTO_1 anode current 10 A/div.
Time: 5 ms/div.

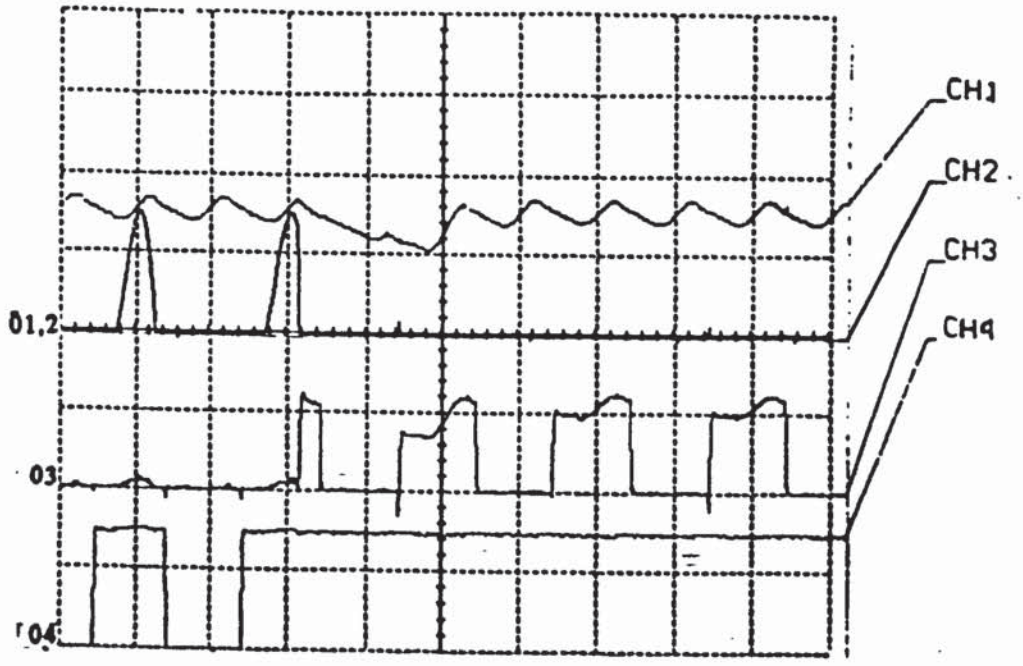


Figure (5-11) Converter (A) transfers from rectifier to inverter operation at $\alpha = \beta = 0°$ (resistive load).

CH1: DC output voltage 50 V/div.

CH2: GTO_2 anode current 20 A/div.

CH3: GTO_1 anode current 10 A/div.

CH4: GTO_2 gate signal 10 V/div.

Time: 10 ms/div.

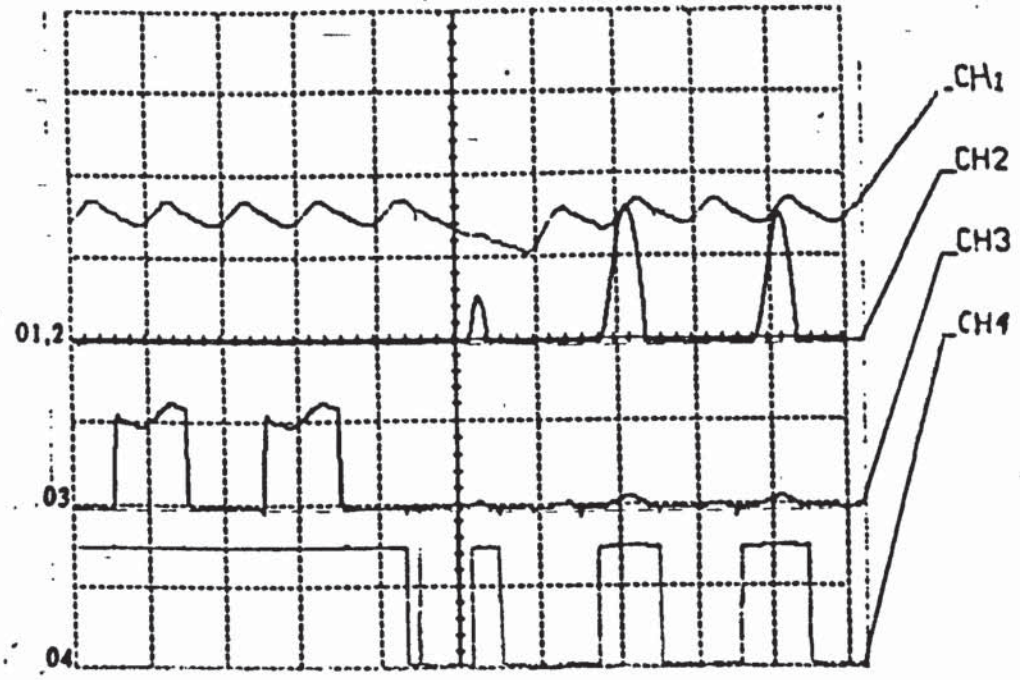


Figure (5-12) Converter (A) transfers from inverter to rectifier operation at $\alpha = \beta = 0°$ (resistive load).

CH1: DC output voltage 50 V/div.

CH2: GTO_2 anode current 20 A/div.

CH3: GTO_1 anode current 10 A/div.

CH4: GTO_2 gate signal 10 V/div.

Time: 10 ms/div.

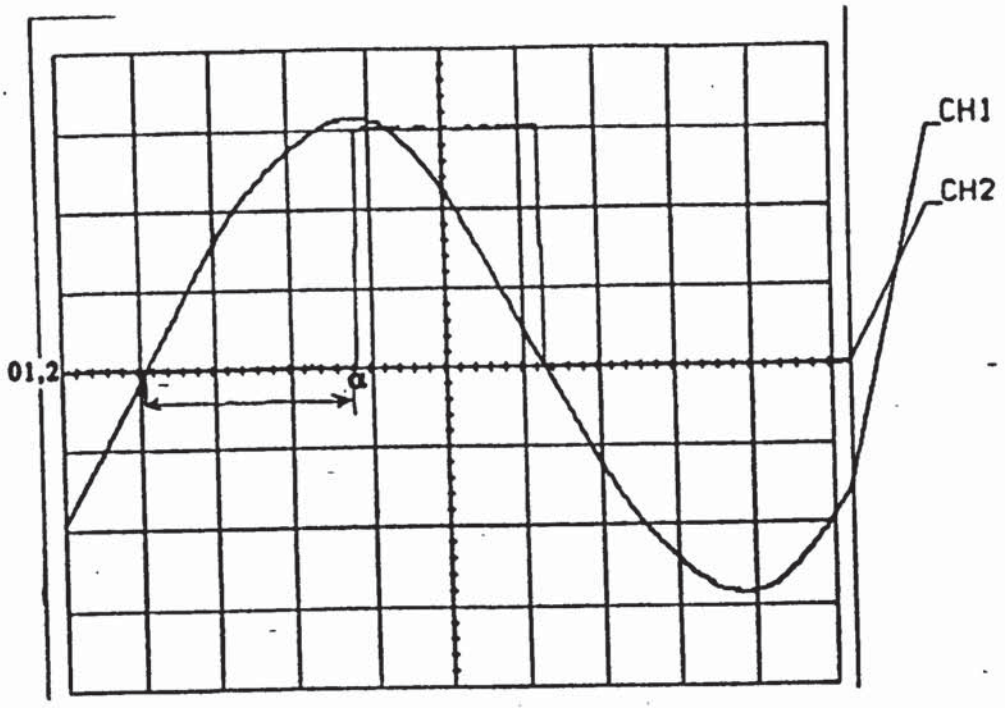


Figure (5-13) Control angle α.
CH1: α control 10 V/div. (α = 90°)
CH2: Sine-wave reference 5 V/div.
Time : 2 ms/div.

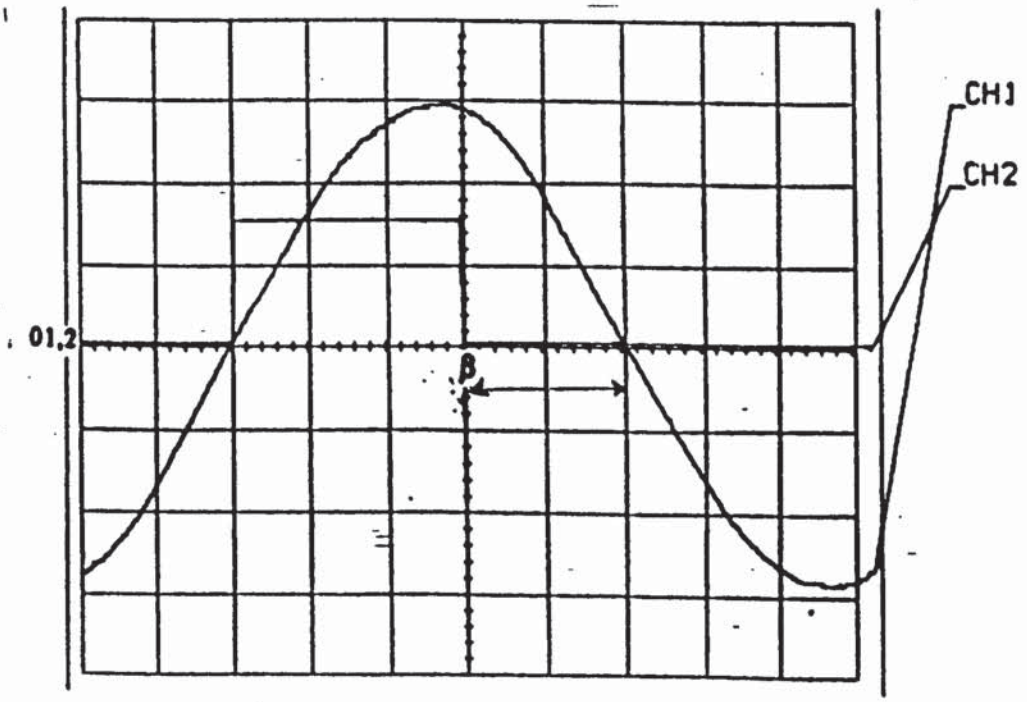


Figure (5-14) Control angle β.
CH1: β control 10 V/div. (β = 72°)
CH2: Sine-wave reference 5 V/div.
Time: 2 ms/div.

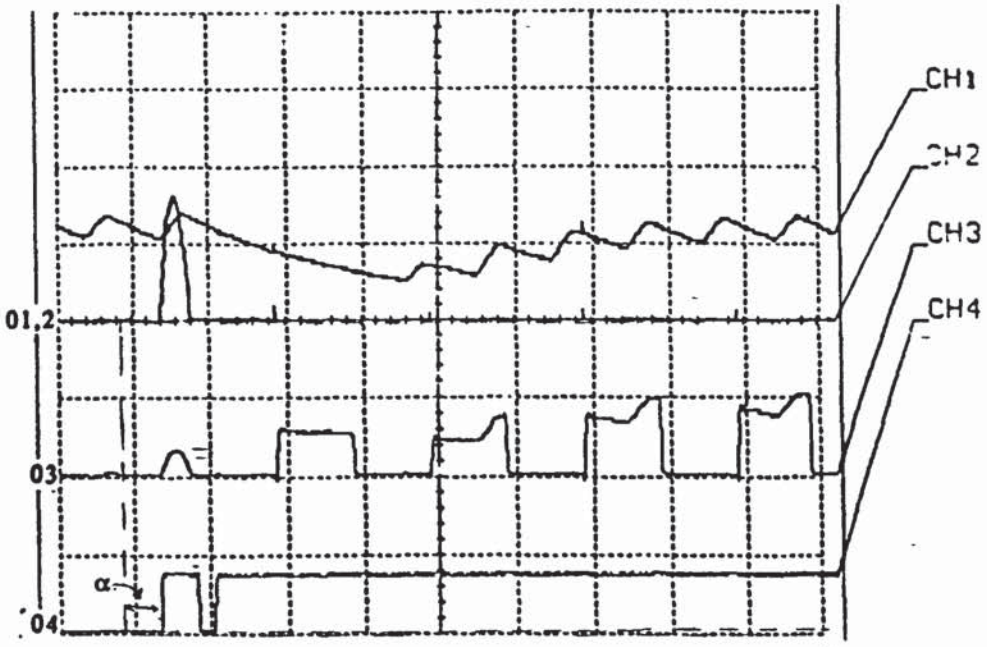


Figure (5-15) Converter (A) transfers from rectifier to inverter operation at $\alpha = 90°$ (resistive load).

CH1: DC output voltage 50 V/div.

CH2: GTO_2 anode current 20 A/div.

CH3: GTO_1 anode current 10 A/div.

CH4: GTO_2 gate signal 10 V/div.

Time : 10 ms/div.

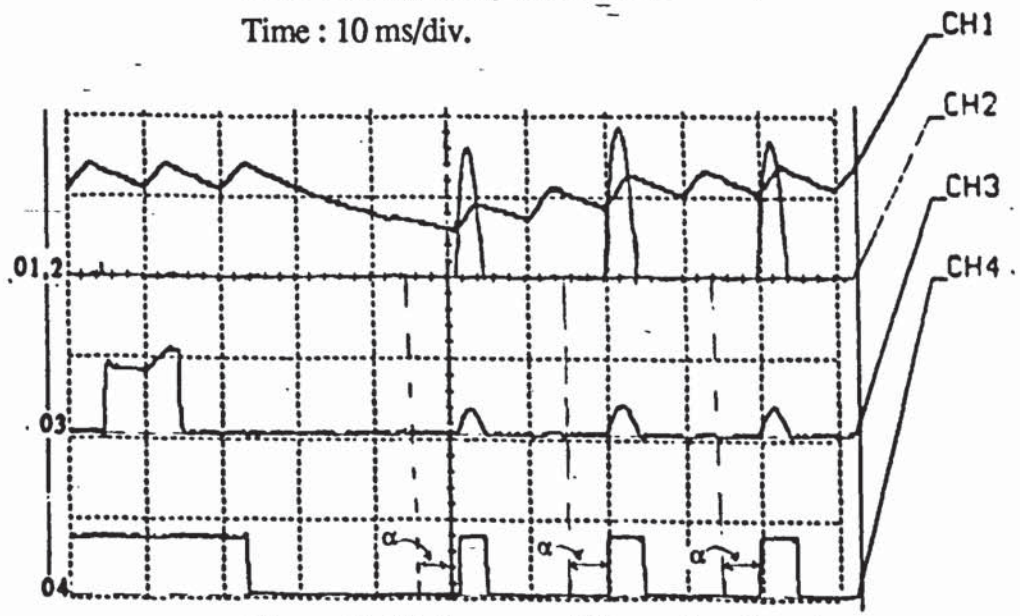


Figure (5-16) Converter (A) transfers from inverter to rectifier operation at $\alpha = 90°$ (resistive load).

CH1: DC output voltage 50 V/div.

CH2: GTO_2 anode current 20 A/div.

CH3: GTO_1 anode current 10 A/div.

CH4: GTO_2 gate signal 10 V/div.

Time: 10 ms/div.

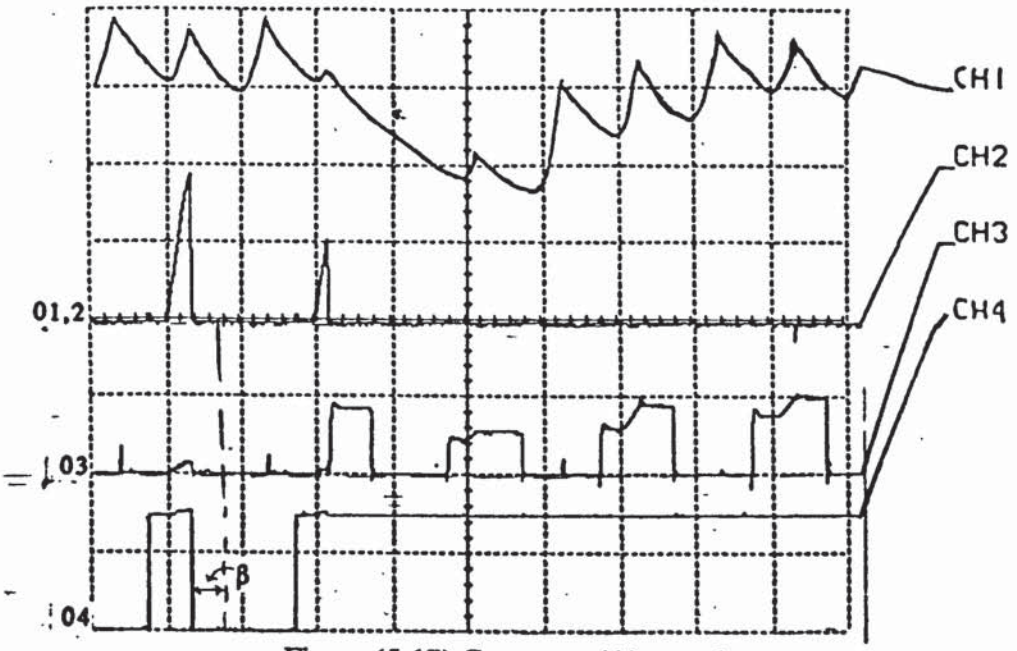


Figure (5-17) Converter (A) transfers from rectifier to inverter operation at $\beta = 72°$ (resistive load).

CH1: DC output voltage 50 V/div.

CH2: GTO_2 anode current 20 A/div.

CH3: GTO_1 anode current 10 A/div.

CH4: GTO_2 gate signal 10 V/div.

Time: 10 ms/div.

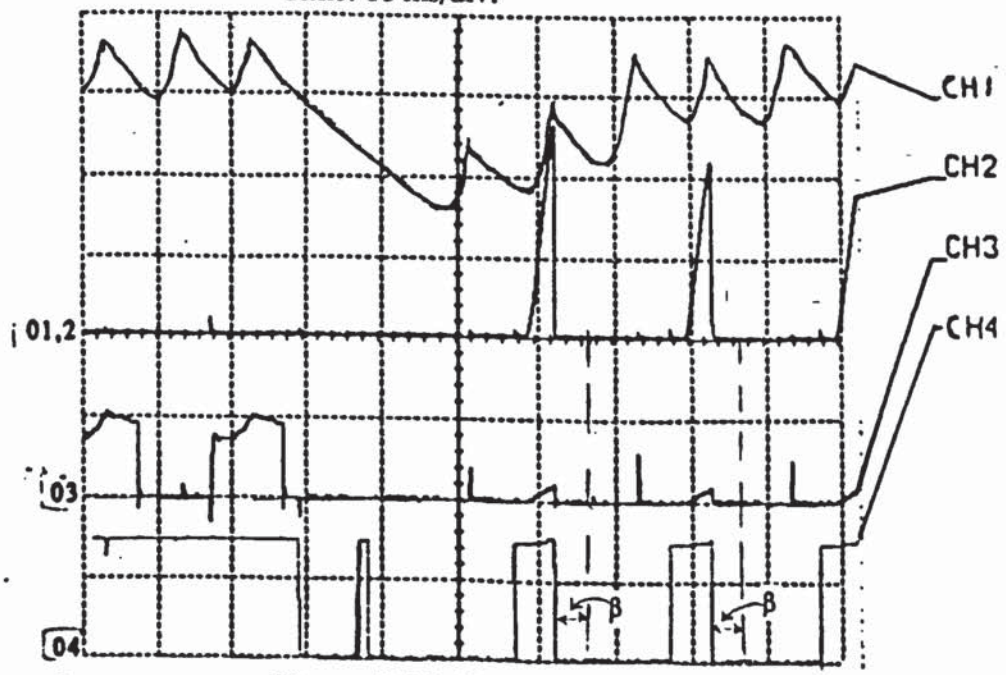


Figure (5-18) Converter (A) transfers from inverter to rectifier operation at $\beta = 72°$ (resistive load).

CH1: DC output voltage 50 V/div.

CH2: GTO_2 anode current 20 A/div.

CH3: GTO_1 anode current 10 A/div.

CH4: GTO_2 gate signal 10 V/div.

Time: 10 ms/div.

5-5 EXPERIMENTAL RESULTS WITH AN INDUCTIVE LOAD.

The system was operated with an inductive load (L = 15 mH, R = 17 Ω); These values were chosen, in order to limit the voltage transient across the transistor to 650 V (refer to section (5-2)).

Figures (5-19) and (5-20) respectively show the theoretical and practical waveforms for the load voltage and current at steady-state condition when converter (A) operates as an inverter. For the positive half cycle, the load current i_L grows exponentially through GTO3 and GTO5 according to:

$$V_L = V_S = L\frac{di_L}{dt} + i_L R \qquad (5\text{-}9)$$

Where V_S is the DC voltage applied to inverter (A) and V_L is the load voltage.

When GTO3 and GTO5 are turned off, GTO1 and GTO7 are turned on, thereby reversing the load voltage. Due to the inductive nature of the load, the load current cannot reverse immediately and the load reactive energy flows back into the supply via GTO2 and GTO8 which operate as diodes. The load voltage is now:

$$V_L = -V_S = L\frac{di_L}{dt} + i_L R \qquad (5\text{-}10)$$

The load current falls exponentially and at zero, GTO1 and GTO7 become forward-biased and conduct load current, thereby feeding power to the load. The output voltage is a square wave and has an RMS value of V_S. During the first half cycle, with no initial load current, by solving equation (5-9) the load current is:

$$i_L = \frac{V_S}{R}\left(1-\exp\left\langle -Rt/L\right\rangle\right) \qquad (5\text{-}11)$$

Under steady-state conditions, the initial current is I_0 as shown in figure (5-19), and equation (5-9) yields:

$$i_L = \frac{V_S}{R} - \left\langle\frac{V_S}{R} - I_0\right\rangle \exp\left\langle -Rt/L\right\rangle \qquad (5\text{-}12)$$

Where:

$0 \leq t \leq t_1$.

$V_L = V_S$.

$I_0 \leq 0$.

During the second half-cycle ($t_1 \leq t \leq t_2$) when the supply is effectively reversed across the load, equation (5-10) yields.

$$i_L = \frac{V_S}{R} + \left\langle \frac{V_S}{R} + I_1 \right\rangle \exp\left\langle -Rt / L \right\rangle \qquad (5\text{-}13)$$

Where:

$0 \leq t \leq (t_2 - t_1)$.

$V_L = -V_S$.

$I_1 \geq 0$.

Since $I_1 = -I_0$, the initial steady-state current I_1 can be found from equation (5-12) when, at $t = t_1$, $i_L = I_1$ yielding:

$$I_1 = \frac{V_S}{R} \frac{\left(1 - \exp\left\langle -Rt_1 / L \right\rangle\right)}{\left(1 + \exp\left\langle -Rt_1 / L \right\rangle\right)} \qquad (5\text{-}14)$$

The zero current cross-over point t_x, shown on figure (5-19), can be found by solving equation (5-12) for t when $i_L = 0$, which yields:

$$t_x = \frac{L}{R} \ln\left\langle 1 - I_0 R / V_S \right\rangle \qquad (5\text{-}15)$$

The derivations of the above formulas are given in Appendix (D). Theoretically, the current I_1 and the zero current cross over point t_x can be calculated as follows:

Referring to figure (5-20), the maximum load voltage is 170 V. From equation (5-14), and by putting R = 17 Ω, L = 15 mH, t_1 = 10 ms, the amplitude of the current $I_1 = I_0 = 9.9$ A. From equation (5-15), $t_x = 3.45$ ms.

Referring again to figure (5-20), the amplitude of $I_1 = I_0 = 9$ A, and $t_x = 3$ ms. There is a small difference between the theoretical and practical results (9% with the current and 13% with tx) due to the accuracy of the parameters and the measurement results.

Figure (5-21) shows the steady state waveforms of the DC voltage, GTO2 and GTO3 anode currents when converter (A) operates as an inverter. The current is transferred from GTO3 to GTO2 which operates as a diode which returns the reactive energy from the load back to the DC supply.

Figure (5-22) shows the the steady-state waveforms when converter (A) operates as a rectifier. The peak current through each GTO is approximately 20 A and the DC voltage is 85 V.

Figure (5-23) shows the waveforms when converter (A) transfers from rectifier to inverter operation at $\alpha = \beta = 0°$. GTO2 transfers from a controlled device to a diode (always on), to carry the stored energy from the load. Figure (5-24) shows the waveforms when converter (A) transfers from inverter to rectifier operation at $\alpha = \beta = 0°$. In both cases,the change over takes place without transient.

Figure (4-25) shows the waveforms when converter (A) transfers from rectifier to inverter operation at $\alpha = 90°$ and $\beta = 0°$. Figure (5-26) shows the waveforms when converter (A) transfers from inverter to rectifier operation at $\alpha = 90°$ and $\beta = 0°$. Figure (5-27) shows the waveforms when converter (A) transfers from rectifier to inverter operation at $\beta = 90°$ and $\alpha = 0°$. Figure (5-28) shows the waveforms when converter (A) transfers from inverter to rectifier operation at $\beta = 90°$ and $\alpha = 0°$.

The above results show that the system works well with resistive and inductive loads, without transient. However, there are some points which are worth mentioning at this stage. When either converter (A) or (B) operates as an inverter with a resistive load, the antiparallel GTOs have no effect, since there is no energy to be fed to the DC link.

When either converter (A) or (B) transfers from rectifier to inverter operation, a delay time is introduced, to transfer the antiparallel GTO in each arm to a diode before the change takes place (for more details refer to Chapter 4). This procedure was introduced to prevent any voltage spikes when GTO/diode transformation takes place with an inductive load.

An RC snubber was connected across each transformer secondary to protect the devices from such fault (supply failures, load change). As explained in equation (5-3) the value of capacitance is given by:

$$C = \frac{VA}{31f(V_{pk})^2}$$

Where:

VA = volt- ampere rating of transformer (VA).

f = supply frequency (Hz).

V_{pk} = peak voltage rating of the semiconductor device (V).

The volt-ampere rating of each transformer is 2 kVA. The peak non-repetitive reverse voltage of the GTO is 1200 V and the peak reverse voltage of the diode is 1000 V (refer to figure (5-1) there is a diode in series with each GTO). For a margin of safety, the calculation was carried out with Vpk = 800 V. Referring to the above equation, the capacitor value is C = 2 μF

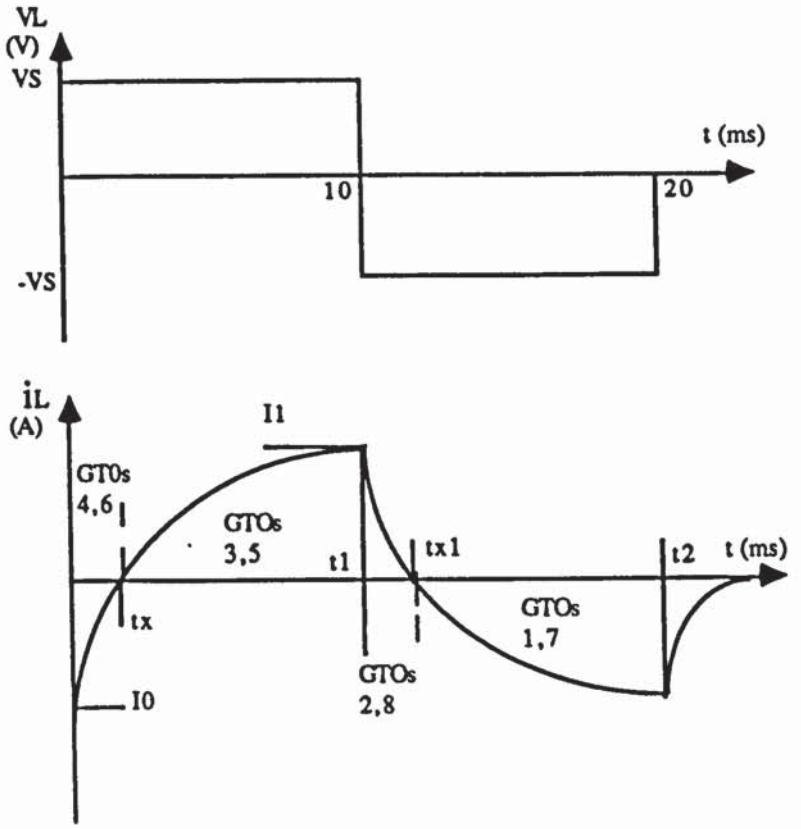


Figure (5-19) Theoretical load current and voltage for inverter operation (inductive load).

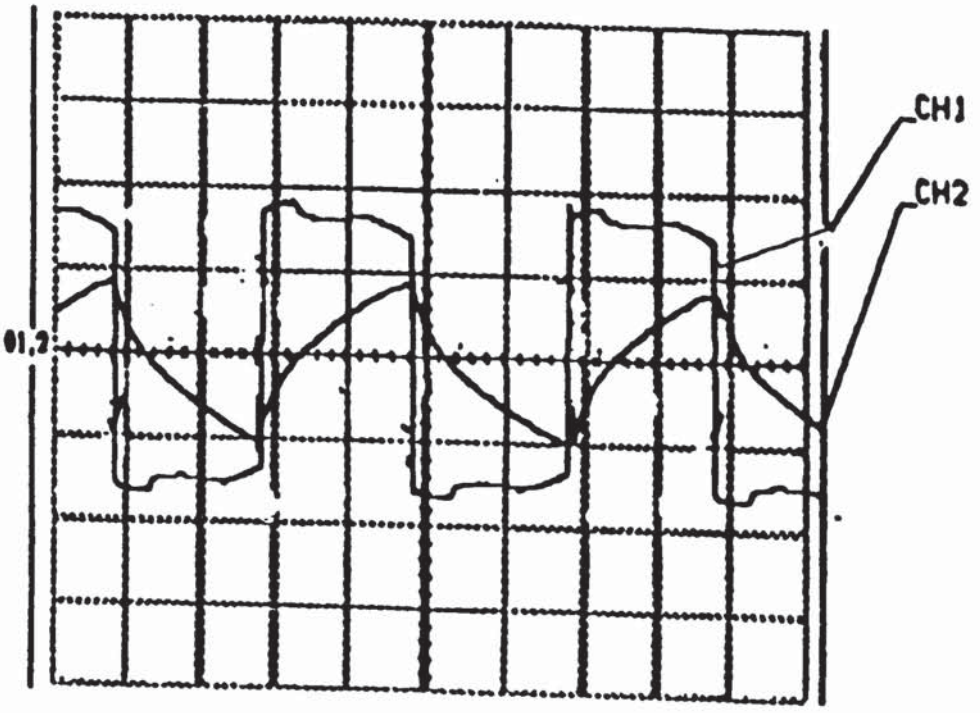


Figure (5-20) Steady-state load voltage and current when converter (A) operates as an inverter (inductive load).

CH1: Load voltage 100 V/div.

CH2: Load current 9 A/div.

Time: 5 ms/div.

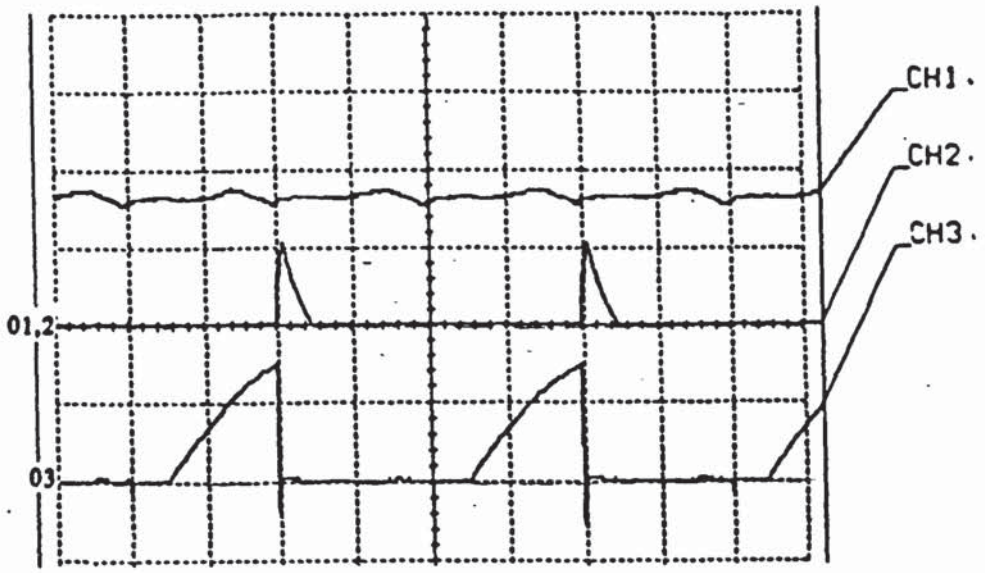


Figure (5-21) Steady-state condition when converter (A) operates as an inverter (inductive load).
CH1: DC output voltage 50 V/div.
CH2: GTO_2 anode current 10 A/div.
CH3: GTO_3 anode current 10 A/div.
Time: 5 ms/div.

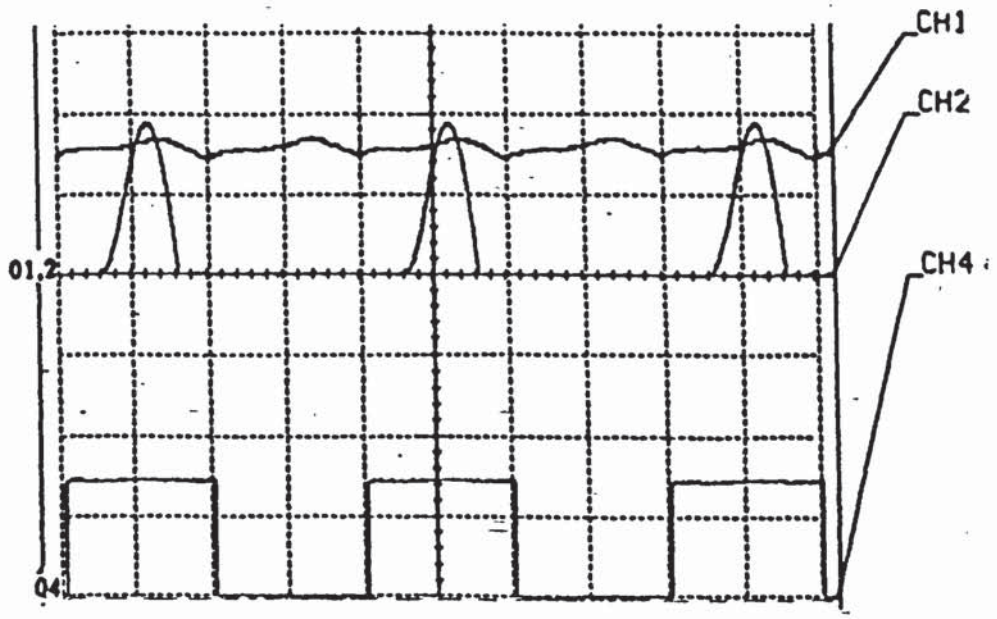


Figure (5-22) Steady-state condition when converter (A) operates as a rectifier (inductive load).
CH1: DC output voltage 50 V/div.
CH2: GTO_2 anode current 10 A/div.
CH4: GTO_2 gate signal 10 V/div.
Time: 5 ms/div.

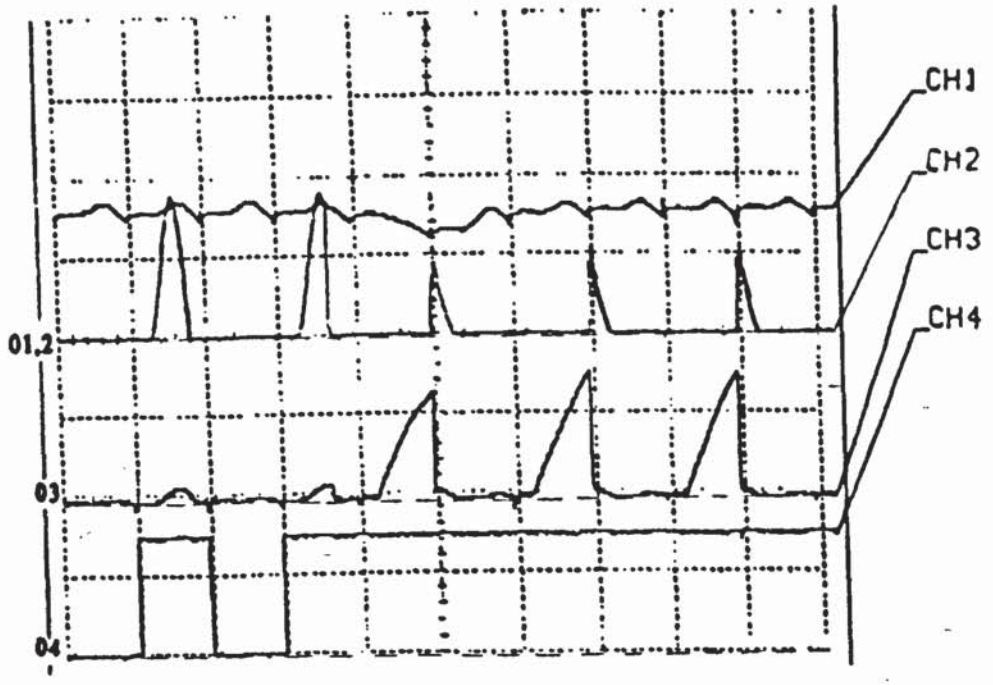


Figure (5-23) Converter(A) transfers from rectifier to inverter operation at $\alpha = \beta = 0°$ (inductive load).

CH1: DC output voltage 50 V/div.

CH2: GTO_2 anode current 10 A/div.

CH3: GTO_3 anode current 10 A/div.

CH4: GTO_2 gate signal 10 V/div.

Time: 10 ms/div.

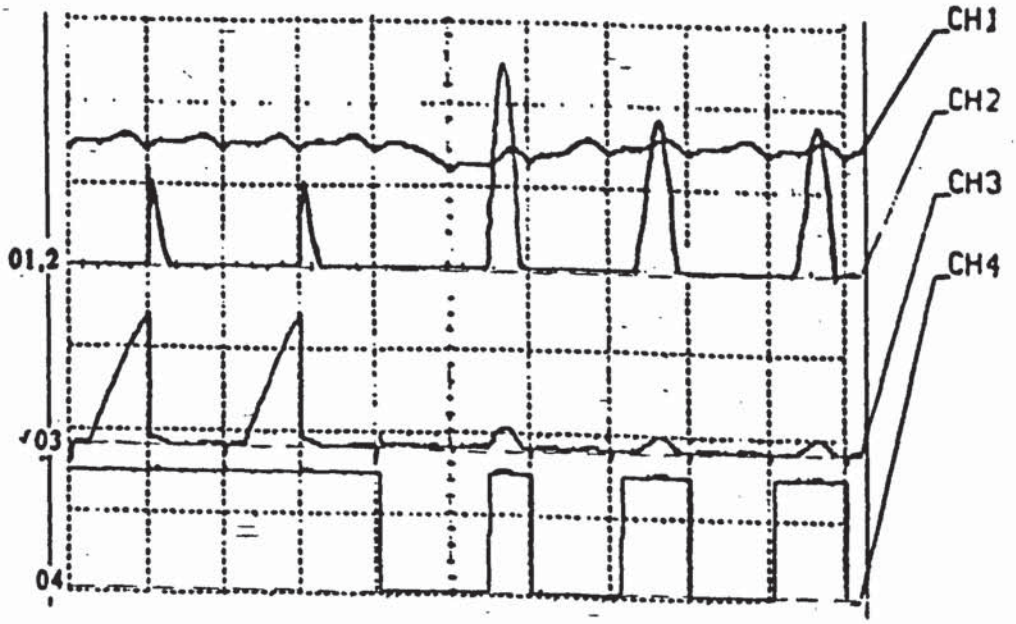


Figure (5-24) Converter(A) transfers from inverter to rectifier operation at $\alpha = \beta = 0°$ (inductive load).

CH1: DC voltage output 50 V/div.

CH2: GTO_2 anode current 10 A/div.

CH3: GTO_3 anode current 10 A/div.

CH4: GTO_2 gate signal 10 V/div.

Time: 10 ms/div.

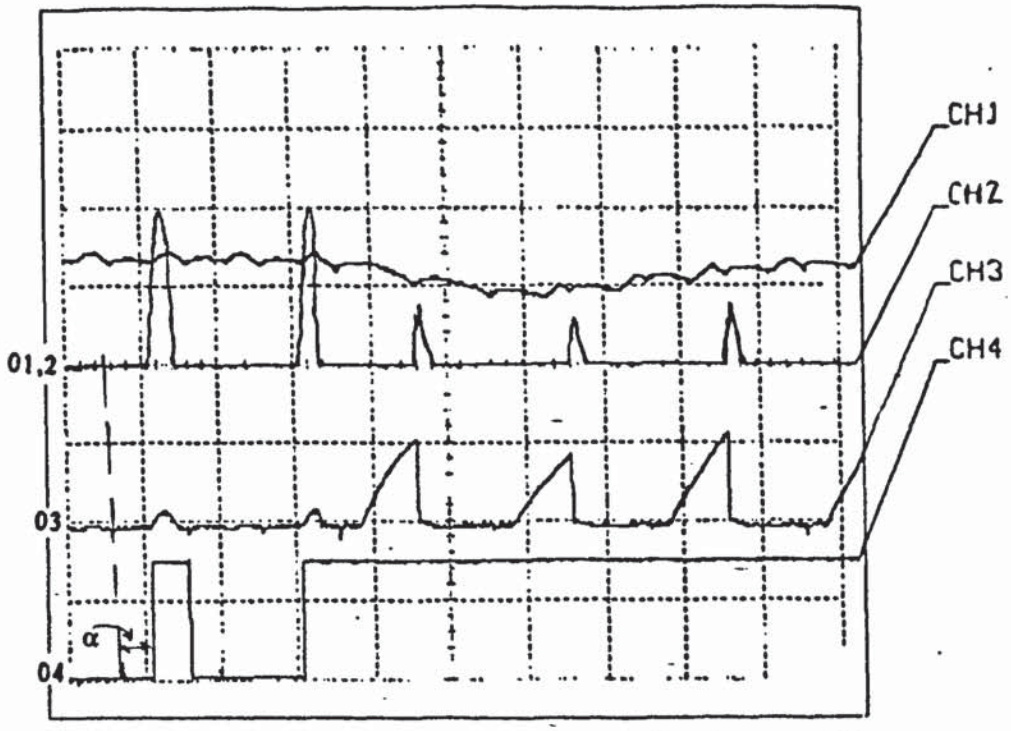


Figure (5-25) Converter(A) transfers from rectifier to inverter operation at $\alpha = 90°$ (inductive load).

CH1: DC output voltage 50 V/div.

CH2: GTO_2 anode current 10 A/div.

CH3: GTO_3 anode current 10 A/div.

CH4: GTO_2 gate signal 10 V/div.

Time: 10 ms/div.

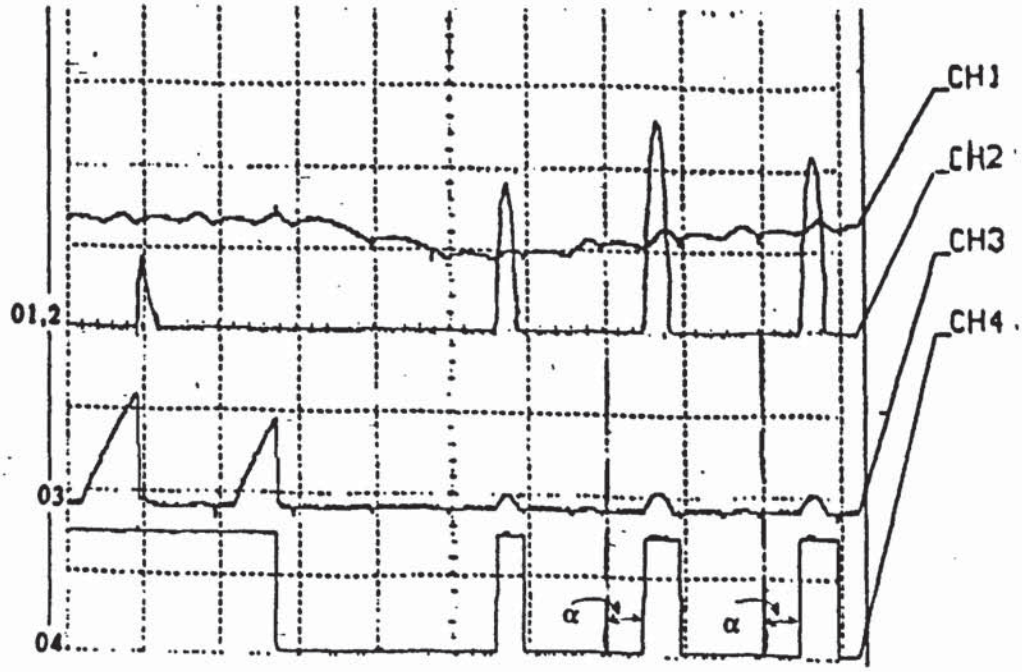


Figure (5-26) Converter (A) transfers from inverter to rectifier operation at $\alpha = 90°$ (inductive load).

CH1: DC voltage output 50 V/div.

CH2: GTO_2 anode current 10 A/div.

CH3: GTO_3 anode current 10 A/div.

CH4: GTO_2 gate signal 10 V/div.

Time : 10 ms/div.

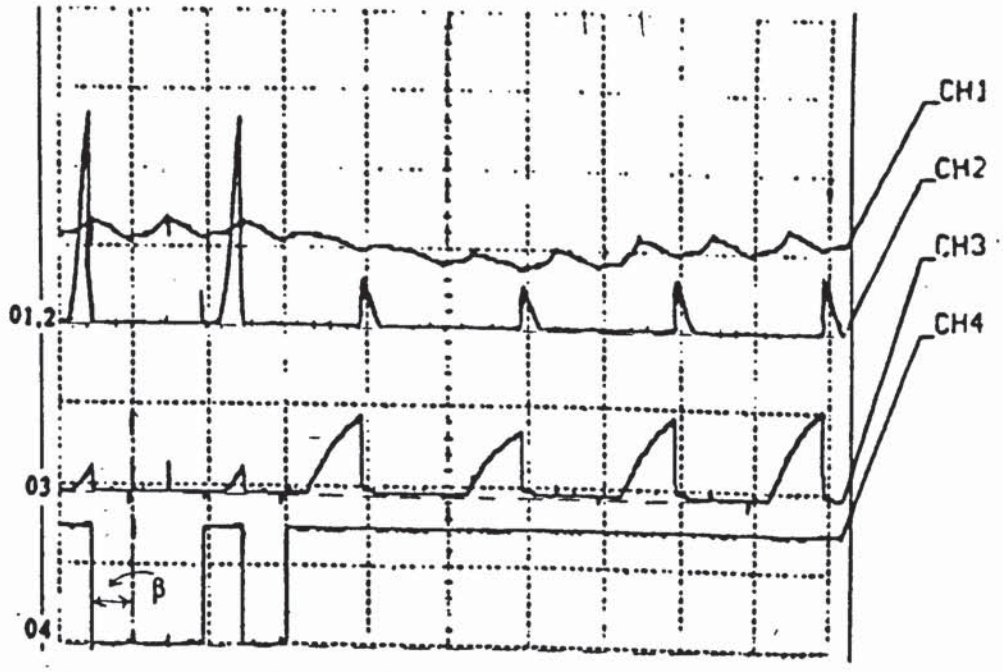


Figure (5-27) Converter (A) transfers from rectifier to inverter operation at $\beta = 90°$ (inductive load).
CH1: DC output voltage 50 V/div.
CH2: GTO_2 anode current 10 A/div.
CH3: GTO_3 anode current 10 A/div.
CH4: GTO_2 gate signal 10 V/div.
Time: 10 ms/div.

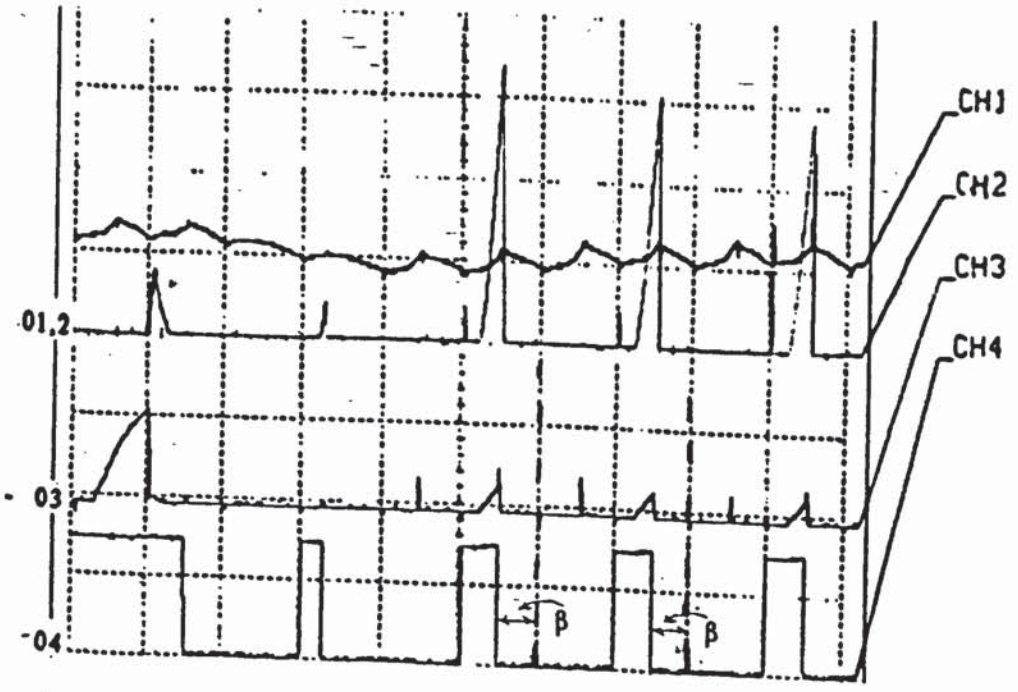


Figure (5-28) Converter(A) transfers from inverter to rectifier operation at $\beta = 90°$ (inductive load).
CH1: DC output voltage 50 V/div.
CH2: GTO_2 anode current 10 A/div.
CH3: GTO3 anode current 10 A/div.
CH4: GTO_2 gate signal 10 V/div.
Time: 10 ms/div.

5-6 POWER FACTOR IMPROVEMENT.

The power factor of a sinusoidal AC system is equal to the cosine of the angle between the current and the voltage ϕ. This angle is called the displacement angle (power factor = cos ϕ). However, a rectifier draws a non-sinusoidal current from the AC system and the value cos ϕ does not represent the power factor. The firing delay has the effect of delaying the supply current relative to its phase voltage and the power factor is (2,3):

$$P.F. = \frac{\text{mean power}}{V_{RMS}\, I_{RMS}} \tag{5-16}$$

The current contains harmonic components which result in an RMS value higher than the RMS value of its fundamental component. Thus, the power factor is less than the cosine of the displacement angle.

The supply voltage of the rectifier may be considered to be sinusoidal and consequently the mean power is:

$$P_{mean} = V_{RMS}\, I_{1RMS} \cos\phi_1 \tag{5-17}$$

Where the suffix 1 relates to the fundamental component of the current and ϕ_1 is the phase angle between the voltage and the fundamental component of the current.

Therefore:

$$P.F. = \frac{I_{1RMS}}{I_{RMS}} \cos\phi_1 \tag{5-18}$$

Where:

$\frac{I_{1RMS}}{I_{RMS}}$ is defined as the input distortion factor and

$\cos \phi_1$ is the input displacement factor.

The rectifier circuit of figure (5-29-a) is used to compare the variation of the power factor by varying angles α and β.

5-6-1 RECTIFIER POWER FACTOR FOR VARIATION OF ANGLE α.

Figure (5-29-a) shows a single phase fully controlled GTO thyristor rectifier. The load is assumed to be highly inductive and the output current is always continuous. Figure (5-29-b) shows the circuit waveforms for variation of angle α, assuming that the GTOs will be turned-off due to the natural commutation.

The mean output voltage is:

$$V_{dc} = \frac{1}{\pi}\int_{\alpha}^{\pi+\alpha} V_m \sin \omega t \, d(\omega t) = \frac{2V_m}{\pi}\cos \alpha \qquad (5\text{–}19)$$

Supply current waveform may be expressed by the Fourier series:

$$i(t) = I_{dc} + \sum_n (a_n \cos(n\,\omega t) + b_n \sin(n\,\omega t)) \qquad (5\text{-}20)$$

Where:

$$I_{dc} = \frac{1}{2\pi}\int_{\alpha}^{2\pi+\alpha} i(t)\, d(\omega t) = 0 \qquad (5\text{-}21)$$

$$a_n = \frac{1}{\pi}\int_{\alpha}^{2\pi+\alpha} i(t) \cos(n\omega t)\, d(\omega t) \qquad (5\text{-}22)$$

$$b_n = \frac{1}{\pi}\int_{\alpha}^{2\pi+a} i(t) \sin(n\omega t)\, d(\omega t) \qquad (5\text{-}23)$$

$$c_n = \sqrt{a_n^2 + b_n^2} \qquad (5\text{-}24)$$

$$\phi_n = \tan^{-1}\frac{a_n}{b_n} \qquad (5\text{-}25)$$

From figure (5-29-b) the fundamental component is:

$$a_1 = \frac{1}{\pi}\int_{\alpha}^{\pi+\alpha} I_L \cos(\omega t)\, d(\omega t) \;\; \frac{1}{\pi}\int_{\pi+\alpha}^{2\pi+\alpha} I_L \cos(\omega t)\, d(\omega t) \qquad (5\text{-}26)$$

$$a_1 = \frac{4I_L}{\pi}\sin \alpha \qquad (5\text{–}27)$$

$$b_1 = \frac{1}{\pi}\int_{\alpha}^{\pi+\alpha} I_L \sin(\omega t)\, d(\omega t) - \int_{\pi+\alpha}^{2\pi+\alpha} I_L \sin(\omega t)\, d(\omega t) \qquad (5\text{-}28)$$

$$b_1 = \frac{4I_L}{\pi}\cos\alpha \qquad (5\text{-}29)$$

$$c_1 = \frac{4I_L}{\pi}\sqrt{\sin\alpha^{\,2} + \cos\alpha^{\,2}} = \frac{4I_L}{\pi} \qquad (5\text{-}30)$$

$$\phi_1 = \tan^{-1}\frac{a_1}{b_1} = \tan^{-1}\left(\frac{\sin\alpha}{\cos\alpha}\right) = -\alpha \qquad (5\text{-}31)$$

The RMS value of the fundamental current is:

$$I_{1RMS} = \frac{c_1}{\sqrt{2}} = \frac{2\sqrt{2}I_L}{\pi} \qquad (5\text{-}32)$$

The RMS value of the input current is:

$$I_{RMS} = \left[\frac{1}{\pi}\int_{\alpha}^{\alpha+\pi} I_L^2\, d(\omega t)\right]^{\frac{1}{2}} = I_L \qquad (5\text{-}33)$$

Referring to equation (5-18), the power factor is:

$$P.F. = \frac{I_{1RMS}}{I_{RMS}}\cos -\alpha = \frac{2\sqrt{2}}{\pi}\cos\alpha \qquad (5\text{-}34)$$

The power factor is lagging.

5-6-2 RECTIFIER POWER FACTOR FOR VARIATION OF ANGLE β.

The power factor decreases as firing angle α decreases. Forced commutation can improve the input power factor and this can be achieved by controlling angle β. Figure (5-29-c) shows the waveforms as angle β changes. The free-wheeling diode is connected to provide a path for the inductive load current. The mean output voltage is:

$$V_{dc} = \frac{1}{\pi}\int_{0}^{\pi-\beta} V_m \sin\omega t\, d(\omega t) = \frac{V_m}{\pi}(1+\cos\beta) \qquad (5\text{-}35)$$

and the fundamental component of the input current is:

$$a_1 = \frac{1}{\pi}\int_0^{\pi-\beta} I_L \cos(\omega t)\, d(\omega t) - \frac{1}{\pi}\int_{\pi}^{2\pi-\beta} I_L \cos(\omega t)\, d(\omega t) \tag{5-36}$$

$$a_1 = \frac{2I_L}{\pi}\sin\beta \tag{5-37}$$

$$b_1 = \frac{1}{\pi}\int_0^{\pi-\beta} I_L \sin(\omega t)\, d(\omega t) - \frac{1}{\pi}\int_{\pi}^{2\pi-\beta} I_L \sin(\omega t)\, d(\omega t) \tag{5-38}$$

$$b_1 = \frac{2I_L}{\pi}(1+\cos\beta) \tag{5-39}$$

$$c_1 = \frac{2I_L}{\pi}\sqrt{\sin\beta^2 + (1+\cos\beta)^2} \tag{5-40}$$

$$c_1 = \frac{2\sqrt{2}I_L}{\pi}\sqrt{1+\cos\beta} \tag{5-41}$$

But:

$$1+\cos\beta = 2\cos^2\frac{\beta}{2} \tag{5-42}$$

Therefore:

$$c_1 = \frac{2\sqrt{2}I_L}{\pi}\sqrt{2}\cos\frac{\beta}{2} \tag{5-43}$$

The RMS value of the fundamental current is:

$$I_{1RMS} = \frac{c_1}{\sqrt{2}} = \frac{2\sqrt{2}I_L}{\pi}\cos\frac{\beta}{2} \tag{5-44}$$

The input displacement factor is:

$$\phi_1 = \tan^{-1}\frac{a_1}{b_1} = \tan^{-1}\left(\frac{\sin\beta}{1+\cos\beta}\right) = \tan^{-1}\left(\frac{\sin\beta}{2\cos^2\frac{\beta}{2}}\right) \tag{5-45}$$

But:

$$\sin\beta = \sin 2\frac{\beta}{2} = 2\sin\frac{\beta}{2}\cos\frac{\beta}{2} \tag{5-46}$$

Therefore:

$$\phi_1 = \tan^{-1}\left(\frac{2\sin\frac{\beta}{2}\cos\frac{\beta}{2}}{2\cos^2\frac{\beta}{2}}\right) = \frac{\beta}{2} \qquad (5\text{–}47)$$

The RMS input current is:

$$I_{RMS} = \sqrt{\frac{1}{\pi}\int_0^{\pi-\beta} I_L^2\, d(\omega t)} = I_L\sqrt{1-\frac{\beta}{\pi}} \qquad (5\text{-}48)$$

Referring to equation (5-18), the power factor is:

$$P.F. = \frac{I_{1RMS}}{I_{RMS}}\cos\frac{\beta}{2} = \frac{2\sqrt{2}I_L\cos^2\frac{\beta}{2}}{\pi I_L\sqrt{1-\frac{\beta}{\pi}}} \qquad (5\text{-}49)$$

$$P.F. = \frac{2\sqrt{2}\cos^2\frac{\beta}{2}}{\pi\sqrt{1-\frac{\beta}{\pi}}} = \frac{\sqrt{2}\,(1+\cos\beta)}{\sqrt{\pi\,(\pi-\beta)}} \qquad (5\text{-}50)$$

The power factor is leading.

The power factor was investigated analytically for a fully controlled bridge with a highly inductive load. Tables (5-2) shows the theoretical and practical results for the power factor when angles α and β are varied. When angle $\alpha > \phi$ (ϕ is the phase angle of the load, $\phi = \tan^{-1}\omega L/R$), the load current becomes discontinuous, for the theoretical results and when $\alpha > \phi$, it was assumed that an active load is connected to the output of the rectifier to maintain the current flow continuously. For the practical result the rectifier was tested with an inductive load (L = 80 mH. R = 9 Ω), this gives phase angle $\phi = 70°$. For the practical results α was varied from 0° to 54°. There is a slight difference between the theoretical and practical results (7% maximum difference). This is due to the accuracy of the power factor meter, the exact values of angles α and β and the commutation angle of the GTO. Figure (5-30)

shows the variation of power factor with α and β. Table (5-2) and figure (5-31) show the theoretical variation of V_{dc}/V_m with α and β, the load current is also assumed to be always continuous.

Figures (5-32) and (5-33) show the supply and load voltages and currents with a highly inductive load and with $\alpha = \beta = 0°$. The load current is almost constant and the supply current is almost a square wave.

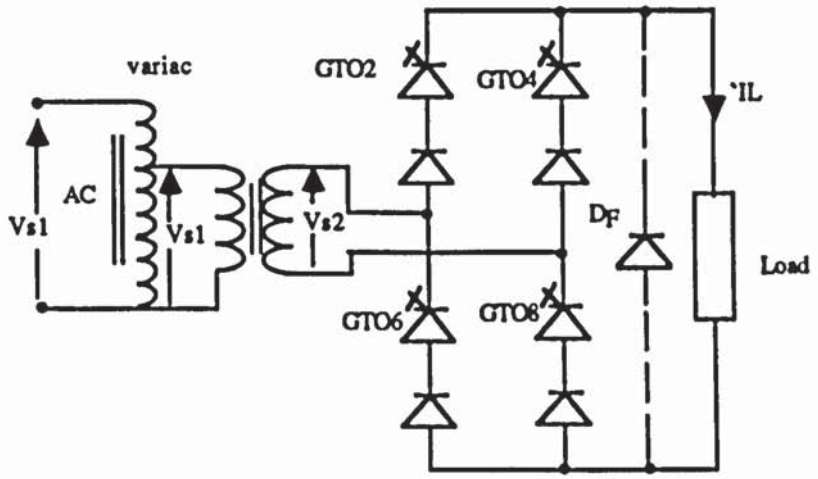
Figures (5-34) and (5-35) show the supply and load voltages and currents for $\alpha = 54°$. Figures (5-36) and (5-37) show the supply and load voltages and currents when $\beta = 54°$.

The notches in each half-cycle of the input voltage waveform occur at commutation instants and due to the supply inductance (the leakage inductances of the variac and the transformer). Referring to figure (5-29-a),V_{s1} is the AC supply voltage, V_{s2} is the voltage after the variac and transformer and L_S is the total leakage inductance of the AC line.

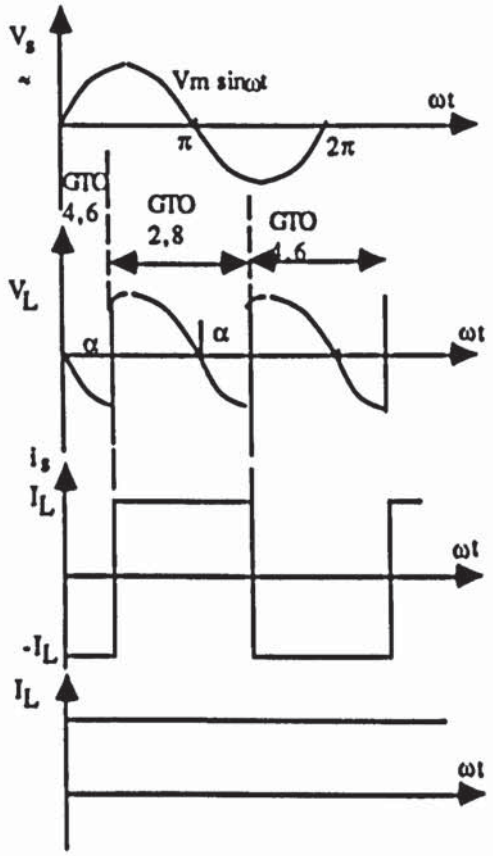
$$V_{s2} = V_{s1} - L_s \frac{di_s}{dt} \qquad (5\text{-}51)$$

When a GTO starts to conduct at angle α, the rate of rise of the anode current is positive giving a positive induced voltage across the inductor L_s. Referring to equation (5-51) and figure (5-34), the supply is reduced by $L_s\, di_s/dt$ every time a GTO commence conduction.

When angle β is controlled, the current is started at 0° and is chopped at $\beta°$. The GTOs are turned-off by forced commutation and the rate of rise of the current is negative, which produces a negative voltage across the inductor L_s. Again referring to equation (5-51) and figure (5-36), the supply voltage is increased by $L_s\, di_s/dt$ every time the GTO is turned-off and the current is chopped.

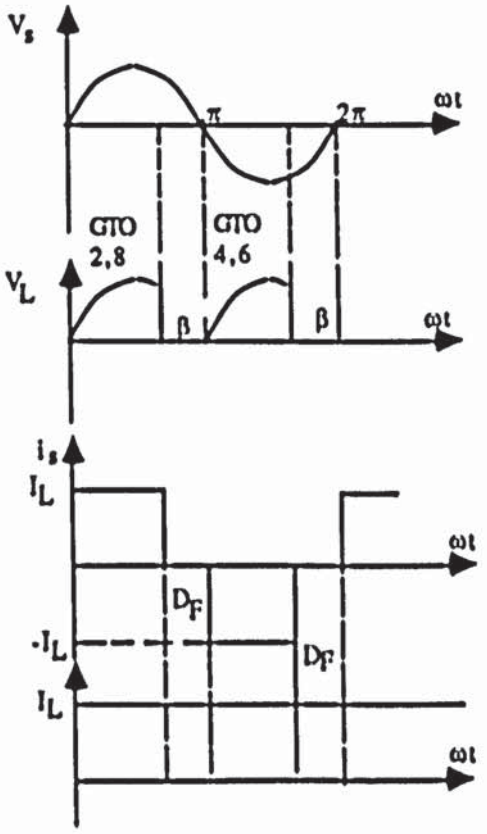


(a) Circuit connections.



(b) Voltage and current waveforms when α changes.

(for these waveforms D_F is removed)



(c) Voltage and current waveforms when β changes.

Figure (5-29) Single phase bridge rectifier.

angle in degrees	P.F for α theoretical	P.F for α practical	P.F for β theoretical	P.F for β practical
0	0.900	0.908	0.900	0.915
15	0.869	0.863	0.924	0.930
30	0.779	0.800	0.920	0.925
45	0.636	0.700	0.887	0.900
54	0.529	0.55	0.854	0.86
60	0.45		0,826	0.855
75	0.233		0.741	0.770
90	0		0.636	0.683

Table (5-2) Variation of power factor with α and β.

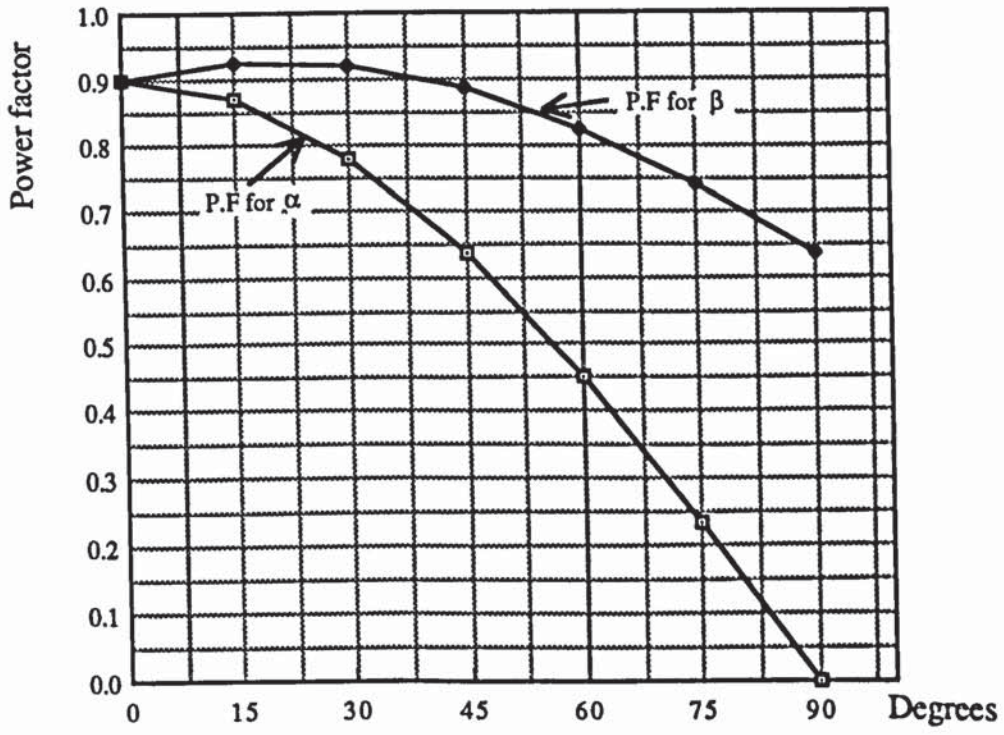


Figure (5-30) Variation of Power factor with α and β

angle in degrees	Vdc/Vm for α	Vdc/Vm for β
0	0.636	0.636
15	0.614	0.625
30	0.551	0.593
45	0.450	0.543
60	0.318	0.477
75	0.164	0.400
90	0	0.318
105	-0.164	0.235
120	-0.318	0.159
150	-0.551	0.042
180	-0.636	0

Table (5-3) Variation of Vdc/Vm with α and β.

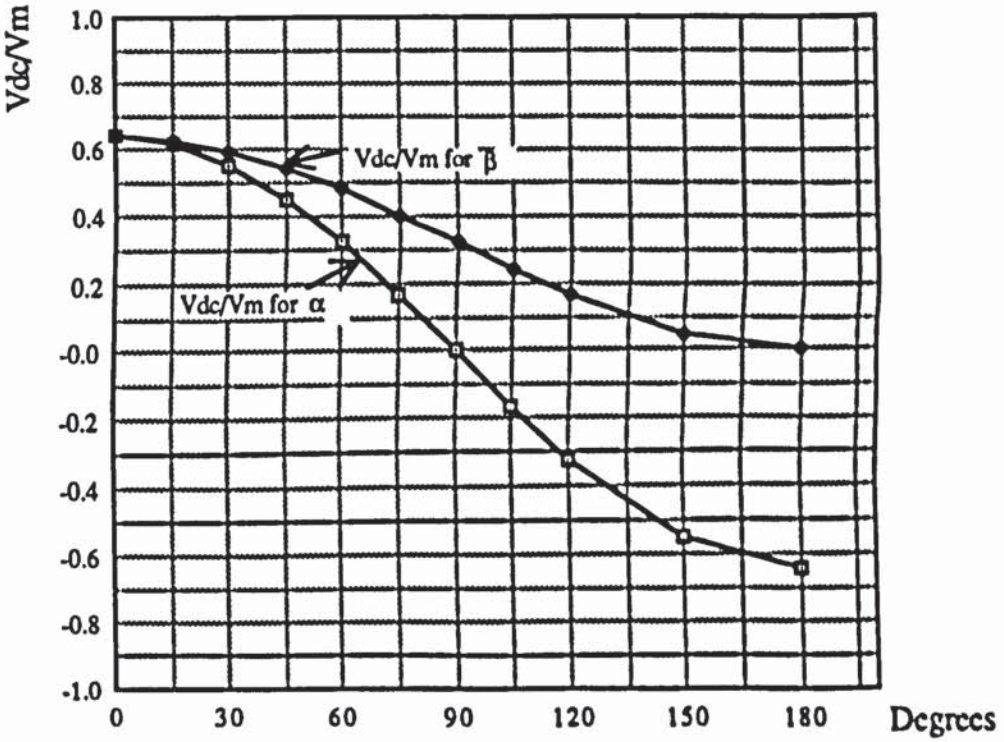


Figure (5-31) Variation of Vdc/Vm with α and β.

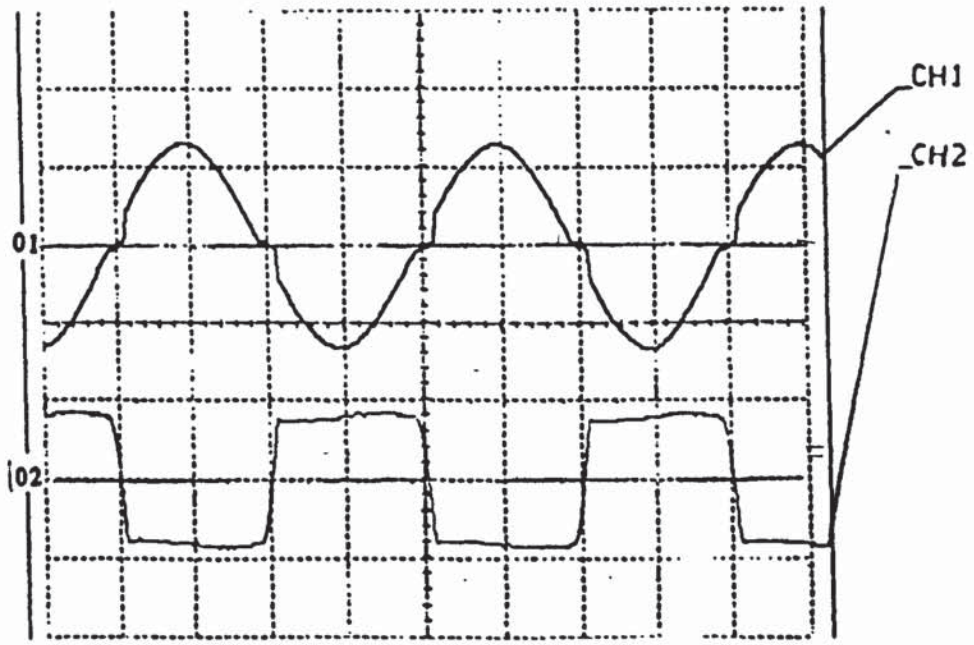


Figure (5-32) Supply voltage and current for a highly inductive load.
$\alpha = \beta = 0°$.
CH1: Supply voltage 100 V/div.
CH2: Supply current 10 A/div.
Time: 5 ms/div.

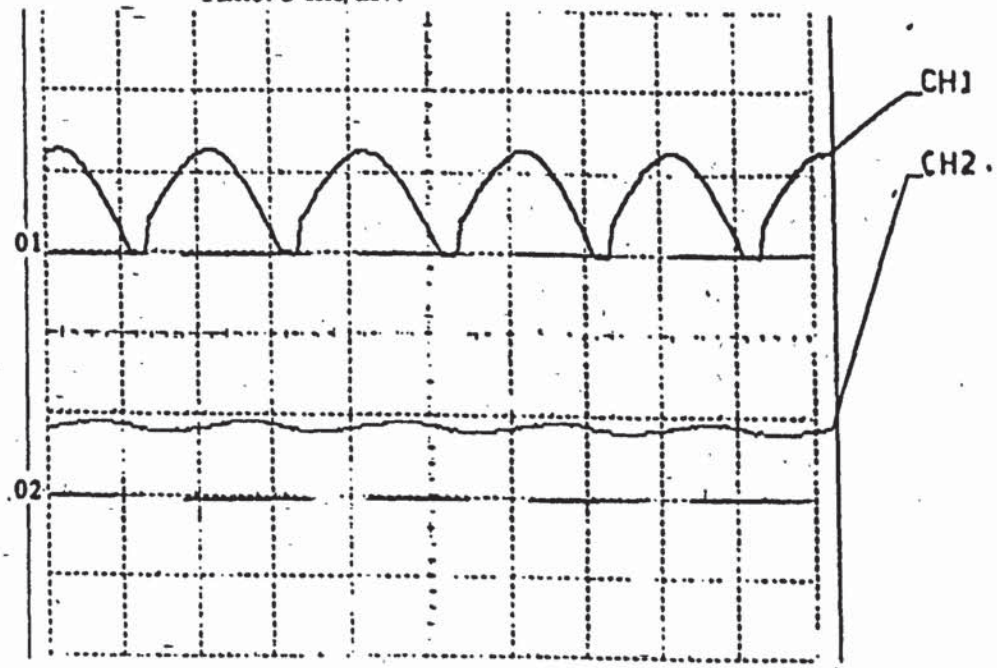


Figure (5-33) Load voltage and current for a highly inductive load.
$\alpha = \beta = 0°$.
CH1: Load voltage 100 V/div.
CH2: Load current 10 A/div.
Time: 5 ms/div.

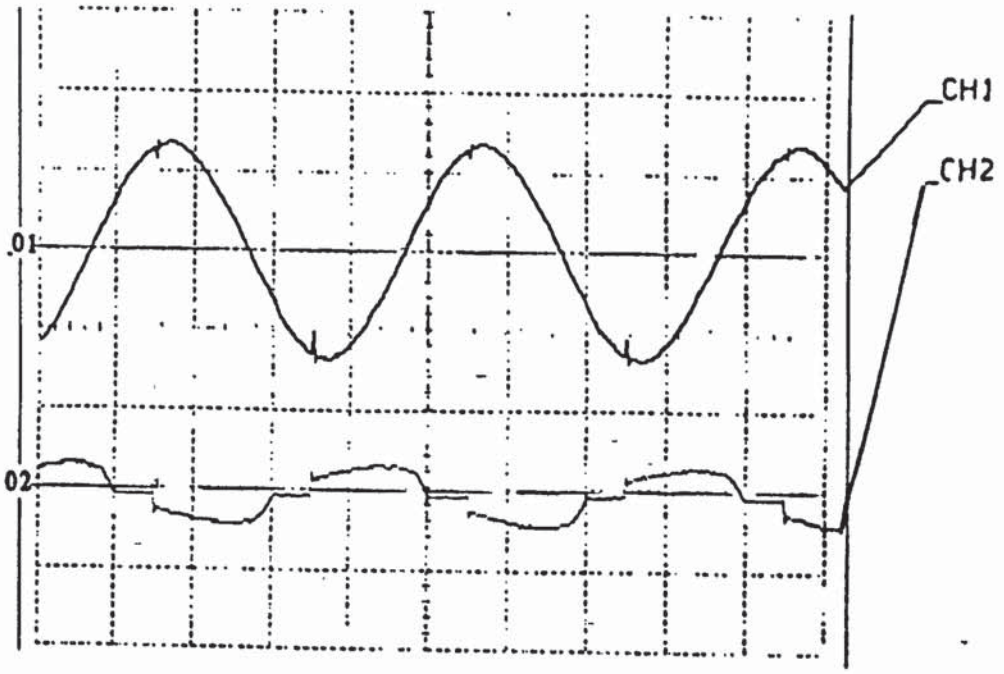


Figure (5-34) Supply voltage and current for a highly inductive load.
$\alpha = 54°$, $\beta = 0°$.
CH1: Supply voltage 100 V/div.
CH2: Supply current 15 A/div.
Time: 5 ms/div.

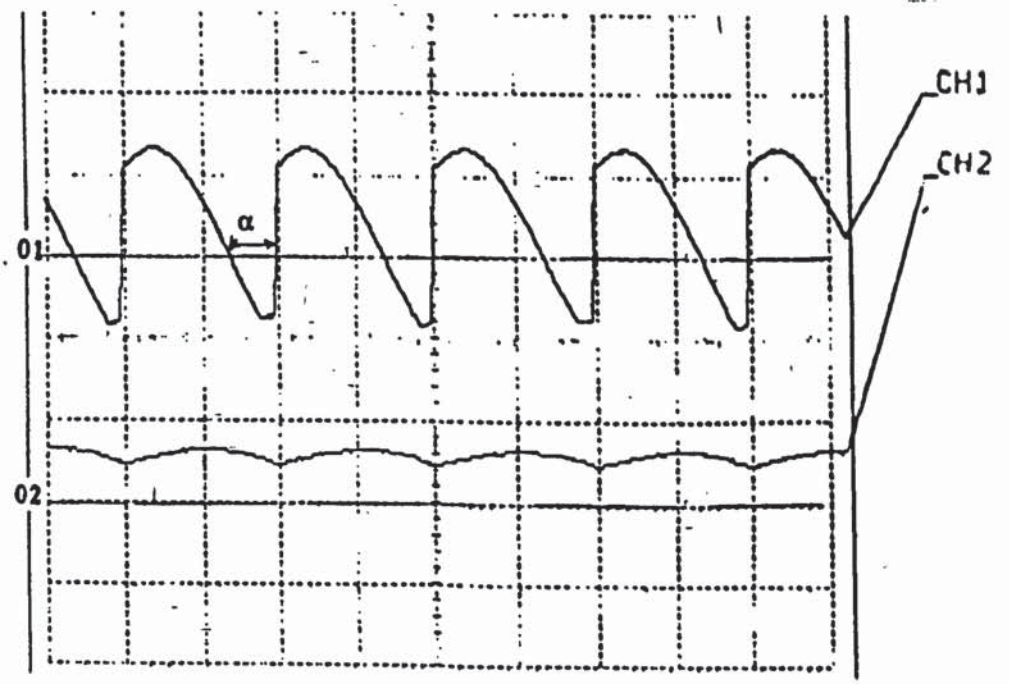


Figure (5-35) Load voltage and current for a highly inductive load.
$\alpha = 54°$, $\beta = 0°$.
CH1: Load voltage 100 V/div.
CH2: Load current 10 A/div.
Time: 5 ms/div.

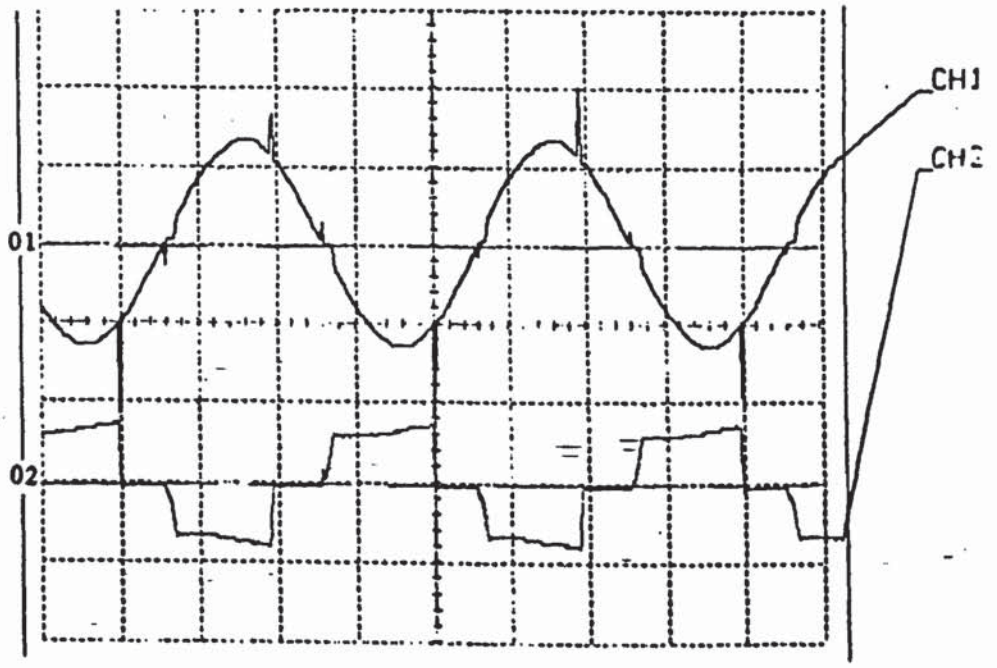


Figure (5-36) Supply voltage and current for a highly inductive load.
$\beta = 54°$, $\alpha = 0°$.
CH1: Supply voltage 100 V/div.
CH2: Supply current 10 A/div.
Time: 5 ms/div.

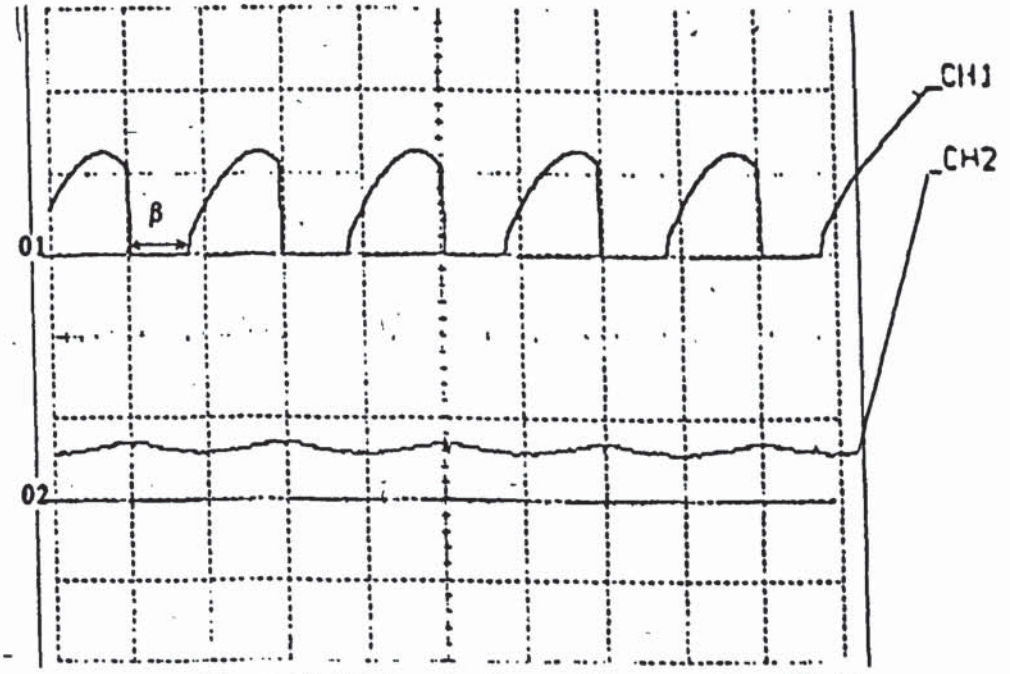


Figure (5-37) Load voltage and current for a highly inductive load.
$\beta = 45°$, $\alpha = 0°$.
CH1: Load voltage 100 V/div.
CH2: Load current 10 A/div.
Time: 5 ms/div.

CHAPTER SIX

CONCLUSIONS AND SUGGESTIONS FOR FURTHER WORK

6-1 CONCLUSIONS.

The thesis has described the operation of a two way AC-AC converter using GTO thyristors. A single phase system containing two GTO converters connected in series was built, analysed and tested. One converter operates as a rectifier while the other converter operates as an inverter; fast reversal of the power flow between the two converters was achieved and reported. Other configuration systems for reversal of the power flow as was described in Chapter 1, showed that with forced commutated converters, reversal of power flow with unity power factor could be achieved. Although the results of these configuration were encouraging, it seemed difficult to control the power factor in cases when leading or lagging power factor is needed.

This work shows that the system may be operated at leading or lagging power factor. It was pointed out in Chapter 1 that the main disadvantage of this work is the over all switching losses due to the type of GTO used in the system. This has a very low reverse blocking voltage capability and a diode was used in series with each device. The system can be operated with four-quadrant operation and can be used for a variable speed drive or to link two systems of different frequencies.

The characteristics of the GTO thyristor, the design of the snubber and the gate drive circuits were described in Chapter 2. The snubber and the gate drive circuits have considerable influence on the characteristics of the GTO thyristor. The snubber circuit layout should be arranged to have minimum inductance thus giving a low voltage spike during the fall time of the anode current. It is also shown that when the snubber capacitor is increased a considerable reduction in the overshoot voltage is achieved. The value of the snubber resistor must be chosen to discharge the capacitor

sufficiently rapidly when the GTO turns-on. It was also mentioned that the drive circuit must have a small layout inductance, in order to give a good rate of rise of reverse current when the GTO turns-off. It is believed that Chapter 2 will enhance the understanding and design of the snubber and drive circuits for the GTO thyristor.

A small scale AC-AC converter was described in Chapter 3. Two centre-tap converters with conventional thyristors are used to deliver or receive power. Chapter 3 also presents a full investigation and analysis of the thyristor turn-off time. In this small scale system, power flow in two directions was achieved but some problems occurred and these are discussed at the end of Chapter 3.

Chapter 4 presents the operation and design of the control circuit for the single phase system. A comparator was used to compare the input voltage levels of the two converters. Depending on the direction of the power flow and the output state of this comparator, the rectifier and inverter drive pulses will transfer from one group of devices to another. A rectifier control circuit was designed which has the advantage of controlling both ends of each half cycle of the load voltage and current. With this scheme a considerable improvement in the rectifier power factor can be achieved. For the inversion mode, the drive pulses were generated using a multivibrator and with a 50 Hz output. The input of each converter is connected to AC mains or to the load via a switching transistor, the transistor drive circuit is also described in Chapter 4.

The experimental results are presented in Chapter 5. Two problems occurred which caused some transistors and diodes to fail and gave some restrictions to operate the system at certain current and voltage levels. Firstly the switching transient of the transistor was too high so an RC snubber circuit was connected across the variac in order to reduce the transient caused by the leakage inductance of the variac. In addition, the snubber capacitor across the transistor was increased from 0.22 μF to 2μF and the voltage transient was reduced to 650 V. The second problem was the inrush current into the filter capacitor. To reduce this current to an acceptable value, a

ramp-up circuit was designed. The aim of the ramp-up circuit was to reduce the firing angle of the devices until the capacitor at the output of the rectifier is fully charged.

The system was tested with resistive and inductive loads. The input from the variac was set at 160 VRMS, the DC voltage link was 85 V in both cases. Many waveforms were represented for steady-state conditions and at the instant when the reversal of the power flow takes place. The results were very encouraging and the reversal of the power flow took place without a transient. At the end of chapter 5, theoretical and practical studies are represented for the rectifier power factor; The author compared the changing of the power factor by changing the firing angles α and β. It was shown that there will be a great improvement in the input power factor by changing the delay angle β. In this situation, the rectifier will be operated as a forced commutated converter instead of a line commutated one. Although the project achieved its aim further works could be done as explained below.

6-1 SUGGESTIONS FOR FURTHER WORK.

As previously stated, the project itself has been built to investigate different points. The following areas, which have emerged from the present work, could be subjects for further research.

1- The research could be extended to a three-phase system and this could be done either by a single phase or three-phase rectifier feeding a three-phase inverter.This would provide the opportunity to connect the output of the inverter to an induction motor. Thus the reversal of power flow would be achieved by regenerative braking.

2- PWM could be used in the control circuit to improve the input power factor and reduce the harmonics on the AC line current. However most of the hardware built by the author can still be used, such as the GTOs snubber circuits, drive circuits and heat sinks.

3- Symmetrical GTOs could be used to reduce the voltage drop in each converter arm. This could improve the efficiency of the system.

4- The author did not investigate the harmonics for the rectification or the inversion mode. This could be done practically using the same system or theoretically by simulation of the system using computer simulation techniques.

REFERENCES

1- VIRIYA, P. and MATSUSE, K.
"Low-harmonics GTO converter for fundamental Power Factor compensation"
IEEE Trans. Power Electron. Vol. 6, No. 3 July 1991, pp. 371-379.

2- LANDER, C. W.
"Power Electronics"
McGRAW-HILL Book Company (UK) Limited, 1987.

3- RASHID, B. W.
"Power Electronics, circuits, devices and applications"
Prentice-Hall, Inc., New Jersey 1988.

4- THORBORG, K.
"Power Electronics"
Prentice-Hall International (UK) Ltd., 1988.

5- WILLIAMS, B. W.
"Power Electronics, devices, drives and applications"
Macmillan Education Ltd., Hong Kong, 1987.

6- BIRD, B. M. and KING, K. G.
"An introduction to Power Electronics"
John Wiley and Sons Ltd., 1983.

7- BARADLY, D. A.
"Power Electronics"
Van Nostrand Reinhold (UK) Co. Ltd, 1987.

8- GWYTHER,H. F. G.
" Solving problems in Electrical Power and Power Electronics"
Longman Scientific & Technical, 1988.

9- DAVIS, R. M. and ALEXANDER, C. G.
"A bi-directional power flow converter for fixed polarity DC load"
Third Int.Conf. Power Electronics and Variable Speed Drives, 1988, pp. 142-145.

10- HALL, J. K. and MAK, O. C.
"AC-DC system power flow control by PWM converter"
Fourth Int.Conf. Power Electronics and Variable Speed Drives, NO. 324, 17-19 July 1990, pp. 312-315.

11- HALL, J. K. and SHAW, S. H.
"A bi-directional AC-DC converter"
23rd UPEC conference proceedings, 20 to 22 Sept. 1988.

12- WERNEKINCK, E., KAWAMURA, A. and HOFT, R.
"A high frequency AC/DC converter with unity power factor and minimum harmonic distortion"
IEEE Trans. on Power Electronics, vol. 6, No. 3, July 1991, pp.364-370.

13- GREEN, A. W., BOYS, J. T. and GATES, G. F.
"Three phase voltage source reversible rectifier"
IEE Proceedings Vol. 135, Non. 1988, pp. 362-270.

14- KATAOKA, T. MIZUMACHI, T. K. and MIYARI, S.
"A pulse width controlled AC to DC converter to improve power factor and waveform AC line current"
IEEE Trans. Ind. Appl., Vol. IA-15, Nov-Dec. 1979, pp. 670-675.

15- KOCHER, M. J. and STEIGERWALD, R. L.
"An AC to DC converter with high quality input waveform"
IEEE Tras. Ind. Appl., Vol. IA-19, July-Aug. 1983, pp. 586-599.

16- MOHAN, N., UNDELAND, T. M. and ROBBINS, W.P.
"Power Electronics Converters, Applications andDesign"
John Willey and Sons, 1989.

17- KAGOTANI, T., KUROKI, K., SHINOHARA, J. and MISAIZU, A.
"A novel UPS using high frequency switch mode rectifier and high frequency PWM inverter"
IEEE Power Electronics Specialist Conference Record, 1989, 1, pp. 53-57.

18- LIAW, C. M., CHEN, T. H., WANG, T. C., CHO, G. J., LEE, C. M. and WANG, C. T.
"Design and implementation of a single phase current forced switching mode bilateral converter"
IEE Proceedings-B, Vol. 138, No. 3, May 1991, pp. 129-136.

19 GREEN, A. W. and BOYS,J. T.
"Hysteresis current-forced three-phase voltage-sourced reversible rectifier"
IEE Proceedings-B, Vol. 136, No. 3, May 1989, pp. 113-120.

20- ITOH, R. and ISHIZAKA, K.
"Single phase sinusoidal converter using MOSFETs"
IEE Proceedings-B, Vol. 136, No. 5, 1989, pp. 237-242.

21- GREEN,A. W. and BOYS, J. T.
"Current-forced single phase reversible rectifier"
IEE Proceedings-B, Vol. 136, No. 5, Sep. 1989, pp. 205-211.

22- NONNON, P., ESCALLIER, D., POULIQUEN, J. L., SAADATE, S. and LE DOEUFF,R..
"A study of bidirectional active and reactive power exchange and of the harmonic distortion in GTO thyristors rectifier"
Fourth Int.Conf. Power Electronics and Variable Speed Drives, NO. 324, 17-19 July 1990, pp. 317-320.

23- WILSON, J. W. A.
"The forced commutated inverter as a regenerative rectifier"
IEEE Trans. Ind. Appl. Vol. IA-14, No. 4, July-Aug. 1978. pp. 335-340.

24- DORADLA, S. R., NAGAMINI, C. and SANYAL, S.
"A sinusoidal Pulse width Modulated three-phase AC to DC converter fed DC motor drive"
IEEE Trans. Ind. Appl. Vol. IA-21, No. 6, Nov.-Dec. 1985, pp. 1394-1408.

25- LIPO, T. A.
"Recent progress in the development of solid-state AC motor drives"

IEEE Trans.on Power Electronics. Vol. 3, No. 2, April 1988, pp.105-117.

26- GYUGI, L. and PELLY, B. R.
"Static power frequency changers"
New York: Wiley-Interscience, 1976.

27- VENTURINI, M and ALESINA, A.
"The generalized trans continuously adjustable input power factor"
IEEE PESC Conf. Rec., 1980, pp. 242-252.

28- VENTURINI, M.
"A new sine wave in.sine wave out conversion technique eliminates reactive components"
Proceeding Power Control 7, 1980, pp. E3-1 to E3-15.

29- VENTURINI, M. and ALESINA, A.
"Analysis and design of optimum-amplitude nine switch direct AC-AC converters"
IEEE Trans. on Power Electronics. Vol. 4, No. 1, Jan. 1989, pp. 101-112.

30- HOMBU, N., UEDA, S., and MATSUDA, Y.
"A new current source GTO inverter with sinusoidal output voltage and current"
Conf. Rec. IEEE IAS Annual Meeting, 1984, pp. 807-812.

31- OHNISHI, T. and OKISTSU, H.
"A novel PWM technique for three-phase inverter/converter"
Conf.Rec. IPEC-Tokyo 1983, pp. 384-395.

32- WIECHMANN, E. P., ZIOGAS, P. D. and STEFANOVIC, V. R.
"A novel bilateral power conversion scheme for variable frequency static power supplies"
IEEE Trans. Ind. Appl., Vol. 1A-21, NO., 5, Sep/Oct., 1985, pp.1226-1233.

33- BOSE, B. K.
"Power Electronics an emerging technology"
IEEE Trans. Ind. Elect.., Vol. 36, No. 3,August 1989, pp. 403-411.

34- OOI, B. T., DIXON, J. W., KULKAMI, A. B. and NISHIMOTO, M.
"An integrated AC drive system using a controlled current PWM rectifier/inverter link"
IEEE PESC. Vancouver, BC,Canada, pp. 494-501.

35- OOI, B. T., DIXON, J. W., KULKAMI, A. B. and NISHIMOTO, M.
"Characteristics of a controlled current PWM rectifier-inverter link"
IEEE IAS Annu. Meeting, Denver, CO, 1986, pp. 685-691.

36- STIHI, O. and OOI, B. T.
"A single phase controlled current PWM rectifier"
IEEE Trans. Power Electro., Vol. 3, NO. 4, Oct. 1988, pp. 453-459.

37- HABETLER, T. G.
"Angle controlled current regulated rectifier for AC/DC converters"
IEEE Trans.on Power Electronics. Vol. 6, NO. 3, July 1991, pp.463-469.

38- KLAASSENS, J. B. and SMITS, E.J. F. M.
"Series resonant AC power interface with an optimal power factor and enhanced conversion ratio"
IEEE Trans. Power Electron., PE-3, NO. 3, July 1988, pp. 335-343.

39- KLAASSENS, J. B. and DE BEER, F. G.
"Three-phase AC to AC series resonant power converter with a reduced number of thyristors"
IEEE Trans. Power Electron., Vol. 6, NO. 3, July 1991, pp. 346-355.

40- KLAASSENS, J. B.
"DC TO AC series resonant converter system with high internal frequency generating multiterminal AC waveforms for multikilowatt power levels"
IEEE Trans. Power Electron., Vol. PE-2, NO. 3, July 1987 pp. 247-256.

41- SOOD, P. K and LIPO, T. A.
"Power conversion distribution system using a resonant high-frequency AC link"
Conf. Rec. IAS Annual Meeting 1986, PP. 533-541.

42- HUISMAN, H.
"A three-terminal to three terminal series resonant power converter with optimal input current waveforms, Part 1: Control Strategy, Part 2: Application and results"
IEEE Trans. Inds. Electron., IE-35, NO. 2, May 1988, pp. 263-277.

43- SAKURADA, S. and IKEDA, Y.
" Recent trends of the Gate Turn-Off Thyristor"
Hitachi Review, 1981,Vol. 30, No. 4, pp. 197-200.

44- SAGIN, M.
" A survey of devices, technologies and applications"
Wireless World, April 1977, PP. 86-92.

45- GRANT, D. and HONDA, A.
"Applying International Rectifier's Gate Turn-Off Thyristors"
International Rectifier Application Notes, AN-315A.

46- OHKA, K, P.
"Technology"
Electronic Design 26, December 1976, pp. 60-63.

47- SHEPHERD, W and HULLY, L. N.
"Power Electronics and Motor Control"
Cambridge University Press, 1987.

48- NAGANO, T et al.
"High power low forward drop Gate Turn-Off Thyristor"
IEEE Conference Record 78, Industrial Application Society, pp.1003-1006.

49- IKEDA, Y et al.
"Gate Turn-Off Thyristor and Drive Circuits"
Hitachi Review 29, June 1980, pp. 127-130.

50- BISWAS, S. K., BASAK, B. and VITHAYATHIL, J.
" An auto-protecting Gate drive circuit for GTO Thyristors"
IEEE Trans. Ind. Appl. Vol. 24, No. 1,1988 PP. 464-469.

51- STEIGERWARD, R. L.
"Application techniques for high power Turn-Off Thyristors"
IEEE Ind. Appl. Soc. (IAS) Conf. Record, 1975, pp. 165-174.

52- BURGUM, F. J. and HOULDSWORTH, J. A.
"Drive circuits for Gate Turn-Off Switches"
Proceeding of the PCI Conf. 1981, pp. 168-174.

53- EDWARD, Y. Y. H. and SEN, P. C.
"Effect of Gate Drive Circuit on GTO Thyristor Characteristics"
IEEE Tran. Ind. Elect. Vol. IE-33, NO. 3, August 1986
pp. 325-331.

54- KAO, Y. C. and BREWSTER, J. B.
"Recent development in gate controlled switches"
IEEE Power. Electronics. Specialists Conf. (PESC) Proceedings,1973, pp. 90-96.

55- "Hitachi GTO Thyristor Operation Manual"
No. SD-E701, Hitachi Ltd. March 1980.

56- TAYLOR, P. D.
"A comparison of GTO Thyristor devices designs"
IEE Conference Record Power Electronics and Variable Speed Drives, May 1984.

57- MARCONI ELECTRONIC DEVICES.
" Gate Turn-Off Thyristor Data"

58- OKAMURA, M., WAGANO, T. and OGAWA, T.
"The current status of the power Gate Turn-Off Switch (GTO)"
IEEE/IAS Int. Semiconductor Power Converter Conf. Rec., 1977, pp.-89-49.

59- OHASHI, H.
"Snubber Circuit for High-Power Gate Turn-Off Thyristors"
IEEE Transaction on Industry Applications. Vol. IA-19, NO.4 August 1983, pp. 655-664.

60- McMURRAY, W.
"Optimum Snubbers for Power Semiconductors"
IEEE Transaction on Industry Applications. Vol. IA-8, NO.5 September 1972, pp. 595-600.

61- UNDELAND, T., JENSET, F.,STEINBAKK, A., ROGNE, T. and HERNES, M.
"A Snubber Configuration for both Power Transistor and GTO PWM Inverters"
15th Annual IEEE PESC,1984 PP. 42-53.

62- GIBSON, H and BALLAD, J.P.
"Circuit and component constraints on high current GTO Turn-OFF"
IEE Colloquium Digest, NO. 56, 1985, PP. 1-6.

63- KAO, Y. C and BREWSTER, J. B.
"Recent Development in Gate controlled Switches"
Power Electronics Specialists Conference Record, 1973, pp. 90-96.

64- BASSETT, R. and CHAMUND, D.
"Reducing Switching Stress on GTOs by using optimum FRDs"

PCIM Europe, January 1990, pp. 33-38.

65- MADDOCK, B. J. and CALCUTT, D. M.
"Electronics, a course for Engineers"
Longman Group UK Limited, 1988.

66- FARNELL ELECTRONICS COMPONENTS LIMITED.
"National Semiconductor Corporation Data Sheet"
PP. 3-285-3-295.

67- BEDFORD, B. D. and HOFT, R. G.
"Principle of Inverter Circuit"
New York: John Wiley & Sons, Inc., 1964

68- MULLARD TECHNICAL HANDBOOK.
"Book 4, Integrated Circuit"
Mullard Limited, 1986.

69- THOMSON-CSF
"The power transistors in its Environment", 1979.

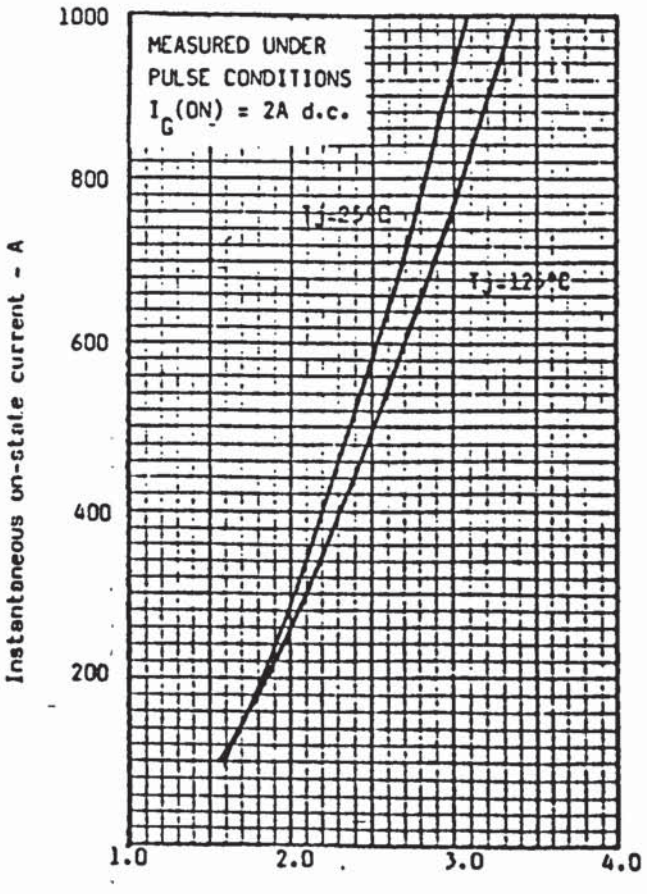
70- GENERAL ELECTRIC COMPANY.
"Silicon controlled rectifier manual"
General electric company, copyright, 1967.

APPENDIX A.

GTO DATA SHEET.

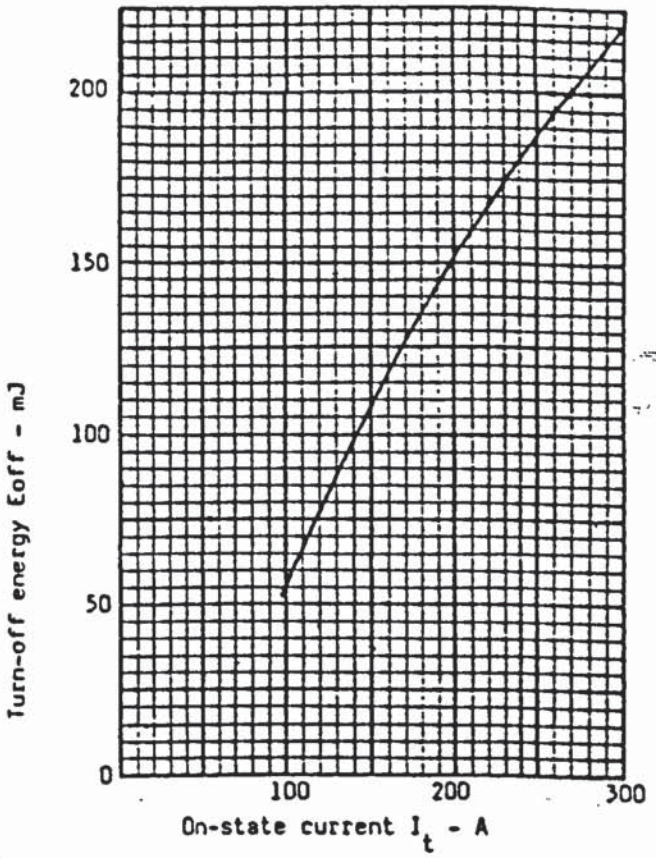
Type Number		GT224K10
V_{DRM}	Repetitive peak off-state voltage	1200 V
V_{RRM}	Repetitive peak reverse voltage	16 V
Current rating:		
I_{TCM}	Repetitive peak controllable on-state current	300 A
$I_{T(AV)}$	Mean on-state current (T_{HS} = 80 °C)	100 A
$I_{T(RMS)}$	RMS on-state current (T_{HS} = 80 °C)	150 A
$R_{th\ (j\text{-}h)}$	DC thermal resistance junction to heat sink surface, anode side (Mounting Torque 30 Nm)	0.2 °C/W
Surge rating:		
I_{TSM}	Surge (non-repetitive) on-state current (10ms half sine, T_j = 125 °C)	1800 A
I^2t	I^2t for fusing (10ms half sine, T_j = 125 °C)	1200 A^2s
dI/dt	Critical rate of rise of on-state current (From 600 V to 300 A, T_j = 125 °C I_{FG} > 10 A, rise time < 1 µs)	500 A/µs
dV/dt	Rate of rise of off-state voltage (R_{GK} < 18 Ω, 50% V_{DRM}, T_j = 125 °C)	500V/µs
V_{RGM}	Peak reverse gate voltage	16 V
Temperature rating:		
T_{vj}	Virtual junction temperature	125 °C
Characteristics, T_{case} 125 °C unless otherwise stated		Limit Maximum
V_{TM}	On-state voltage (at 300 A peak, IG(on) = 2 A)	2.1V
I_{DM}	Peak off-state current (R_{GK} < 18 Ω)	25 mA
t_{gt}	Turn-off time (I_{FG} = 10 A, rise time < 1 µs from 750 V to 300 A, Resistive load)	5 µs
t_{gs}	Storage time	10 µs
t_{gf}	Fall time	1.3 µs
t_{gq}	Gate controlled turn-off time (For t_{gs}, t_{gf}, and t_{gq}; Snubber: R_S = 15 Ω C_S = 1µf and dig/dt = - 15 A/µs, Resistive load)	11 µs

V_{GT}	Gate trigger voltage (V_D = 24 V, I_T = 5A)	
	T_{case} = 125 °C	0.75 V
	T_{case} = 25 °C	0.9 V
	T_{case} = -40 °C	1 V
I_{GT}	Gate trigger current (V_D = 24 V, I_T = 5A)	
	T_{case} = 125 °C	0.6 A
	T_{case} = 25 °C	1 A
	T_{case} = -40 °C	1.6 A
I_{RGM}	Reverse gate cathode (V_{RGM} = 16 V, No gate/cathode resistor)	25 mA



MAXIMUM (LIMIT) ON-STATE CHARACTERISTICS

DEPENDENCE OF ON-STATE CURRENT WITH TURN OFF ENERGY



Conditions

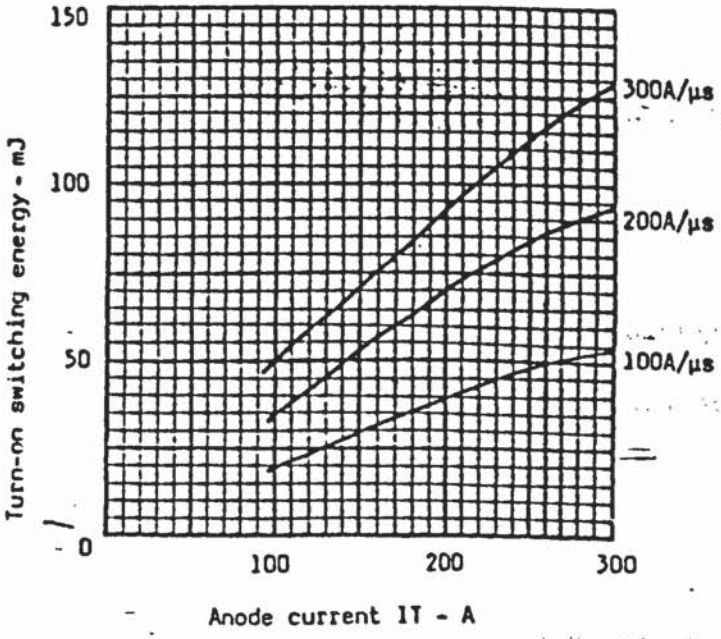
V_D = 1000V

dIg/dt = 15A/µs

Cs = 1µF

Rs = 15Ω

Tj = 125°C



Conditions

V_D = 700V

I_{GM} = 10A

dI_g/dt = 10A/µs

Tj = 125°C

Cs = 1µF

Rs = 15Ω

DEPENDENCE OF ON STATE CURRENT WITH TURN ON ENERGY

APPENDIX B

INVERTER OPERATION WITH A PURELY INDUCTIVE LOAD

The principle of a single phase half bridge inverter with a purely inductive load can be explained by referring to figure (B-1). When GTO_1 is turned-on for a time T/2, the instantaneous voltage across the load is $V_{DC}/2$. When GTO_1 is turned-off and GTO_2 is turned-on at t = T/2, the load voltage reverses but the load current cannot change with the output voltage. The current continues to flow through diode D_2, load and the lower half of the DC source until it falls to zero. At this point, the load current transfers to GTO_2. Similarly, when GTO_2 is turned-off at t = T, the load current flows through D_1, the load and the upper half of the DC source and when it reaches zero, it transfers to GTO_1. It is noted that for a purely inductive load, the conduction time of the GTO equals that of the diode and this equals T/4. There must be a delay time between the extinction of the outgoing GTO and the firing of the next incoming GTO, otherwise a short circuit would result through the two GTOs. A full design and operation of a delay circuit which can be used in an inverter system is given in appendix (C).

At steady-state conditions, when GTO_1 is conducting, the load voltage is:

$$v_L = L\frac{di_L}{dt} \qquad \text{(B-1)}$$

GTO_1 conducts for T/4 and at the end of this time, the load current reaches its maximum value. The rate of rise of the load current can be calculated as:

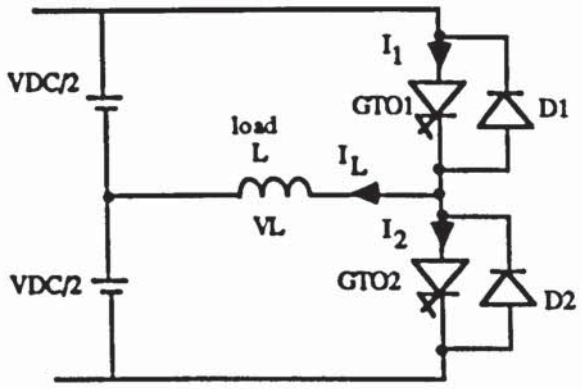
$$\frac{di_L}{dt} = \frac{I_{Lmax.}}{T/4} \qquad \text{(B-2)}$$

The maximum load voltage is VDC/2, by using this value and solving equation (B-2) into (B-1) this gives:

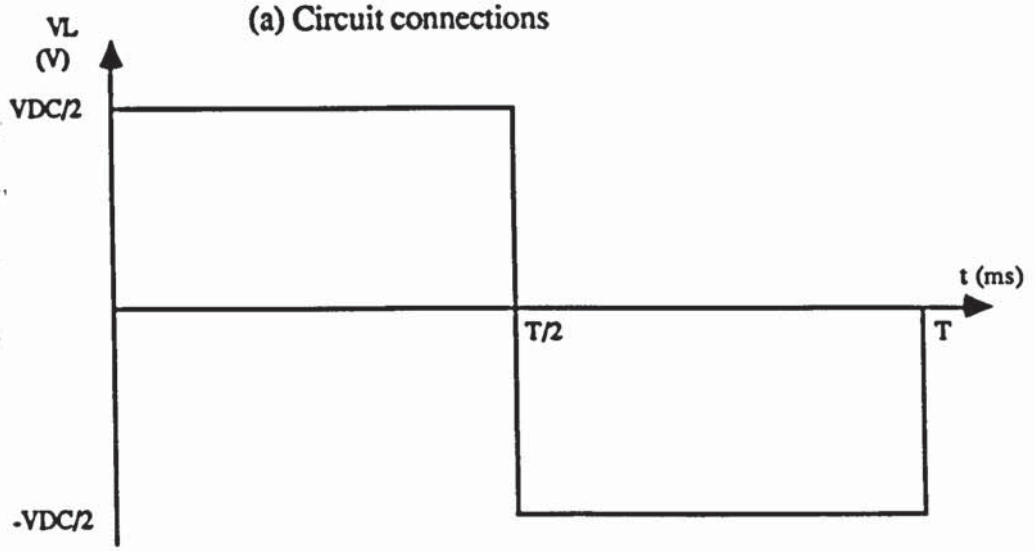
$$\frac{V_{DC}}{2} = L\frac{I_{Lmax.}}{T/4} \qquad \text{(B-3)}$$

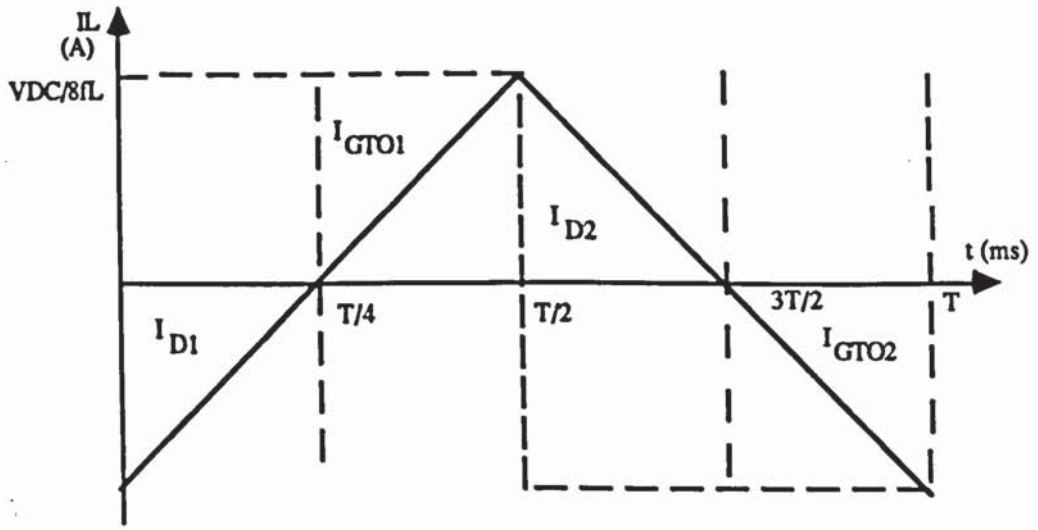
By putting f = 1/T, where f is the switching frequency, the maximum load current is:

$$I_{Lmax.} = \frac{V_{DC}}{8fL} \qquad \text{(B-4)}$$



(a) Circuit connections





(b) Load voltage and current with an inductive load.

Figure (B-1) Single phase half bridge inverter.

APPENDIX C

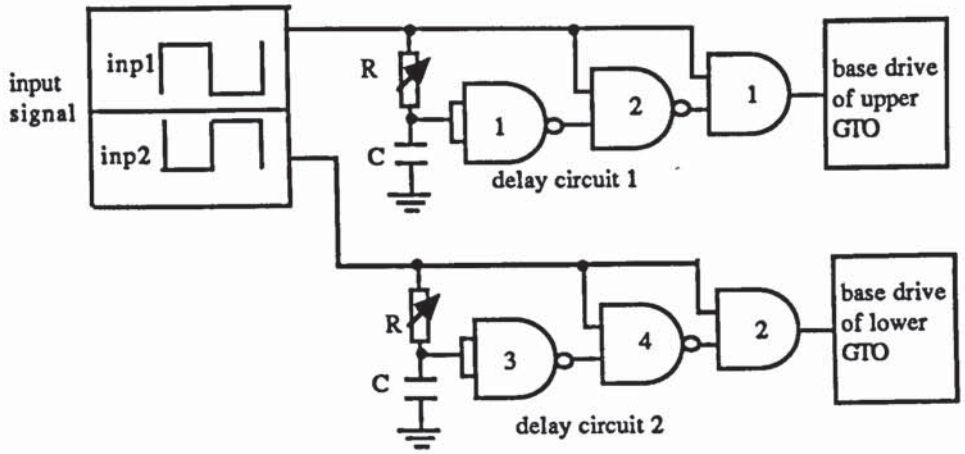
DELAY CIRCUIT FOR AN INVERTER DEVICES

It is well known that a GTO device takes a significant length of time to turn-off after the initiation of turn-off procedure. In any inverter system, an optimum delay time must be introduced to the devices drive circuits. Otherwise, both devices in one branch turn-on while the inverter is connected to the DC supply and this could cause a serious damaging fault within the inverter circuit.

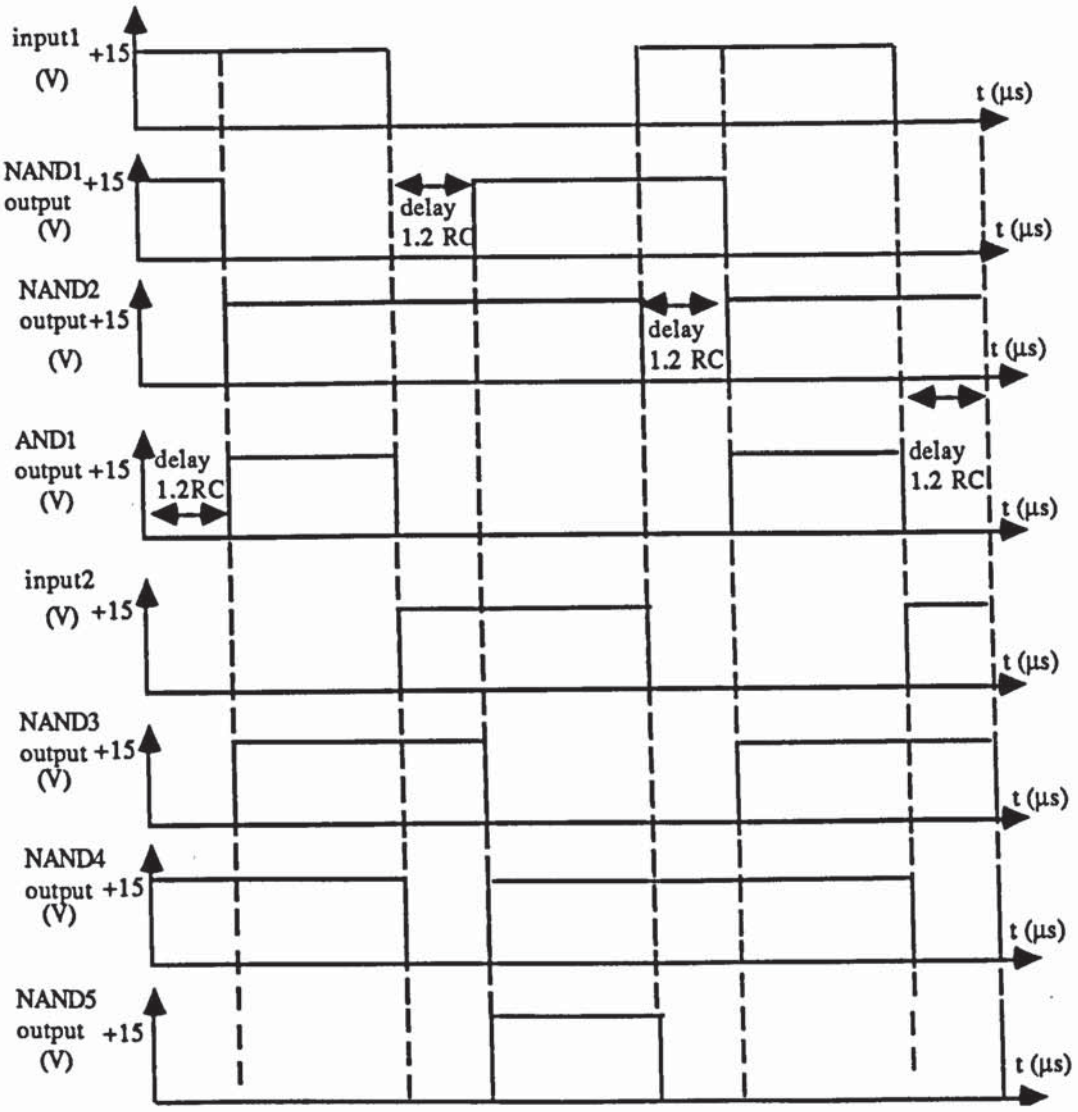
A circuit was designed to delay the turn-on pulse of the GTO until its complementary device is extinguished. The circuit connections and waveforms are shown in figure (C-1).

First the input signal (inp_1) feeds an RC circuit, the capacitor voltage is inverted by using $NAND_1$. The output of the $NAND_1$ gives a delay to the original signal. The width of this delay equals 1.2 RC and this can be controlled by means of the variable resistor (R). The output of $NAND_1$ and the original input pulse feed the inputs of $NAND_2$. At the positive going edge of the original signal $NAND_2$ gives a low state output for 1.2 RC time width. After this delay, the output of $NAND_2$ goes to high state until the beginning of next cycle. The output of $NAND_2$ and the original input signal (inp_1) feed the inputs of AND_1, hence the high part of the original input signal is cat from its positive going edge to a preset delay value (delay = 1.2RC). The output signal of AND_1 supplies the gate drive circuit of the upper GTO of the inverter branch. When this signal is high the GTO turns-on and when this signal is low the GTO turns-off.

When the complementary input signal (inp_2) feeds the second delay circuit, the same procedure as outlined above occur. AND_2 supplies the gate drive circuit of the lower GTO after the upper one turned-off. Referring to the waveforms of figure (C-1) there is a delay time between the outgoing signal and the next incoming signal.



(a) Circuit connections.



(b) Circuit waveforms.

Figure (C-1) Delay circuit for an inverter devices.

APPENDIX D

INVERTER CIRCUIT WITH RL LOAD.

Figure (D-1) shows a bridge inverter for producing an AC voltage and employing GTOs. For a positive half cycle, the load current grows exponentially through GTO_1 and GTO_2 according to:

$$V_L = V_S = L\frac{di_L}{dt} + i_L R \qquad \text{(D-1)}$$

where:

V_S is the DC voltage supply to the inverter .

V_L is the load voltage.

I_L is the load current.

R and L are the load resistor and inductor.

When GTO_1 and GTO_2 are turned-off, GTO_3 and GTO_4 are turned on, thereby reversing the load voltage. Because of the inductive nature of the load, the load current cannot reverse and the load reactive energy flows back into the supply via D_3 and D_4. The load voltage is:

$$V_L = -V_S = L\frac{di_L}{dt} + i_L R \qquad \text{(D-2)}$$

The load current falls exponentially and at zero, GTO_3 and GTO_4 become forward-biased and conduct load current, thereby feeding power to the load. The output voltage is a square wave and has an RMS value of Vs. During the first half-cycle, with no initial load current, by solving equation (D-1) using Laplace Transform:

$$RI_L + sLI_L = \frac{V_S}{s} \qquad \text{(D-3)}$$

or:

$$I_L = \frac{V_S}{L}\left(\frac{1}{s\left(s + \frac{R}{L}\right)}\right) \qquad \text{(D-4)}$$

The inverse Laplace Transform of equation (D-4) is:

$$i_L = \frac{V_S}{R}\left(1-\exp\left\langle -Rt/L \right\rangle\right) \qquad \text{(D-4)}$$

Under steady-state conditions, the initial current is (I_0) as shown in figure (D-1), and equation (D-1) gives:

$$RI_L + sLI_L = \frac{V_S}{s} + LI_0 \qquad \text{(D-6)}$$

$$I_L = \frac{V_S}{L}\left(\frac{1}{s\left(s+\frac{R}{L}\right)}\right) + I_0\left(\frac{1}{\left(s+\frac{R}{L}\right)}\right) \qquad \text{(D-7)}$$

The inverse Laplace Transform of equation (D-7) is:

$$i_L = \frac{V_S}{R} - \left\langle \frac{V_S}{R} - I_0 \right\rangle \exp\left\langle -Rt/L \right\rangle \qquad \text{(D-8)}$$

Where:

$0 \le t \le t_1$.

$V_L = V_s$.

$I_0 \le 0$.

During the second half cycle ($t_1 \le t \le t_2$) when the supply is effectively reversed across the load and the initial condition I_1, equation (D-2) yields.

$$RI_L + sLI_L = \frac{-V_S}{s} + LI_1 \qquad \text{(D-9)}$$

$$I_L = \frac{-V_S}{L}\left(\frac{1}{s\left(s+\frac{R}{L}\right)}\right) + \frac{I_1}{\left(s+\frac{R}{L}\right)} \qquad \text{(D-10)}$$

giving:

$$i_L = \frac{-V_S}{R} + \left\langle \frac{V_S}{R} + I_1 \right\rangle \exp\left\langle -Rt/L \right\rangle \qquad \text{(D-11)}$$

Where:

$0 \le t \le t_2 - t_1$.

$V_L = -V_S$.

$I_1 \geq 0$.

Since $I_1 = -I_0$, the initial steady-state current I_1 can be found from equation (D-8) when, at $t = t_1$, $i_L = I_1$ yielding:

$$I_1 = \frac{V_S}{R} \frac{\left(1 - \exp\left\langle -Rt_1 / L \right\rangle\right)}{\left(1 + \exp\left\langle -Rt_1 / L \right\rangle\right)} \tag{D-12}$$

The zero current cross-over point t_x, shown on figure (D-1) can be found by solving equation (D-8) for t when $i_L = 0$ which yields:

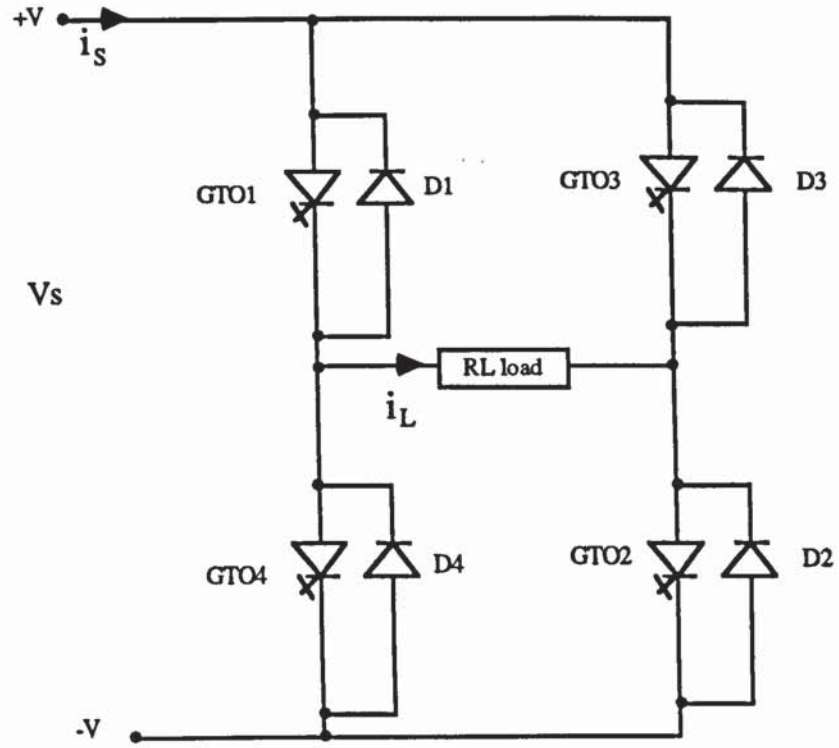
$$0 = \frac{V_S}{R} - \left\langle \frac{V_S}{R} - I_0 \right\rangle \exp\left\langle -Rt_x / L \right\rangle \tag{D-13}$$

$$\frac{V_S}{R} = \left(\frac{V_S}{R} - I_0\right) EXP\left(\frac{-Rt_x}{L}\right) \tag{D-14}$$

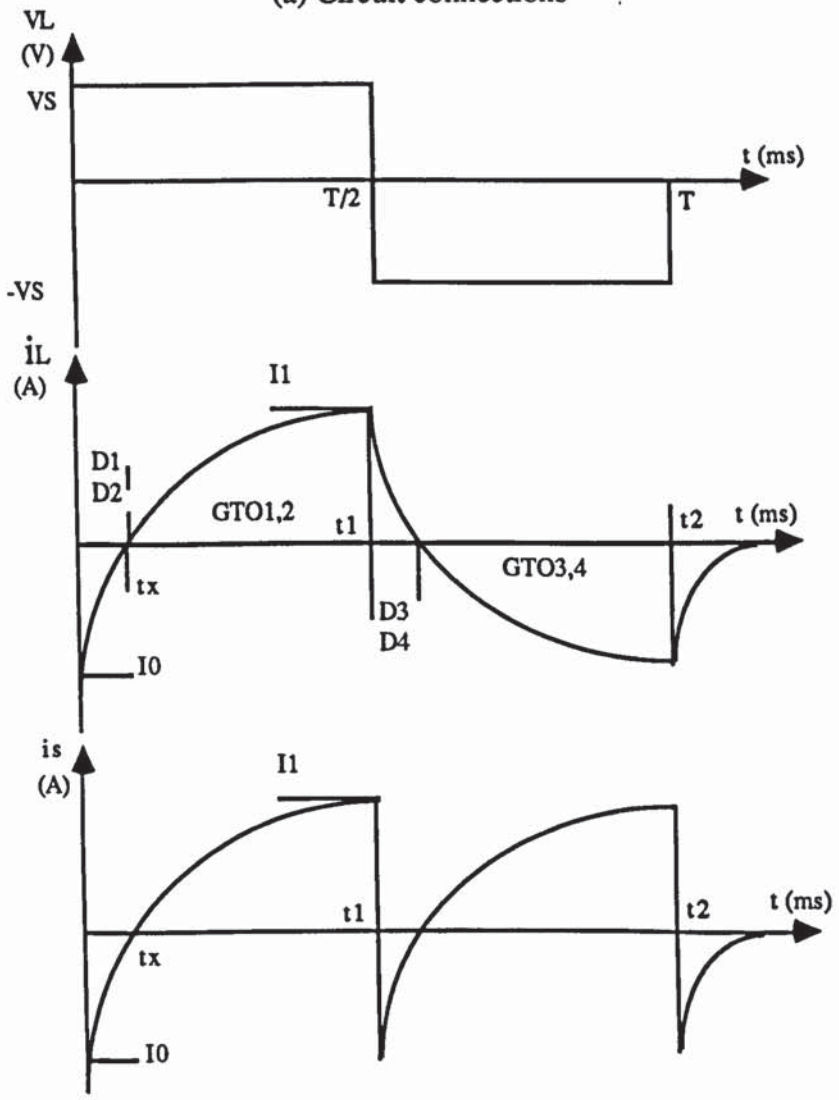
$$\ln\left(\frac{V_S}{R}\right) = \ln\left(\frac{V_S}{R} - I_0\right) - \left(\frac{Rt_x}{L}\right) \text{ or } \frac{Rt_x}{L} = \ln\left(\frac{\left(\frac{V_S}{R} - I_0\right)}{\left(\frac{V_S}{R}\right)}\right) \tag{D-15}$$

Therefore:

$$t_x = \frac{L}{R} \ln\left\langle 1 - I_0 R / V_S \right\rangle \tag{D-16}$$



(a) Circuit connections



(b) Current and voltage waveforms.

Figure (D-1) Inverter circuit with RL load.

APPENDIX E

THYRISTOR TURN OFF TIME OPERATING IN CENTRE TAP INVERTER.

To calculate the turn-off time of the thyristors operating in a centre tap inverter as shown in figure (E-1) it is assumed that TH_1 has been on and that it is to be turned off by triggering TH_2. Figure (E-2) shows the equivalent circuit when thyristor TH_2 is on. The current i_2 flowing in the thyristor TH_2 is chosen as the independent variable. The initial condition at time t = +0 are:

Current in inductor L : $i_2 (+0) = I_L$

Voltage across capacitor C : $e_{C1} (+0) = E_d$

Note that the commutation capacitor has a value 4C which is due to the 2:1 turns ratio of the centre tap inverter.

From the equivalent circuit in figure (E-2), the loop voltage equations are:

$$E_d = L\frac{di_2}{dt} - e_{C1}(+0) + \int_0^t \frac{i_2 + I_L}{C_1} \qquad \text{(E-1)}$$

The Laplace transform of equation (E-1) with the initial conditions is:

$$\frac{2E_d}{s} = Lsi_2(s) - LI_L + \frac{i_2(s)}{sC_1} + \frac{I_L}{s^2C_1} \qquad \text{(E-2)}$$

Solving equation (E-2) for $i_2(s)$:

$$i_2(s) = \frac{\frac{2E_d}{L} + sI_L - \frac{I_L}{sLC_1}}{s^2 + \frac{1}{LC_1}} \qquad \text{(E-3)}$$

The inverse transformer of equation (E-3) gives:

$$i_2 = \frac{2E_d}{wL}\sin\omega t + I_L(2\cos\omega t - 1) \qquad \text{(E-4)}$$

Where:

$$\omega = \frac{1}{\sqrt{LC_1}} \tag{E-5}$$

The commutation interval ends when the inductor voltage is zero.

$$L\frac{di_2}{dt} = 0 \tag{E-6}$$

$$\frac{di_2}{dt} = \frac{2E_d}{\omega L}\omega \cos\omega t - 2w\, I_L \sin\omega t \tag{E-7}$$

Equation (E-6) occurs after a time tc where:

$$\tan\omega t_C = \frac{E_d}{\omega L I_L} \tag{E-8}$$

Therefore:

$$t_c = \sqrt{LC_1}\tan^{-1}x \tag{E-9}$$

Where:

$$x = \frac{E_d}{I_L}\sqrt{\frac{C_1}{L}} \tag{E-10}$$

This may be expressed as the ratio of the instantaneous load impedance at commutation, E_d/I_L, to the characteristics impedance of the commutation circuit Z_0.

Where:

$$Z_0 = \sqrt{\frac{L}{C1}}$$

The actual turn-off time is the time during which TH1 remains reversed biased. The reverse bias becomes zero when the capacitor voltage is zero and:

$$L\frac{di_2}{dt} = E_d \tag{E-11}$$

From equation (4):

$$L\frac{di_2}{dt} = 2E_d\omega \cos\omega t_0 - 2\omega\, LI_L \sin\omega t_0 = E_d \tag{E-12}$$

Hence

$$E_d\omega \cos\omega t_0 - \omega L I_L \sin\omega t_0 = \frac{E_d}{2} \qquad \text{(E-13)}$$

Let:

$$E_d\omega = R \sin\psi \qquad \text{(E–14)}$$

$$\omega L I_L = R \cos\psi \qquad \text{(E–15)}$$

Therefore:

$$R = \sqrt{E_d^2 + (\omega L I_L)^2} \qquad \text{(E-16)}$$

From equation (13):

$$\sqrt{E_d^2 + (\omega L I_L)^2}\, \sin(\psi - \omega t_0) = \frac{E_d}{2} \qquad \text{(E-17)}$$

$$\sin(\psi - \omega t_0) = \frac{E_d}{2\sqrt{E_d^2 + (\omega L I_L)^2}} \qquad \text{(E-18)}$$

$$\psi - \omega t_0 = \sin^{-1} \frac{E_d}{2\sqrt{E_d^2 + (\omega L I_L)^2}} \qquad \text{(E-19)}$$

$$\omega t_0 = \psi - \sin^{-1}\left[\frac{E_d}{2\sqrt{E_d^2 + (\omega L I_L)^2}}\right] \qquad \text{(E-20)}$$

From equations (E-14) and (E-16):

$$\psi = \sin^{-1}\frac{E_d}{R} = \sin^{-1}\left[\frac{E_d}{\sqrt{E_d^2 + (\omega L I_L)^2}}\right] \qquad \text{(E-21)}$$

Substituting equation E-(21) into (E-20):

$$\omega t_0 = \sin^{-1}\left[\frac{E_d}{\sqrt{E_d^2 + (\omega L I_L)^2}}\right] - \sin^{-1}\left[\frac{E_d}{2\sqrt{E_d^2 + (\omega L I_L)^2}}\right] \qquad \text{(E-22)}$$

But:

$$\omega = \frac{1}{\sqrt{LC_1}} \quad \text{which gives} \quad \omega L = \sqrt{\frac{L}{C_1}} \qquad \text{(E-23)}$$

$$x = \frac{E_d}{I_L}\sqrt{\frac{C_1}{L}} \quad \text{which gives} \quad (wLI_L)^2 = \frac{E_d^2}{x^2} \qquad \text{(E-24)}$$

Substituting equations (23) and (24) into (22):

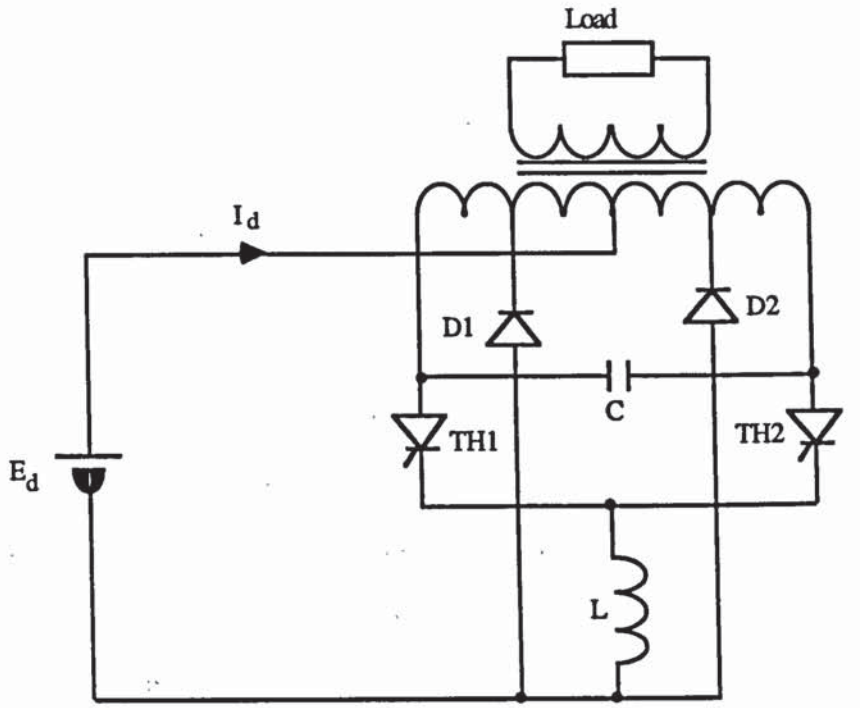
$$g(x) = \frac{t_0}{\sqrt{LC_1}} = \sin^{-1}\left[\frac{x}{\sqrt{x^2+1}}\right] - \sin^{-1}\left[\frac{x}{2\sqrt{x^2+1}}\right] \qquad \text{(E-25)}$$

As previously mentioned $C_1 = 4C$, the turn-off time of the thyristor operating in a centre tap inverter is:

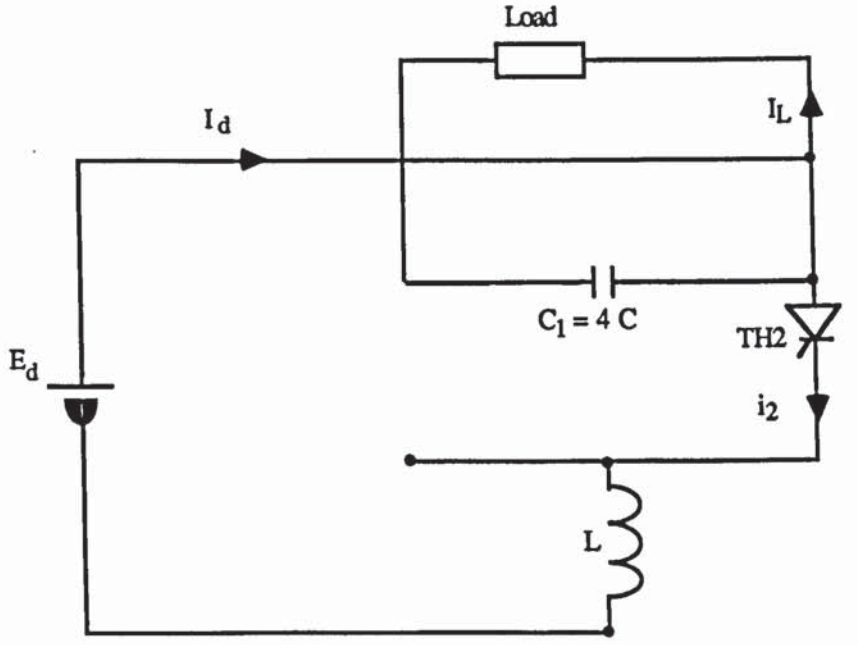
$$t_0 = g(x)\sqrt{4LC} \qquad \text{(E-26)}$$

$$g(x) = \sin^{-1}\left[\frac{x}{\sqrt{x^2+1}}\right] - \sin^{-1}\left[\frac{x}{2\sqrt{x^2+1}}\right] \qquad \text{(E-27)}$$

$$x = \frac{E_d}{I_L}\sqrt{\frac{4C}{L}} \qquad \text{(E-28)}$$



(a) Circuit connections.



(b) Equivalent circuit when TH1 turns-off and TH2 turns-on.

Figure (E-1) Centre tap inverter.

APPENDIX F

HEAT SINK REQUIREMENT FOR GTO.

Semiconductor power losses are dissipated in the form of heat which must be transferred away from the switching junction. With a power device, the physical size is too small to permit sufficient heat flow to the surrounding medium. Enhancement is necessary and special provision for easy heat flow to the heat sink is incorporated in the design of the encapsulation. The main purpose of the heat sink is to enhance the steady heat flow path from the encapsulation of the device to the ambient medium (55). An equivalent circuit may be used to model the heat flow and calculate the size of heat sink required. The full thermal radiation model, or thermal equivalent circuit for a mounted semiconductor is shown in figure (F-1). The average power dissipation P_d and maximum junction temperature T_{jmax}, along with the ambient temperature T_a, determine the design of the heat sink according to:

$$P_d = \frac{T_{jmax} - T_a}{R_{\theta j\text{-}a}} \qquad \text{(F-1)}$$

where:

$R_{\theta j\text{-}a}$ is the total thermal resistance from the junction to the ambient air. From figure (F-1), $R_{\theta j\text{-}a}$ is:

$$R_{\theta j\text{-}a} = R_{\theta j\text{-}c} + \frac{R_{\theta c\text{-}a}\left(R_{\theta c\text{-}s} + R_{\theta s\text{-}a}\right)}{\left(R_{\theta c\text{-}a} + R_{\theta c\text{-}s} + R_{\theta s\text{-}a}\right)} \left(^{\circ}C/W\right) \qquad \text{(F-2)}$$

Generally, when employing a heat sink $R_{\theta c\text{-}a}$ is large compared with the other model components and equation (F-2) may be simplified to:

$$R_{\theta j\text{-}a} = R_{\theta j\text{-}c} + R_{\theta c\text{-}s} + R_{\theta s\text{-}a} \left(^{\circ}C/W\right) \qquad \text{(F-3)}$$

where:

$R_{\theta j\text{-}c}$ is the junction to case thermal resistance.

$R_{\theta c\text{-}s}$ is the case to heat sink thermal resistance.

$R_{\theta s\text{-}a}$ is the heat sink to the ambient thermal resistance.

The total power dissipation P_d is the sum of the switching transition loss P_s, the on-state conduction loss P_c, and the off-state leakage loss P_l.

a) Switching transition power loss:

Figure (F-2) shows typical power device voltage-current switching waveforms. Normally an exact solution is not required and an approximation based on straight-line switching is usually adequate (5). Switching losses occur at both turn-on and turn-off.

For a resistive load, P_s is:

$$P_s = \frac{V_s I_m f_s \tau}{6} \text{ (W)} \qquad \text{(F-4)}$$

For an inductive load, P_s is:

$$P_s = \frac{V_s I_m f_s \tau}{2} \text{ (W)} \qquad \text{(F-5)}$$

where:

τ is the period of the switching interval.

V_s and I_m are the maximum voltage and current levels as shown in figure (F-2).

b) Conduction power loss.

The average conduction loss under steady-state current conditions is given by:

$$P_c = V_{on} I_{on} \delta \quad \text{(W)} \qquad \text{(F-6)}$$

Where δ is the duty cycle, I_{on} is the device current and V_{on} is the voltage drop across the device.

c) Off-state leakage power loss.

During the switch-off period, a small exponentially temperature dependent current I_l, will flow through the switch. The loss due to this leakage current is:

$$P_l = I_l V_s (1 - \delta) \text{ (W)} \qquad \text{(F-7)}$$

Normally P_l is only a small part of the total loss and it can be neglected.

In the calculation of the GTO heat sink, the following parameters were used:

The device was supposed to operate with 50 A anode current, 100 V supply voltage and with 1 kHz switching frequency and 0.5 duty cycle. From the data sheet for the device:

- The on-state voltage at 50 A is 1.25 V.

- $R_{\theta j\text{-}h}$ DC thermal resistance junction to heat sink surface = 0.2 °C/W.

- Turn-on time 5 μS.

- Total turn-off time 11 μS.

- Tcase 125° C.

- The ambient temperature was assumed to be 30° C.

From the above parameters:

The on state power loss is given by:

$$P_c = V_{on} I_A \delta = (1.25)\ (50)\ (O.5) = 31.25 \text{ W.}$$

From equation (F-5), the switching losses for inductive load are:

$$P_s = \frac{(100)(50)(5 + 11)(1000)}{2} = 40 \text{ W}$$

The total power losses P_d are : 31.25 + 40 = 71.25 W.

From equation (F-1):

$$T_{jmax} = T_a + P_d (R_{\theta j\text{-}C} + R_{\theta c\text{-}a} + R_{\theta s\text{-}a})$$

$$R_{\theta j\text{-}C} + R_{\theta c\text{-}a} = 0.2\ ^{\circ}C/W.$$

Therefore:

$$125 = 30 + 71.25\ (\ 0.2 + R_{\theta s\text{-}a}\ )$$

The thermal resistance of the heat sink is:1.13 °C/W.

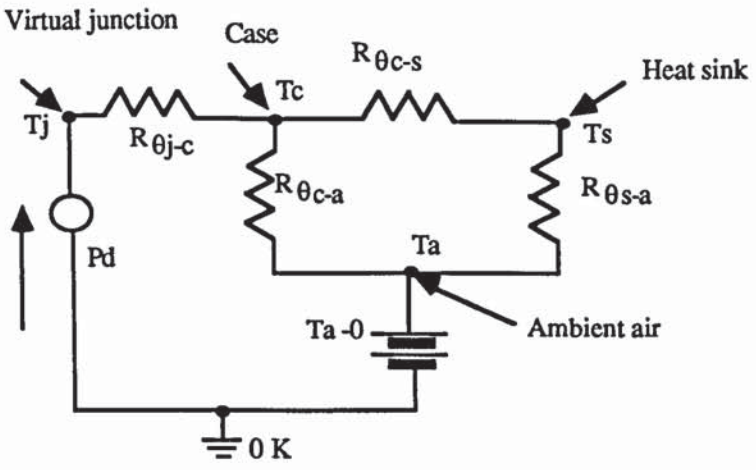


Figure (E-1) Semiconductor thermal radiation equivalent circuit.

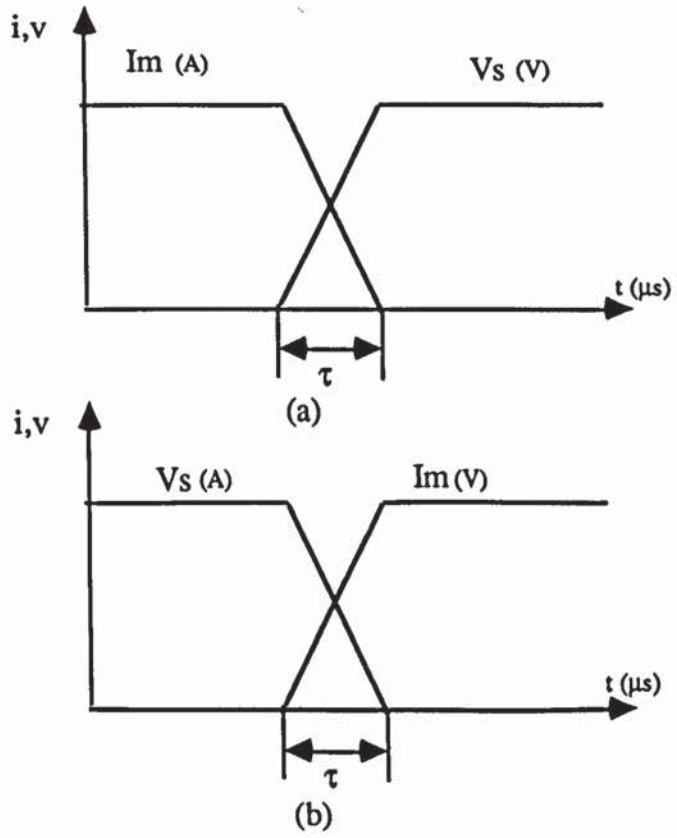


Figure (F-2) Typical voltage and current waveforms for a semiconductor at:

(a) Turn-off

(b) Turn-on

APPENDIX G

HIGH FREQUENCY SHUNT DATA SHEET.

The high frequency shunt (H.F) type ISM 5P/10 permits, in conjunction with a wide-band oscilloscope allow the measurement of current with high di/dt rates in the nanosecond region. Its frequency response is similar to that of a DC coupled oscilloscope and the bandwidth B of the shunt is correspondingly defined by a 3 db attenuation at the top-end of the (transformer) range. Within the specified bandwidth the H.F shunt has the characteristic of a pure non-inductive resistor. The inherent rise-time Ta of the shunt can be derived from the equation Ta = 0.35/B and for very short signal rise times the inherent rise-time can be allowed for in the well-known manner by "geometric addition". Due to its coaxial and screened construction, the shunt is immune to noise from external sources. Any noise which might possibly be observed on the oscilloscope can be eliminated by appropriate measures such as mains filtering, proper earthing and elimination of earth-loops, screening of scope casing and the provision of ferrite-beads for the suppression of lead-born noise.

Technical Data.

Surge rating	$I_{max} = 5$ kA
continuous rating	i = 30 A RMS
Limiting I^2t integral	$\int_0^{\tau} I^2 t\, dt = 2.10^4\ A^2 sec$
Effective resistance at 20 °C	R = 10 mΩ ±1%
Temperature coefficient	$T_k = 0.00005/°C$
Bandwidth (-3dB)	B = 200MHz
Rise time	$T_a = 1.8$ ns
Ripple and overshoots	W = 1%