Synthesis of Interleaved, Unipolar, Switched Capacitor DC-DC Converters

H. Taghizadeh[*], *MIEEE*, A. Cross[†] *MIEEE*, N. Narayanan K.[*] *MIEEE*, A. Urquhart[*] *MIET*

[*]Dept. Mechanical, Electrical and Manufacturing Engineering, Loughborough University, Epinal Way, Loughborough LE11 3TU, UK.
[†]Dept. Electrical and Electronic Engineering, Aston University, Birmingham B4 7ET, UK.

***Abstract*- Switched Capacitor (SC) DC-DC converters are showing great potential for new applications such as data-centres, electric vehicles and power transmission. Many SC topologies have been synthesised on an ad-hoc basis, although new computer methods are being introduced to formalise this process. This paper presents a general synthesis technique that can be incorporated into a computer algorithm to assist with the development of new SC circuits. The technique is based on interleaving SC converter circuits, where two unipolar converters are connected in parallel, and each leg is driven by separate, complementary gate signals. By applying this method to the traditional Ladder SC converter, a topology termed as a Simplified Interleaved Ladder (SIL) converter, is synthesised and tested using a hardware prototype. The resonant implementation of the SIL converter has desirable features for MV/LV applications when compared with other existing SC circuits.**

I. Introduction

Switched Capacitor (SC) DC-DC converters are being developed for a broad-range of applications ranging from low-voltage, on-chip power supplies to high-voltage DC transmission (HVDC). Their attractive features include an inductor/transformer-less topology for all-silicon fabricated power supplies, high step-up and step-down voltage conversion ratios, easy implementation of zero-current switching (ZCS) and a modular structure. The latter is particularly suited to high-voltage applications, where the voltage stress can be evenly distributed across the cells of the converter.

There have been many different SC topologies proposed over the years, of note being the Fibonacci, Doubler, Series-Parallel, Multi-Modular SC Converter (MMSCC) [1], Dickson, Ladder and Cockcroft-Walton based circuits, which will be henceforth referred to as traditional SC converters. Furthermore, it is interesting to note that a recent review [2], still ranks these traditional converters as still being the preferred topologies, despite extensive publication of new circuits in the literature in the past few decades. A reason for this may be that the cellular nature of an SC converter leads to a large number of possible topological combinations, with many of them having no advantage over the traditional SC circuits.

This paper presents results from on-going work to develop a systematic method of both automatically synthesising and appraising different SC topologies using computer-based algorithms. The method is based on the canonical, switched-capacitor cell shown in Fig. 1, and its associated connection matrix definition, known as the c-matrix, which lends itself to rapid computer aided appraisal of SC circuits [3]. Further detail of the cell and c-matrix formulation is given later in Section I-C.

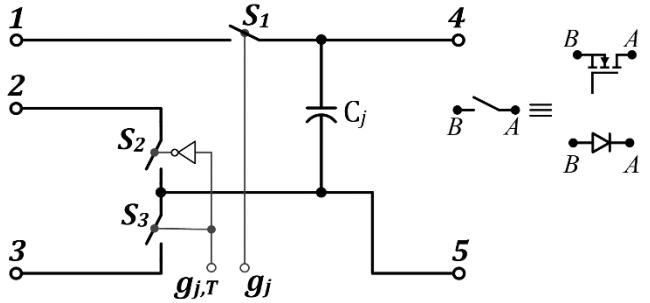

Fig. 1 The canonical switched capacitor cell

I-A. Appraisal

The method of appraisal is based on work by Seeman [4], through the calculation of charge-transfer values Δq, or their normalised equivalents called charge-multipliers α. In [3] a charge multiplier formulation of the state equations for the canonical cell was automatically solved using a computer algorithm. Similarly, in [6] a computer algorithm was presented that allowed the calculation of the voltage-rating multipliers β. The values of α and β, which are analogous to current and voltage respectively, are used to calculate the VA ratings of individual switches and capacitors. For converters with a given voltage conversion ratio r, the appraisal criteria used in [3] and [6] include:

- Number of switches. This is associated with switch cost, gate-drive cost, converter size and overall reliability.
- Whether switch and/or capacitor voltage ratings are equal to the low-side converter voltage, for example the input supply for step-up operation. If so, this avoids the need for series-connected transistors in HV applications, which have proved impractical. Lossy and costly balancing circuits for series-connected capacitors can also be avoided.
- Overall switch VA rating. This is related to the total switch cost of the converter as well as its volume and weight. For SC converters, this also affects the conduction losses and hence the associated cooling requirements and converter running costs.
- Overall capacitor VA rating. The total cost of the capacitors, and their volume, weight and conduction losses are determined by this criterion. Conduction losses follow from the requirement that the same

percentage voltage ripple specification is applied to all cell capacitors.

The comparison of converters in this paper applies to the resonant SC implementation, which is used for high power applications. Switching losses are therefore neglected in the appraisal but could easily be included in the analysis for low-power, hard-switched converters if required.

I-B. Synthesis

In its most basic form, the automatic computer synthesis of SC topologies consists of generating every combination of canonical cell interconnection, gate-drive clock polarity and topology type. The appraisal criteria outlined in the previous section would then be calculated for each topology and selection of a particular circuit would be based on a pre-defined requirements specification. Such a technique is only possible with the aid of a computer because of the large number of circuit combinations. For example, with four cells, which is the minimum needed to synthesise the traditional Ladder SC converter, there are 217,728 possible circuit combinations to synthesise and appraise. Each combination requires the numerical solution of the cell state equations, as described in [3] and [6], and without a computer, the complete appraisal of such a large number of combinations would not be possible.

For converters with six or less cells, this exhaustive method of synthesis and appraisal is computationally feasible using today's office-grade desktop PCs. For example, the calculation of appraisal criteria for converters with six cells and a step-up ratio of $r = 5$, takes approximately 1-hour using a multicore Intel i5 based PC computer. The run-time increases significantly if other conversion ratios are also included in the calculations. More significantly, the number of circuit combinations grows by a factor of approximately 1000 for each additional cell, so that run-times of several months are needed for converters with at seven or more cells. In addition, the computer files that are needed to store the intermediate results from appraisal calculations require several tera-bytes of storage. Converters with more than six cells are anticipated for applications such as MV and HVDC applications, where high voltage conversion ratios are needed using cells with switch/capacitors having relatively low voltage ratings. Whilst alternative search techniques exist, such as Genetic Algorithm (GA) and Particle Swarm Optimisation (PSO), the pseudo-random nature of the search space does not lend itself to these methods. The authors are therefore developing High Performance Computing (HPC) techniques to overcome this computational burden, and the results of this work will be published in a future paper.

Importantly, the existing c-matrix method described in [3] and [6] does not allow the representation and appraisal of interleaved versions of SC converters. Interleaving involves connecting two identical single-leg converters in parallel driven by complementary global clock signals [6]. These interleaved converters have many attractive features compared with single-leg equivalents but are currently excluded from the c-matrix search-space. The main contribution of this paper is therefore the presentation of a new technique that allows the inclusion of interleaved topologies in c-matrix form, using a new multiplexer canonical SC cell. However, simply including such converters into the existing search space would result in a significant increase in the number of circuit combinations, and the extra computational burden would be impractical to manage. Therefore, this paper also introduces a computationally efficient method of appraisal that does not require the solution to the cell state equations for these additional interleaved converters. This method is based on a search for so-called equipotential nodes between the two parallel legs of the interleaved converter. If such nodes exist, this can lead to the elimination of redundant capacitors and switches – known as circuit reduction, which in some cases produces new topologies with very favourable characteristics. This technique specifically lends itself to being implemented on a computer. A computerised solution is essential because of the large numbers of circuit combinations that need to be appraised. However, for demonstration purposes in this paper, the technique is only applied to the small set of candidate topologies that make up the seven members of the traditional SC converter family. Even with this small set of candidates, the so-called Capacitor Optimised Interleaved Ladder (COIL) converter and Simplified Interleaved Ladder converter (SIL) are reported in this paper, which have important advantages over competing topologies. The resonant version of the SIL converter is compared in detail against a similar topology known as a D-2L-Tank [7], which has recently been proposed.

Various methods of appraisal and synthesis for SC converters have been described, starting with fundamental work in [8]. Since then, there has been little progress to note until recently with [9-11]. In [9], appraisal was considered by a detailed calculation of cell capacitor and resonant inductor volume and switch losses, but synthesis was not considered. Methods of automatic topology formulation have been proposed for two-phase [10] and multi-phase [11] SC converters. However, these circuits are synthesised from individual switches and capacitors rather than the canonical cells proposed here. The use of individual components dramatically increases the number of circuit combinations. To overcome this, constraint equations were used to limit the search-space to those circuits termed 'realizable', that is, those circuits achieving the required voltage conversion ratio r. Nevertheless, as stated in [10] and [11], the size of the resulting solution-space limits these techniques to cells of four and five respectively. However, at least four cells are needed to synthesise the traditional ladder SC converter with the minimum voltage gain of three, and therefore these methods are currently impractical for the studies proposed here.

I-C. Review of the c-Matrix Formulation of SC Converters

Before continuing, the main concepts from [3] and [6] are briefly re-introduced. The canonical cell was shown in Fig. 1, where the implementation of the cell switches for step-up conversion using two-quadrant devices is included in the figure.

The interconnection of the converter's cells is defined using a connection matrix $\boldsymbol{c}$, where each element c_{ij} represents the cell number to which the $i^{th} = 1 \rightarrow 3$ input of the j^{th} cell shown in Fig. 1, is connected,

$$\boldsymbol{c} = \begin{pmatrix} c_{11} & c_{12} & \cdots & c_{1N} \\ c_{21} & c_{22} & \cdots & c_{2N} \\ c_{31} & c_{32} & \cdots & c_{3N} \end{pmatrix} \quad (1)$$

The switch S_1 gate signal for the i^{th} cell is defined using the gate signal vector $\boldsymbol{G}$:

$$\boldsymbol{G} = (g_1\, g_2\, \cdots\, g_N) \quad (2)$$

and the topology input signal for the i^{th} cell, which determines the on/off state of switch S_3 is,

$$\boldsymbol{G_T} = \left(g_{1,T}\, g_{2,T}\, \cdots\, g_{N,T}\right) \quad (3)$$

Upstream cells are those nearest to the converter input and downstream cells are those closer to the load. The analysis presented here assumes a voltage step-up from source to load, but equally applies to a step-down converter.

As the cell is driven by gate signals having high/low states, the expressions for the cell voltage and currents are then state equations having two numeric values. In terms of appraisal, the number of switches is calculated from the $\boldsymbol{G_T}$ vector, and the switch/capacitor VA ratings are computed using the computer algorithm described in [6] to solve the converter state equations.

The paper is arranged as follows. Section II describes the method of forming an interleaved converter from two single-leg converters and the algorithmic steps required to attempt circuit reduction using equipotential nodes. Section II-A introduces the new multiplexer canonical cell, which is used to combine the outputs of the two interleaved legs. Section II-B then develops the computerised method of interleaving by manually describing the process using the traditional Doubler SC converter as an example. Section II-C then presents the results of applying the computerised algorithm to the traditional Ladder SC converter, where the COIL and SIL circuits are revealed. Section II-D carries out a detailed comparison of the SIL converter against a new so-called D-2L-tank circuit which has only recently been published in the literature and has a similar topology. Finally, section III presents measured results from a hardware prototype of the SIL converter, which is then followed by conclusions in section IV.

II. Interleaved, 2-Leg Converters

The method of synthesis is based on an interleaving approach and places two identical SC converter legs in parallel, where each converter leg consists of $N/2$ cells, N being the total number of cells. Both converter legs are connected to a common DC source V_{in}, and common load. Each leg is fed with complementary global clock signals g and $\bar{g}$. In terms of an exhaustive search, the application of these interleaving rules to the existing combinations of single-leg converters dramatically reduces the additional computational effort needed to appraise these circuits. This is because (a) the practical nature of the rules eliminates many redundant interleaved topology combinations and (b) there is no need to solve the cell state equations for the interleaved topology as the values that have already been calculated for the single-leg converter can be reused.

The general arrangement of the interleaved converter is shown in Fig. 2. The outputs of the two converters are normally terminated with a sample-and-hold cell, but this is now replaced by a new 2:1 multiplexer cell, which is shown on the right in Fig. 2 and described in more detail in section II-A below.

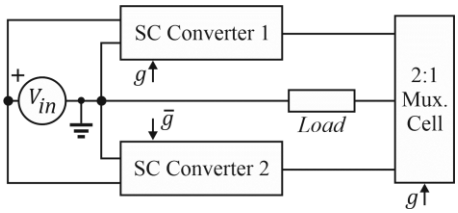

Fig. 2 Interleaving of two identical SC converters with complementary clock signals g and $\bar{g}$

Once the candidate topology has been synthesised, a reduction of the overall circuit is attempted through the removal of redundant cell capacitors and switches. This is achieved by searching through the normalised node voltages, or more specifically, through the voltage-rating multipliers β, which have integer values, to find any nodes that have the same voltages during the same charging state. These are termed equipotential nodes, which can be connected by the addition of a wire. This process is easily automated using the proposed c-matrix definition of an SC converter.

This computer algorithm has initially been applied to the traditional SC converter topologies – Fibonacci, Doubler, MMSCC, Dickson, Ladder and Cockcroft-Walton. This confirmed that other than the output sample-and-hold cell, which has an obvious equipotential node at the converter output, only the Doubler and Ladder circuits exhibit an opportunity for circuit reduction, the other converters being wholly flying-capacitor based [12]. Likewise, the 2-leg version of the Series-Parallel converter cannot be reduced, but the reasons for this are less obvious. The application of the algorithm to this restricted subset of seven converters was for demonstration purposes only but showed how the algorithm can rapidly reject what intuitively seem like promising candidates for interleaving. The application of the algorithm to the Doubler and Ladder converters is discussed in detail in sections II-B and II-C respectively.

A correction to our previous publications [3] and [6] is made at this point: the topology which was referred to as the Dickson SC converter, should have been termed a Cockcroft-Walton based circuit as defined by Seeman [4]. This correction is important as we discuss the Dickson SC converter in more detail in Section II-D.

II-A. The 2:1 Multiplexer Cell

The existing canonical cell shown in Fig. 1 cannot be used to synthesise interleaved converters. Therefore, an additional cell type is required, which is used to multiplex the outputs of the two parallel converters into a single output. This cell is known as a 2:1 multiplexer cell and is shown in Fig. 3.

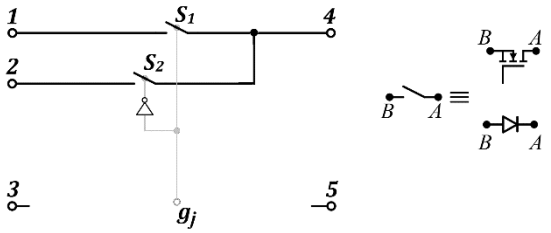

Fig. 3 The 2:1 Multiplexer cell

The cell consists of two switches with complementary gate-signals derived from the global clock g. The cell is based on the five-terminal SC cell shown in Fig. 1, so that it can be defined using the c-matrix proposed in [3] and [6]. Terminals 3 and 5 are unconnected and appear as open-circuit nodes.

The state equations for the charge multipliers $\Delta q_j[g_j]$ at terminals 1-3 of the j^{th} cell are,

$$\begin{aligned}\Delta q_{1j}[g_j] &= g_j\,\Delta q_{4j}[g_j]\\ \Delta q_{2j}[g_j] &= \bar{g}_j\,\Delta q_{4j}[g_j]\\ \Delta q_{3j}[g_j] &= X\end{aligned} \tag{4}$$

where X represents an open-circuit or don't care connection. The corresponding state equations for the voltages at terminals 4 and 5 $v_{,j}[g_j]$ are,

$$\begin{aligned}v_{4,j}[g_j] &= g_j\,v_{1,j}[g_j] + \bar{g}_j\,v_{2,j}[g_j]\\ v_{5,j}[g_j] &= X\end{aligned} \tag{5}$$

These state equations for the multiplexer cell can be incorporated into the algorithms described in [3] and [6], so that the charge and voltage-rating multipliers can be calculated for the 2-leg interleaved converters. A multiplexer cell is designated by the symbol M in the topology vector $\boldsymbol{G_T}$.

II-B. The Interleaved, Doubler Converter

The traditional Doubler SC converter is now used as an example to develop the interleaving algorithm that is suitable for automation using a computer. The Doubler SC converter consists of cascaded doubler cells, with each stage being separated by a sample-and-hold cell. The converter therefore has an even number of cells and a voltage conversion ratio $r = 2^{N/2}$. The interleaved version of this topology, which follows from Fig. 2, is shown in Fig. 4. The upper and lower legs are both terminated using complementary sample-and-hold cells, which fulfil the function of the 2:1 multiplexer cell shown in Fig. 3. The c-matrix definition for an N-cell Doubler SC converter is given by,

$$\boldsymbol{c} = \begin{pmatrix} 0 & 1 & 2 & 3 & 4 & \cdots & N-1 \\ 0 & X & 2 & X & 4 & \cdots & X \\ 0 & 0 & 0 & 0 & 0 & \cdots & 0 \end{pmatrix} \tag{6}$$

and the corresponding gate signal vector $\boldsymbol{G}$ and cell topology vector $\boldsymbol{G_T}$, where T denotes a boolean True are,

$$\begin{aligned}\boldsymbol{G_1} &= (g \quad \bar{g} \quad g \quad \bar{g} \quad g \quad \cdots \quad \bar{g})\\ \boldsymbol{G_{T1}} &= (g \quad T \quad g \quad T \quad g \quad \cdots \quad T)\end{aligned} \tag{7}$$

A subscript 1 is used to denote the upper converter in Fig 4. The gate signals for the lower converter 2 are the complement of converter 1 and using subscript 2 for this converter,

$$\begin{aligned}\boldsymbol{G_2} &= (\bar{g} \quad g \quad \bar{g} \quad g \quad \bar{g} \quad \cdots \quad g)\\ \boldsymbol{G_{T2}} &= (\bar{g} \quad T \quad \bar{g} \quad T \quad \bar{g} \quad \cdots \quad T)\end{aligned} \tag{8}$$

Applying the state equation algorithm to a converter with an arbitrarily chosen 8 cells for each leg, the normalised node voltages, denoted by the voltage multipliers $\boldsymbol{\beta}$, are calculated for the output terminals 4 and 5 of each cell according to [6]. For converter 1, this gives $\boldsymbol{\beta_{41}}$ and $\boldsymbol{\beta_{51}}$,

$$\boldsymbol{\beta_{41}} = \left[\begin{bmatrix}1\\2\end{bmatrix} \begin{bmatrix}2\\2\end{bmatrix} \begin{bmatrix}2\\4\end{bmatrix} \begin{bmatrix}4\\4\end{bmatrix} \begin{bmatrix}4\\8\end{bmatrix} \begin{bmatrix}8\\8\end{bmatrix} \begin{bmatrix}8\\16\end{bmatrix} \begin{bmatrix}16\\16\end{bmatrix}\right] \tag{9}$$

$$\boldsymbol{\beta_{51}} = \left[\begin{bmatrix}0\\1\end{bmatrix} \begin{bmatrix}0\\0\end{bmatrix} \begin{bmatrix}0\\2\end{bmatrix} \begin{bmatrix}0\\0\end{bmatrix} \begin{bmatrix}0\\4\end{bmatrix} \begin{bmatrix}0\\0\end{bmatrix} \begin{bmatrix}0\\8\end{bmatrix} \begin{bmatrix}0\\0\end{bmatrix}\right] \tag{10}$$

where the upper term in each sub-vector corresponds to the global clock g being high, and the lower term is for g being in a low-state. Similarly, the voltage multipliers for converter 2, $\boldsymbol{\beta_{42}}$ and $\boldsymbol{\beta_{52}}$ are,

$$\boldsymbol{\beta_{42}} = \left[\begin{bmatrix}2\\1\end{bmatrix} \begin{bmatrix}2\\2\end{bmatrix} \begin{bmatrix}4\\2\end{bmatrix} \begin{bmatrix}4\\4\end{bmatrix} \begin{bmatrix}8\\4\end{bmatrix} \begin{bmatrix}8\\8\end{bmatrix} \begin{bmatrix}16\\8\end{bmatrix} \begin{bmatrix}16\\16\end{bmatrix}\right] \tag{11}$$

$$\boldsymbol{\beta_{52}} = \left[\begin{bmatrix}1\\0\end{bmatrix} \begin{bmatrix}0\\0\end{bmatrix} \begin{bmatrix}2\\0\end{bmatrix} \begin{bmatrix}0\\0\end{bmatrix} \begin{bmatrix}4\\0\end{bmatrix} \begin{bmatrix}0\\0\end{bmatrix} \begin{bmatrix}8\\0\end{bmatrix} \begin{bmatrix}0\\0\end{bmatrix}\right] \tag{12}$$

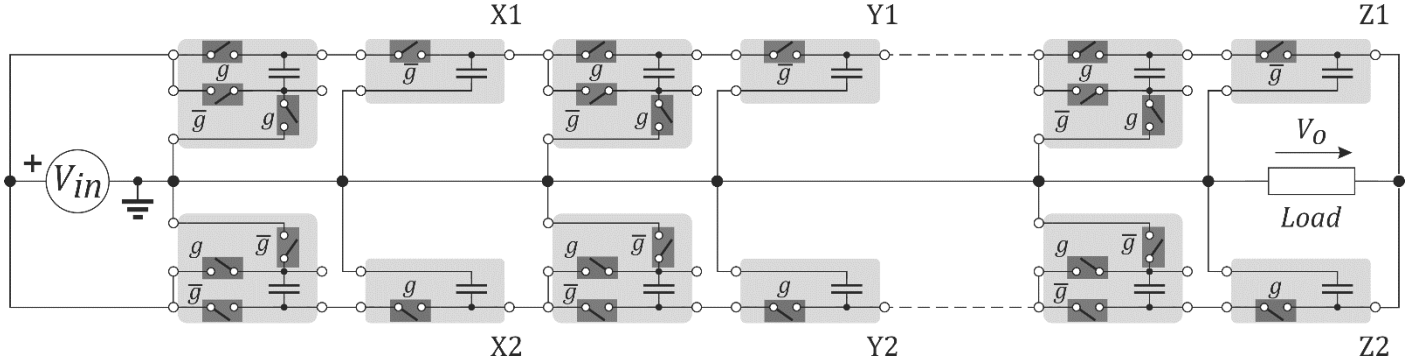

Fig. 4 Interleaved version of the traditional Doubler SC converter, with a red cell gate = g and green cell gate = $\bar{g}$

The numerical sequence can easily be identified for converters with higher numbers of cells per leg (>8), by inspection of these values.

The cell output nodes 4 and 5 are of importance as they represent the node voltages of the capacitors in each cell. More importantly it can be seen from these results that for even numbered cells,

$$\boldsymbol{\beta_{41}} = \boldsymbol{\beta_{42}}$$
$$\boldsymbol{\beta_{51}} = \boldsymbol{\beta_{52}} \quad (13)$$

These equipotential nodes, which are denoted as X_1,/X_2, Y_1,/Y_2 and Z_1,/Z_2 in Fig. 4, can be connected together. such a connection is shown for X_1,/X_2 in Fig. 5. The opposite sides of the capacitors are already connected to ground as shown in Fig 5, so the two cell capacitors C_1 and C_2 are now in parallel.

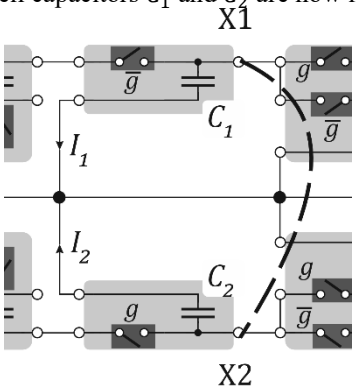

Fig. 5 Hardwired connection of the equipotential nodes X_1/X_2

The current flowing into this *equivalent* capacitor is the sum of the currents I_1 and I_2, also shown in Fig. 5. These normalised currents, denoted by the charge multipliers $\boldsymbol{\alpha}$, can be calculated using the state equation algorithm described in [3]. The values for the normalised currents for converter 1, denoted $\boldsymbol{\alpha_{C1}}$ are,

$$\boldsymbol{\alpha_{C1}} = \begin{bmatrix}\begin{bmatrix}8\\-8\end{bmatrix} & \begin{bmatrix}-4\\4\end{bmatrix} & \begin{bmatrix}4\\-4\end{bmatrix} & \begin{bmatrix}-2\\2\end{bmatrix} & \begin{bmatrix}2\\-2\end{bmatrix} & \begin{bmatrix}-1\\1\end{bmatrix} & \begin{bmatrix}1\\1\end{bmatrix} & \begin{bmatrix}-0.5\\0.5\end{bmatrix}\end{bmatrix} \quad (14)$$

The values for the second converter, $\boldsymbol{\alpha_{C2}}$ are found to be equal and opposite so that,

$$\boldsymbol{\alpha_{C1}} + \boldsymbol{\alpha_{C2}} = \mathbf{0} \quad (15)$$

This shows the charge transfer into the combined parallel capacitors for X_1,/X_2 is zero, which makes the capacitors redundant, and they can be removed from the circuit. The same is found for the capacitors associated with equipotential nodes Y_1,/Y_2 and Z_1,/Z_2, and this results in a significant reduction in the overall capacitor VA rating of the converter.

Whilst the removal of the capacitors in the final sample-and-hold cell is possible, in practice a small output capacitor is still required to provide smoothing of the converter output voltage during the finite commutations of the two output switches used to for the 2:1 multiplexer function.

Further simplification of the circuit can be carried out, which leads to the removal of switches. This is achieved by searching for other equipotential nodes associated with the cell input terminals 1-3. These are connected through cell switches S_1-S_3 respectively as shown in Fig. 1. This means that input terminals can become inactive if their corresponding switches are open, their voltages then being determined by connections to upstream cells. Therefore, when searching through *input* terminals for equipotential nodes, only the active states should be considered. These active states are determined by the switch gate-signals, which themselves depend on the cell's entry in the $\boldsymbol{G}$ and $\boldsymbol{G_T}$ vectors. The $\boldsymbol{\beta}$ values for terminals 1, 2 and 3 of converter 1 using (2) are,

$$\boldsymbol{\beta_{11}} = \begin{bmatrix}\begin{bmatrix}\mathbf{1}\\1\end{bmatrix} & \begin{bmatrix}1\\\mathbf{2}\end{bmatrix} & \begin{bmatrix}\mathbf{2}\\2\end{bmatrix} & \begin{bmatrix}2\\\mathbf{4}\end{bmatrix} & \begin{bmatrix}\mathbf{4}\\4\end{bmatrix} & \begin{bmatrix}4\\\mathbf{8}\end{bmatrix} & \begin{bmatrix}\mathbf{8}\\8\end{bmatrix} & \begin{bmatrix}8\\\mathbf{16}\end{bmatrix}\end{bmatrix} \quad (16)$$

$$\boldsymbol{\beta_{21}} = \begin{bmatrix}\begin{bmatrix}1\\\mathbf{1}\end{bmatrix} & \begin{bmatrix}X\\X\end{bmatrix} & \begin{bmatrix}2\\\mathbf{2}\end{bmatrix} & \begin{bmatrix}X\\X\end{bmatrix} & \begin{bmatrix}4\\\mathbf{4}\end{bmatrix} & \begin{bmatrix}X\\X\end{bmatrix} & \begin{bmatrix}8\\\mathbf{8}\end{bmatrix} & \begin{bmatrix}X\\X\end{bmatrix}\end{bmatrix} \quad (17)$$

$$\boldsymbol{\beta_{31}} = \begin{bmatrix}\begin{bmatrix}\mathbf{0}\\0\end{bmatrix} & \begin{bmatrix}X\\X\end{bmatrix} & \begin{bmatrix}\mathbf{0}\\0\end{bmatrix} & \begin{bmatrix}X\\X\end{bmatrix} & \begin{bmatrix}\mathbf{0}\\0\end{bmatrix} & \begin{bmatrix}X\\X\end{bmatrix} & \begin{bmatrix}\mathbf{0}\\0\end{bmatrix} & \begin{bmatrix}X\\X\end{bmatrix}\end{bmatrix} \quad (18)$$

where the inactive states are shown in a lighter font and these should be disregarded. The strategy is to look for equipotential nodes between the inputs shown in (16)-(18) and the output terminals 4 and 5; importantly to search for input nodes that connect to cells further upstream from their existing connections. This then opens the possibility of bypassing intermediate cells, and these cells can then be removed from the circuit. For the 8-cell converter considered here this involves the comparison of the active values for the inputs shown by (16)-(18) with the output values (9) and (11). Note that both states for terminal 4 and 5 are always active. This exercise reveals twelve such alternative routings, and a summary of six of these connections for converter 1 are shown in Table I.

TABLE I
Equipotential nodes between converter 1 and 2, terminals 1 and 4

Converter 1, terminal 2		Converter 1, terminal 4
Cell 3		Cell 1
Cell 5		Cell 3
Cell 7	Alternative connection to:	Cell 5
Converter 1, terminal 1	→	**Converter 2, terminal 4**
Cell 3		Cell 1
Cell 5		Cell 3
Cell 7		Cell 5

By making these connections, which are shown by the dotted wires in Fig. 6, the wiring around the inputs of these cells can be removed, which is also shown in the figure.

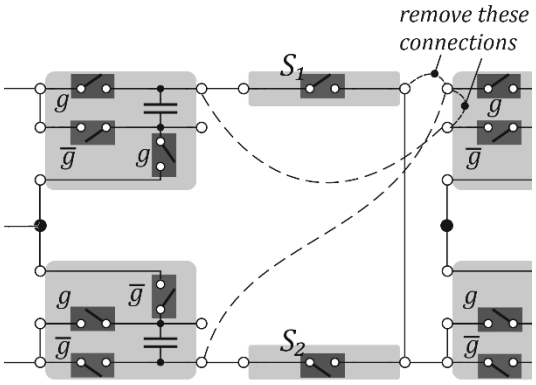

Fig. 6 Connections between equipotential nodes from converter 1 to 2.

The remaining six equipotential nodes follow from the symmetry of the converter. For example, a connection can be made between terminal 1 of the lower right-hand cell in Fig. 6 and terminal 4 of the upper left-hand cell.

Fig. 6 shows that if the input connections are removed from both the upper and lower right-hand cells, then switch pair S_1/S_2 become redundant and can be removed from the circuit. The resulting simplified converter circuit is shown in Fig. 7 and is called a Simplified Interleaved Doubler SC converter. The two output switches that remain from simplification of the sample-and-hold cells are shown as a 2:1 multiplexer cell. In addition, the small output capacitor C_O, has been included, and is used to smooth the output commutations of the multiplexer switch. For the example used here, the overall number of cells has been reduced from $N = 16$ to $N = 9$.

Fig. 7 also shows the convention used for cell numbering. The voltage conversion equation is given by $r = 2^{N_C/2}$, where N_C is the number of cells with capacitors. This equation is then same as the traditional doubler circuit. Alternatively, in terms of N, this becomes $r = 2^{(N-1)/2}$ for the interleaved circuit.

Using the new definition of a 2:1 multiplexer cell, and the cell numbering convention shown in Fig. 6, the $\boldsymbol{c}$, $\boldsymbol{G}$ and $\boldsymbol{G_T}$ matrices for the 9-cell Simplified Interleaved Doubler are,

$$\boldsymbol{c} = \begin{pmatrix} 0 & 0 & 2 & 1 & 4 & 3 & 6 & 5 & 7 \\ 0 & 0 & 1 & 2 & 3 & 4 & 5 & 6 & 8 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & X \end{pmatrix} \tag{19}$$

$$\begin{aligned} \boldsymbol{G} &= (g \quad \bar{g} \quad g \quad \bar{g} \quad g \quad \bar{g} \quad g \quad \bar{g} \quad \bar{g}) \\ \boldsymbol{G_T} &= (g \quad \bar{g} \quad g \quad \bar{g} \quad g \quad \bar{g} \quad g \quad \bar{g} \quad M) \end{aligned} \tag{20}$$

where the new 2:1 multiplexer Cell is seen as the last entry in the $\boldsymbol{G_T}$ vector.

The state equation algorithm was updated to include the multiplexer cell. The algorithm was then used to calculate the charge $\boldsymbol{\alpha}$, and voltage-rating multipliers $\boldsymbol{\beta}$, for the capacitors and switches of the 9-cell, Simplified Interleaved Doubler SC converter as shown in Table 2. Values for a traditional 8-cell Doubler SC converter are shown in Table 3 for comparison.

These tables show that the total normalised capacitor VA rating for the Simplified Interleaved Doubler converter is half that of the traditional circuit, which is a significant saving. In addition, the removal of switches from the simplified converter has reduced the total normalised switch VA rating by approximately 20%. However, the peak voltage rating of the last two S_1 switches has increased from 8 to 12 and the number of switches has increased from 16 to 26, which could be a disadvantage for low-power circuits where the cost of gate-drive circuits may be a limiting factor.

TABLE 2
Charge/voltage-rating multipliers for a 9-cell, Simplified Interleaved, Doubler SC converter, $r = 16$

	Switch S_1	**Switch S_2**	**Switch S_3**
$\boldsymbol{\alpha}$	-[8,8,4,4,2,2,1,1,1]/2	[8,8,4,4,2,2,1,1,1]/2	[8,8,4,4,2,2,1,1,X]/2
$\boldsymbol{\beta}$	[1,1,3,3,6,6,12,12,8]	[1,1,1,1,2,2,4,4,8]	[1,1,2,2,4,4,8,8,X]

	Capacitor	**Total normalised VA**	
		Switch	**Capacitor**
$\boldsymbol{\alpha}$	[8,8,4,4,2,2,1,1,X]/2	6.5	2.0
$\boldsymbol{\beta}$	[1,1,2,2,4,4,8,8,X]		
No. switches	26	**All switch $\boldsymbol{\beta} = \mathbf{1}$?**	No

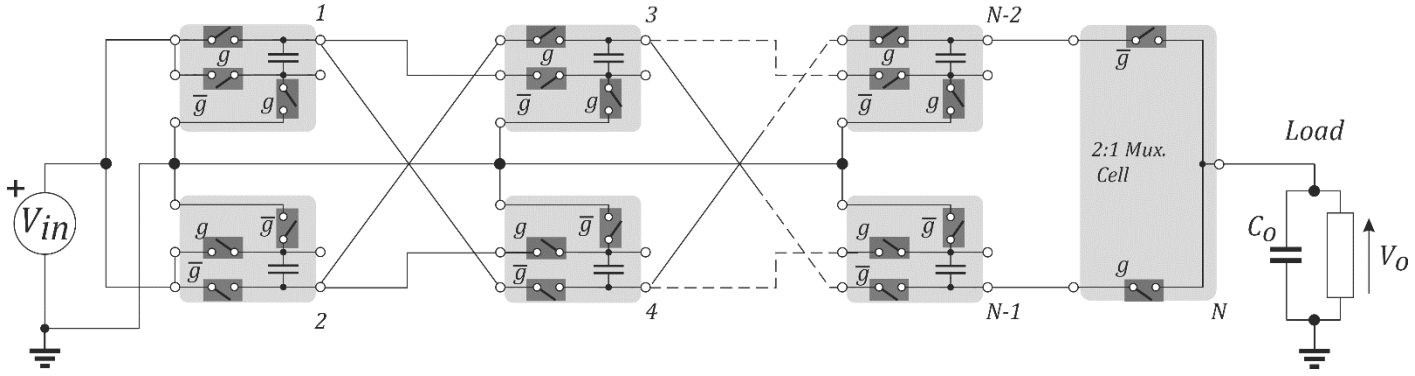

Fig. 7 Simplified Interleaved Doubler SC converter including output capacitor C_o

TABLE 3
Charge/voltage-rating multipliers for a 8-cell, traditional doubler SC converter, $r = 16$

	Switch S_1	Switch S_2	Switch S_3
$\boldsymbol{\alpha}$	-[8,8,4,4,2,2,1,1]	[8,X,4,X,2,X,1,X]	[8,X,4,X,2,X,1,X]
$\boldsymbol{\beta}$	[1,1,2,2,4,4,8,8]	[1,X,2,X,4,X,8,X]	[1,X,2,X,4,X,8,X]

	Capacitor	Total normalised VA	
		Switch	Capacitor
$\boldsymbol{\alpha}$	[8,4,4,2,4,1,1,0.5]	8.0	4.0
$\boldsymbol{\beta}$	[1,2,2,4,4,8,8,16]		

No. switches	16	All switch $\boldsymbol{\beta} = \mathbf{1}$?	No

The Simplified Interleaved Doubler circuit is not a new topology, having been described in a 1995 patent [13]. This patent was discussed in [14] for on-chip applications, which being silicon based, are inherently hard-switched. The circuit was referred to as the Cernea converter after its inventor.

The hard-switched doubler circuit is suitable for low-voltage, low power circuits, but becomes impractical for high voltages. This is because the voltage stress on the switches increases exponentially with the number of cells N. The voltage ratings of existing IGBT technology are therefore exceeded even for a small number of cells. This should be compared with the traditional Ladder SC converter and its interleaved version which are discussed next. The Ladder converter is suitable for high-voltage applications since the voltage stress on the switches and capacitors is equal to the input supply voltage for all the cells. In addition, the resonant version of the Ladder converter is easily implemented, which makes it suitable for high-power applications such as photovoltaic and windfarm HVDC connections.

II-C. The Interleaved Ladder Converter

For the discussions that follow, the traditional Ladder SC converter with an arbitrary five cells is shown in Fig. 8 for reference and presented in its more common schematic format.

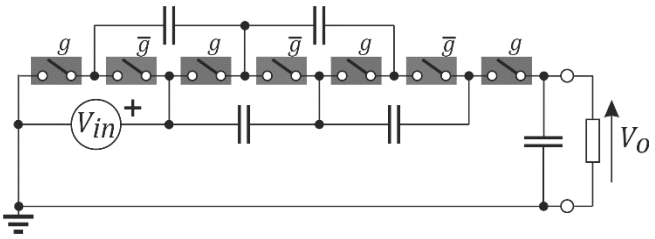

Fig. 8 Traditional Ladder, 5-cell SC converter

The interleaved version of the Ladder converter using the canonical cell representation is shown in Fig. 9. Each leg consists of one doubler cell, followed by a cascade of ladder-rung cells. The traditional converter has an even number of cells and a voltage conversion ratio $r = N/2 + 1$.

The c-matrix definition for a N-cell Ladder SC converter is,

$$\boldsymbol{c} = \begin{pmatrix} 0 & 1 & 2 & 3 & 4 & \cdots & N-1 \\ 0 & 0 & 1 & 2 & 3 & \cdots & X \\ 0 & X & X & X & X & \cdots & 0 \end{pmatrix} \tag{21}$$

and the corresponding gate signal vector $\boldsymbol{G_1}$ and cell topology vector $\boldsymbol{G_{T1}}$,for converter 1 of an interleaved implementation, where F denotes a boolean False, are:

$$\begin{aligned} \boldsymbol{G_1} &= (g \quad \bar{g} \quad g \quad \bar{g} \quad g \quad \cdots \quad \bar{g}) \\ \boldsymbol{G_{T1}} &= (g \quad F \quad F \quad F \quad F \quad \cdots \quad T) \end{aligned} \tag{22}$$

The corresponding vectors for converter 2 are then,

$$\begin{aligned} \boldsymbol{G_2} &= (\bar{g} \quad g \quad \bar{g} \quad g \quad \bar{g} \quad \cdots \quad g) \\ \boldsymbol{G_{T2}} &= (\bar{g} \quad F \quad F \quad F \quad F \quad \cdots \quad T) \end{aligned} \tag{23}$$

Using these arrays, the computer algorithm was used to automatically synthesise the interleaved version of the ladder converter. The synthesis was carried out in two stages, first the algorithm identified equipotential nodes for the elimination of cell capacitors. Whilst the resulting topology was not optimised in terms of a minimum the number of switches, it did have very desirable features and is described separately in section II-C-I below. This converter has been termed a Capacitor Optimised Interleaved Ladder (COIL) converter. Finally, the algorithm was used to additionally minimise the number of switches, which resulted in another converter circuit termed the Simplified Interleaved Ladder (SIL)

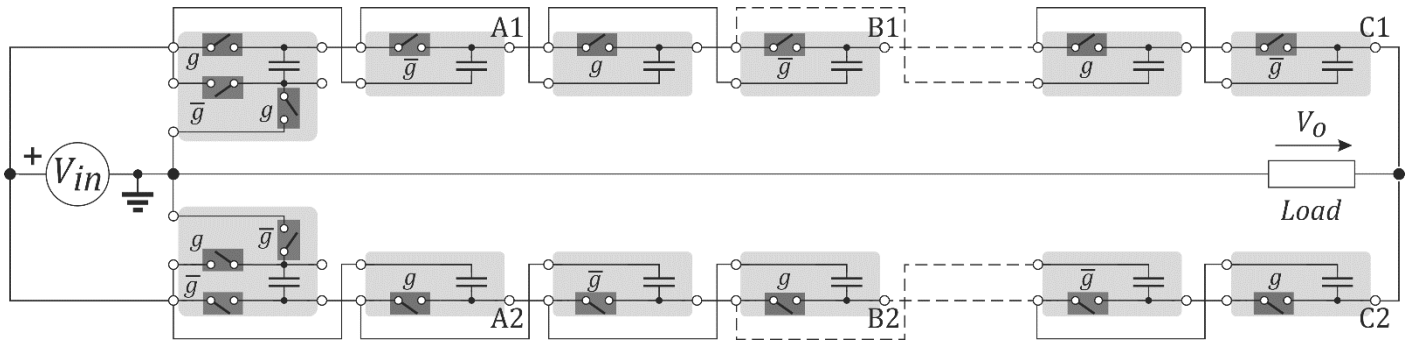

Fig. 9 Interleaved version of the traditional Ladder SC converter

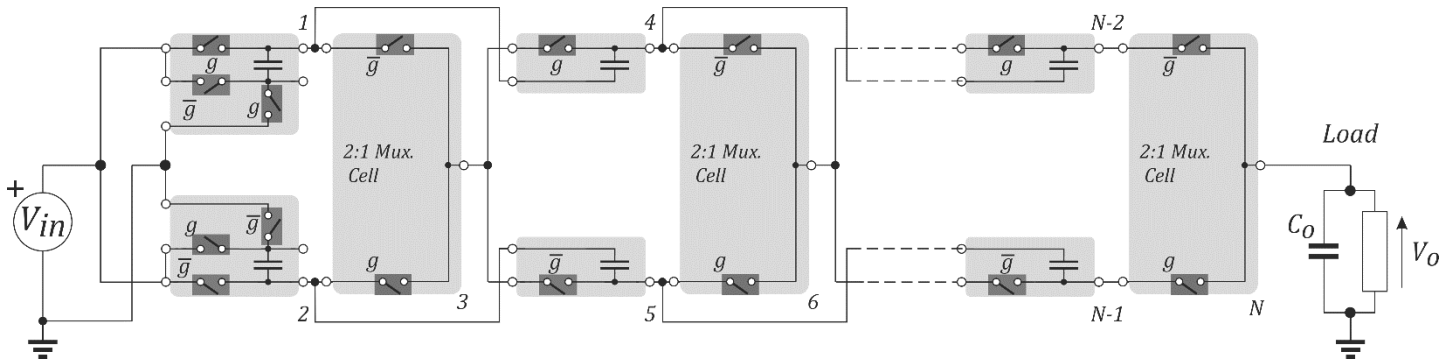

Fig. 10 Capacitor Optimised Interleaved Ladder (COIL) SC converter

II-C-I. The Capacitor Optimised Interleaved Ladder Converter

Applying just capacitor reduction to the interleaved Ladder of Fig. 9, results in the removal of the capacitors from the even-numbered cell pairs A1/2, B1/2 and C1/2, with the addition of wire links between equipotential nodes of the two parallel legs. The switch pairs that remain from these reduced cells form 2:1 multiplexer cells. The final converter, which has been termed a Capacitor Optimised Interleaved Ladder (COIL) SC converter is shown in Fig. 10. The equation for the voltage conversion ratio, which does not include the multiplexer cells, is the same as that for a traditional Ladder converter $r = N_C/2 + 1$, or in terms of N, this becomes $r = N/3 + 1$.

The $\boldsymbol{c}$, $\boldsymbol{G}$ and $\boldsymbol{G_T}$ matrices for a 12-cell COIL circuit are,

$$\boldsymbol{c} = \begin{pmatrix} 0 & 0 & 1 & 3 & 3 & 4 & 6 & 6 & 7 & 9 & 9 & 10 \\ 0 & 0 & 2 & 1 & 2 & 5 & 4 & 5 & 8 & 7 & 8 & 11 \\ 0 & 0 & X & X & X & X & X & X & X & X & X & X \end{pmatrix} \quad (24)$$

$$\boldsymbol{G} = (g \quad \bar{g} \quad \bar{g} \quad g \quad \bar{g} \quad \bar{g} \quad g \quad \bar{g} \quad \bar{g} \quad g \quad \bar{g} \quad \bar{g})$$
$$\boldsymbol{G_T} = (g \quad \bar{g} \quad M \quad F \quad F \quad M \quad F \quad F \quad M \quad F \quad F \quad M) \quad (25)$$

and these arrays were used to calculate the charge $\boldsymbol{\alpha}$, and voltage-rating multipliers $\boldsymbol{\beta}$, for the capacitors and switches of a 12-cell COIL converter, which are shown in Table 4. The values for a traditional 8-cell ladder SC converter are shown in Table 5 for comparison. The notable difference between Tables 4 and 5 is that the total normalised capacitor VA rating for the COIL converter is approximately half that of the traditional circuit, which is a significant saving. For example, if both converters were designed with the same total capacitor VA rating, the traditional ladder circuit would have almost twice the output voltage ripple of the interleaved converter.

TABLE 4
Charge/voltage-rating multipliers for a 12-cell Capacitor Optimised Interleaved Ladder (COIL) SC converter, $r = 5$

	Switch S_1	**Switch S_2**	**Switch S_3**
$\boldsymbol{\alpha}$	-[1,1,1,1,1,1,1,1,1,1,1,1]/2	[4,4,1,X,X,1,X,X,1,X,X,1]/2	[4,4,X,X,X,X,X,X,X,X,X,1]/2
$\boldsymbol{\beta}$	[1,1,1,1,1,1,1,1,1,1,1,1]	[1,1,1,X,X,1,X,X,1,X,X,1]	[1,1,X,X,X,X,X,X,X,X,X,1]

	Cell Capacitor	**Total normalised VA**	
		Switch	**Capacitor**
$\boldsymbol{\alpha}$	[4,4,X,3,3,X,2,2,X,1,1,X]/2	3.2	2.0
$\boldsymbol{\beta}$	[1,1,X,1,1,X,1,1X,1,1,X]		

No. switches	20	**All switch $\boldsymbol{\beta} = \mathbf{1}$?**	Yes

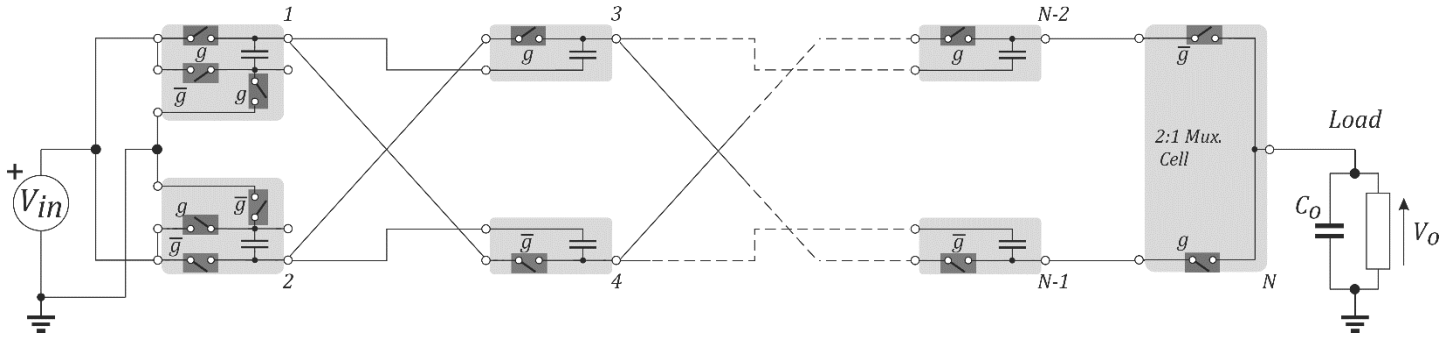

Fig. 11 Simplified Interleaved Ladder (SIL) SC converter

TABLE 5
Charge/voltage-rating multipliers for a 8-cell traditional Ladder SC converter, $r = 5$

	Switch S_1	**Switch S_2**	**Switch S_3**
$\boldsymbol{\alpha}$	-[1,1,1,1,1,1,1,1]	[4,X,X,X,X,X,X,X]	[4,X,X,X,X,X,X,X]
$\boldsymbol{\beta}$	[1,1,1,1,1,1,1,1]	[1,X,X,X,X,X,X,X]	[1,X,X,X,X,X,X,X]

	Cell Capacitor	**Total normalised VA**	
		Switch	**Capacitor**
$\boldsymbol{\alpha}$	[4,3,3,2,2,1,1,0.5]	3.2	3.7
$\boldsymbol{\beta}$	[1,1,1,1,1,1,1,5]		
No. switches	10	**All switch $\boldsymbol{\beta} = \mathbf{1}$?**	Yes

The savings in overall capacitor VA rating were achieved without any increase in overall switch VA rating, and importantly the unity-normalised voltage rating for all the converter switches was maintained. On the other hand, the number of switches is double that for the traditional ladder circuit, and whilst this is not such a concern for high-power, high-voltage applications, the increase in the number of gate-drives can be an issue for lower power/voltage applications.

II-C-II. The Simplified Interleaved Ladder Converter

The algorithm was then applied to the interleaved Ladder to minimise both capacitors and switches. The minimisation of switches had the effect of removing the multiplexer cells from the COIL converter. This was achieved by the algorithm inserting cross-diagonal-links between equipotential nodes, and the resulting circuit, which was termed a Simplified Interleaved Ladder (SIL) SC converter, is shown in Fig. 11. The voltage conversion ratio equation in terms of N_C is the same as that for the COIL converter $r = N_C/2 + 1$, but in terms of N it becomes $r = (N-1)/2 + 1$.

The $\boldsymbol{c}$, $\boldsymbol{G}$ and $\boldsymbol{G_T}$ matrices for a 9 cell SIL converter are,

$$\boldsymbol{c} = \begin{pmatrix} 0 & 0 & 2 & 1 & 4 & 3 & 6 & 5 & 7 \\ 0 & 0 & 1 & 2 & 3 & 4 & 5 & 6 & 8 \\ 0 & 0 & X & X & X & X & X & X & X \end{pmatrix} \tag{26}$$

$$\begin{aligned} \boldsymbol{G} &= (g \quad \bar{g} \quad g \quad \bar{g} \quad g \quad \bar{g} \quad g \quad \bar{g} \quad \bar{g}) \\ \boldsymbol{G_T} &= (g \quad \bar{g} \quad F \quad F \quad F \quad F \quad F \quad F \quad M) \end{aligned} \tag{27}$$

and these arrays were used to calculate the charge $\boldsymbol{\alpha}$, and voltage-rating multipliers $\boldsymbol{\beta}$, for the capacitors and switches of the converter, which are shown in Table 6. These values can be compared against those for the traditional 8-cell ladder SC converter in Table 5.

TABLE 6
Charge/voltage-rating multipliers for a 9-cell Simplified Interleaved Ladder (SIL) SC converter, $r = 5$

	Switch S_1	**Switch S_2**	**Switch S_3**
$\boldsymbol{\alpha}$	-[1,1,1,1,1,1,1,1,-1]/2	[2,2,X,X,X,X,X,X,1/2]	[2,2,X,X,X,X,X,X,X]
$\boldsymbol{\beta}$	[1,1,2,2,2,2,2,2,1]	[1,1,X,X,X,X,X,X,1]	[1,1,X,X,X,X,X,X,X]

	Cell Capacitor	**Total normalised VA**	
		Switch	**Capacitor**
$\boldsymbol{\alpha}$	[4,4,3,3,2,2,1,1,X]/2	3.2	2.0
$\boldsymbol{\beta}$	[1,1,1,1,1,1,1,1,1,X]		
No. switches	14	**All switch $\boldsymbol{\beta} = \mathbf{1}$?**	No, but limited to 2×

Tables 6 shows that the total normalised capacitor and switch VA ratings for the SIL are the same as those for the COIL converter. Likewise, the SIL converter has approximately half the capacitor requirement of the traditional ladder circuit. However, this key saving was achieved with an additional 30% reduction in the number of switches when compared with the COIL circuit - this reduction in switches approaches 50% for converters with higher conversion ratios/number of cells. On the other hand, the voltage rating multipliers of the S_1 switches were doubled from 1 to 2 for all but the first pair of cells and the multiplexer switches. Fortunately, this factor of two increase in voltage rating remains the same for converters where more cells are used to achieve higher gains r. In these cases, such as in HVDC applications, this shortcoming may be outweighed by the simpler, modular structure of the SIL, or in low-power circuits where the lower number of gate-drives compared with the COIL would be a significant advantage. Alternatively, for unidirectional converters where S_1 is a diode, the factor of two is not a problem since two diodes are easily connected in series.

II-D. Comparison of the SIL converter with existing circuits

In terms of traditional, single-leg SC converters, the COIL/SIL circuits are direct competitors to the Cockcroft-Walton SC topology. For the same $r = 5$ conversion ratio, the Cockcroft circuit would require five cells, with overall normalised switch and capacitor VA ratings of 3.2 and 2.5 respectively. By comparison, Table 4 and 6 shows that whilst the COIL/SIL converters match the Cockcroft circuit for switch VA, they significantly improve on capacitor VA. This is achieved without the need for normalised cell 1 switch voltage ratings of $2V_{in}$, which is needed with the Cockcroft circuit.

When compared with other interleaved converters, a resonant circuit has recently been reported in [7], which has a similar topology to the SIL converter. This converter has resulted from recent work on hybridisation of SC converters, which is looking at the optimum placement of the inductor in resonant implementations of SC circuits. Hybridisation is seeking to improve soft-switching of these converters and reduce capacitor in-rush current. Whilst new topologies are being devised through this work, the new circuits are resonant combinations of the well-known traditional circuits such as Cockcroft-Walton, Dickson and Series Parallel. However, [7] presented a resonant version of a new interleaved converter, which has similarities to the SIL circuit. The newly published converter was called a *D-2L-Tank*, as shown as figure 1-(e) of [7]. The D-2L-Tank converter is shown here in canonical-cell form in Fig. 12. Comparison with the SIL converter in Fig.10 shows that the D-2L-Tank circuit is a similar topology but with 'common bottom-plate capacitors' as discussed in [7].

The $\boldsymbol{c}$ and $\boldsymbol{G_T}$ matrix definitions for a 9-cell D-2L-Tank having a voltage conversion ratio $r = 5$ are:

$$\boldsymbol{c} = \begin{pmatrix} 0 & 0 & 2 & 1 & 4 & 3 & 6 & 5 & 7 \\ 0 & 0 & X & X & X & X & X & X & 8 \\ 0 & 0 & 1 & 2 & 3 & 4 & 5 & 6 & X \end{pmatrix} \tag{28}$$

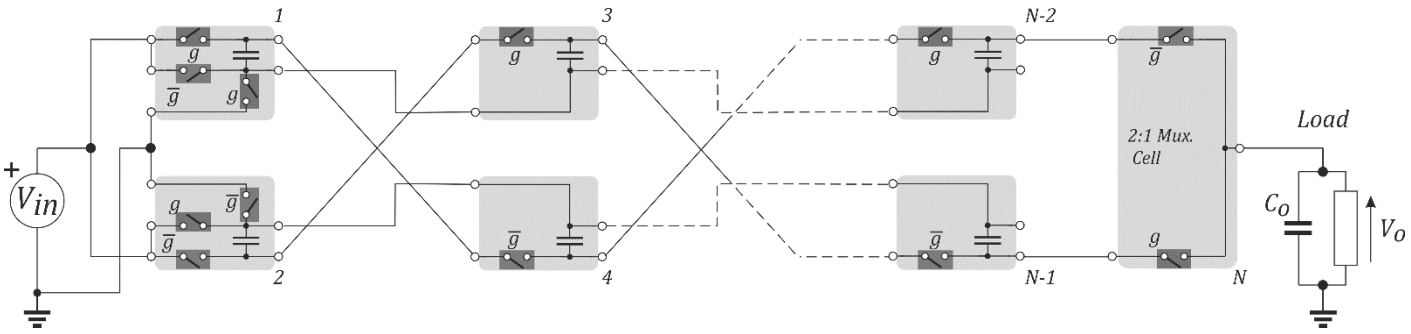

Fig. 12 D-2L-Tank SC converter [7]

$$\boldsymbol{G_T} = (g \quad \bar{g} \quad T \quad T \quad T \quad \mathrm{T} \quad \mathrm{T} \quad T \quad M) \tag{29}$$

with the $\boldsymbol{G}$ vector being the same as the SIL converter.

Using these $\boldsymbol{c}$, $\boldsymbol{G}$ and $\boldsymbol{G_T}$ arrays to calculate appraisal parameters for the D-2L-Tank shows that the parameters are almost identical to those for the SIL converter other than a difference in the capacitor charge/voltage ratings. The capacitor charge and voltage rating multipliers for the SIL and D-2L-Tank converters are shown for comparison purposes in Table 7.

TABLE 7
Charge/voltage-rating multipliers for the cell capacitors of a 9-cell, Simplified Interleaved Ladder (SIL) and D-2L-Tank SC converters, $r = 5$

	Simplified Interleaved Ladder (SIL)	**D-2L-Tank**
$\boldsymbol{\alpha}$	[2,2,1.5.1.5,1,1,0.5,0.5,X]	[0.5,0.5,0.5.0.5,0.5,0.5,0.5,0.5,X]
$\boldsymbol{\beta}$	[1,1,1,1,1,1,1,1,X]	[1,1,2,2,3,3,4,4,X]

Table 7 shows that the SIL converter has a significant advantage over the D-2L-Tank circuit in that its cell capacitors all have the same voltage rating, which is equal to the low-side supply voltage. This is very important for MV/HV applications such as photovoltaic farms and HVDC transmission links, where the voltage ratings of individual film capacitor are limited. If the D-2L-Tank converter were to be used for these applications, it would need series-connected capacitors, which entails costly and lossy voltage balancing networks.

Another use of the computer algorithm proposed here is the insight given into how the D-2L-Tank circuit is synthesised as no information was given in [7] other than a statement that it was based on the Dickson topology. Whilst this statement was unqualified, the claim conflicts with the findings stated in the previous Section II of this paper, in that the interleaving algorithm found the Dickson circuit did not offer any opportunities for capacitor/switch reduction. An intermediate version of the D-2L-Tank, that has capacitor reduction only and no switch reduction, was published beforehand [16] and refers to its origins as being what was termed an Intermediate Ladder/Dickson topology or Stacked Ladder in [17].

To investigate further, the interleaving algorithm was applied in reverse such that it was used to search for single-leg topologies that when interleaved, would produce the D-2L-Tank circuit. For a 6-cell converter this investigation revealed that there were 32 single-leg, candidate solutions that would generate the D-2L-Tank. Most of these circuits had no regular form; however, one circuit was identified as the Stacked Ladder from [17]. More importantly a pure Ladder based circuit was also located by the algorithm, which is shown in Fig. 13.

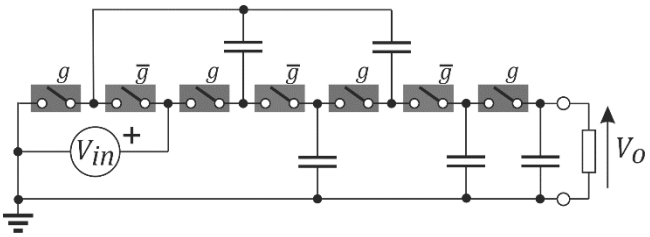

Fig. 13 Ladder based converter with common bottom-plate capacitors

Comparison of the Ladder converter of Fig. 13 with the traditional Ladder converter shown in Fig. 8 reveals that this circuit is a common bottom-plate capacitor implementation of the traditional Ladder converter. Therefore, contrary to [7], it would be more appropriate to say that the D-2L-Tank is derived from a Ladder circuit rather than from a Dickson circuit. It might be argued from [7] that D-2L-Tank owes its origins to a Dickson circuit because it can also be derived from the intermediate Ladder/Dickson of [17]. However, as an intermediate topology it is neither one or the other, and so again, a derivation from the pure Ladder of Fig. 13 is a less ambiguous statement.

In addition, [7] goes on to propose that Dickson circuits should be defined as those with a common bottom-plate capacitor; however, this is inconsistent with findings here in that the circuit shown in Fig. 13 which has common bottom-plate capacitors, is Ladder based.

It should be noted that the Ladder based circuit of Fig. 13 was recently discussed by Hu et-al for use as a Hybrid SC Buck converter for computer memory module applications [18], [19]. As a non-hybrid SC converter, it holds no particular merits and hence may have been overlooked as a candidate for interleaving through a manual process. However, it was rapidly identified by the computer algorithm described in this paper as the basis for the useful, recently published D-2L-Tank converter.

II-E. Resonant Implementation of Interleaved Converters

The resonant version of an SC converter requires an additional capacitor at its output to provide a voltage rather than current source output. This capacitor C_O, also provides

decoupling from the finite commutation times of the multiplexer switches. However, including this capacitor means there is an unequal resonant frequency ω_0 between the charging and discharging phases during a switching period. During the charging phase of a cell, it is given by ω_{01},

$$\omega_{01} = \frac{1}{\sqrt{L_c C_c}} \tag{30}$$

where L_c and C_c are the cell capacitor and resonant inductor. Conversely during a discharging phase it is ω_{02},

$$\omega_{02} = \frac{1}{\sqrt{L_c C_c \left(\frac{1}{1+(4/N)(C_c/C_o)}\right)}} \tag{31}$$

The converter switching frequency should be chosen as the lesser value of ω_{01} and ω_{02} to ensure ZCS during both charging and discharging phases, which is then given by (30). This means there will be a period of discontinuous current, during each half of a switching cycle, which increases the RMS conduction losses of the converter [15]. To minimise these losses, the converter design should aim for $\omega_{02} \approx \omega_{01}$. For converters with a small number of cells, this implies $C_o > C_C$, which adds to the overall converter capacitor VA.

The use of an interleaved topology for a resonant SC converter also improves the output voltage ripple on the output capacitor C_o. The current waveform for this capacitor, located in the output sample-and-hold cell of a traditional, non-interleaved SC converter is shown in Fig. 14(a).

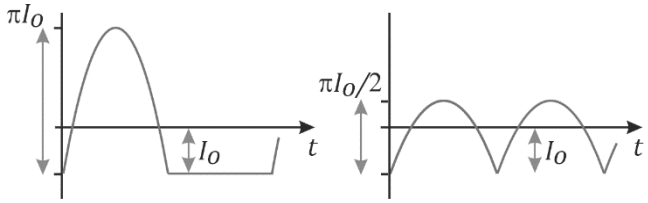

Fig. 14 Current waveforms for output capacitor C_o for a resonant switched SC converter (a) non-interleaved converter and (b) interleaved converter

The waveform consists of a half-wave sinusoid with a DC offset which is equal to the DC output current I_o, from the converter. The peak-to-peak magnitude of this current is πI_o. The current waveform for the interleaved converter is a full-wave sinusoid with DC offset I_o and is shown in Fig. 14(b). This waveform has a peak-to-peak value of is $\pi I_o/2$. It can be shown that the peak-to-peak voltage ripple for the non-interleaved and interleaved converters is respectively,

$$\frac{I_o}{\omega_{01} C_o}\left(2\sqrt{\pi^2-1} + 2\sin^{-1}\left(\frac{1}{\pi}\right) - \pi\right) \tag{32}$$

$$\frac{I_o}{\omega_{01} C_o}\left(\sqrt{\pi^2-4} + 2\sin^{-1}\left(\frac{2}{\pi}\right) - \pi\right) \tag{33}$$

The ratio of these two equations shows that the peak-to-peak ripple voltage for the interleaved converter is 5.23 times lower than that for the non- interleaved version when using the same values for I_o, C_o and ω_{01}. Similarly, it can be shown that the RMS ripple current is also lower by a factor of 2.51.

III. HARDWARE VALIDATION OF THE SIL CONVERTER

III-A. Configurable SC Converter Hardware Test Platform

A resonant implementation of the SIL converter was built as a hardware prototype to validate its operation. A resonant inductor L_j was placed in series with each cell capacitor as shown in Fig. 15. The prototype utilised existing SC resonant cell module hardware that had been developed previously to look at the effects of circuit parasitics on the converter performance. These parasitics are a particular concern for high power, high-voltage converters such as for HVDC applications, where the large size of the cell modules as well as the requirements for voltage clearance leads to a distributed rather than lumped design. This results in high levels of parasitic inductance and capacitance both within and between the cells, which causes overvoltage and current switching transients as well as detuning of the resonant circuits.

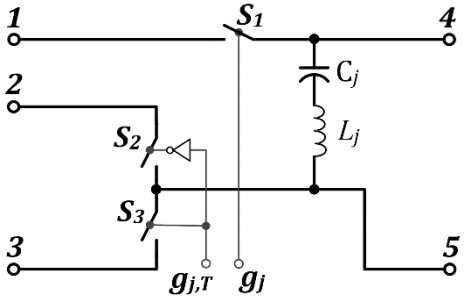

Fig. 15 Resonant implementation of the canonical cell with inductor L_j

One of the prototype cell modules, which is a unidirectional, voltage step-up cell, meaning that switch S_1 is implemented as a diode, is shown in Fig. 16. Note this hardware is a small-scale prototype; scaling is a commonly used approach in the HVDC industry for proof-of-concept and initial control design.

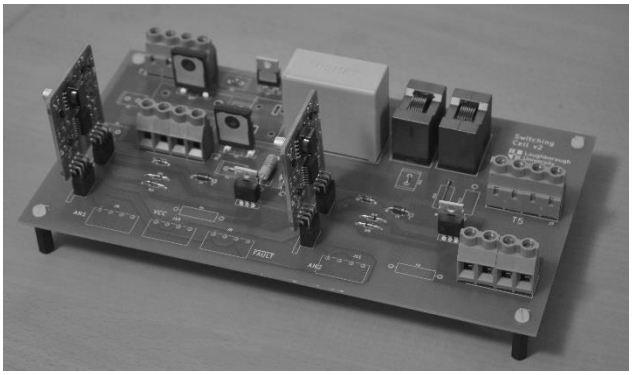

Fig.16 Prototype SC cell hardware

Fig. 16 emphasises the lengths of the PCB tracking between cell switches which have been deliberately exaggerated, to exacerbate the effects of parasitics. The parasitics result in highly oscillatory voltage waveforms with large over-voltages. This has been mitigated by adding small, passive voltage clamp circuits across the switches as shown in Fig. 17.

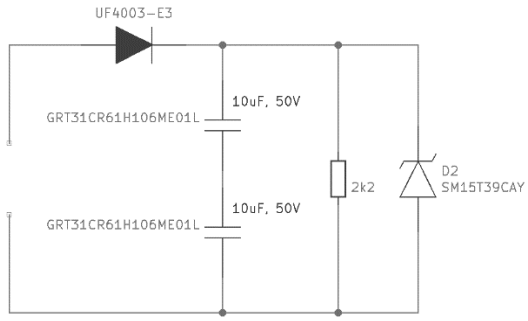

Fig. 17 Voltage clamp used to control switching voltage transients

Series connected Multi-Layer Ceramic Chip (MLCC) capacitors were used to limit overshoot across the cell switches whilst the resistor is used to dissipate the small residual energy from the transient. A Transient Voltage Suppressor (TVR) D2, is used to protect the capacitors in case of converter faults.

The SC cells used a film capacitor of $C_C = 22$ µF and a series resonant inductor $L_C = 11$ µH. The $S1$ diode was implemented as two parallel, APT100S20BG, 200V Schottky diodes. Two IPP016N08 80V MOSFETs were used for $S2$ and $S3$. The diode and MOSFET had current ratings of 120 A and 196 A respectively, much higher than was needed for the prototype tests, so that switch resistance did not dominate the damping of the resonant circuit.

III-B. Results from Prototype Measurements

Eight test-modules were connected as the 8-cell SIL converter prototype with a 150 µF film capacitor included for input DC supply decoupling. Two additional APT100S20BG diodes were used for the output multiplexer switches.

A value of $C_o = 2C_C$ was chosen for the prototype having a value of 44 µF. The switching frequency using (30) was therefore 10.23 kHz, and a value of 10.00 kHz was used to allow for component tolerances. The prototype was fed with cell gate signals generated using a low-cost ST micro-controller. A DC bench supply provided a nominal converter input voltage of $V_{in} = 40$ V, and a variable resistive load was used to draw a nominal 250 W from the converter. The converter hardware is shown in Fig. 18.

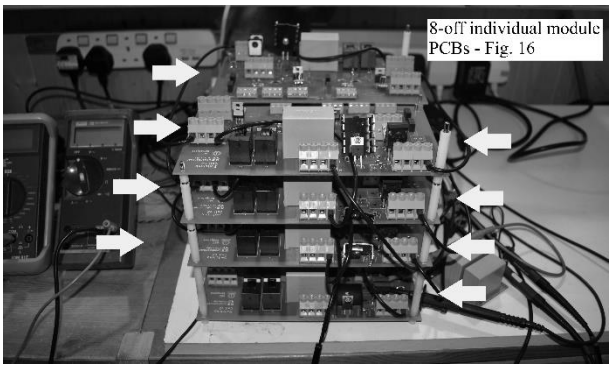

Fig. 18 Prototype SIL converter hardware using 8-off modules and Mux

The current flowing from output terminal 4 of the odd-numbered cells is shown in Fig. 19.

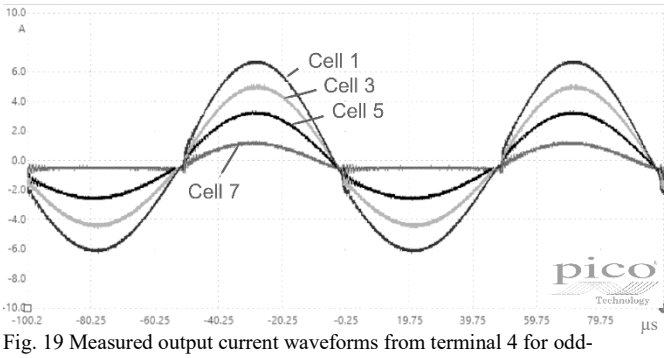

Fig. 19 Measured output current waveforms from terminal 4 for odd-numbered cells. Vertical axis: 2 A/div, time axis: 20 µs/div.

Fig. 19 shows the cell currents are close to sinusoidal for the odd-numbered cells 1, 3 and 5 and a half-wave sinusoid for the output cell 7, which provides ZCS for the cell switches.

Fig. 20 shows the switch S_1 diode voltages for the odd-numbered cells 1, 3, 5 and 7. It can be seen that simplification of the circuit by removal of switches has caused cell 3, 5 and 7 to be equal to $2V_{in} = 80$ V whereas the cell 1 voltage remains at $V_{in} = 40$ V. The voltages at inputs to the multiplexer switches, vary between $120\,V$ and the output voltage $V_o = 200$ V. Hence these switches support a voltage $V_{in} = 40$ V.

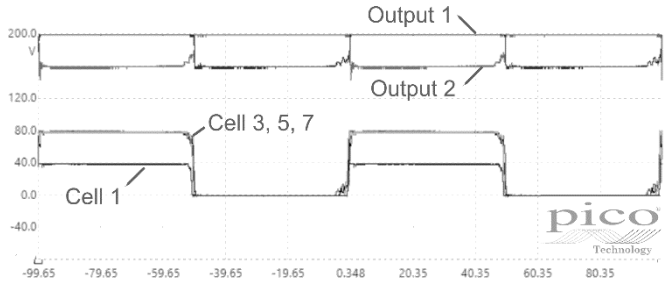

Fig. 20 Measured S_1 voltage waveforms for odd-numbered cells and mux. cell diode anode voltages Output 1 and 2. Vertical axis: 40 V/div, time axis: 20 µs/div.

The measured ripple current through the converter output capacitor C_o in Fig. 21 shows the difference in consecutive half-sinusoid waveforms that correspond to the two switching states of the converter. This is due to a small asymmetry between the two converter legs that arises from the different stray inductance of the connecting paths between the hardware modules.

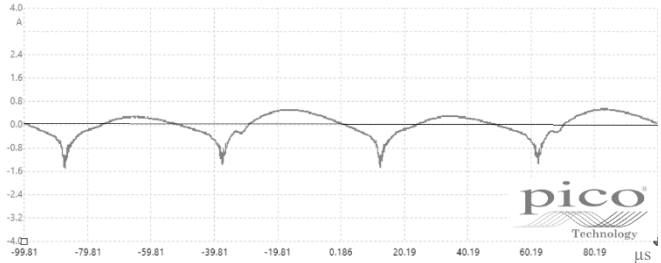

Fig. 21 Measured current through output capacitor C_o. Vertical axis: 0.8 A/div, time axis: 20 µs/div

The measured peak-peak voltage ripple was 195 mV, whereas the prediction from (33) with a measured DC output current of $I_o = 1.3$ A, gives 304 mV. This difference is expected given the distorted nature of the sinusoids in Fig. 18.

Whilst the prediction is not accurate, it is sufficient to demonstrate the much lower ripple the SIL circuit has compared with the traditional converter.

The measured output voltage and efficiency curves when the SIL is subject to a DC load variation from $90 \rightarrow 150$ W are shown in Fig. 22.

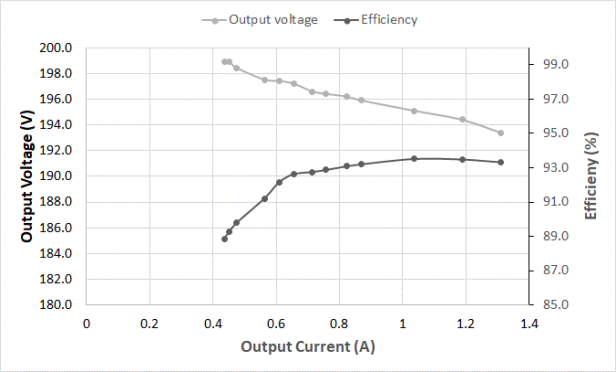

Fig. 22 Measured converter output voltage (V – blue curve ▲) and efficiency (% - red curve ●) with a load variation from $90 \rightarrow 150$ W.

The voltage regulation curve seen in Fig 17, has the expected linear droop characteristic that is common with SC converters. The maximum efficiency of 93 % is not high and is due to the use of hardware that is not tailored to this converter prototype; however, a demonstration of high efficiency was not main the objective of this exercise.

If the hardware were to be configured as a traditional ladder converter with the same number of cells and hence the same conversion ratio, $r = 5$, the increased capacitor VA rating from 2.0 to 3.7, would equate to 1.85 times higher installed capacitance. For a practical implementation, every cell capacitor used in the SIL converter would have to be implemented as two parallel connected capacitors for the traditional ladder circuit. Whilst the impact would be modest for the prototype used here, for medium to high power, MV/HV applications, the associated size, cost and weight of the DC film capacitor would be significant, as can be appreciated from today's multi-modular converters (MMC) used for HVDC links.

IV. Conclusions

A synthesis technique of using interleaved, unipolar SC converters followed by circuit reduction has been presented in this paper. The technique has been developed so that it is suitable for implementation as a computer algorithm and can be used to explore the many billions of combinations of SC circuits that are possible even with a small number of cells.

The method searches for the equipotential nodes that may arise between the two parallel legs of an interleaved converter. In some cases, connecting these nodes leads to the redundancy of converter switches or capacitors, which can then be removed from the circuit. If switch reduction is possible, the examples in this paper show that converter schematics will have diagonal branch connections between the legs.

The technique was applied to a small subset of seven traditional SC converters, where it was found that only the doubler and ladder circuits led to circuit reduction. The interleaved doubler circuit was used as an example to describe the development of the interleaving algorithm. This creates a topology that had already been described in [13]. However, subsequent application of the method to the Ladder circuit leads to the Capacitor Optimised Interleaved Ladder (COIL) and Simplified Interleaved Ladder (SIL) topologies. These two circuits have a significantly lower overall capacitor VA rating than competing topologies. The SIL converter has many fewer switches than the COIL circuit, but this is achieved with a doubling of the switch 1 voltage ratings. However, this increased switch rating is not a significant problem for unidirectional converters, where switch 1 will be a diode, which can be easily implemented as two series devices.

A detailed comparison of the SIL converter against the recently published D-2L-Tank shows that it has significant advantages in the implementation of the cell capacitor for MV/HV applications. This work also showed that the D-2L-Tank should be classified as a ladder-based topology rather than Dickson as suggested elsewhere.

The paper also demonstrates that interleaved topologies lead to a significant reduction in the output capacitor C_o, that is needed in resonant converter implementations.

A 250 W hardware prototype with 40:200 voltage step-up ratio was used to demonstrate the operation of the SIL circuit and showed that the converter operated as expected.

Since the method is easily computerised, the next steps will be to apply it beyond the small subset of traditional topologies used here and early results are revealing unique circuits, which have no foundation in the traditional converters.

Currently the technique will work with any conceivable unipolar SC converter topology, which are those having a grounded load. However, it can also be extended to bipolar arrangements, where the two legs provide a positive and negative output, giving a doubling of the voltage conversion ratio r. It is anticipated that this process will lead to the synthesis of a Symmetric MMSCC converter [20], which is expected to produce other favourable, new topologies. These new MMSCC converters as well as the new unipolar circuits that are now being discovered will be the subject of a future paper.

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References

[1] F. H. Khan and L. M. Tolbert, "A Multilevel Modular Capacitor-Clamped DC–DC Converter," *IEEE Trans. Industry Applications*, vol. 43, no. 6, pp. 1628-1638, Nov 2007.

[2] M. Forouzesh, Y. P. Siwakoti, S. A. Gorji, F. Blaabjerg and B. Lehman, "Step-Up DC–DC Converters: A Comprehensive Review of Voltage-Boosting Techniques, Topologies, and Applications," *IEEE Transactions on Power Electronics*, vol. 32, no. 12, pp. 9143-9178, Dec. 2017.

[3] H.Taghizadeh, A.M.Cross, R.Whitehouse, and C.Barker, "An Algorithm for Automatically Calculating Component Current Ratings in Switched-Capacitor DC-DC Converters," *IEEE Access*, vol. 6, pp. 15702-15712, Feb 2018.

[4] M. D. Seeman and S. R. Sanders, "Analysis and optimization of switched-capacitor DC-DC converters" *IEEE Trans. Power Electronics*, vol. 23, no. 2, pp. 841851, Mar. 2008.

[5] H. Taghizadeh, A. Cross and N. Narayanan-Kuruveettil, "Auto-Appraisal of Voltage Rating for Switched-Capacitor DC-DC Converters," *The 10th International Conference on Power Electronics, Machines and Drives (PEMD 2020)*, 2020, pp. 176-181.

[6] M. D. Seeman, "A Design Methodology for Switched-Capacitor DC-DC Converters", Technical Report No. UCB/EECS-2009-78, Electrical Engineering and Computer Sciences, University of California at Berkeley, May 2009, pp. 64-66.

[7] N. M. Ellis, R. Amirtharajah, "Large Signal Analysis on Variations of the Hybridized Dickson Switched-Capacitor Converter," *IEEE Transactions on Power Electronics*, vol. 37, no. 12, pp. 15005-15019, Dec. 2022.

[8] M. S. Makowski and D. Maksimovic, ``Performance limits of switched-capacitor DC-DC converters," *Proc. Rec. 26th Annu. IEEE Power Electron. Spec. Conf. (PESC)*, vol. 2. Jun. 1995, pp. 1215-1221.

[9] P. H. McLaughlin, J. S. Rentmeister, M. H. Kiani and J. T. Stauth, "Analysis and Comparison of Hybrid-Resonant Switched-Capacitor DC–DC Converters With Passive Component Size Constraints," *in IEEE Trans. on Power Electronics*, vol. 36, no. 3, pp. 3111-3125, March 2021.

[10] D. Ø. Larsen, M. Vinter and I. Jørgensen, "Systematic Synthesis of Step-Down Switched-Capacitor Power Converter Topologies," *in IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 66, no. 5, pp. 863-867, May 2019.

[11] R. Karadi, "Methodology and Algorithm for Synthesis of Multi-Phase Switched-Capacitor Power Converter Topologies" *2020 IEEE 21st Workshop on Control & Modeling for Power Electronics*, 2020, pp. 1-8.

[12] Fan Zhang, F. Z. Peng and Zhaoming Qian, "Study of the multilevel converters in DC-DC applications," 2004 IEEE 35th Annual Power Electronics Specialists Conference (IEEE Cat. No.04CH37551), Aachen, Germany, 2004, pp. 1702-1706 Vol.2.

[13] R. A. Cernea, "Charge pump circuit with exponential multiplication," U.S. patent 5,436,587, 25 July 1995.

[14] T. Tanzawa, "Innovation of Switched-Capacitor Voltage Multiplier: Part 1: A Brief History," *IEEE Solid-State Circuits Magazine*, vol. 8, no. 1, pp. 51-59, Winter 2016.

[15] Nakul Narayanan K., L. Umanand, A. Cross and H. Taghizadeh, "A Lumped, Resonant Switched Capacitor Converter," *IECON 2021 – 47th Annual Conference of IEEE Industrial Electronics Society*, pp. 1-6, 2021.

[16] P. H. McLaughlin, P. Aung Kyaw, M. H. Kiani, C. R. Sullivan and J. T. Stauth, "Two-Phase Interleaved Resonant Switched-Capacitor DC-DC Converter with Coupled Inductors and Custom LC Resonator" *IEEE Applied Power Electronics Conference and Exposition (APEC)*, pp. 37-44, March 2019

[17] Y. Li, J. Chen, M. John, R. Liou and S. R. Sanders, "Resonant switched capacitor stacked topology enabling high DC-DC voltage conversion ratios and efficient wide range regulation" *2016 IEEE Energy Conversion Congress and Exposition (ECCE)*, pp. 1-7, 2016.

[18] T. Hu, M. Huang, R. P. Martins and Y. Lu, "A 12-to-1 V Quad-Output Switched-Capacitor Buck Converter With Shared DC Capacitors," IEEE Journal of Solid-State Circuits, pp. 1-11, Aug. 2023.

[19] "Switched Capacitor Integrated Buck (SCIB) Power Converter Reference Design.", Texas Instruments Test Report: PMP22510.

[20] Q. Wei, C. Dong, J. G. Cintron-Rivera, M. Gebben, D. Wey, and P. Fang Zheng, "A Switched-Capacitor DC-DC Converter With High Voltage Gain and Reduced Component Rating and Count," *IEEE Transactions on Industry Applications*, vol. 48, pp. 1397-1406, 2012.