Repurposable Hardware in Smart Photonic Components

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Abstract. Key to the development of cost effective integrated components is low cost, low power circuitry capable of being repurposed from providing manufacturing based functions, such as characterisation and calibration, to operational control functions. Although these individual functions are well known, efficient and low cost implementations are required to enable competitive module pricing. In the case of an optical Mach Zehnder Modulator (MZM), bias currents require complex control functions, for example based around digitally synthesized sinusoidal pilot tones and harmonic detection via filters [1][2].

Control methods making use of calibrated laboratory equipment have been proposed [2], whereas here we consider the practical adoption of these methods with low cost and low power components which could be readily integrated into an optical module. In particular we investigate the behaviour and capabilities required for automatic digital bias control functionality implemented in a small gate count, low cost Field Programmable Gate Array (FPGA) when used in conjunction with a MZM. We assess the suitability of highly efficient implementations of DSP functions within the bias controller, such as digital filters, for example investigating the use of a computationally efficient algorithm for computing a single component of a discrete Fourier transform [3], and demonstrate the viability of using low cost digital hardware to implement a circuit capable of monitoring the MZM transfer function.

The concept of creating cost effective, repurposable hardware is crucial for implementation and inclusion in optical devices deployed in communications networks and beyond.

1. Introduction:

1.1. Theory of operation:

The MZM provides a means of controlling the amplitude of an optical wave. In the device an input waveguide is split into two equal arms via a Y junction. If a voltage is applied across one of the arms an electric field is generated across that arm which varies the refractive index of the substrate material and thereby introduces a phase shift in the optical wave passing through it. When the two arms are then recombined the phase shift between them is converted into an amplitude difference. If there is no phase difference then the optical waves in the two arms combine constructively and maximum output

is seen. If the two arms are in complete antiphase then the waves combine destructively and a minimum output is seen. The difference in the voltage applied for no phase shift and the voltage required for a phase shift of π is referred to as the ½ - wave voltage or $V\pi$.

The basic transfer function of the modulator, when driven by a single time dependent voltage *v(t)*, is

$$I_{OUT}(t) \propto \frac{I_{In}}{2}\left[1 + \cos\left(\frac{\pi v(t)}{V_\pi}\right)\right]$$

where

$I_{OUT}(t)$ is the output Optical Intensity,

I_{In} is the input Optical Intensity
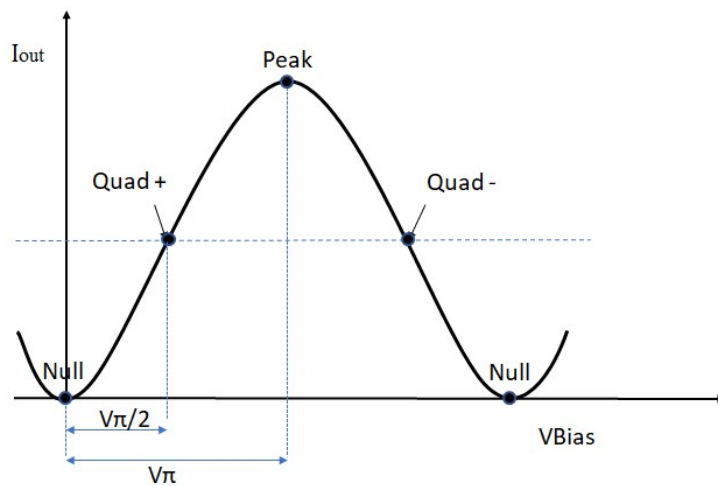
and is plotted in Figure 1.

Figure 1 Transfer function of a Mach Zehnder Modulator showing the key operating points

Analysis of the transfer function using Bessel functions [2] has shown that operating at odd integer multiples of $V\pi/2$, i.e. quadrature points, forces even order harmonic distortion terms to be zero while operating at integer multiples of $V\pi$ (peak/null bias points) forces the odd order harmonic terms including the fundamental to be zero. Furthermore it has been calculated ([4] Section IV) that the amplitude of the 2nd harmonic of a pilot tone applied to the bias input electrode of a modulator is directly proportional to the 2nd derivative of the optical output power.

Bias control algorithms tend to fall into two categories – dither (applying a low frequency pilot tone whose modulation depth is expressed as a % of $V\pi$) and ratiometric (based on a characterised input to output power ratio), and the pros and cons of each method are widely discussed in the literature [6][7][8].

A dither-based approach to maintain a bias point, where either primary or 2nd order distortion is zero, is to add a low frequency sinusoid to the bias electrode. This moves the bias point causing harmonics of the dither frequency to appear on the modulated optical signal, so if a bias point where the 2nd harmonic distortion is zero (quadrature point) is required, the dither frequency 2nd

harmonic should be detected and using a feedback loop the bias should be adjusted until the 2nd harmonic is at a minimum. Conversely to operate at a point where the primary is zero (peak or null) the dither frequency should be detected and the bias voltage should be adjusted to minimise the signal power at the dither frequency [2]. When using this approach it is necessary to have correctly characterised the modulator first in order to determine a suitable starting value for the control loop.

It should be noted that the use of a dither frequency can enable a high degree of precision in the bias point control but the presence of a dither signal may not be tolerable in the end application (analogue, RF over Fibre, othogonal frequency division multiplexing) due to the presence of intermodulation products [6].

The dither based approach consists of a local oscillator or other source, for example an FPGA or microcontroller for digital frequency synthesis, which generates a low-frequency pilot tone, normally in the kHz range, and a single fiber-optic coupler that taps a small percentage of the MZM's optical output power and feeds it to a single photodetector. From a manufacturing perspective it can be seen that this pilot tone-type bias controller will cost less to assemble than a ratiometric-type controller, because it requires only one tap coupler, which does not operate in polarization-maintaining fibre; it requires only one photodetector in the control circuit; and the proper feedback circuit settings do not depend on the specific performance parameters of the modulator, tap coupler, or photodetector.

2. Experimental Setup:

In [2] bias control methods using harmonic analysis are examined using calibrated laboratory equipment. The question then is whether it is practical to adopt this method with commercially available, low cost and low power components which could be integrated into an optical module.

The purpose of this experimental activity was therefore to validate the behaviour of such a control system when implemented using low cost components and computationally efficient algorithms. To this end it was proposed to digitally generate a 4 kHz pilot tone to be applied to the DC electrode of a MZM while applying digital pseudo random (PRBS) traffic at 10 Gbps to the RF electrode, and examine the performance of digital filters based on the algorithm described in [3] when determining the presence and absence of the applied pilot tone and its 2nd harmonic. To carry out these investigations the experimental setup shown in Figure 2 was implemented.

The analogue electronics (Filters, photo diode (PD)), digital components (FPGA, ADC, DAC) and user interface blocks (USB) were implemented on a custom designed circuit board by TerOpta Ltd. The optical components were connected together on the workbench. A LiNbO$_3$ MZM (JDSU OC192) was connected to a 10 Gbs Anritsu Data source generating a PRBS31 sequence, through a JDSU H301 modulator data driver. The laser source used was a C Band tuneable Oclaro laser set to 1554.98 nm and using a launch power of 10 dBm.

The amplitude of the pilot tone was set to 75 mV peak to peak which equals 1% of the bias electrode V$_\pi$ for this MZM. Increasing this value may be beneficial in the short term if the pilot tone harmonic method is only to be used during characterisation of the device; however, as stated previously, it may not be desirable if a pilot tone control method is to be employed [5]. As discussed in [7], the effect of the pilot tone is not only due to the amplitude of the applied electrical signal but also to the intensity of the optical signal at the receiver; this can be adjusted by changing the percentage of the optical signal routed to the controller through the tap coupler. In this experiment a 5% tap was used together with an attenuator to limit the optical signal at the controller anti-aliasing filter to -18 dBm.
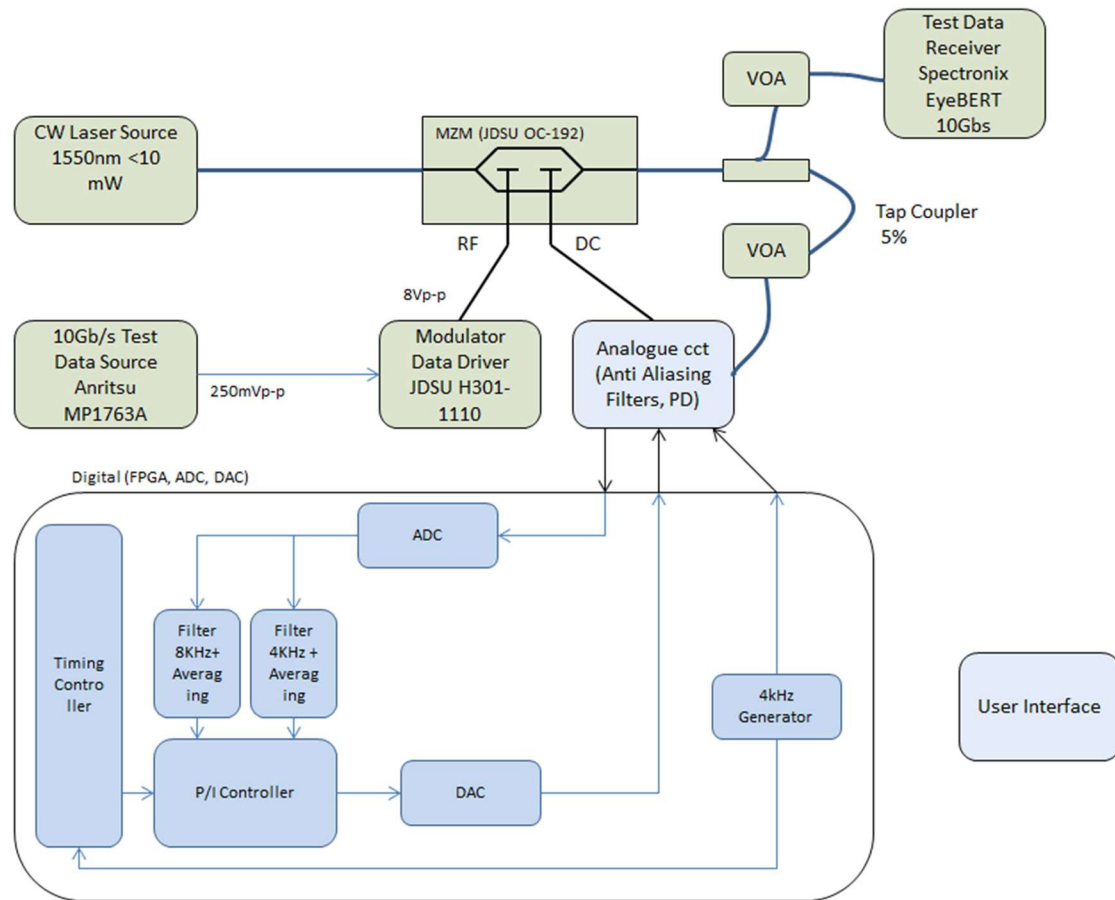
Figure 2: Experimental setup

      In keeping with the target of demonstrating practical repurposable hardware, the FPGA used was a low cost, low power MAX10™ device from Intel. This has a small number of DSP specific macrocells capable of performing multiplication and accumulation actions so the filter algorithm has been chosen for efficiency. The design itself was implemented using the hardware description language VHDL using Intel's Quartus Prime development tools. The implementation of the filter has been adapted to the proposed FPGA platform whilst aiming to achieve the best possible accuracy. To test the effectiveness of the filter implementation a VHDL simulation was performed and the result compared with that predicted by calculation.

2.1. Filter Implementation

Using a filter based on Goertzel's algorithm it is possible to perform tone detection using fewer computational resources than an equivalent Fast Fourier Transform or a traditional FIR or IIR filter architecture. Historically such filters have found uses in analogue electrical telephony e.g. dual tone multi frequency (DTMF) detection where a small set of discrete, orthogonal tones are used in pairs to indicate key presses on a telephone line.

      When implementing the Goertzel algorithm the processing is performed on blocks of data, however, as the numerical calculations are very simple, and as FPGAs are fast and inherently parallel by design, it is not necessary to store all the samples in a block before computing the result. Three parameters are required to be defined, the sample rate, the block size and a pair of precomputed

coefficients (one sine the other cosine). In this experiment, this is reduced further as only the cosine term is used.

The usual Nyquist rules are applied to setting the sampling rate. Ideally the frequencies of interest need to be integer factors of the sample rate. In this case the sample rate was also determined by the available sample rates of the on chip ADC function in the FPGA. The Block size controls the bin width or frequency resolution and is analogous to the number of points in an equivalent FFT. For the frequencies of interest to be centred in their respective filters they need to be integer multiples of the value of sample rate/block size.

Finally, as discussed in [9], we can calculate:

$$k = (int)(0.5 + \frac{\text{Block Size} * \text{Target Frequency}}{\text{sample rate}})$$

then

$$w = (2*\pi/N)*k$$
$$\text{cosine} = \cos w$$
$$\text{sine} = \sin w$$
$$\text{coeff} = 2 * \text{cosine}.$$

In this experiment a 4 kHz sine wave was used as the fundamental pilot tone giving the following parameters:
    Block Size: 1500 samples
    Sample Rate: 20 kHz
producing calculated cosine terms of 0.309021 for the fundamental tone filter and -0.809021 for the second harmonic filter.

When implementing the filter a three stage pipeline is defined: Q0, Q1, and Q2 (see Figure 3). For every input sample the following three equations are calculated:
$$Q0 = \text{coeff} * Q1 - Q2 + \text{sample}$$
$$Q1 = Q0$$
$$Q2 = Q1.$$
After running the per-sample equations for the whole block, the results are calculated as follows:
$$\text{real} = (Q1 - Q2 * \text{cosine})$$
$$\text{imaginary} = (Q2 * \text{sine})$$
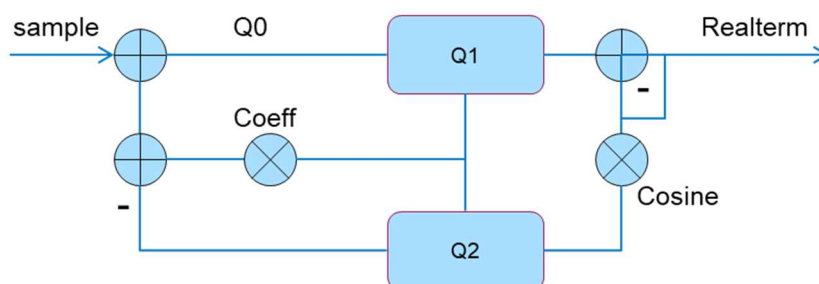$$\text{magnitude}^2 = \text{real}^2 + \text{imaginary}^2$$

Figure 3: Filter implementation showing relationship of Q0, 1, 2, Coeff and Cosine (as defined in equations above)

Implementing a filter using this method, with a 13 Hz bandwidth centred on the target frequency, requires very few resources when compared with traditional IIR and FIR designs. Using MatLab to generate comparable functions shows the complexity of an equivalent FIR implementation would be greater than 6500th order, whereas an IIR implementation would be 11 x 2nd order sections. These would both involve the calculation and storage of many coefficients and the implementation of potentially large logic trees in the FPGA in order to realise the filter. The implemented filter requires by comparison, 2 coefficients (1 Sine, 1 Cosine implemented as 16 bit signed fixed point numbers). As only the real term was evaluated, and the value coeff equals 2x cosine term, it was only necessary to hardcode a single coefficient, further reducing complexity and FPGA resource use. By using only the real term we see a positive and negative answer from the filter which can be used to indicate the direction in which the closed loop controller should move the bias voltage. This was implemented using 457 look up tables, 286 single bit storage elements (DFF's) and 4 DSP slices in the MAX10 FPGA.

Fixed point arithmetic was used throughout using a 16 bit representation of the fractional part of the numbers and a single multiplier stage (35x17 bit signed). The representation of the Cosine term in this format gave an approximation which was correct to better than 5 decimal places.

3. Results:

A coarse voltage sweep on the DC electrode was performed using the hardware model. The applied DC Bias voltage DAC was varied across its range representing -10V to +10V in small discrete steps, that voltage was then held for 100 seconds. At each step the output power, filter outputs and averaged filter outputs, calculated using an exponentially weighted moving average (EWMA) were recorded at 1 second intervals. The results are presented below as a plot of bias voltage vs stated parameter (Figures 4 to 6). The vertical movement at each bias point represents the variation due to observed noise in the readings.

Figure 4 shows the combined results of the sweep, plotting the applied DC bias voltage in mV (BiasmV) and the calculated real terms from the 4 kHz and 8 kHz filters with EWMA applied against time. The optical power is also represented as the sampled ADC reading (OPMon) taken of the photodiode. This chart confirms that the response of the circuit agrees with theory in that the 4 kHz filter response is at a maxima or minima when optical power is at a maximum which is when the MZM is at quadrature. The 8 kHz filter response is showing a DC offset, however, the minima and maxima of the 8 kHz response correspond to minimum optical power which is seen when operating at the Peak or Null points of the MZM transfer function.

In Figures 5 and 6, the two filter responses are shown separately as a plot of the recorded output from the FPGA implemented filter directly against the applied DC bias voltage in mV. The height of each vertical bar plotted shows the range of the results recorded at that voltage. It can be seen that the filter centred on the pilot tone fundamental frequency of 4 kHz exhibited a strong response with large amplitude and relatively little variation, whereas the 2nd harmonic filter centred on 8 kHz produced a much weaker, less distinct result. Although it is expected from theory that the 2nd harmonic will be of considerably lower amplitude than the fundamental, the large variation in the filter output has been determined to be predominantly due to interference from electrical noise introduced by switching convertors and digital circuitry on the test board. In order to improve the 8 kHz filter response by allowing for a greater analogue gain to be applied to the feedback signal, an internal attenuation was required to be applied digitally, in the FPGA, on the input to the 4 kHz filter so as to prevent saturation. This analogue gain also emphasised any noise present in the detector chain or on the optical signal from elsewhere in the system. Even in the presence of this noise the output of this

resource efficient filter implementation still clearly demonstrates the predicted sinusoidal response of the pilot tone fundamental (Figure 5) and 2nd harmonic (Figure 6) amplitudes as a sweep across the MZM transfer function is performed.
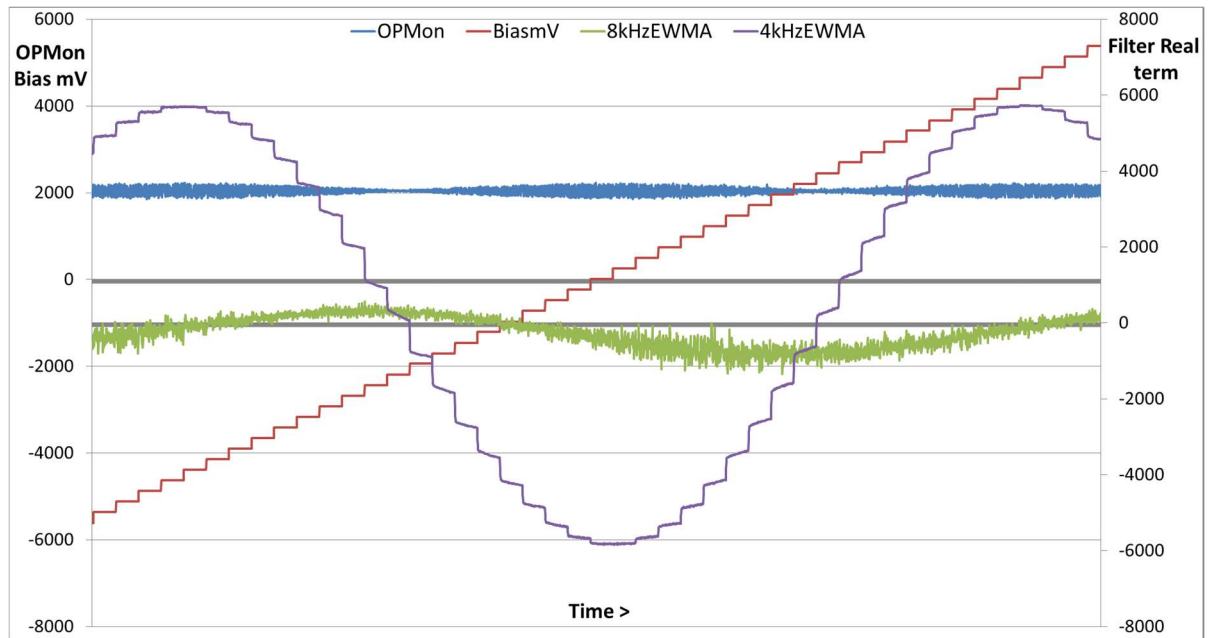

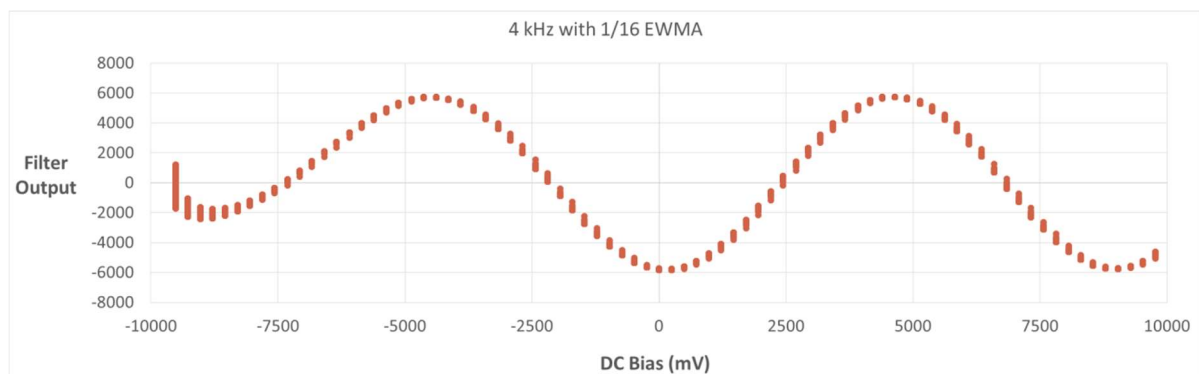**Figure 4: Filter outputs (4kHzEWMA and 8kHzEWMA) and optical power (OPMon) vs Applied bias voltage (BiasmV)**

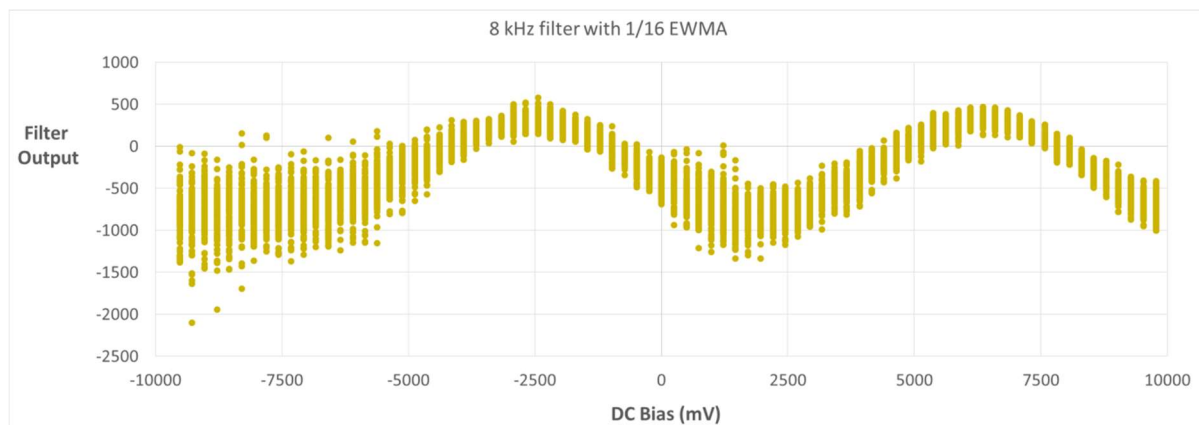**Figure 5: Fundamental frequency filter output with averaging vs Bias voltage**

Figure 6: 2nd harmonic frequency filter output with averaging vs Bias voltage

4. Conclusion:

This experimental work has demonstrated the viability of using low cost digital hardware to implement a circuit capable of monitoring the transfer function of a Mach Zehnder Modulator. Specifically of note is that this is the first reported use of efficient Goertzel algorithm based filters in this MZM application. The possibility of creating small implementations of digital functions using commercially available components is key to the concept of creating repurposable hardware which is practical for implementation and inclusion in optical devices deployed in communications networks and beyond.

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