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Improved FPGA time-to-digital converter architecture to improve precision, converter linearity and reduce dead-time

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ABSTRACT

Time-to-digital converters (TDCs) and time correlated single photon counters (TCSPC) are instruments commonly used in LiDAR systems, quantum optics experiments and many other applications. This work presents a new time-to-digital converter architecture to improve dead time, converter linearity and precision.

The priority encoder is a large combinatorial logic circuit and is often the bottleneck in field programmable gate array (FPGA) TDC designs, as the conversion must complete within the TDC's clock period. This work utilizes a new dual clock domain architecture which has allowed for the TDC clock rate to increase by 38.1% from previous work and potentially double for more modern FPGA devices. This reduces the required delay line length and allows for more precise and linear converters as both integral non-linearity and measurement uncertainty scale according to the square root of the number of delay elements used in the delay line. Single shot precision has improved by 12.9% and converter differential non-linearity and integral non-linearity has reduced by 1.27 and 1.57 least significant bits respectively.

This work demonstrates a significant improvement to the performance of FPGA based TDCs at the expense of using slightly more block random access memory.

Keywords: time-to-digital converters, photon counting and time correlated single photon counting.

1. INTRODUCTION

Time-to-digital converters (TDCs) play an important role in numerous applications and systems, such as Positron Emission Tomography (PET) systems, quantum optics experiments, LiDAR, fluorescence lifetime imaging (FLIM) systems and quantum key distribution amongst many others. TDCs essentially measure the time difference between a start and stop signal, with the time difference between the signals' rising edges being of interest. In this work, there is no dedicated start signal as time differences are measured relative to when the measurement process was started. Each rising edge of a successfully measured stop signal will produce a "time stamp" which will be transferred to a personal computer (PC) for further processing and analysis.

A large number of TDC based instruments make use of application specific integrated circuits (ASICs) such as those made by AMS [1] to perform time measurements to a high precision and resolution. As such devices typically require a field programmable gate array (FPGA) to communicate time stamps to a PC, work has been undertaken [2,3,4] to implement delay line based TDCs within FPGAs. This reduces the cost and complexity of the timing instrument.

However, implementation of TDCs within FPGAs poses numerous challenges, in regard to resolution, converter linearity, precision and converter dead-time (the amount of time required after a measurement has occurred before another measurement can take place). This work proposes a change to the architecture of a typical FPGA TDC which allows for higher clock rates. In turn, this reduces dead-time, improves linearity and increases the precision of FPGA realized TDCs.

2. BACKGROUND

Most FPGA based TDCs utilize the carry chain (a linear vertical and relatively predictable signal path through the FPGA, originally intended for fast addition circuits) to create a delay line based TDC as shown in Figure 1.

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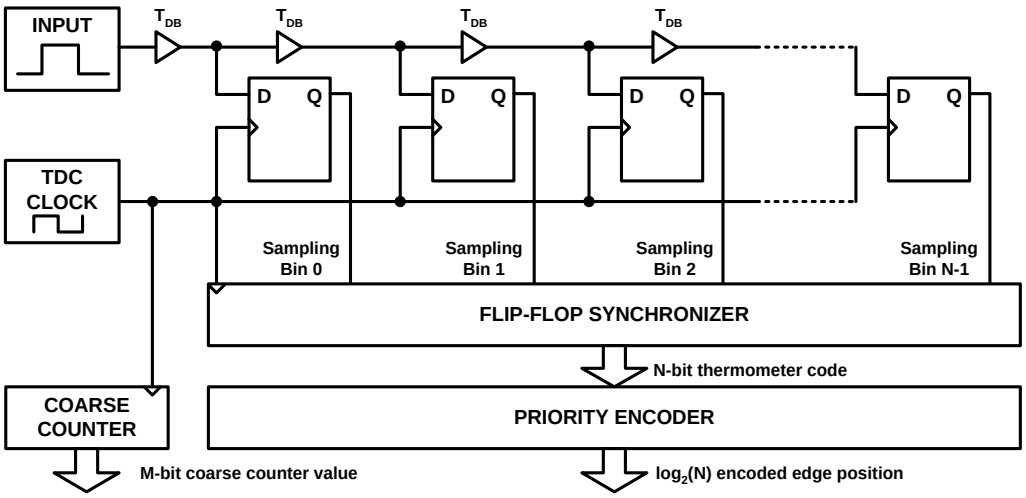


Figure 1: A simplified block diagram of a carry-chain line based TDC

The delay line can be thought as dividing the TDC's clock period up into *N* slices, allowing for the input edge position to be determined to a resolution smaller than the TDC's clock period T_{clk} [3]. In such an approach, the resolution is limited by the propagation delay between sampling flip-flops, represented in Figure 1 by buffer delay T_{DB}. The sub-clock period edge position can be utilized with a clock cycle counter known as the "coarse counter" that is *M*-bits wide to produce the time-stamp with an almost arbitrary measurement range (MR) with high resolution.

The buffer delay T_{DB} should ideally be consistent and in the FPGA it is typically created via the signal's propagation time through the carry chain to the respective sampling flip-flops. However, the propagation path is not consistent throughout the carry chain, resulting in nonlinearities in the delay line's transfer function. Previous work [4] measures and calibrates for delay line nonlinearities on-chip, allowing for time-stamps to be directly used by subsequent post-processing and analysis algorithms. Performance of FPGA delay lines is limited by a phenomena known as "ultra-wide bins", where the propagation delay between slices is typically much greater than the delay within a slice [5].

A two-stage flip-flop synchronizer is utilized after the sampling flip-flops to reduce the likelihood of metastable events being propagated throughout the rest of the digital circuitry to a negligible amount. The number of logic '1' sampled from the delay line indicates the input edges position with respect to the TDC's clock, as show in Figure 2 for a simplified case. This code of 0s and 1s with an ideally singular transition is known as a thermometer code and will be *N*-bits wide.

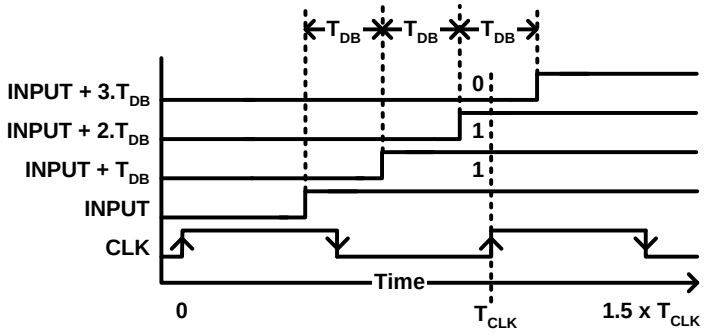


Figure 2: Example thermometer code

This *N*-bit thermometer code is then converted to a $\log_2(N)$ code using a priority encoder, which can represent all possible positions where the rising edge transition occurred. If *N* is not a power of two, padding bits are added to make the thermometer code passed to the priority encoder a power of two.

In previous work [4], the TDC's clock rate was always limited by the propagation delay throughout the priority encoder, achieving a maximum clock frequency of 131.25MHz. Another Spartan 6 based TDC [6] operates at a clock rate of 125MHz, although the priority encoder may not be the limiting factor.

The rationale behind pushing for higher TDC clock rates is threefold. Firstly, the increased clock frequency will reduce converter dead time. This will allow for single photon statistics to be more accurately measured [7]. Secondly, it has been shown that converter integral non-linearity scales in in accordance to $\sqrt{N}$ [8]. Hence, for high linearity measurements, it is imperative that the delay line is as short as possible. Finally, arrival time uncertainty also scales in accordance to $\sqrt{N}$ [8]. Hence, improving the clock frequency of TDCs is crucial, as it will allow for smaller values of *N*/shorter delay lines.

3. METHODOLOGY

The approach explored in this work is to evaluate whether the priority encoder circuit and subsequent calibration logic can use a separate, lower frequency clock domain from that of the TDC's core elements (the coarse counter and delay lines). This should allow for the TDC components to be operated at a higher frequency, which should minimize the delay line length and therefore improve precision and linearity of the TDC.

As seen below in Figure 3, a cross clock domain first in first out (FIFO) buffer is utilized to separate the TDC clock domain operating at 181.25MHz from the subsequent 48MHz domain. It is worth noting that to ensure that thermometer codes and coarse counter values are synchronized to each other, an $N + M$ bit FIFO is required such that matching thermometer and coarse counter values can be stored for later processing in the slower clock domain. In this design explored, $N = 300$ and $M = 36$, resulting in a FIFO 336-bits wide. Block RAM inside of the FPGA is utilized to create the FIFO with a depth of 16, requiring 10 9k BRAM primitives per TDC channel. Note that control logic to handle writing and reading to and from the FIFO is omitted from the diagram for clarity.

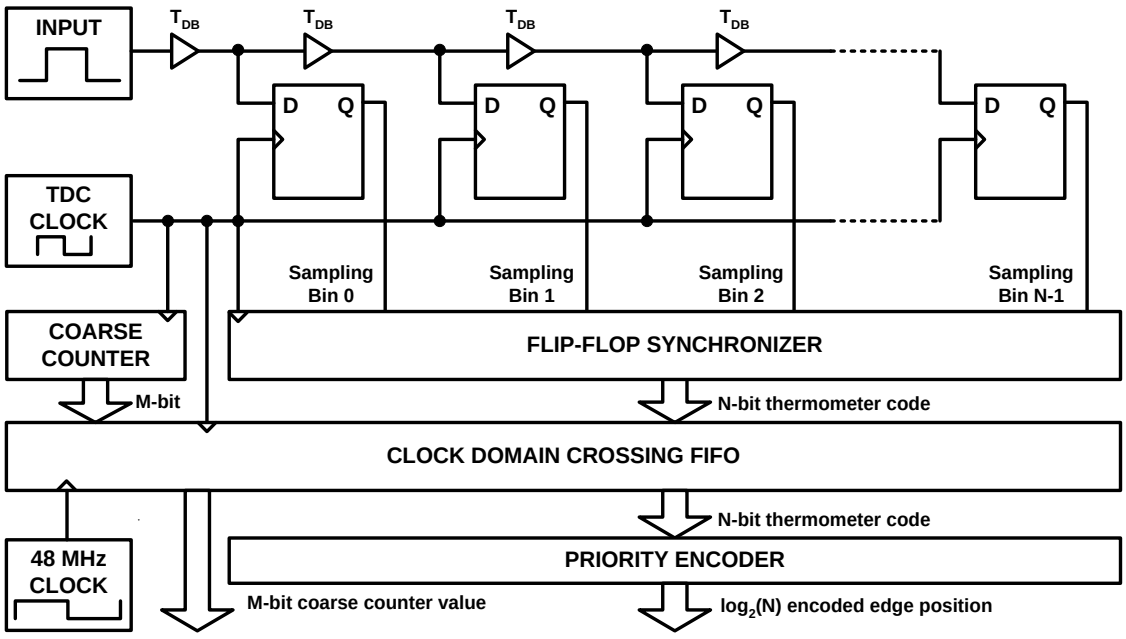


Figure 3: Simplified block diagram of the modified architecture

The 48MHz clock domain can now be utilized to perform the priority encoding and subsequent calibration processes before writing the calibrated time stamp to a channel FIFO buffer, such that time stamps can be temporally stored before transfer

to the PC. This removes the problem of trying to perform the priority encoding at the TDC clock rate and still allows for a burst TDC measurement rate of 48MHz, which is far higher than needed for typical single photon detectors.

The engineering challenge now shifts from the priority encoder to the how well the N + M-bit code can be routed to the block RAM primitives that are distributed across the FPGA. These are finite resource and are located in fixed positions across the FPGA. For the sake of comparison, the same hardware platform and experimental setup used in [4] will be used such that a fair comparison can be drawn.

4. RESULTS & DISCUSSION

The FPGA used for the evaluation of this technique is a Spartan 6 LX-150 (Opal Kelly XEM6310) module mounted on a custom PCB, as shown below in Figure 4. This PCB contains 16-input channels with 50Ω termination and software configurable constant level discriminator voltages, 8-programmable 50Ω line drivers and a 10MHz oven-controlled crystal oscillator (OCXO) and jitter attenuator to provide the TDC with a long term stable clock with low jitter. The jitter attenuator is required to minimize jitter from the Spartan 6's digital clock manager (DCM), which is used to generate the TDC's clock from the 10MHz OCXO.

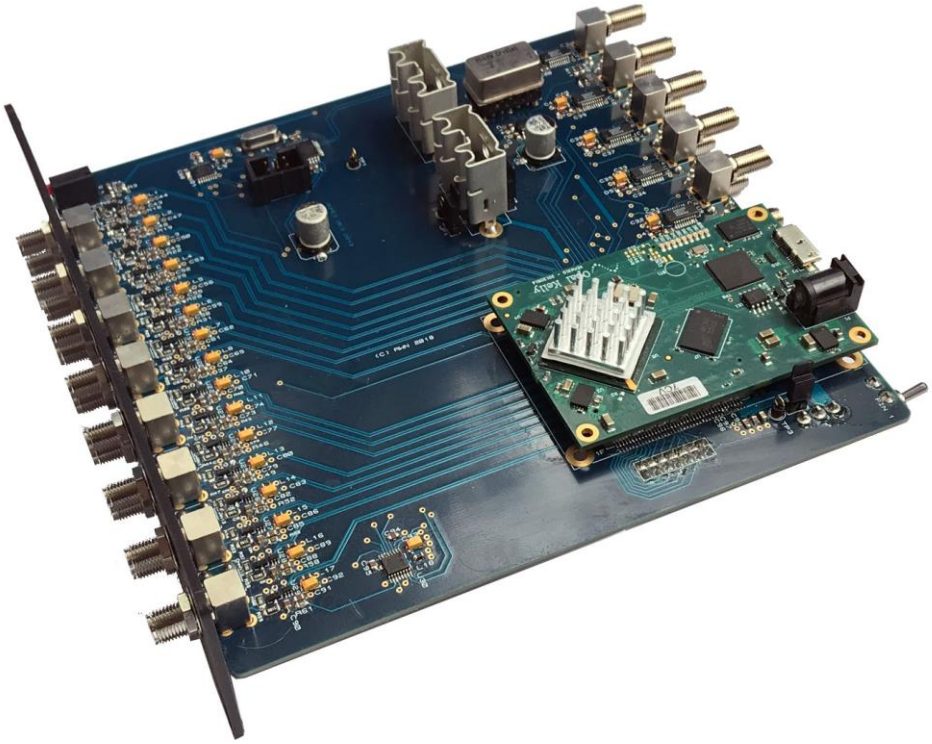
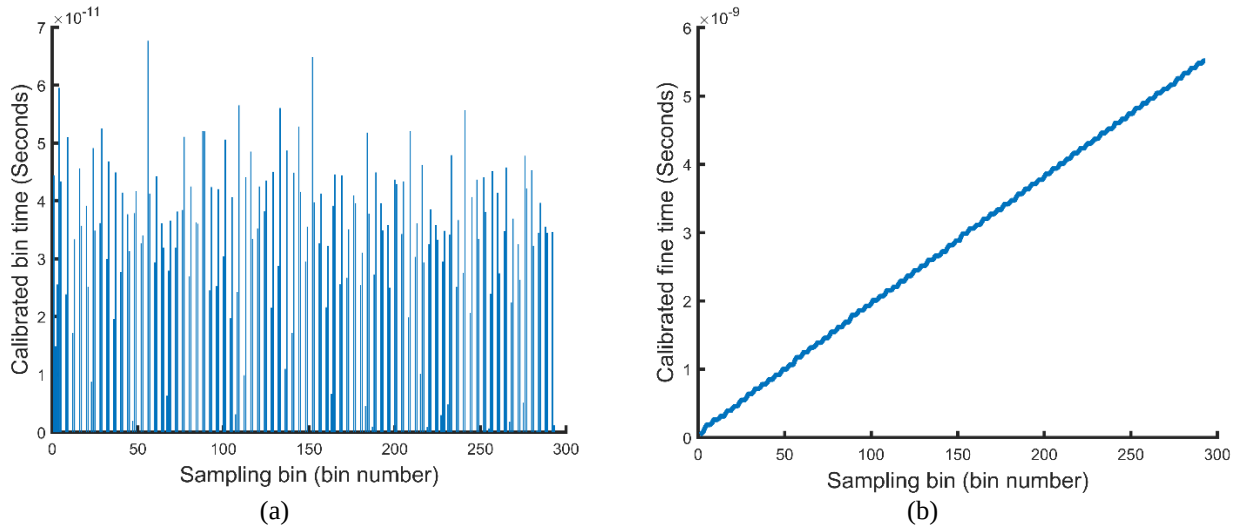


Figure 4: The Spartan 6 LX150 hardware platform used for evaluation

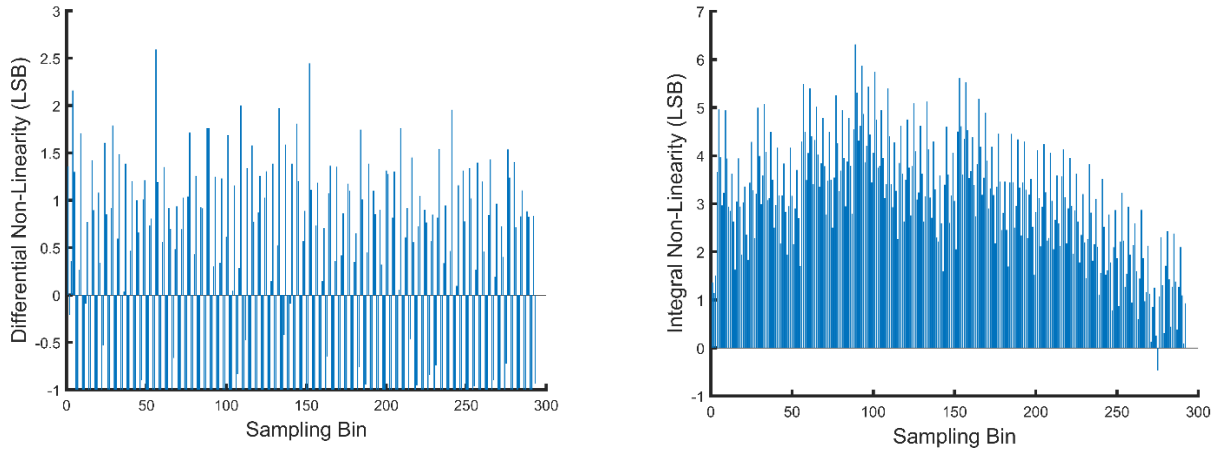
The same process discussed in [4] is utilized to statistically measure the TDC's bin sizes and transfer function, shown below in Figure 5 (a) and Figure 5 (b) respectively. With the higher clock rate, the TDC's delay line now only covers 293 bins with an average bin size or T_{DB} of 18.83ps. Note that in comparison to the previous work, the average bin size has increased, which is most likely due to the increased converter linearity and a smaller number of missing codes.



(a) (b)

Figure 5: (a) Example TDC delay line bin sizes (b) The resultant transfer function for the TDC delay line

Differential non-linearity (DNL) and integral non-linearity (INL) have been calculated from the bin-size data and it is shown in Figure 6 (a) and Figure 6 (b) respectively. The maximum DNL error experienced is 2.6 least significant bits (LSB) and maximum INL error is 6.3 LSB. This is a reduction from a DNL of 3.87 and an INL 7.87 obtained from the conventional approach in earlier work [4]. This indicates that there is merit in reducing delay line length in improving linearity. However, the speed grade (2) of the Spartan 6 LX-150 is a limiting factor in pushing TDC clock speed further. Test compilations targeting an Artix 7 XC7S100 (speed grade 2) yields possible clock frequencies in excess of 280 MHz, demonstrating the capability of the technique with more modern FPGA devices.



(a) (b)

Figure 6: (a) Differential non-linearity (DNL) for a typical delay line (b) Integral non-linearity for a typical delay line

The single shot precision (SSP) of the instrument was measured with an HP8082A pulse generator and a Mini-Circuits ZFRSC-42-S+ 50Ω splitter. The pulse generator is used to drive the splitter and the two outputs of the splitter are used to drive two channels of the TDC with essentially the same pulse, presenting a fixed and consistent delay between the two channels, essentially as close as an input delta function as possible. Subsequent to this, the time differences between the two channels are measured across a large series of time stamps and is then histogrammed. This allows for the precision of the TDC itself to be measured (SSP) and a typical SSP for the TDC developed is shown in Figure 7 with a 20ps histogram bin size.

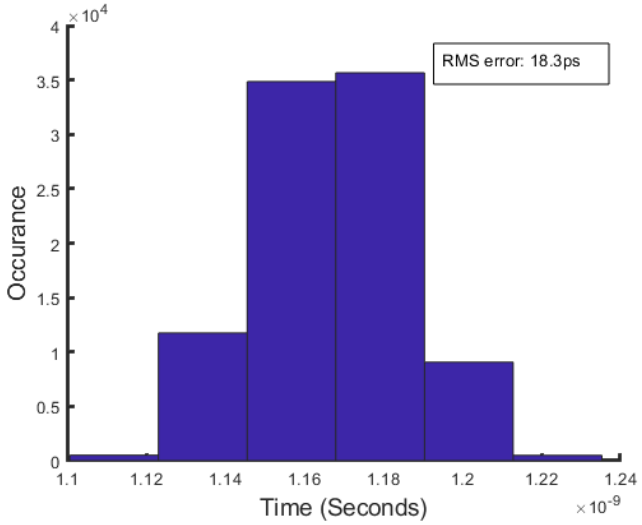


Figure 7: Typical single shot precision (SSP) for the TDC developed, measured across a pair of channels. Note the histogram has a bin size of 20ps.

The resultant time difference data exhibits an error of 18.3ps RMS or 12.95ps RMS single channel. This is an improvement of approximately 12.9% on the same hardware platform in comparison to the conventional architecture covered in [4] which achieved an SSP of 21ps RMS. This is in good accordance to the $\sqrt{N}$ scaling predicted by [8].

5. CONCLUSION

A new FPGA delay line based TDC architecture has been presented which allows for higher TDC clock rates. Previous work which operated at 131.25MHz now operates at 181.25MHz on the same hardware platform, an improvement of 38.1%. This increased clock rate is demonstrated to improve the precision of the TDC, with the SSP reducing by 12.9% in this work. Linearity is also improved, with the maximum DNL and INL reducing by 1.27 and 1.57LSB respectively. The increased clock rate also reduces converter dead time to ~11ns in this case, which has numerous benefits in photon counting applications.

This improved performance is achieved via moving the priority encoder circuitry (and subsequent calibration logic) onto a lower frequency clock domain, which in prior work has been the limiting factor for TDC clock speed. To achieve this, a FIFO buffer has been introduced into the data path to transfer thermometer codes and coarse counter values from the TDC clock domain to the slower clock domain. However, this performance increase is at the expense of slightly increased block RAM usage, with 10 additional 9k block ram primitives being required per timing channel.

Further work will look at optimising the number of thermometer bits, as it is envisaged that reducing the number of thermometer bits will allow for the TDC to logic to operate even faster.

6. ACKNOWLEDGEMENTS

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