Journal of Physics: Conference Series

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To cite this article: Yu Jia *et al* 2018 *J. Phys.: Conf. Ser.* **1052** 012097

PowerMEMS 2017 IOP Publishing
IOP Conf. Series: Journal of Physics: Conf. Series **1052** (2018) 012097 doi:10.1088/1742-6596/1052/1/012097

# Interdigitated cantilever array topology for low frequency MEMS vibration energy harvesting

**Yu Jia**[1,2], **Emmanuelle Arroyo**[1], **Sijun Du**[1] **and Ashwin Seshia**[1]
[1]Nanoscience Centre, University of Cambridge, Cambridge, CB3 0FF, UK
[2]Department of Mechanical Engineering, University of Chester, Chester CH2 4NU, UK

E-mail: `yu.jia.gb@ieee.org`

**Abstract.** Micro-fabricated vibration energy harvesters enable merits such as miniaturisation, economies of scale for manufacturing, and ease of integration with semiconductor IC technologies. However, the frequency range of ambient vibration is generally low (10's Hz to 100's Hz). Existing MEMS vibration energy harvesters that target these frequencies typically are in the centimetre scale range. This sacrifices the miniaturisation aspect as well as introducing new challenges in packaging and integration for the unconventionally large MEMS devices. This paper proposes a new interdigitated fork cantilever array topology, which allows for up to about a third reduction in resonant frequency compared to the classical cantilever topology, for the same design area and without compromising on power optimisation. Further resonant frequency reduction is also possible, but at the expense of power optimisation. This opens up design flexibility to achieve low frequency MEMS resonators that are more suitable to practically target ambient vibration, without sacrificing the aforementioned merits of MEMS technology.

## 1. Introduction

Vibration energy harvesting (VEH) holds the promise to realise a self-sustaining on-board power source for autonomous sensors and microelectronics. MEMS fabrication technology brings several benefits to miniaturisation, ease of integration with IC and economies of scale for manufacturing. Micro-cantilever topology has been widely employed for MEMS VEH due to its good power responsiveness, ease of design, minimal fabrication process complexity, and relatively low frequency [1, 2].

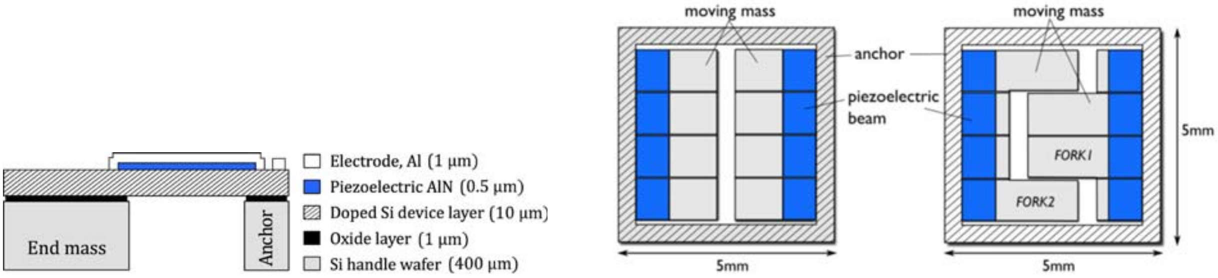
However, the dominant active frequency of ambient vibration for most applications typically range from 10's Hz to 100's Hz [3], which presents a key design challenge for MEMS resonators. Therefore, the implemented micro-cantilevers tend to measure greater than several centimetres in dimension, which also result in atypical out-of-plane travel for the MEMS oscillators that can attain $\sim$1 mm in peak displacement [4]. The unconventionally large size of the required VEH device erodes the traditional scaling and integration benefits of MEMS technologies. Furthermore, large dies with substantial vertical travel also introduces a non-trivial and expensive packaging challenge.

To address the current undesirable volumetric sacrifice to accommodate low frequency devices, this paper presents a new interdigitated fork topology for micro-cantilever arrays. For a given design area (die size), the new design is capable of up to a third reduction in the fundamental resonant frequency without sacrificing power optimisation.

## 2. Design and simulation

The MEMS VEH devices were designed for a specific automotive application. Following FFT and STFT vibration analysis of the measured data, active frequencies were revealed to be in the vicinity of ∼500 Hz. The design area considered here is a 25 mm$^2$ square die and the devices were fabricated as per the stack of material shown in figure 1a. The fabrication process employs AlN as the piezoelectric material, deposited on doped silicon as the device and bottom electrode layer. The proof mass was patterned from an un-etched silicon wafer. Due to etching tolerances, a minimum gap of 100 $\mu$m was observed between various proof mass entities.

A pair of classical cantilevers and a pair of fork cantilevers were separately fitted within the 25 mm$^2$ design space as shown in figure 1b. The new topology comprises a pair of interdigitated cantilevers: a fork and a reverse fork structure. The precise frequency of the fork cantilevers can be tuned during the design stage by adjusting the length of each mass arms that occupies the space of the accompanying reverse fork.



(a) Stack of materials for piezoelectric MEMS (b) Classical cantilever (left) and fork cantilever (right).

Figure 1: MEMS fabrication process and design of classical cantilever and the proposed interdigitated fork cantilevers. Cantilevers fitted within the same design area of 5 mm by 5 mm. Blue shaded region illustrate the active piezoelectric areas.

As shown in the simulation results summarised in table 1, the fork cantilevers can achieve ∼30% lower resonant frequency than classical cantilevers, without compromising power output. All the devices have the same proof mass and active piezoelectric area to allow a fair comparison. By varying the mass arm length in the new fork design, the frequency can be varied. However, as the adjustment is in essence the reshaping of the same mass entity, the end mass does not quantitatively change. Instead, it is the effective length of the cantilever oscillator that is being altered. With a longer effective length, the resonant frequency is lowered and the maximum strain induced is also increased.

Table 1: Parameters for micro-cantilever designs within a fixed design area of 12.5 mm$^2$. Proof mass m, active piezoelectric area $A$, FEA simulated 1st mode resonant frequency $f_0$, average induced strain $\varepsilon$ at acceleration of 1 g assuming $Q$ of 100, and theoretical power $P$ at resonance based on FEA and calculation.

| | Classical cantilever | Fork cantilever I | Fork cantilever II |
|---|---|---|---|
| $m$ (mg) | 4.12 | 4.12 | 4.12 |
| $A$ (mm$^2$) | 3.2 | 3.2 | 3.2 |
| $f_0$ (Hz) | 744 | 501 | 551 |
| $\varepsilon$ (1) | $2.7 \times 10^{-4}$ | $4.0 \times 10^{-4}$ | $3.4 \times 10^{-4}$ |
| $P$ ($\mu$W) | 1.71 | 2.64 | 2.12 |

## 3. Experimental results and discussion

A fabricated device is shown in figure 2, where an 11 mm square silicon die contains a pair of fork cantilevers and an equivalent classical cantilever for comparison. The die in the figure sits within a deep cavity leadless chip carrier (16 mm in length). A ∼1 mm thick spacer (not shown) elevates the silicon die, in order to allow unrestricted travel of the shuttle during vibration. In both the classical and new designs, the cantilevers have four split electrode regions per device, which allow the possibility of connecting the separate piezoelectric regions in series to maximise voltage output [5].

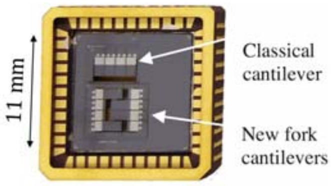


Figure 2: Photograph of a 11 mm square silicon die containing 1 classical cantilever device and two interdigitated fork cantilevers, in a chip carrier.

All devices were characterised on a mechanical shaker controlled by a waveform generator. The frequency domain power response is presented in figure 3. Measured resonant frequencies reveal 770 Hz for the classical cantilever, 525 Hz for Fork 1 and 586 Hz for Fork 2. This corresponds to 32% and 24% reduction in frequency for Fork 1 and Fork 2 respectively, over the classical cantilever. Apart from the anticipated offset in absolute values due to fabrication tolerance, the relative reduction is in line with the simulation.

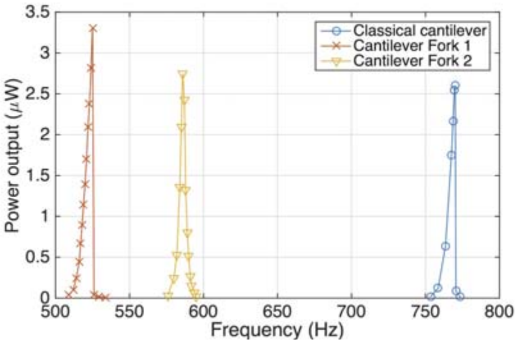
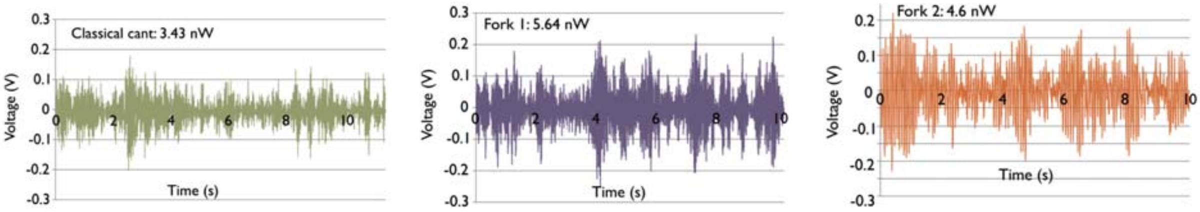


Figure 3: Experimentally measured power response in the frequency domain at 0.5 g of acceleration. Fork 1 peaks at 525 Hz, Fork 2 peaks at 586 Hz and Classical cantilever peaks at 770 Hz. Values are measured across matched load for each device.

Furthermore, at the 0.5 g of acceleration shown in figure 3, the resonant power output for the fork cantilevers performed slightly better than the classical cantilever. This is due to the larger induced average strain in the fork cantilevers. Figure 4 shows typical time domain responses of fork and classical cantilevers when subjected to band-limited (0 Hz to 800 Hz) noise excitation and the comparative results are presented in table 2.

The experimental results validate the design and theory in terms of demonstrating a new lower frequency cantilever topology within a given design space, without compromising on size or power output as compared to the classical design. This introduces new design flexibilities to accommodate the frequency ranges of varying applications, without having to scale up the overall size of the MEMS device.



(a) Classic MC: 3.4 nW (b) Fork 1 MC: 5.6 nW (c) Fork 2 MC: 4.6 nW

Figure 4: Typical time domain average power responses when subjected to band-limited (0 Hz to 800 Hz) noise excitation at 0.00125 $g^2$/Hz.

Table 2: Experimental results when subjected to band-limited (800 Hz) noise excitation at 0.00125 $g^2$/Hz. The 1st mode resonant frequency $f_0$ was experimentally measured in air, power $P$ is the average power record across the matched load resistance $R$ for the first resonant peak.

| | Classical cantilever | Fork cantilever I | Fork cantilever II |
|---|---|---|---|
| $f_0$ (Hz) | 770 | 525 | 586 |
| $R$ (kΩ) | 850 | 1,250 | 1,250 |
| $P$ (nW) | 3.43 | 5.64 | 4.60 |

Within the 25 $mm^2$ die-level design area and the specific MEMS process explored within this paper, if the frequency of the MEMS devices were all optimised to the target frequency vicinity of $\sim$500 Hz, 2 fork cantilevers can fit into the die area while only 1 classical cantilever can be accommodated. Therefore, the new fork cantilever topology will enable up to two times as many VEH devices to be manufactured per wafer.

## Conclusion

A new interdigitated fork cantilever array topology has been numerically and experimentally investigated for MEMS piezoelectric vibration energy harvesting. The new topology allows for up to about a third reduction in resonant frequency for a given design area compared to a classical plain cantilever topology, without compromising on power optimisation. This opens up further flexibility in designing towards relatively lower frequency ranges needed for practical applications, while relaxing the tradeoffs on the miniaturisation and ease of integration benefits brought about by the MEMS technology.

## Acknowledgments

This work was supported by EPSRC (Grant EP/L010917/1) and Innovate UK (Grant 102152).

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