Assembly of a high-dielectric constant thin TiO_x layer directly on H-terminated semiconductor diamond

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A high-dielectric constant (high-*k*) TiO_x thin layer was fabricated on hydrogen-terminated diamond (H-diamond) surface by low temperature oxidation of a thin titanium layer in ambient air. The metallic titanium layer was deposited by sputter deposition. The dielectric constant of the resultant TiO_x was calculated to be around 12. The capacitance density of the metal-oxide-semiconductor (MOS) based on the TiO_x/H-diamond was as high as 0.75 $\mu F/cm^2$ contributed from the high-*k* value and the very thin thickness of the TiO_x layer. The leakage current was lower than 10^{-13} A at reverse biases and 10^{-7}A at the forward bias of -2 V. The MOS field-effect transistor based on the high-*k* TiO_x/H-diamond was demonstrated. The utilization of the high-*k* TiO_x with a very thin thickness brought forward the features of an ideally low subthreshold swing slope of 65 mV per decade and improved drain current at low gate voltages. The advantages of the utilization high-k dielectric for diamond MOSFETs are anticipated.

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The outstanding properties of diamond such as wide band gap energy (5.47 eV), high thermal conductivity, high breakdown field, and high carrier mobility offer the highest figure-of-merits for electronic devices applications. It is well known that both acceptor (boron: 0.37 eV) and donor (phosphorus: 0.57 eV) form deep levels in diamond, making the practical applications of diamond as a traditional semiconductor difficult.[1] Fortunately, the unique surface conductivity of hydrogen-terminated diamond (H-diamond) provides a promising semiconductor channel for the development of metal-oxide semiconductor field effect transistors (MOSFETs) or metal Schottky-FETs capable of operation under a broad temperature range from 20 to 673 K.[2-5] The improvement of the output of the MOSFETs has usually relied on the following two aspects up to now: the increase of the semiconductor channel conductivity and the optimization of the device configuration. The holes related to the H-diamond surface are usually located at the surface with a sheet density of 10^{12}~10^{13} cm^{-2} after exposure to air.[3] A hole density as high as 10^{14} cm^{-2} was also reported on H-diamond after NO_2 adsorption or heating in NH_3 ambient.[6,7] By using submicron gate length, the maximum drain current density of the MOSFET based on NO_2 gas processed H-diamond surface reached as high as 1.3A/mm.[7]

Alternatively, in order to further improve the drain current density and reduce the threshold voltage, the enhancement of the capacitive coupling between the gate and the semiconductor channel is also crucial. Up to now, in addition to the gate insulators such as SiO_2 and AlN, [8,9] Al_2O_3 is the mostly utilized insulator on H-diamond surface for MOSFETs.[5] As previously disclosed, a gate insulator with high dielectric constant (high-*k*) could control high carrier densities even at small electric fields.[10] We have developed several high-*k* gate insulators on H-diamond surface for the fabrication of MOSFETs, such as Ta_2O_5, HfO_2, and ZrO_2/Al_2O_3.[10-12] Although these insulators had *k* values higher than that of Al_2O_3, the effective capacitance are still needed to be improved to compete with a single Al_2O_3 layer. The reasons for the relatively small gate capacitances are (i) the insertion of a thin Al_2O_3 layer between diamond and the high-*k* oxides and (ii) the large thickness of the gate insulators.

Therefore, the development of a thin high-*k* insulator directly contacting to the H-diamond surface is our ultimate target to achieve high-output diamond MOSFETs and low energy consumption. Titanium

dioxide (TiO_2) is a promising candidate as a high-*k* gate insulator with a *k* value as high as 100.[13] Although atomic layer deposition (ALD) is considered to be a powerful strategy for the growth of TiO_2 thin films, the properties of the ALD-TiO_2 thin films and the semiconductor surface are sensitive to the precursors.[14] In addition, elevated temperatures (100-300^oC) were generally required for the deposition of high-*k* TiO_2 thin films by ALD.[15] Reactive sputter-deposition of TiO_2 usually makes damage to the H-diamond surface by oxygen species.[16] In this work, we aim to develop high-*k* TiO_x thin films by sputter-deposition of a Ti thin film directly on the H-diamond surface, subsequently followed by air oxidation at low temperatures.

The 200nm-thick H-diamond epilayer used in this study was deposited on the Ib-type HPHT single crystalline diamond (100) substrate by a microwave plasma-enhanced chemical vapor deposition technique for 2 hours.[17] Before the deposition, the diamond (100) substrate was boiled in a mixture solution of H_2SO_4 and HNO_3 for 3 hours. The deposition temperatures for the H-diamond epilayer were 900~940 ºC with H_2 and CH_4 flow rates of 500 and 0.5 sccm, respectively. The microwave power is 400 W. The TiO_x thin film was formed on diamond substrates by thermal oxidation of the Ti thin film in air. The Ti thin film with a nominal thickness around 10 nm was deposited by a radio-frequency sputter apparatus at 150 W with a base pressure of 10^{-8} Torr. During sputtering, Ar was used as the working gas at a pressure of 1 Pa. The as-deposited Ti thin film was confirmed to be metallic by a multimeter. After air oxidation, the TiO_x film turned to be an insulator. To fabricate the TiO_x/H-diamond MOSFETs, source and drain contacts were firstly deposited on the H-diamond surface with a mesa structure, which was achieved by the standard photolithography process. The source and drain electrodes were deposited by using an electron-beam evaporator, which were the multilayer of Au/Ti/Pd (200/20/10 nm). The Pd directly contacts to H-diamond surface. Assisted by a photolithography process, a Ti thin film (10 nm) was deposited on the gate area followed by air oxidation at 120^oC to form the TiO_x layer. Tungsten carbide was grown by sputter deposition at ambient substrate temperature (no intentional heating) as the gate electrode on the top of the TiO_x layer.

The composition and chemical bonding states of the TiO_x phase were analyzed by X-ray

photoelectron spectroscopy (XPS) measurements (Thermo ESCAlab 250), by which the source was Al K_α X-radiation with an excitation energy of 15 keV and emission current of 6 mA. The analyzer pass energy was 20 eV with step of 0.1 eV and dwell time of 50 ms for the measurements. The current-voltage (I-V) characteristics of the TiO_x/H-diamond MOS structure and the MOSFET was measured by a HP 4140B semiconductor test system and an electrical probe station. The capacitance-voltage (C-V) measurements were carried out by a Keithley 4200 semiconductor analyzer. The gate bias was swept from negative to positive followed by an opposite sweeping direction in the C-V measurements. The frequency was from 10-100 kHz.

In order to confirm the formation of TiO_x, the chemical bonding states of the TiO_x thin film was analyzed by XPS. The resultant XPS spectra were calibrated in binding energies by referring to the C 1s peak at 248.8 eV from surface contamination. [18] Figure 1 (a) shows the XPS spectrum corresponding to the Ti 2p region acquired from the TiO_x sample. The peak position at 458.9 eV was identified, which can be attributed to the Ti^{4+} valence state.[19] The peak at 464.7 eV corresponds to the Ti $2p_{1/2}$ of the Ti^{4+} valence state. No peak from the metallic Ti was observed from the TiO_x layer, consistent with the electrical conductivity measurements. In order to further confirm the formation of TiO_x, the O 1s spectrum was also collected, as shown in Fig.1 (b). The peak deconvolution analysis leads to two peaks, located at around 530.4 and 531.6 eV, respectively. The peak at 530.4 eV is due to the lattice oxygen bonded in TiO_x, and the other one at 531.6 eV is from the non-lattice oxygen due to C-O bonding by air absorption. [19] The composition of the 15 nm-TiO_x layer was calculated to be around $TiO_{1.88}$ from the XPS spectra. The valance band spectra related to TiO_x and H-diamond were also measured by XPS, for which three set of samples: pure H-diamond, 15 nm TiO_x on oxygen-terminated diamond (O-diamond), and 5 nm-TiO_x/H-diamond, were utilized. The compositions of all the TiO_x layers here were almost the same. The valance band maximum (VBM) and C 1s (C-C) of the H-diamond were 1.2 eV and 284.3 eV, respectively.[21] For the 15 nm-TiO_x on O-diamond, the VBM was around 3.1 eV. The core energy levels of C 1s and Ti 2p 3/2 for the sample of 5 nm-TiO_x/H-diamond were 284.1 eV and 459.1 eV, respectively.

Therefore, the valance band offset (ΔE_V) between TiO_x and H-diamond can be estimated by the following expression[20]

$$\Delta E_v = (E_{CL} - E_{VBM})_{H-diamond} - (E_{CL} - E_{VBM})_{TiOx} - \Delta E_{CL} \quad (1)$$

where $(E_{CL} - E_{VBM})_{H-diamond}$ is the difference in binding energy between the C 1s and the VBM value of the H-diamond, $(E_{CL} - E_{VBM})_{TiOx}$ is the difference in binding energy between the Ti 2p3/2 and the VBM value of the TiO_x. The ΔE_{CL} is the difference in binding energy between the Ti $2p_{3/2}$ and C 1s of the sample 5nm-TiO_x/H-diamond. The valence band offset was thus estimated to be around 2.6 eV for the TiO_x/H-diamond junction. The microstructure of the TiO_x/diamond was investigated by transmission electron microscopy (TEM), as shown in Fig.2. The thickness of the TiO_x layer was measured to be around 15 nm. The composition of the cross-section of the TiO_x/diamond was examined by energy dispersive X-ray analysis (EDX). The corresponding elements mapping was obtained by EDX, shown in in Fig. 2 (b) and (c), revealing the uniform distribution of the Ti and O elements within the TiO_x film without diffusion into diamond. The high-resolution TEM (HRTEM) image in Fig. 2 (d) discloses that the TiO_x thin film is amorphous.

The TiO_x/H-diamond MOSFET structure was illustrated in Fig. 3(a). The I-V characteristics of the TiO_x/H-diamond MOS structure was obtained from the gate and source, as displayed in Fig. 3(b). The leakage current at reverse bias (positive gate voltage) is extremely low, beyond the detection limit (10^{-13} A) of the measurement system. At forward bias (negative gate voltage), the leakage current is as low as 10^{-7} A at -2 V. The low leakage current reveals the good dielectric properties of the TiO_x fabricated by the present low-temperature method. The electrical transport at forward bias was well fitted by Fowler-Nordheim field emission tunneling mechanism: $I \propto V^2 \exp\left(\frac{b}{V} + a\right)$ [21], as shown in Fig. 3(c). This suggests the holes tunneling process from diamond through the TiO_x insulator at high electric fields is the main leakage mechanism.

Figure 4 (a) illustrates the C-V characteristics of the TiO_x/H-diamond MOS structure, which were measured at different frequencies. The depletion and accumulation of charge depending on the gate bias

are obviously observed, revealing a typical MOS structure behavior. The gate capacitance shows little dependence on frequency or little frequency dispersion at the frequency range from 10-100k Hz. The maximum gate capacitance density in the accumulation region reaches as high as 0.75 $\mu F \cdot cm^{-2}$, which is more than twice of our previous results on high-*k*/H-diamond MOS structures based on ZrO_2 and HfO_2 [11,12]. The capacitance density is close to those of electrolyte gated FET.[22] The dielectric constant of the fabricated TiO_x was estimated to be around 12. The C-V characteristics suggest that the gate capacitance at 0 V is at the minimum, similar to that in the depletion mode. Therefore, there is little charge at 0 V and the MOSFETs based on the TiO_x/H-diamond should exhibit normally-off feature. The normally-off feature is possibly due to the existence of fixed positive charges in the TiOx layer. The C-V characteristics was also measured by sweeping the gate bias from positive to negative direction followed by an opposite direction sweeping, as shown in Fig. 4 (b). There is almost no hysteresis or voltage shift during the gate biases sweeping, suggesting little charges trapped at the TiO_x/H-diamond interface or in the TiO_x thin film due to carriers injection.

The dependence of the drain current density on the drain voltage (I_{DS}-V_{DS}) at different gate voltages for the TiO_x/H-diamond MOSFET with a gate length of 40 μm and width of 200 μm, is illustrated in Fig. 5 (a). The gate voltage (V_{GS}) is varied from 0 to -2 V with a step of -0.5 V. The *p*-type channel characteristics is expectedly revealed in the TiO_x/H-diamond MOSFET. The maximum I_{DS} (I_{DSmax}) for the gate length 40 μm is 2.8 $mA \cdot mm^{-1}$ at V_{GS}= -2 V and increased to be 5.1 $mA \cdot mm^{-1}$ with the gate length decreased to 30 μm. The I_{DSmax} values are larger than those obtained on the SD-$LaAlO_3$/ALD-Al_2O_3/H-diamond MOSFETs with the same device dimensions[20]. We note that higher drain current density was achieved even at smaller gate voltages, i.e. V_{GS}=-2 V here, compared to V_{GS}=-8 V for the SD-$LaAlO_3$/ALD-Al_2O_3/H-diamond MOSFETs[20]. The ON resistance (R_{ON}), composed of source/drain contact resistance, channel resistance beneath the oxide, and resistance between source/drain and gate, was calculated from the linear regime in Fig. 5(a), which was around 218 Ω·mm at V_{GS}=-2V. This value is also lower than those obtained from the SD-$LaAlO_3$/ALD-Al_2O_3/H-diamond MOSFETs with a similar gate length of 40 μm [20]. The TiO_x/H-diamond MOSFET is basically operated in

enhancement mode. The threshold voltage calculated to be around -0.7 V by plotting the curve of $-\sqrt{I_{DS}}$ *vs*. V_{GS}. The drain on/off current ratio at the V_{DS} of -2.5 V is larger than 10^8, which is desirable for the practical logic circuit applications. The effective hole mobility was calculated to be around 88 $cm^2/V\cdot s$.

The subthreshold swing (*SS*) is one of the key parameters to determine the power consumption for the integrated circuit applications. A low *SS* value is preferred to minimize the power consumption. As revealed in Fig. 5(b), the *SS* value was calculated to be 65 mV per decade in the depletion region at a drain voltage of -2.5 V. The *SS* value of the 15nm-TiO_x/H-diamond is much lower than that of 25 nm-Al_2O_3/H-diamond (120 mV per decade). Typically, the subthreshold swing relates to the semiconductor and insulator through the following expression[23]

$$SS = \left(1 + \frac{C_s + C_{it}}{C_{ox}}\right)\frac{kT}{q}\ln(10) \qquad (2)$$

In order to reduce the *SS* value, the gate oxide insulator C_{ox} should be increased and the capacitance C_s associated with the semiconductor channel and C_{it} related to the interface defects should be decreased. In the ideal case, the minimum *SS* value is around 60 mV per decade at room temperature. Therefore, the *SS* value of the TiO_x/H-diamond MOSFET is very low, promising for low-power consumption integrated circuits. According to eq. (2), $(C_s+C_{it})/C_{ox}$ was estimated to be around 0.23, from which the $(C_s + C_{it})$ was estimated to be around 16 pF. If the semiconductor capacitance is neglibile in the deep subthreshold region, the interface states density D_{it} was evaluated to be around $10^{12}eV^{-1}cm^{-2}$.

Up to now, direct deposition of high-*k* Ta_2O_5 was only conducted on oxygen-terminated boron-doped p-type diamond by our group initially[10]. However, in order to supress the large leakage current, the thickness of the Ta_2O_5 film was as high as 118 nm, leading to an effectively low capacitance density. Hydrogenated diamond surface displays negative electronic affinity, which enables the wide selection of the high-*k* oxides as the gate of diamond MOSFETs. Although the TiO_x in the present work has a lower bandgap than diamond, the leakage current is quite low. The low temperature oxidation process in air has little damage on the H-diamond surface. Compared to previous high-*k* oxides/H-diamond MOS structures, there is no insertion layer between the high-*k* TiO_x and diamond. This greatly benefits to the achievement

of the effectively high capacitance density. As a result, the control of high channel density at low fields becomes possible, and the subthreshold swing slope is ideally low. These features provide promising avenue for the development of low-power consumption diamond integrated circuits.

In summary, the direct assembly of thin high-*k* TiO_x layer on H-diamond was achieved at low temperature with a value of around 12. Due to the thin thickness of the TiO_x layer, a high capacitance density of 0.75 $\mu F \cdot cm^{-2}$ was obtained. By using the TiO_x layer as the gate insulator, the MOSFET based on H-diamond was demonstrated with enhancement mode. The resultant TiO_x/H-diamond MOSFET revealed a relatively low ON-resistance and high on/off current ratio. Benefited from the high-*k* value and the thin thickness of TiO_x, an ideally low subthreshold swing slope was achieved. In addition, the trap density of the TiO_x/H-diamond was rather low. The *k*-value may be increased when the crystallinity of the TiO_x was improved by increasing the annealing temperature.

ACKNOWLEDGMENTS

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Figure captions

FIG. 1. XPS spectra of the 15nm-TiO_x revealing the chemical states of (a) Ti 2p and (b) O 1s.

FIG.2 (a) Cross-section TEM image of the TiO_x/diamond. The top showing the corresponding materials in the image. (b), (c) EDX elemental mapping of O and Ti, respectively, (d) HRTEM image of the TiO_x/diamond.

FIG. 3. Electrical properties of the MOS structure based on TiO_x/H-diamond. (a) Schematic device geometry, (b) current-voltage characteristics, and (c) fitting of the IV at forward biases by tunneling mechanism.

FIG.4. (a) Capacitance voltage characteristics at different frequencies and (b) capacitance-voltage characteristics for different bias sweeping directions.

FIG. 5. (a) Drain current versus drain voltage at different gate biases and (b) drain current dependence on gate voltage at a drain voltage of -1 V.

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Figure 1

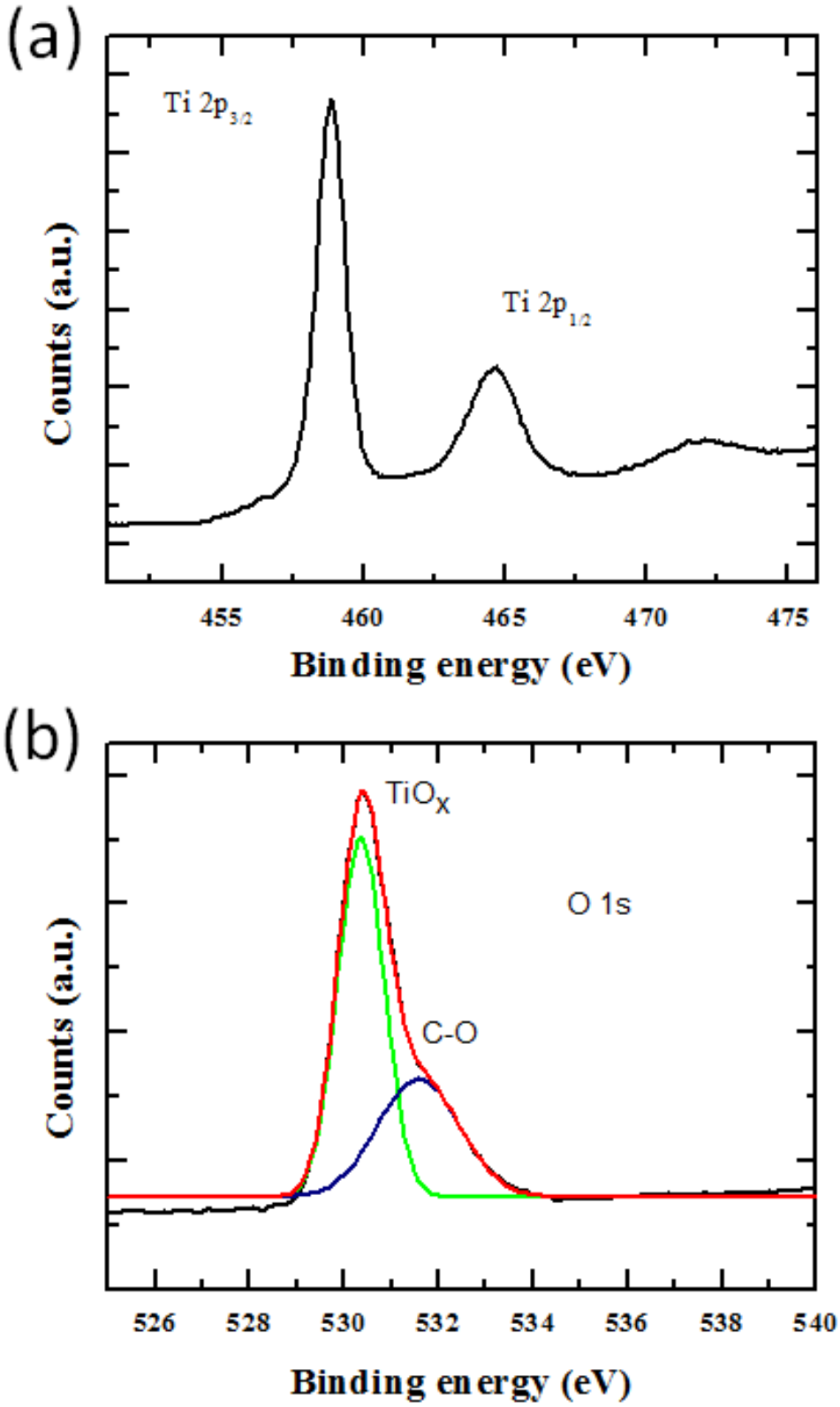

(a)
Ti 2p3/2
Ti 2p1/2
Counts (a.u.)
455
460
465
470
475
Binding energy (eV)
(b)
TiOX
O 1s
C-O
Counts (a.u.)
526
528
530
532
534
536
538
540
Binding energy (eV)

Figure 2

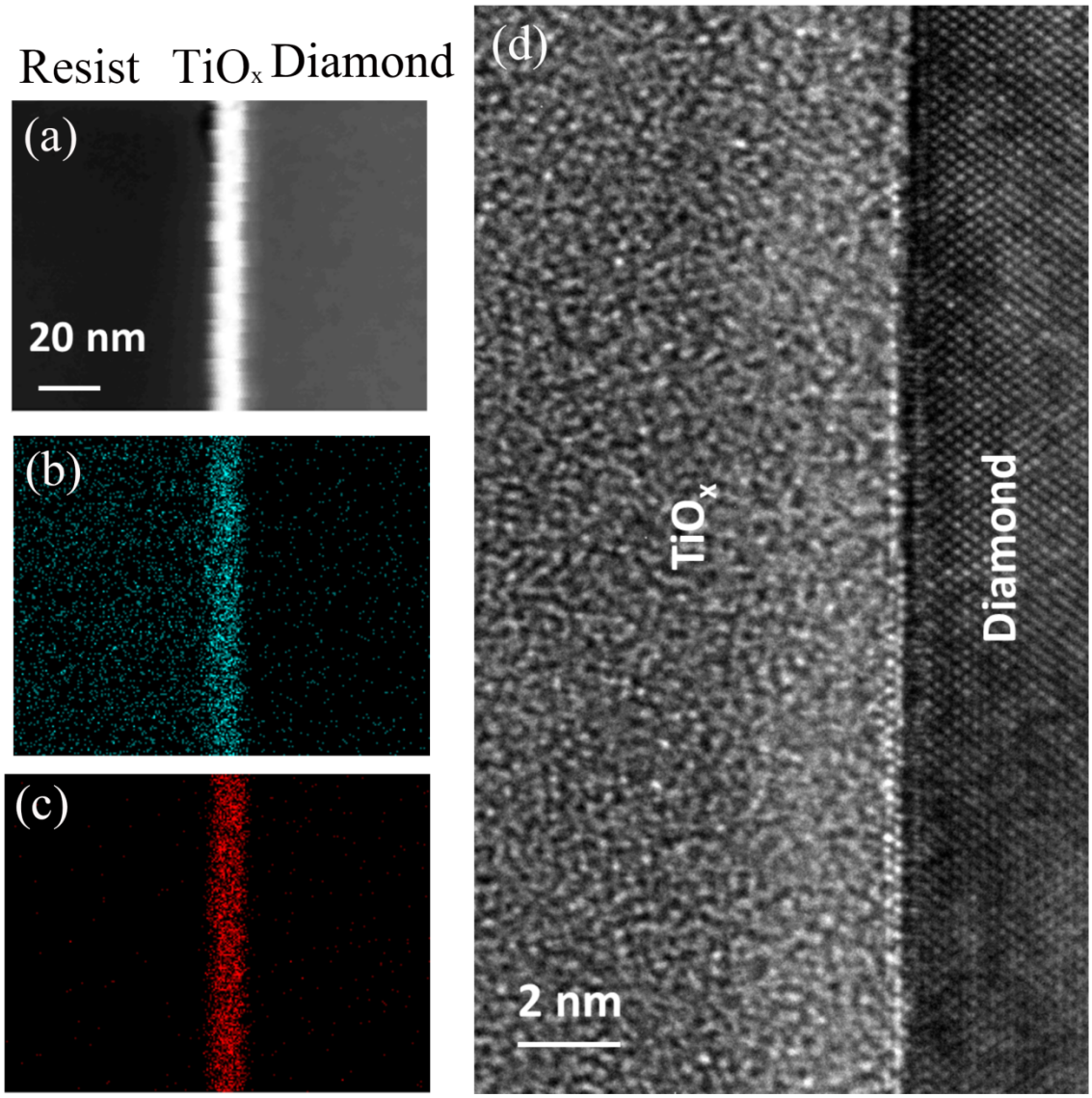


Figure 3

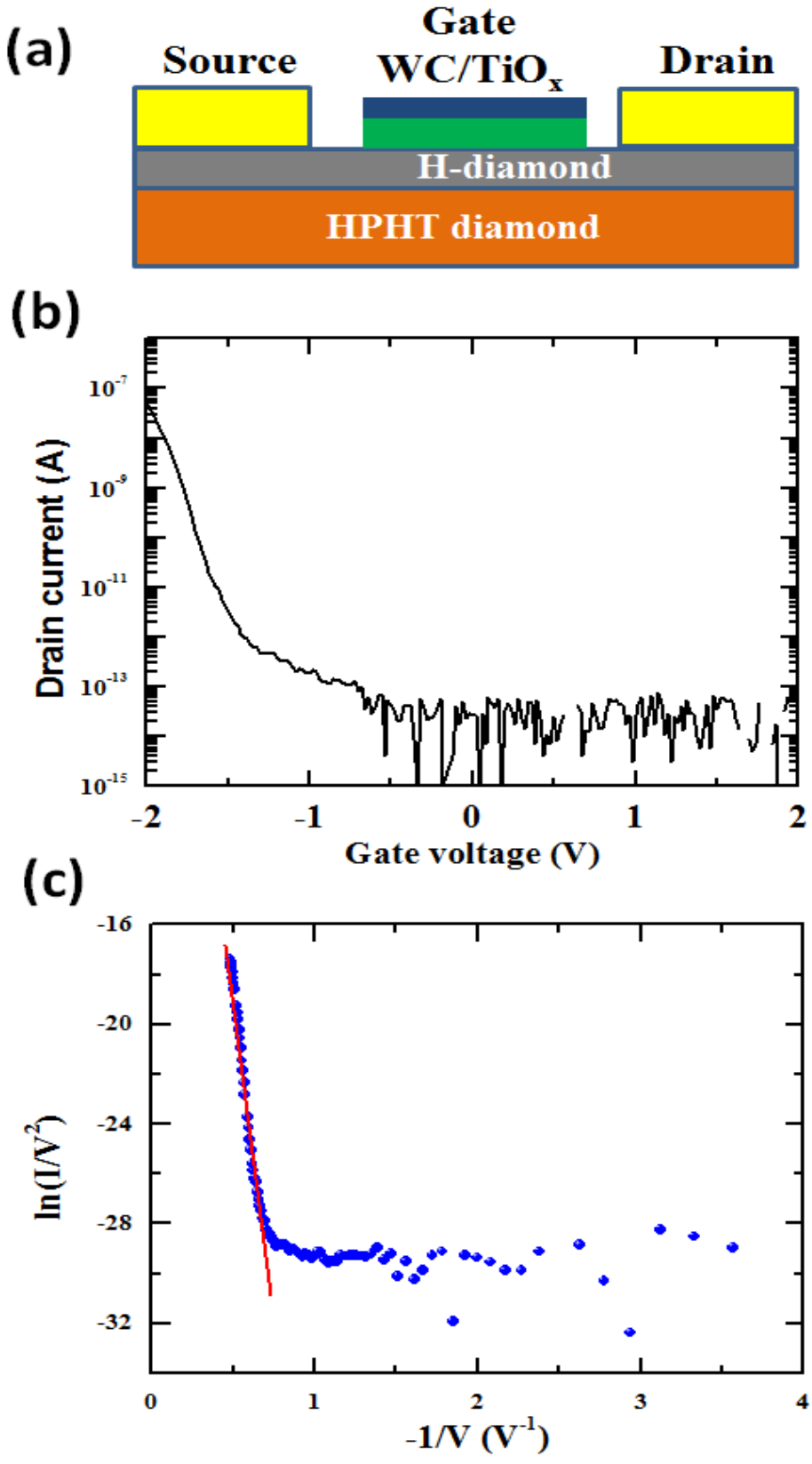

(a)
Source
Gate
WC/TiOx
Drain
H-diamond
HPHT diamond
(b)
Drain current (A)
10-7
10-9
10-11
10-13
10-15
-2
-1
0
1
2
Gate voltage (V)
(c)
ln(I/V2)
-16
-20
-24
-28
-32
0
1
2
3
4
-1/V (V-1)

Figure 4

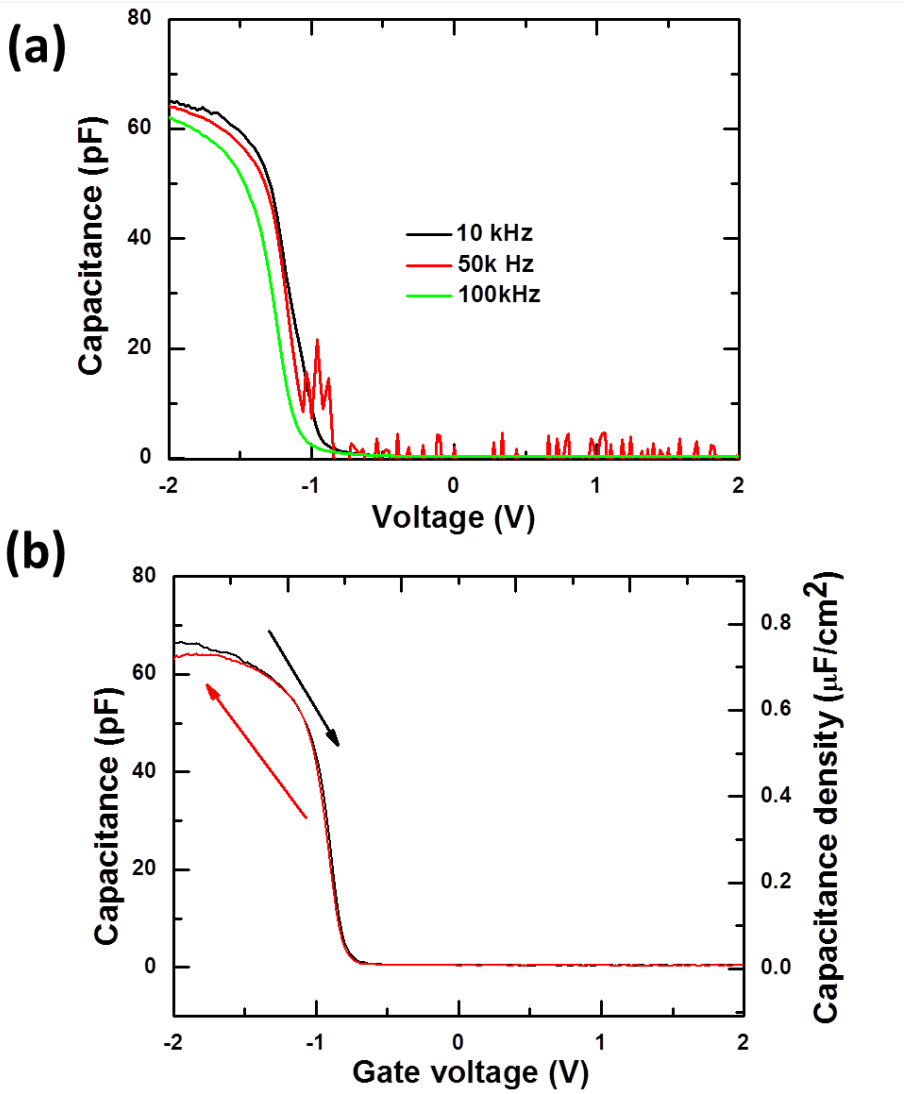
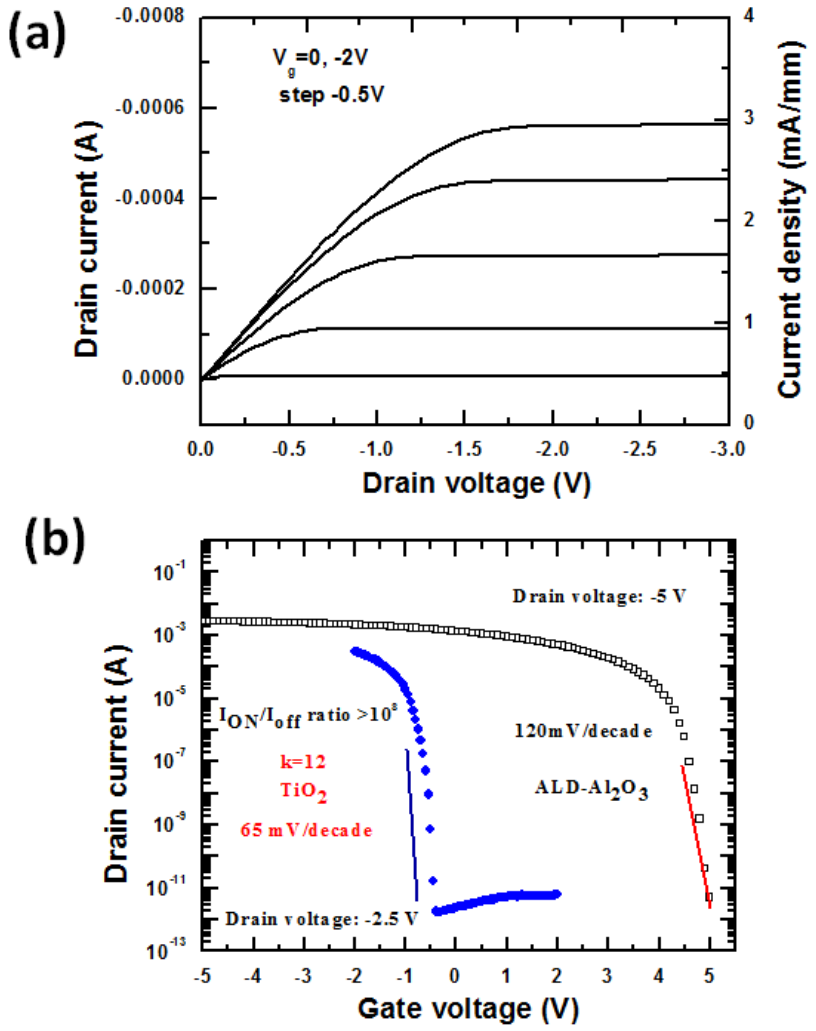

(a)
Capacitance (pF)
Voltage (V)
10 kHz
50k Hz
100kHz
(b)
Capacitance (pF)
Capacitance density (μF/cm²)
Gate voltage (V)

Figure 5


(a)
V_g=0, -2V
step -0.5V
Drain current (A)
Current density (mA/mm)
Drain voltage (V)
-0.0008
-0.0006
-0.0004
-0.0002
0.0000
0.0
-0.5
-1.0
-1.5
-2.0
-2.5
-3.0
4
3
2
1
0
(b)
Drain voltage: -5 V
I_{ON}/I_{off} ratio >10^5
120mV/decade
k=12
TiO_2
65 mV/decade
ALD-Al_2O_3
Drain voltage: -2.5 V
Drain current (A)
Gate voltage (V)
10^{-1}
10^{-3}
10^{-5}
10^{-7}
10^{-9}
10^{-11}
10^{-13}
-5
-4
-3
-2
-1
0
1
2
3
4
5