Piezoelectric Vibration Energy Harvesting: a Connection Configuration Scheme to Increase Operational Range and Output Power

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Abstract

For a conventional monolithic piezoelectric transducer (PT) using a full-bridge rectifier, there is a threshold voltage that the open-circuit voltage measured across the PT must attain prior to any transfer of energy to the storage capacitor at the output of the rectifier. This threshold voltage usually depends on the voltage of the storage capacitor and the forward voltage drop of diodes. This paper presents a scheme of splitting the electrode of a monolithic piezoelectric vibration energy harvester into multiple (n) equal regions connected in series in order to provide a wider operating voltage range and higher output power while using a full-bridge rectifier as the interface circuit. The performance for different series stage numbers has been theoretically studied and experimentally validated. The number of series stages ($n \geq 1$) can be predefined for a particular implementation, which depends on the specified operating conditions, to achieve optimal performance. This enables the system to attain comparable performance compared to active interface circuits under an increased input range while no additional

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active circuits are required and the system is comparatively less affected by synchronized switching damping (SSD) effect.

I. Introduction

Ultra low power wireless sensors and sensor systems are of increasing interest in a variety of applications ranging from structural health monitoring to industrial process control. Electrochemical batteries have thus far remained the primary energy sources for such systems despite the finite associated lifetimes imposed due to limitations associated with energy density. However, certain applications require the operation of sensors and sensor systems over significant periods of time including implantable biomedical electronic devices and tire pressure sensors, where battery usage may be impractical and add cost due to the requirement for periodic re-charging and/or replacement [Belleville et al., 2010]. In order to address this challenge and extend the operational lifetime of wireless sensors, there has been an emerging research interest on harvesting ambient vibration energy [Szarka et al., 2012], [Mitcheson et al., 2008].

Piezoelectric materials are widely used in small scale vibration energy harvesters (VEH) as mechanical-to-electrical transducers due to their relatively high power density, scalability and compatibility with conventional integrated circuit technologies [Elvin and Erturk, 2013], [Han et al., 2014]. A typical piezoelectric VEH can provide an power density of around 10 - 500 $\mu\mathrm{W} \cdot \mathrm{cm}^{-2}$, which sets a significant constraint on designing the associated power-conditioning interface circuit [Kim et al., 2011]. The most commonly used passive rectification method is a full-bridge rectifier; however, this sets a high threshold voltage for the generated energy by the harvester to be transferred to a storage capacitor [Qian et al., 2013]. This limitation prevents the system from operating if the environmental excitation is not high enough to attain the required operational threshold voltage and the vibrational energy due to this small excitation is therefore not transferred to the energy storage device [Krihely and Ben-Yaakov, 2011]. Furthermore, for excitation resulting in harvester output slightly greater than the threshold voltage, a very

significant amount of energy is wasted as a result [Liang and Liao, 2012].

In order to increase the power efficiency of a VEH system, most of interface circuits seek to develop a mechanism to minimize the energy wasted due to the threshold set by a full-bridge rectifier [Sun et al., 2012]. The interface circuit does not only need to consume ultra-low power, but it also should be able to recover the power as effectively as possible from the piezoelectric transducer (PT) [Romani et al., 2014], [Aktakka and Najafi, 2014], [Yuan and Arnold, 2011]. Therefore, in order to design the piezoelectric VEH system to deliver a high output power, both the interface circuit and the harvester mechanism should be well designed and the design interaction should be thoroughly examined [Dini et al., 2015], [Le et al., 2006], [Sankman and Dongsheng, 2015]. Approaches such as the SSHI (Synchronized Switch Harvesting on Inductor) interface is considered to provide ideally no charge wastage if the resistance of the RLC loop is negligible [Badel et al., 2005], [Shaohua and Boussaid, 2015]. Other synchronized switch interfaces, such as Synchronous Electric Charge Extraction (SECE), are also widely used for high-efficiency circuits [Gasnier et al., 2014].

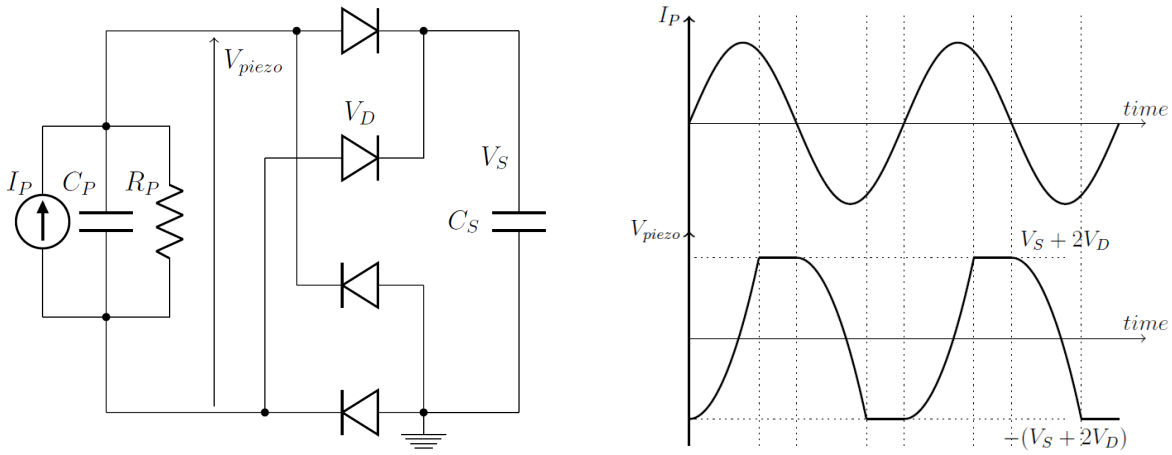
Despite the performance, there are four main drawbacks existing in these active interface circuits. First, the overall volume and complexity of an energy harvesting system are significantly increased by complex interface circuits along with off-chip capacitors, resistors and inductors, where inductors must be implemented off-chip to achieve good performance for most interfaces. Second, active interface circuits continuously consumes energy. Although some reported interface circuits attain sub-μW power loss, there is still an amount of energy is drawn from the energy reservoir when there is no input excitation. This could eventually deplete all stored energy and both the interface circuit and load electronic devices will stop operating. In addition, SSHI and SECE circuits can only achieve high efficiency at a limited range of excitation levels. This limits

the overall performance of the system in real-world implementations. Furthermore, SSHI and SECE interface circuits can only provide higher performance than simple full-bridge rectifiers for weakly coupled piezoelectric transducers due to the Synchronized Switch Damping (SSD) effect [Badel et al., 2006], [Ji et al., 2016]. If the the coupling is strong and the PT vibrates at resonance, the periodic current pulses applied to invert or extract charge on a PT result in an electrical actuation that opposes the vibration. All of the above four limitations introduced by system complexity and volume, quiescent power consumption, real-world wide range excitation levels and SSD effect result in the reported active rectifiers achieving acceptable performance only in a limited operating range.

In this paper, a passive approach using a simple full-bridge rectifier is proposed with associated modifications in the connection configuration scheme for the piezoelectric transducer. This approach is able to achieve comparable performance to some active interface circuits without the drawbacks mentioned above. With the proposed approach, the electrode of a monolithic PT is split into multiple ($n \geq 2$) equal pieces connected in series and the number n can be pre-determined according to the excitation amplitude of the ambient vibration. A suitable value of n helps maximizing the operation range and harvested power. Theoretical studies on output power and threshold voltage for different values of n are provided in equations and figures. The theoretical derivations are validated by experimental results conducted on commercial piezoelectric vibration energy harvesters.

II. Full-bridge rectifier

A PT vibrating at or close to its resonance frequency can be modeled as a current source I_P in parallel with a capacitor C_P and a resistor R_P [Ottman et al., 2002]. The AC signal generated by



(a) Full bridge rectifier

(b) I_P and V_{piezo} waveform

Fig. 1: Full-bridge rectifier and associated waveform

the PT needs to be rectified in most cases before further power conditioning. The most commonly used passive rectification circuit for a PT is a full-bridge rectifier, which employs four diodes to perform AC-to-DC conversion (see Figure 1a). The energy is then stored in a storage capacitor C_S connected to the output of the rectifier. Figure 1b shows the associated waveform of the current source I_P and V_{piezo}, which is a time-varying voltage across the piezoelectric transducer (PT). In order to charge C_S, V_{piezo} needs to attain $V_S + 2V_D$ or $-(V_S + 2V_D)$ to overcome the threshold voltage set by the rectifier, where V_S is the voltage of the storage capacitor C_S and V_D is the voltage drop of the diodes used in the rectifier. Therefore, the energy used for charging the internal capacitor C_P from $V_S + 2V_D$ to $-(V_S + 2V_D)$ (or vice-versa) is wasted, which can be expressed as:

$$Q_{wasted} = 2C_P(V_S + 2V_D) \tag{1}$$

The peak-to-peak open-circuit voltage of V_{piezo} is noted as $V_{pp(open)}$. In order to transfer energy from the PT to the storage capacitor, $V_{pp(open)} > 2(V_S + 2V_D)$ should be satisfied. Otherwise, all of the harvested energy by the PT is wasted for discharging and charging C_P. So this critical voltage can be set as a threshold voltage for $V_{pp(open)}$ to ensure that the full-bridge rectifier transfers energy to C_S:

$$V_{pp(open)} > V_{TH} = 2(V_S + 2V_D) \tag{2}$$

where $V_{TH} = 2(V_S + 2V_D)$ is the threshold that $V_{pp(open)}$ must attain to transfer any energy to the storage capacitor C_S. If the condition in equation (2) is met, the remaining charge can flow into C_S. The wasted charge is used for discharging and charging C_P and the amount of the wasted charge in a half cycle of I_P is $Q_{wasted} = 2C_P(V_S + 2V_D)$. The power conversion efficiency is extremely low if $V_{pp(open)}$ is slightly higher than V_{TH}. Assuming $V_D = 0.5\,\mathrm{V}$ and $V_S = 3\,\mathrm{V}$, the threshold voltage is as high as $8\,\mathrm{V}$. For MEMS (Microelectromechanical Systems) piezoelectric harvesters, this threshold is hard to attain.

III. Proposed scheme

A commonly used cantilevered PT consists of a substrate and a piezoelectric layer sandwiched between a pair of metal electrode layers. When the cantilever vibrates, a strain in the piezoelectric layer is generated due to the deflection of the cantilever. This response is transduced to electrical charge by the piezoelectric material and a current is generated to charge the inherent capacitor C_P formed by the two metal electrode layers [Miso et al., 2015]. As a result, there is a voltage V_{piezo} developed across the PT. As discussed previously, the most important limitations of a

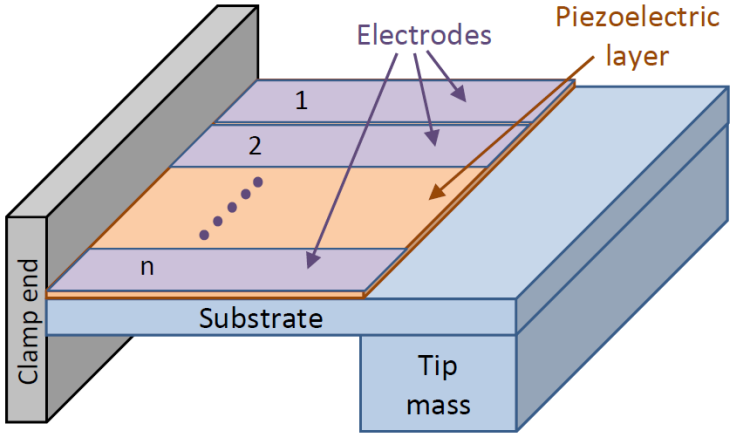


Fig. 2: Splitting a monolithic PT into n regions

full-bridge rectifier are the high threshold voltage and low power efficiency while the threshold is marginally overcome [Dicken et al., 2012]. This paper proposes an approach by splitting both the top and bottom electrode layers into n equal parts [Dayou et al., 2012]; hence, the monolithic PT turns into a harvester with n regions as a result, which is equivalent to n individual harvesters with exactly the same vibration amplitudes, frequencies and phases, as shown in Figure 2. The electrodes should be segmented along the primary strain direction, so that the total strain in the piezoelectric layers in each region is equal.

The current source, internal capacitor and resistor in the monolithic PT are noted as $I_P = I_0 \sin 2\pi f_P t$, C_P and R_P, respectively. The model of the PT used for calculations in this paper takes consideration of the internal leakage resistor R_P because the resonant frequency of the PT is quite low in this implementation, so that R_P is not negligible compared to the impedance of C_P. After splitting the electrode layers into n equal regions, the area is divided by n for each PT compared to the monolithic model. As the total strain in these regions is the same, the current source amplitudes for them should be equal. For one individual region, the current source amplitude, capacitor and resistor can be noted as I_1, C_1 and R_1 respectively. In a cantilever, the

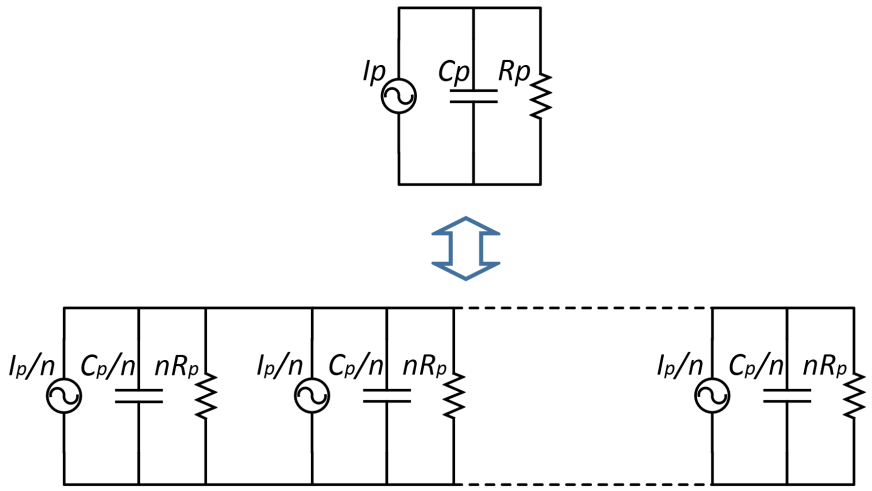


Fig. 3: Monolithic harvester (top) and n-region harvester connected in parallel (bottom)

inherent capacitor and generated current amplitude are proportional to the electrode area and the total strain, respectively; the resistance is inversely proportional to the electrode area. Therefore, the parameters of the new PT can be expressed in terms of the parameters of the monolithic PT: $I_1 = \frac{1}{n} I_0 \sin 2\pi f_P t$, $C_1 = \frac{1}{n} C_P$ and $R_1 = nR_P$.

As the generated charge in one region is divided by n compared to the original monolithic PT ($Q_1 = \frac{1}{n} Q_P$) and the capacitor C_1 is also divided by n ($C_1 = \frac{1}{n} C_P$), the open-circuit voltage for one region equals to the voltage of the original monolithic PT ($V_{pp1(open)} = Q_1/C_1 = Q_p/C_P = V_{pp(open)}$). If the n regions are connected in parallel, the resulting harvester works exactly the same as the original monolithic harvester, as shown in Figure 3.

As expressed in equation (1), the charge wastage due to the self discharging and charging C_P in a half I_P cycle is $Q_{wasted} = 2C_P(V_S + 2V_D)$. In order to minimize Q_{wasted}, C_P can be decreased by connecting the two regions in series. They should be connected with consideration of voltage directions so that the final series harvester model results in a summed-up voltage. Setting the capacitor for each region is C_1, where $C_1 = \frac{1}{n} C_P$, the equivalent capacitor of the

series model is $C_{P+} = \frac{1}{n^2} C_P$ (the symbol '+' means series). Therefore, the equivalent capacitor of this series connected PT is $1/n^2$ of the original one, which reduces Q_{wasted} by a factor of n^2. While the harvester is charging the storage capacitor C_S, the voltage $|V_{piezo}|$ will stay at $(V_S + 2V_D)$. Furthermore, by connecting in series appropriately, the open-circuit peak-to-peak voltage of this new harvester $V_{pp(open)+}$ is now increased by a factor of n. This phenomenon helps retain the rectifier operation even at smaller excitations, as the threshold voltage for the series model is halved.

Similar series configurations of PTs have been mentioned in [Liu et al., 2011], [Yu et al., 2014]. However, as opposed to previous researches, series models with variable stages is first thoroughly derived in this paper and the output performance is calculated to find an optimal series stage number according to variable excitation environments.

IV. MODELING

In this section, theoretical models are developed to establish the effect of series connected PTs on the output power of a full-bridge rectifier. A monolithic PT model is first studied; then the PT is split into n equal regions connected in series. In order to compare the performance between the parallel and series models, the voltage increase in C_S (note ΔV_S) in function of excitation amplitude ($V_{pp(open)}$) for all models can be compared. In addition, the electrical output power of the full-bridge rectifier in function of V_S for different models under a same excitation level is derived and illustrated to find the peak output power for each model.

A. Monolithic model

Calculations are first performed on a monolithic PT to study the open-circuit peak-to-peak voltage $V_{pp(open)}$ and the corresponding output power with employment of a full-bridge rectifier. Assuming the excitation of the PT is sinusoidal, the current source can be written as $I_P = I_0 \sin \omega t$, where $\omega = 2\pi f_P$. The total charge generated by the PT in a half cycle (T/2) should first be calculated, which can be written as:

$$Q_{total} = \int_0^{\frac{T}{2}} I_0 \sin \omega t \mathrm{d}t = \frac{2I_0}{\omega} \tag{3}$$

As discussed in the previous section and shows in figure 1, a vibrating PT can be modeled as a current source I_P in parallel with an internal capacitor C_P and a resistor R_P. Before the full-bridge rectifier becomes conducting, the current from I_P is divided into two parts inside the piezoelectric harvester, I_C and I_R flowing through the capacitor C_P and resistor R_P, respectively. As the diodes are OFF in this case, the PT can be regarded as an open-circuit. The ratio of the current flowing into C_P to the total current I_P is expressed as:

$$\frac{I_C}{I_P}(j\omega) = \frac{R_P}{R_P + \frac{1}{j\omega C_P}} = \frac{j\omega R_P C_P}{1 + j\omega R_P C_P} \tag{4}$$

The charge flowing into the capacitor C_P is:

$$Q_C(j\omega) = Q_{total}\frac{I_C}{I_P}(j\omega) = \frac{2jI_0 R_P C_P}{1 + j\omega R_P C_P} \tag{5}$$

As Q_C is the charge that flows into the capacitor C_P to build the voltage V_{piezo}, the rest of the charge flows into the resistive path and it is dissipated by the resistor R_P. According to the formula $V = Q/C$, the open-circuit peak-to-peak voltage $V_{pp(open)}$ can be written as:

$$V_{pp(open)} = |\frac{Q_C(j\omega)}{C_P}| = |\frac{2jI_0R_P}{1 + j\omega R_P C_P}| = \frac{2I_0R_P}{\sqrt{1 + \omega^2 R_P^2 C_P^2}} \tag{6}$$

To start transferring energy to C_S, $V_{pp(open)}$ after a half cycle $t = \frac{T}{2}$ should overcome the threshold $V_{TH} = 2(V_S + 2V_D)$. Hence, the condition for the rectifier to start transferring charge from the PT to C_S is:

$$\begin{aligned} V_{pp(open)} &> 2(V_S + 2V_D) \\ \Rightarrow \frac{I_0R_P}{\sqrt{1 + \omega^2 R_P^2 C_P^2}} &> V_S + 2V_D \end{aligned} \tag{7}$$

In order to compare the performance between parallel and series models, this condition is assumed to be always satisfied so that both models are valid. The useful charge Q_C in C_P is expressed in equation (5) and the wasted charge Q_{wasted} for self discharging and charging C_P is given in equation (1). After Q_{wasted} is wasted for self-charging, V_{piezo} equals to $V_S + 2V_D$ (or $-(V_S + 2V_D)$) and the harvester starts to charge C_S. Therefore, the remaining charge going into C_S is the difference between Q_C and Q_{wasted}:

$$\begin{aligned} Q_{remain}(j\omega) &= Q_C(j\omega) - Q_{wasted} \\ &= 2C_P(\frac{jI_0R_P}{1 + j\omega R_P C_P} - (V_s + 2V_D)) \end{aligned} \tag{8}$$

After the rectifier becomes conductive, the voltage V_{piezo} attains the threshold and the equivalent circuit transforms to a PT in parallel with C_S and the PT can be regarded as a current

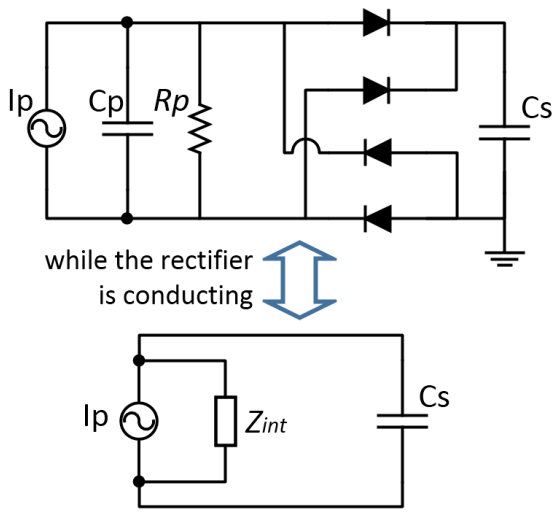


Fig. 4: Equivalent circuit while the full-bridge rectifier is conducting

source I_P in parallel with its internal impedance, as shown in figure 4. The internal impedance is the value that C_P and R_P connected in parallel, expressed as:

$$Z_{int}(j\omega) = \frac{1}{j\omega C_P} // R_P = \frac{R_P}{1 + j\omega R_P C_P} \tag{9}$$

The charge flowing into C_S can then be written as:

$$\begin{aligned} Q_S(j\omega) &= Q_{remain} \frac{Z_{int}}{Z_{int} + \frac{1}{j\omega C_S}} = Q_{remain} \frac{j\omega Z_{int} C_S}{1 + j\omega Z_{int} C_S} \\ &= Q_{remain} \frac{j\omega R_P C_S}{1 + j\omega R_P (C_P + C_S)} \\ &= \frac{2j\omega R_P C_P C_S}{1 + j\omega R_P (C_P + C_S)} \left(\frac{j I_0 R_P}{1 + j\omega R_P C_P} - (V_S + 2V_D) \right) \end{aligned} \tag{10}$$

While a full-bridge rectifier is employed, the capacitor C_S is usually chosen at a value much greater than the PT internal capacitor C_P ($C_S \gg C_P$), so that V_S can keep increasing steadily while external excitation is present. In addition, as R_P is usually at a value from hundreds of

$\mathrm{k}\Omega$ to several $\mathrm{M}\Omega$, hence $\omega R_P C_S \gg 1$. Therefore, equation (10) can be approximately written as:

$$Q_S \approx 2C_P(\frac{I_0 R_P}{\sqrt{1+\omega^2 R_P^2 C_P^2}} - (V_S + 2V_D)) \tag{11}$$

The voltage increase in C_S for harvesters connected in parallel in a half cycle is expressed as (where the symbol "//" means "parallel", equivalent to a monolithic harvester before splitting its electrode):

$$\Delta V_{S//} = \frac{Q_S}{C_S} = 2\frac{C_P}{C_S}(\frac{I_0 R_P}{\sqrt{1+\omega^2 R_P^2 C_P^2}} - (V_S + 2V_D)) \tag{12}$$

B. N-stage series model

While the electrode of the monolithic PT is segmented into n equal regions, the whole PT can be regarded as n individual harvesters connected in series. As the area of piezoelectric layer and electrode layer for each source is $\frac{1}{n}$ of the original PT, so I_{p1}, C_{p1} and R_{p1} for each small PT can be written as:

$$\begin{aligned} I_{p1} &= \frac{1}{n} I_P = \frac{1}{n} I_0 sin\omega t \\ C_{p1} &= \frac{1}{n} C_P \\ R_{p1} &= n R_P \end{aligned} \tag{13}$$

Calculations are started by considering only one PT and V_{piezo1} is the voltage generated by this source. As there are n sources connected in series, the total voltage is $V_{piezo} = \sum_{i=1}^{n} V_{piezo_i} =$

nV_{piezo1}. From equation (2), the condition to charge C_S is $V_{piezo} > 2(V_S + 2V_D)$, hence this condition for one individual source is:

$$V_{piezo1} > \frac{2}{n}(V_S + 2V_D) \tag{14}$$

From this equation, it can be seen that the threshold voltage is now lowered by a factor of n compared to the monolithic model so that harvester is much more likely to start operating at lower excitation levels. Therefore, the wasted charge for dis-charging and charging in one source in a half cycle is:

$$Q_{wasted1} = C_{p1}\frac{2}{n}(V_S + 2V_D) = \frac{2C_p}{n^2}(V_S + 2V_D) \tag{15}$$

The total charge flowing into C_{p1} in a half cycle is:

$$\begin{aligned} Q_{\frac{T}{2}1}(j\omega) &= \int_0^{\frac{T}{2}} I_{p1}\frac{R_{p1}}{R_{p1} + \frac{1}{j\omega C_{p1}}} = \int_0^{\frac{T}{2}} \frac{I_0}{n}\frac{nR_P}{nR_P + \frac{n}{j\omega C_P}} sin\omega t dt \\ &= \frac{2I_0}{n}\frac{R_P C_P}{1 + j\omega R_P C_P} \end{aligned} \tag{16}$$

Before the condition $V_{piezo1} > \frac{2}{n}(V_S + 2V_D)$ is met, the PTs are disconnected from C_S (as the diodes in the rectifier are not conducting). Once the $V_{piezo1} > \frac{2}{n}(V_S + 2V_D)$ is satisfied, all of the sources are connected together with C_S in series. At this time, C_S starts to be charged and the remaining charge flowing into C_S from each single source is:

$$Q_{left1}(j\omega) = Q_{\frac{T}{2}1}(j\omega) - Q_{wasted1} = \frac{2C_P}{n}(\frac{I_0 R_P}{1 + j\omega R_P C_P} - \frac{V_S + 2V_D}{n}) \tag{17}$$

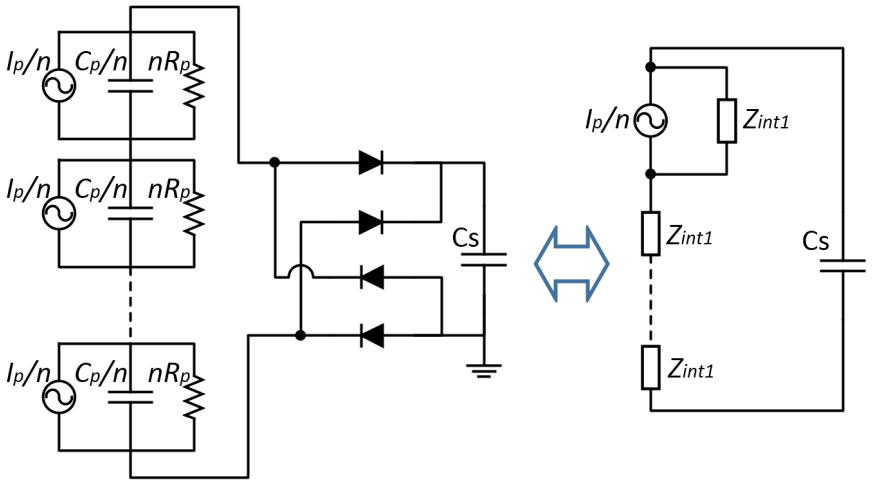


Fig. 5: Equivalent circuit for considering only one source in n-region series connected PTs while the rectifier is conducting

As only one harvester is considered, superposition theory can be used to turn off the current sources of all other $n-1$ harvesters. While the harvester is charging C_S, the equivalent circuit for one single source is shown in figure 5. The internal impedance for each of the source is:

$$Z_{int1}(j\omega) = \frac{nR_P}{1 + j\omega R_P C_P} \tag{18}$$

It can be seen that all the other $n-1$ impedances are connected in series with C_S, hence the total external impedance for one harvester is significantly increased. Hence, the ratio between the I_{ext} and I_{int} for each source being studied is:

$$\frac{I_{ext}}{I_{int}} = |\frac{Z_{int1}}{Z_{int1} + (n-1)Z_{int1} + \frac{1}{j\omega C_s}}| \approx \frac{1}{n} \qquad (as \quad C_S \gg C_P) \tag{19}$$

Therefore, the total charge flowing into C_S from one single harvester is:

$$Q_{S1} = |\frac{1}{n}Q_{left1}(j\omega)| = \frac{2C_P}{n^2}(\frac{I_0 R_P}{\sqrt{1+\omega^2 R_P^2 C_P^2}} - \frac{V_S + 2V_D}{n}) \tag{20}$$

While all the n individual harvesters are considered, the total charge flowing into C_S is:

$$Q_{S+} = \sum_n Q_{S1} = \frac{2C_P}{n}(\frac{I_0 R_P}{\sqrt{1+\omega^2 R_P^2 C_P^2}} - \frac{V_S + 2V_D}{n}) \tag{21}$$

Hence the voltage increase in C_S can be expressed as:

$$\Delta V_{S+(n)} = \frac{Q_{S+}}{C_S} = \frac{2C_P}{nC_S}(\frac{I_0 R_P}{\sqrt{1+\omega^2 R_P^2 C_P^2}} - \frac{V_S + 2V_D}{n}) \tag{22}$$

where the subscript '+(n)' means "n regions connected in series". From equation (6), the open-circuit peak-to-peak voltage of a PT is $V_{pp(open)} = \frac{2I_0 R_P}{\sqrt{1+\omega^2 R_P^2 C_P^2}}$. Therefore, the equation for the voltage increase of a n-region harvester connected in series can be rewritten as:

$$\Delta V_{S+(n)} = \frac{2C_P}{C_S}(\frac{V_{pp(open)}}{2n} - \frac{(V_S + 2V_D)}{n^2}) \tag{23}$$

By setting $n = 1, 2, 4, 8$, the voltage increase in V_S for different n can be written as:

$$\begin{aligned}
\Delta V_{S//(n=1)} &= \frac{2C_P}{C_S}(\frac{V_{pp(open)}}{2} - (V_S + 2V_D)) \\
\Delta V_{S+(n=2)} &= \frac{2C_P}{C_S}(\frac{V_{pp(open)}}{4} - \frac{(V_S + 2V_D)}{4}) \\
\Delta V_{S+(n=4)} &= \frac{2C_P}{C_S}(\frac{V_{pp(open)}}{8} - \frac{(V_S + 2V_D)}{16}) \\
\Delta V_{S+n=(8)} &= \frac{2C_P}{C_S}(\frac{V_{pp(open)}}{16} - \frac{(V_S + 2V_D)}{64})
\end{aligned} \tag{24}$$

C. Performance comparison

In order to compare the performance of the monolithic PT and 2-stage series model, $\Delta V_{S+(n=2)} > \Delta V_{S//(n=1)}$ is assumed:

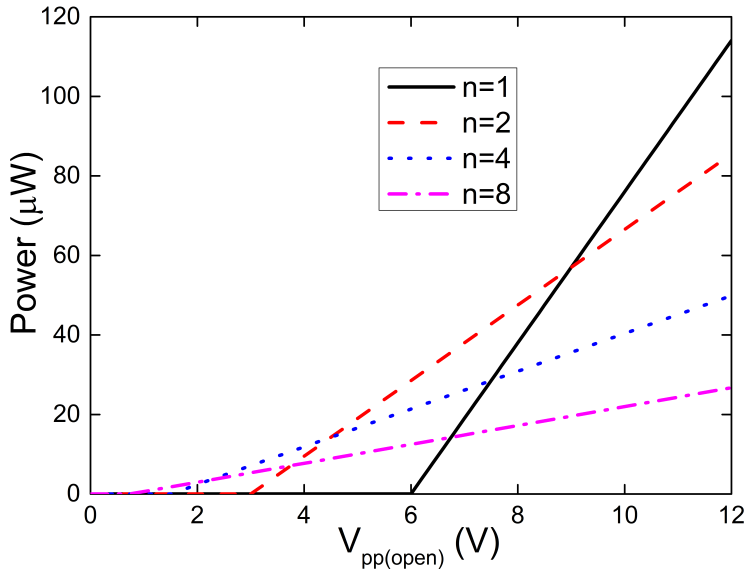
$$\begin{aligned} \frac{V_{pp(open)}}{4} - \frac{(V_S + 2V_D)}{4} &> (\frac{V_{pp(open)}}{2} - (V_S + 2V_D)) \\ V_{pp(open)} &< 3(V_S + 2V_D) \quad (for\ n = 2) \end{aligned} \tag{25}$$

Furthermore, $V_{pp(open)} > (V_S + 2V_D)$ should be satisfied for $n = 2$ so that the harvester can overcome the threshold voltage set by the full-bridge rectifier and start charging, so the condition for improving performance corresponding to splitting into 2 regions in series is:

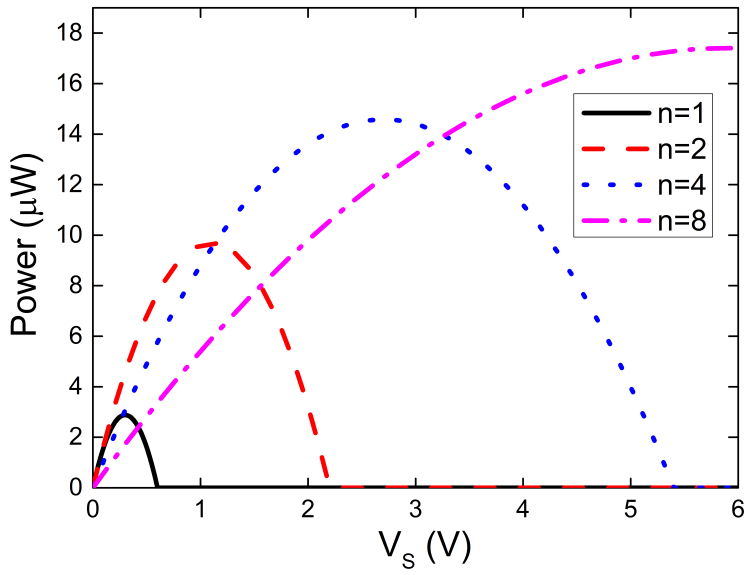
$$(V_S + 2V_D) < V_{pp(open)} < 3(V_S + 2V_D) \quad (for\ n = 2) \tag{26}$$

In terms of the monolithic model, the threshold is $V_{pp(open)} > 2(V_S + 2V_D)$ for starting charging. In addition, although the monolithic model can charge C_S while $2(V_S + 2V_D) < V_{pp(open)} < 3(V_s + 2V_D)$, the performance is worse than the 2-region series model. Using the same methodology, the conditions when $n = 4$ and $n = 8$ models have the best performance are calculated in equation (27). (Other values of n are also possible but the equations below facilitate comparisons with the measured results in the next section)

$$\begin{aligned} \frac{1}{2}(V_s + 2V_D) < V_{pp(open)} < \frac{3}{2}(V_s + 2V_D) \quad (for\ n = 4) \\ \frac{1}{4}(V_s + 2V_D) < V_{pp(open)} < \frac{3}{4}(V_s + 2V_D) \quad (for\ n = 8) \end{aligned} \tag{27}$$



(a) Theoretical output power while fixing $V_S = 2\,\mathrm{V}$ and varying excitation level



(b) Theoretical output power while fixing excitation level $V_{pp(open)} = 3.2\,\mathrm{V}$ and varying V_S

Fig. 6: Theoretical electrical power output of full-bridge rectifier for 1, 2, 4, and 8 series stages

TABLE I: Simulation results (symbol '-' means 'not working')

n=	1	2	4	8
$V_{pp} < 0.75V$	-	-	-	-
$0.75V < V_{pp} < 1.125V$	-	-	-	working
$1.125V < V_{pp} < 1.5V$	-	-	-	**best**
$1.5V < V_{pp} < 2.25$	-	-	working	**best**
$2.25V < V_{pp} < 3V$	-	-	**best**	working
$3V < V_{pp} < 4.5V$	-	working	**best**	working
$4.5V < V_{pp} < 6V$	-	**best**	working	working
$6V < V_{pp} < 9V$	working	**best**	working	working
$V_{pp} > 9V$	**best**	working	working	working

By assuming $V_S = 2\,\mathrm{V}$ and the forward threshold voltage $V_D = 0.5\,\mathrm{V}$, the threshold voltage for a monolithic model is $V_{TH} = 2(V_S + 2V_D) = 6\,\mathrm{V}$. Table I shows comparisons between different series stages and Figure 6a illustrates theoretical output power for different excitation levels ($0\,\mathrm{g}$ to $1\,\mathrm{g}$), which are presented as the open-circuit peak-to-peak voltage $V_{pp(open)}$, varying from $0\,\mathrm{V}$ to $12\,\mathrm{V}$, generated by the PT. This figure is generated from equations (24) while $V_{pp(open)}$ is considered as the variable, and other parameters are set as $C_P = 360\,\mathrm{nF}$, $C_S = 1\,\mathrm{mF}$ and $V_S = 2\,\mathrm{V}$. These values are chosen to match the experimental conditions.

After comparing the performances with a constant V_S while changing the external excitation (changing $V_{pp(open)}$), the output power with a constant excitation level and a varying V_S needs to be examined to find the maximum power points that the rectifier can attain with different series stages. Equation (23) shows the voltage increase in C_S in a half cycle of I_P, so the harvested energy by the full-bridge rectifier in a half I_P cycle can be written as:

$$\Delta E_{\frac{T}{2}} = \frac{1}{2} C_S((V_S + \Delta V_S)^2 - V_S^2) \tag{28}$$

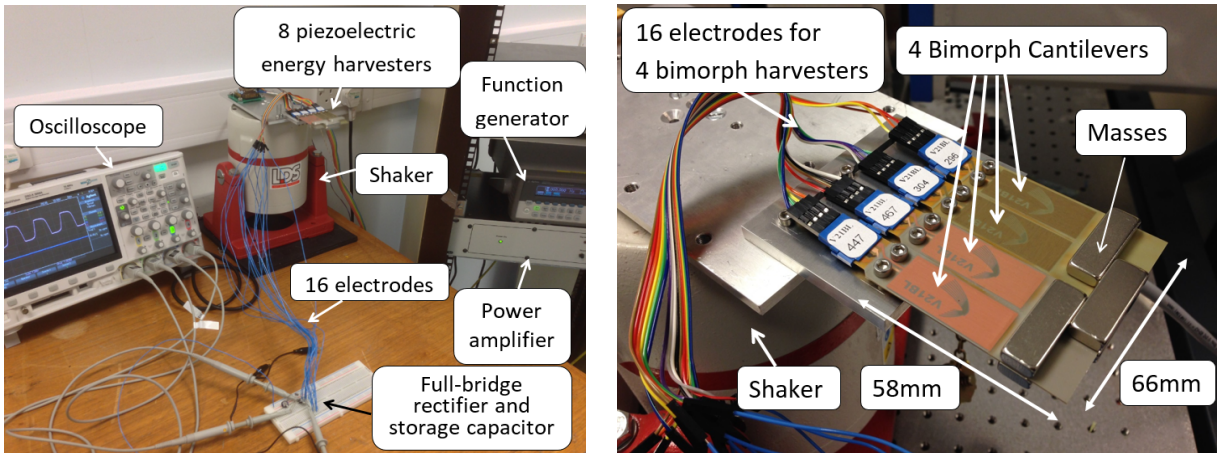
Hence, the output power is:

$$P = \frac{\Delta E_{\frac{T}{2}}}{T/2} = 2 f_P \Delta E_{\frac{T}{2}} = f_P C_S((V_S + \Delta V_S)^2 - V_S^2) \tag{29}$$

where f_P is the excitation frequency and ΔV_S is expressed in equation (23). The theoretical power output for $n = 1$, 2, 4 and 8 is plotted in Figure 6b. It can be seen that connecting in series significantly increases the peak output power. The models with $n = 2$, $n = 4$ and $n = 8$ can theoretically increase the power by around $3\times$, $4.5\times$ and $5.5\times$, respectively, compared to the monolithic PT. According to this figure, the peak output power seems to increase and tend to a limit for higher n. However, more series stages shift the V_S value corresponding to the peak power point to higher voltages. Hence, the voltage regulator circuits placed after the FBRs should be design to handle this high input voltage. Since most of wireless sensors typically require a stable supply between $1.8\,\mathrm{V}$ and $3.3\,\mathrm{V}$, the V_S values shown in figure 6b can meet this requirement well; in contrast, higher V_S may increase the complexity of designing voltage regulators.

V. Experiments and discussions

In this section, experiments are performed to validate the theoretical results and practically shows the performance improvement of the proposed approach. Figure 7a shows the experimental setup. The piezoelectric transducers used in the experiments consist of four cantilevered bi-morph PTs (Mide Technology Corporation V21BL), so there are eight available PTs for experiments.



(a) Experimental setup

(b) PTs used in experiments

Fig. 7: Experiment environment

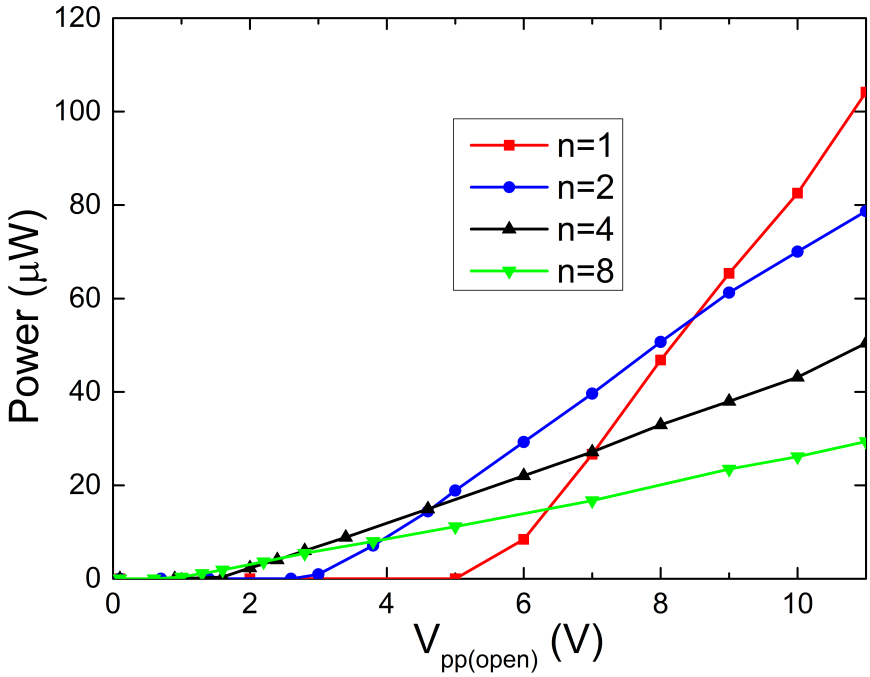


Fig. 8: Measured electrical output power while fixing $V_S = 2\,\mathrm{V}$ and varying excitation level (corresponding to base acceleration varying from $0\,\mathrm{g}$ to $1\,\mathrm{g}$)

The dimensions of the PTs are shown in figure 7b. The four bi-morph PTs are located side by side and their free-end tips are clamped together with masses in order to enable vibration in the same frequency, phase and amplitude. The resulting PT can, therefore, be considered as a monolithic PT with 8 electrode regions that can be connected in parallel or in series for different stages (n can be 1, 2, 4 or 8 in this implementation). The PT is excited on a shaker (LDS V406 M4-CE) at its natural frequency at $19\,\mathrm{Hz}$ and driven by a sine wave from a function generator (Agilent Technologies 33250A $80\,\mathrm{MHz}$ waveform generator) amplified by a power amplifier (LDS PA100E Power Amplifier). In the experiment, the storage capacitor connected at the output of full-bridge rectifier is a super capacitor of $C_S = 5.2\,\mathrm{mF}$. A full-bridge circuit is built using four diodes with a measured forward voltage drop of around $0.5\,\mathrm{V}$.

Experiments are performed with the number of series stages $n = 1,\ 2,\ 4$ and 8. Figure 8 shows the measured output power measured at the storage capacitor C_S for different excitation amplitudes (corresponding to $V_{pp(open)}$) with a constant $V_S = 2\,\mathrm{V}$. For low excitation levels, more series stages seem to perform better. For instance, when $V_{pp(open)} < 6\,\mathrm{V}$, the monolithic model ($n = 1$ while all the eight harvesters connected in parallel) does not harvest any energy as the threshold voltage is not attained. Furthermore, although all the four models can harvest energy for $6\,\mathrm{V} < V_{pp(open)} < 9\,\mathrm{V}$, the one with two series stages ($n = 2$) outputs the highest power. These results closely matches the theoretical calculations.

Figure 9 shows the measured electrical power while the excitation acceleration is kept at $0.2\,\mathrm{g}$ (corresponding to open-circuit voltage $V_{pp(open)} = 3.2\,\mathrm{V}$). The voltage V_S is varied from $0\,\mathrm{V}$ to $6\,\mathrm{V}$ to find the maximum power points for different series stages. From the figure, it can be found that the peak power values of $n = 2$, $n = 4$ and $n = 8$ models are 2.2×, 3.1× and 3.6× higher than the monolithic model ($n = 1$), respectively. The performance improvement of series

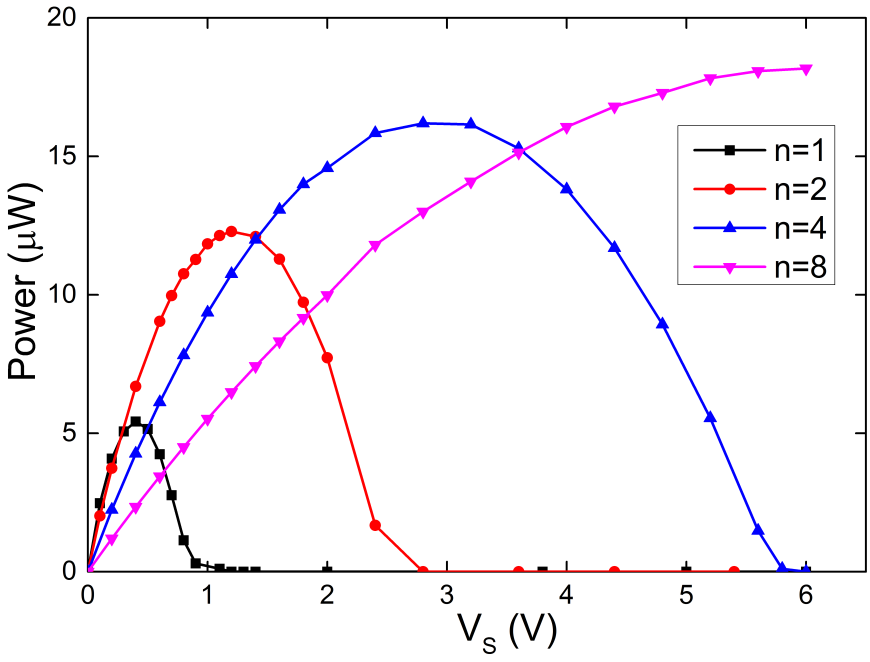


Fig. 9: Measured electrical output power while fixing excitation level and varying V_S (acceleration = $0.2\,\mathrm{g}$, $V_{pp(open)} = 3.2\,\mathrm{V}$, $V_D = 0.5\,\mathrm{V}$)

models approximately matches theoretical results shown in Figure 6b. The differences between theoretical and experimental results are due to non-ideal diodes used in measurements, which introduce associated leakage current.

Figure 10 shows the measured power efficiency for different series stages while the excitation level is swept from zero to $V_{pp(open)} = 12\,\mathrm{V}$. The efficiency is calculated as the power transfered into C_S divided by the raw measured power while PT is only connected to an impedance-matched resistor. The results indicate that each series configuration can attains its peak efficiency point under a specific excitation amplitude range. In other words, for a given implementation environment with a limited range of excitation amplitude, the number of series stages n can be determined to increase the output power and efficiency. While the harvester is implemented in a low excitation environment, more series stages (higher n) are preferred; otherwise, series stages

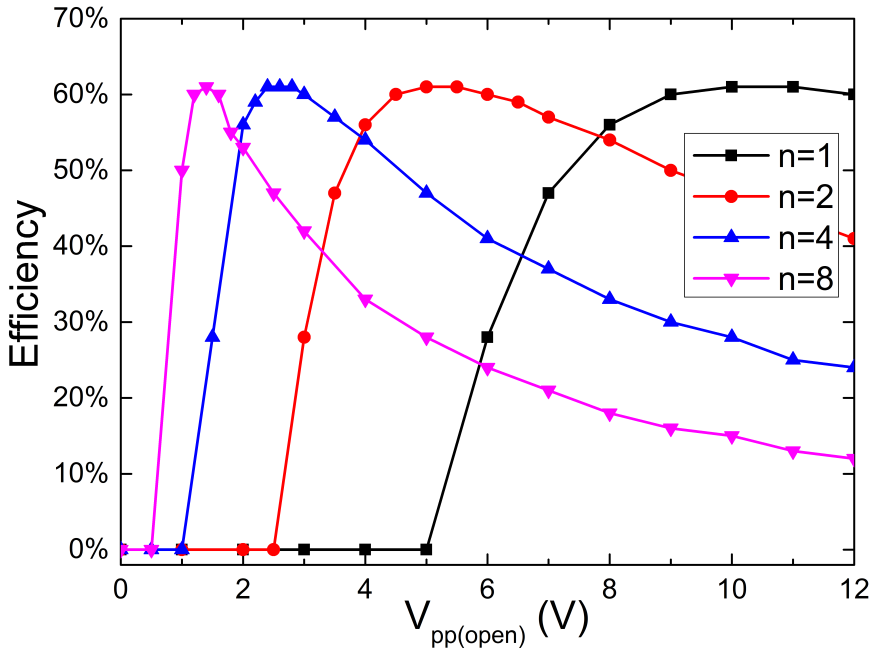


Fig. 10: Measured power efficiency while fixing $V_S = 2\,\mathrm{V}$ and varying excitation level

should be less (smaller n) or even not splitting the PT ($n = 1$). This approach requires a one-time configuration of the PT to determine the number of series stages before implementations and it passively improves power efficiency without employing any active circuits.

Table II compares the performance of the proposed series connection scheme against state-of-the-art active rectification implementations for piezoelectric vibration energy harvesting. The second line in the table indicates the type of implementation. The work in this paper does not employ additional circuits apart from a full-bridge rectifier, so there is no additional power consumption and the simplicity of the system offers the potential for increased stability. Line 5 of the table shows the peak-to-peak open-circuit voltage ($V_{pp(open)}$) produced by the PT for each work. This voltage depends on several factors, such as the excitation amplitude, piezoelectric materials, dimension of the device, internal capacitance, vibration frequency, etc. The last line of the table shows that splitting a monolithic PT into 8 regions connected in series can improve

TABLE II: Performance comparison with reported active rectifiers

Publication	[Krihely and Ben-Yaakov, 2011]	[Ramadass and Chandrakasan, 2010]	[Liang and Liao, 2012]	[Shaohua and Boussaid, 2015]	This work
Type of circuit implementation	Discrete	Integrated	Discrete	Discrete	Not required
Power consumption	35.2 µW	2 µW	Not given	20 µW	0
PT	RBL1-006 Piezo system	V22B Mide technology	T120-A4E-602, Piezo Sys	V22B Mide technology	V21BL Mide technology
Open-circuit voltage produced by PT	40 V	2.4 V	5.84 V	3.28 V	3.2 V
Internal capacitance C_P	60 nF	18 nF	33.47 nF	18 nF	42 nF
Vibration frequency	185 Hz	225 Hz	30 Hz	225 Hz	19 Hz
Performance compared with a monolithic PT in a full-bridge rectifier	3.2×	4×	2×	4.5×	3.6× *

(* 8 stages connected in series)

the harvested energy by up to 3.6× compared to the original monolithic harvester. According to Figure 9, splitting into more stages ($n > 8$) connected in series is believed to further increase the performance, although higher n is not experimentally verified in this paper. The performance boost form the series configurations indicates that using the proposed passive method can also achieve comparable performance compared to some active interface circuits, such as those listed in this table.

Compared to the four drawbacks mentioned in Section I for reported active interface circuits, the proposed series scheme does not employ any active circuits, inductors or capacitors other than four diodes (for a full-wave bridge rectifier). Hence the overall system volume can be significantly

decreased with increased stability. In terms of quiescent power loss, a simple full-bridge rectifier used in the proposed scheme does not consume any quiescent power (diode reverse leakage current is assumed to be negligible) so no energy is drained due to the interface circuit while no excitation is present. In addition, Figure 10 shows that the power efficiency of the proposed scheme is able to attain its peaks under a wide range of excitation amplitude for different series stages. Hence, in order to achieve an efficiency peak, the number of series stages can be pre-determined according to the average excitation amplitude where the system is implemented. This makes the energy harvesting system configurable to different implementation environments. Furthermore, as a simple full-bridge rectifier does not generate synchronized current pulses in the piezoelectric materials; hence, the proposed scheme is less subject to the SSD effect even for highly coupled PTs. Therefore, the mechanical vibration of the PTs will be less affected or damped, which extends the range over which the rectifier operates efficiently.

VI. Conclusion

This paper addresses that a full-bridge rectifier requires a relatively high excitation amplitude to extract energy from the piezoelectric harvester (PT). As a result, a significant part of the generated power is wasted due to the high threshold voltage. A passive scheme of splitting the electrode of a monolithic PT into n equal regions connected in series is proposed in this paper to lower the threshold voltage and increase power output under low input excitation levels. Comparing with active interface circuits, this scheme significantly decreases system volume and increases the output power without employing active components or consuming extra power. In addition, the PTs employing this method are less affected by SSD effect. By using this principle, PTs can be designed to have n equal regions connected in series, of which the number n should

be pre-determined by considering the ambient excitation amplitude for the selected application environment.

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