High Step Up DC-DC Converter topology for PV Systems and Electric Vehicles

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Thesis summary

This thesis presents new high step-up DC-DC converters for photovoltaic and electric vehicle applications. An asymmetric flyback-forward DC-DC converter is proposed for the PV system controlled by the MPPT algorithm. The second converter is a modular switched-capacitor DC-DC converter, it has the capability to operate with transistor and capacitor open-circuit faults in every module. The results from simulations and tests of the asymmetric DC-DC converters have suggested that the proposed converter has a 5% to 10% voltage gain ratio increased to the symmetric structures among 100W – 300W power (such as [3]) range while maintaining efficiency of 89%-93% when input voltage is in the range of 25 – 30 V. they also indicated that the soft-switching technique has been achieved, which significantly reduce the power loss by 1.7%, which exceeds the same topology of the proposed converter without the soft-switching technique. Moreover, the converters can maintain rated outputs under main transistor open circuit fault situation or capacitor open circuit faults.

The simulation and test results of the proposed modularized switched-capacitor DC-DC converters indicate that the proposed converter has the potential of extension, it can be embedded with infinite module in simulation results, however, during experiment. The sign open circuit fault to the transistors and capacitors would have low impact to the proposed converters, only the current ripple on the input source would increase around 25% for 4-module switched-capacitor DC-DC converters.

The developed converters can be applied to many applications where DC-DC voltage conversion is alighted. In addition to PVs and EVs. Since they can ride through some electrical faults in the devices, the developed converter will have economic implications to improve the system efficiency and reliability.

Key Words: DC-DC converter, High step up, asymmetric, switched-capacitor, fault tolerance.

DEDICATION

To my beloved parents, Diqiu He and Zhiping Zeng,
For their love and patience.

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Finally, I dedicate this thesis to my parents for their love, patience and support. Their encouragement and understanding are my pillar to focus and persist in Ph.D. study.

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List of Abbreviations

AC	*alternating current*
DC	*direct current*
PV	*photovoltaic*
IEA	*international energy agency*
EPIA	*European photovoltaic industry association*
UPS	*uninterrupted power supply*
EV	*electric vehicle*
HEV	*hybrid electric vehicle*
SUDCC	*step-up DC-DC converter*
PWM	*pulse-width modulation*
CCM	*continuous current mode*
DCM	*discontinuous current mode*
SEPIC	*single ended primary inductor converter*
PCB	*printed circuit board*
IGBT	*Insulated Gate Bipolar Transistor*
MOSFET	*Metal-Oxide-Semiconductor Field-Effect Transistor*
HVDC	*high voltage DC*
DAB	*dual active bridge*
CI	*coupled inductor*
EMI	*electromagnetic interference*
SC	*switched capacitor*
THD	*total harmonic distortion*
MMSCC	*modular multilevel switched capacitor DC-DC converter*
VMC	*voltage multiplier cell*
VMR	*voltage multiplier rectifier*
QBC	*quadratic boost DC-DC converter*
HBC	*hybrid boost DC-DC converter*
ZVS	*zero voltage switching*
ZCS	*zero current switching*
OCF	*open circuit fault*
SCF	*short circuit fault*
BJT	*Bipolar Junction Transistor*
ESR	*equivalent series resistance*
ESL	*equivalent series resistance*
PID	*proportion-integral-derivative*
MPPT	*maximum power point tracking*
P&O	*perturbation and observation*
INC	*incremental conductance*
RFI	*radio frequency interference*
V	*voltage*
I	*current*
C	*capacitance*
L	*inductance*
R	*resistance*
S	*switch/transistor*
T	*transformer*

N	*turns in transformer end*
D	*duty ratio*
T	*time of a period*
G_{vc}	*transfer function of voltage error amplifier*
G_{vd}	*transfer function of the main circuit converter*
G_{pwm}	*transfer function of the PWM generator*
V_{saw}	*amplitude voltage of the saw-tooth waveform*

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Chapter 1 Background Information

With the rapid development of technology, economy and the growth of population, the overall demand of energy has been increasing dramatically. According to the latest statistics and forecast: 2007 to 2030 from International energy agency (IEA), the world's energy demand has an average annual growth of 1.6% [1].

1.1 Renewable energy systems

Even at current speed of increasing demand of energy, the traditional energy source such as fossil fuel and natural gas can only last for decades [1]. Considering the environment pollution from the traditional energy source, the world is facing a serious problem causing by energy shortage crisis in the foreseeable future [2]. At present, solar energy and wind power are considered to construct the future energy landscape, and the utilizations of the alleged clean energy are significant approaches to solve the problem of energy crisis. In industry and academics, developing more options of clean, efficient and renewable energy has become an important topic in the global range [3]. The solar power has many merits when considered as a renewable energy: it can only be generated during the day, so the maximum power demand has good correlation with the timing of the power generation; also, the solar energy can be considered to be infinity, and has less influence on regional restriction. With these advantages, the solar energy can play as one of the main roles in the stage of future power market [4][5]. As it turns out that photovoltaic (PV) is the most commonly applied technique to harvest

solar energy, therefore, PV technology has become a research hotspot of scholars around the world. According to the European photovoltaic industry association (EPIA), the cumulative global PV capacity in recent years is shown in Fig 1-1 [1]. It can be deduced that the PV capacity would keep growing in the near future. However, the technique for generalize the PV system still has its drawback at present. One of the many technical bottlenecks of photovoltaic power generation system is: the photovoltaic cell components are packed with a feature of wide range of variation in low output voltage [32].

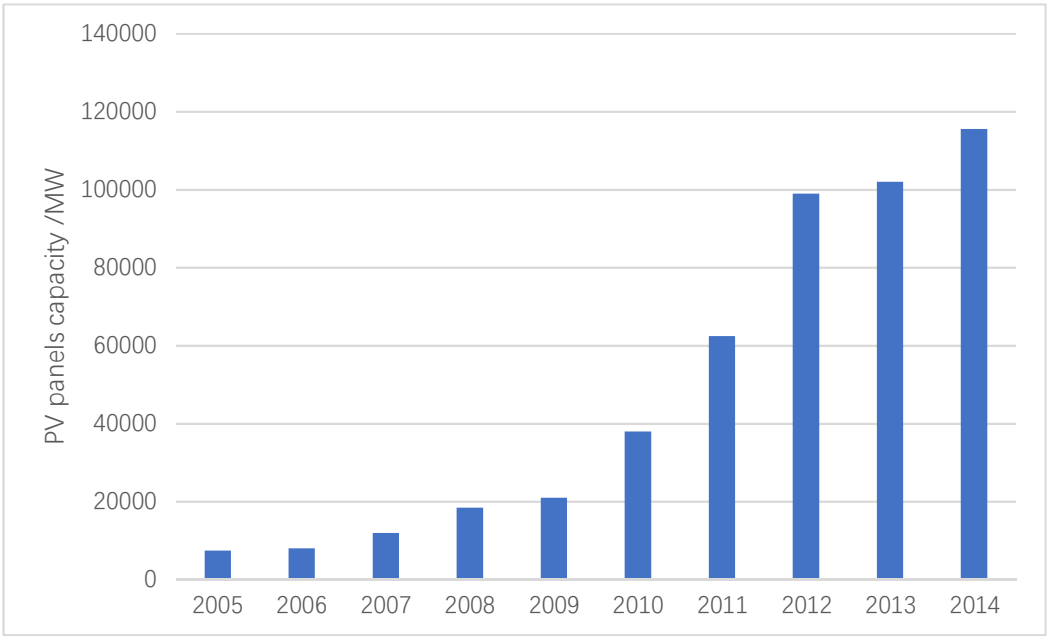


Fig 1-1. Global PV panels capacity [1]

For a normal PV farm, it usually embedded with a lot of photovoltaic panels in series to generate a high DC voltage, and then the DC voltage is to be inverted into AC voltage to integrated with the grid. In practical application, due to the natures of photovoltaic components themselves, the inevitable differences from each other and the influence of shadow block of can cause in-balanced output. A large number of

photovoltaic panels connected in series would cause imbalanced output for each photovoltaic module in respect of efficiency.

Fuel cell, as another kind of advanced clean energy, has features as: large energy density, high efficiency power generation, mobility, near-zero environment pollution and non-restricted by environmental factors [126]. The manufacture of fuel cells and its power generation technology have been highly valued in developed countries such as the United States, Europe and Japan [6]. Currently, the fuel cell is mainly applied in household electronics, portable devices, communication power supply, uninterrupted power supply (UPS), electric vehicles, distributed new energy grid-connected power generation, ship, aerospace and military defense, etc. Fuel cell, similar to PV panel, is another power source that variates in a wider range of low voltage. If multiple fuel cells were to be connected in series to obtain higher DC output voltage, it is more likely that the one failure in any single cell would demise the entire system. On the other hand, the wide range of output voltage can also be a great challenge for the optimal design of single-stage grid-connected inverter. While using two levels of generation structure can divided the whole system control and system utilization into two individual stages, which is easier to realize. In this case, two level generation has attracted more attention from low-power vehicle manufacturer [7]–[9]. Fig 1-2 and Fig 1-3 are diagrams of two-

stage generation systems based on PV, fuel cells and battery respectively [8]–[11].

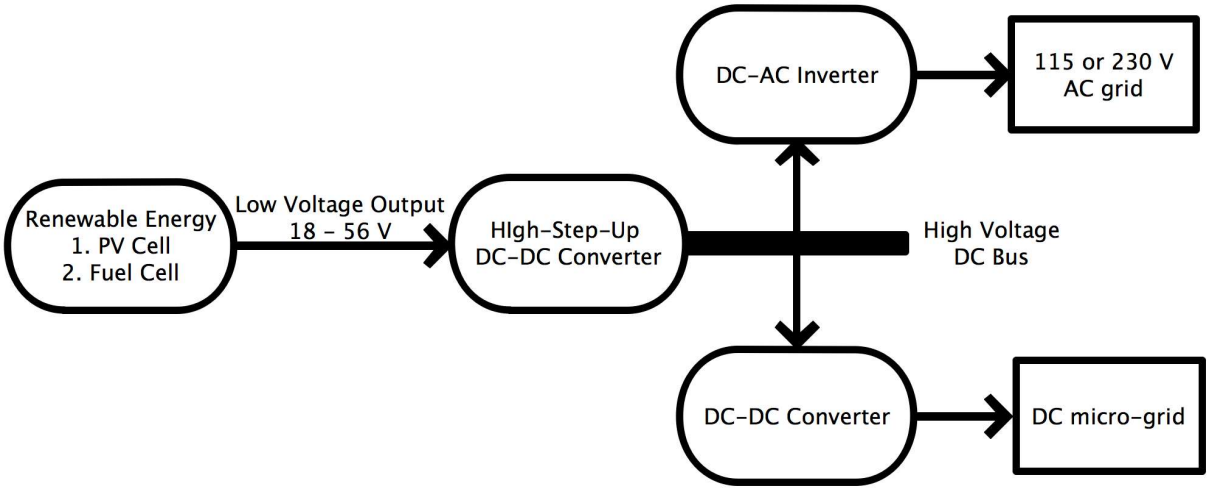


Fig 1-2. PV cell and fuel cell generation system

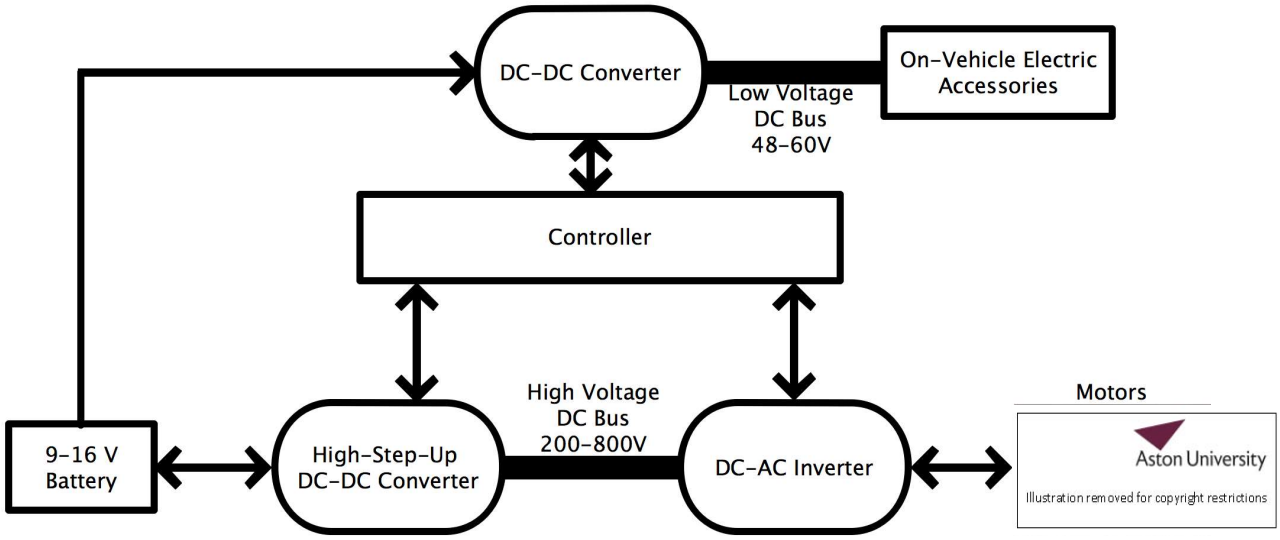


Fig 1-3. Electric vehicle system

1.2 Electric vehicles

The pace of lives in modern city has never been faster than before. It results in rapid social development, as well as dramatic growth in car ownership, which produces a lot of automobile exhaust every year for traditional internal combustion locomotive. The exhaust makes the air pollution increasingly serious.

The electric vehicles can alleviate the resources and environment pressure in the automobile industry to a certain extent. Compared with the traditional automobile, electric cars have great potential in environmental protection since they release negligible exhaust to the environment. The power resource of electric vehicles comes from the grid, where the environment pollution can be dealt with intensity, which is far better than the scenario which each vehicle pollutes the environment individually.

The traditional electric vehicles are powered by single energy source for the whole systems, which has the advantages such as zero emission and low noise. However, the development of the electric vehicle is restricted by the development of the battery, which has the following problems:

(1) The battery power is relatively low, when comparing to fossil fuel, the volume of the battery would be larger than the fuel tank for traditional vehicle. When the electric vehicle is under overload working conditions (such as start, acceleration and climbing), the battery needs to release large instantaneous power. In this case, the instantaneous discharge current of the battery would be too large, to lead to a reduction the life of the battery [157];

(2) The battery charging and discharging cycles are limited, and the replacement cost of the battery would be expensive;

To improve the service life of the battery and to ensure the sufficient power when electric vehicles operate under heavy/over-load, the combination of battery and other energy power supply system came to the attention of the researchers, one of which is

ultra-capacities. An outstanding advantage of ultra-capacitor is its high-power density, which can be used as an auxiliary energy source when the electric vehicle is under heavy/over-load and can be used as an energy recovery device for electric vehicle when braking [156]. However, the ultra-capacitors cannot be installed directly with the battery, they must be connected through boost DC-DC converter.

Boost DC-DC converter is one of the core-components of energy management system for electric vehicles. Like the application in renewable energy system mentioned before, DC-DC converter boosts the battery voltage to support the electric motors, high-step-up DC-DC converter is one of the many choice for the electric motor, namely hybrid car [12]–[14], the elevator [15], urban railway system [16] and so on.

Urban driving environment require the vehicles to accelerate and break frequently, which reduces the efficiency of the engine and increases energy consumption. Electric cars can reduce the energy consumption substantially. The advanced technology of Europe, the United States, Japan and other countries have started the development of electric cars very early [17]. Toyota, as the pioneer of EVs industry, was the first the successor to make a huge profit from its electric vehicles, classic Prius hybrid [17], other hybrid electric vehicles followed: Estima, Crown, Insight and Civic. The study in United States of electric vehicles lags that in Japan, and the truly mass-produced electric vehicles are only the limited to certain individual models from Ford and General Motors. However, Tesla has become a hot topic in recent years, as it is now one of the leading enterprise in pure EVs industry. It developed several models and built charging

station around the world. There are massive number of batteries embedded into one Tesla electric vehicle, which makes the high-step-up voltage conversion technique very suitable to them. Electric vehicle charging stations have been built throughout the country of France. The EV promotions can have national support, including various incentive subsidies and the establishment of national electric vehicle coordination committee, making France one of the most successful countries as the pure EVs industry [17].

Under normal circumstances, single PV cell, fuel cell or battery boosts low voltage level up to 200-400 V or higher voltage level to meet the demand [17]. In addition, the space station and satellite system usually need to boost the PV cell voltage from 16-28 V to 100V through high gain DC-DC converter to supply electricity to the entire system [17]. Therefore, the study of high voltage gains and high efficiency boost converter is of great significance for the rapid development of new renewable energy generation system and EVs.

1.3 Organisation of the thesis

This paper introduces two novel topologies for high-step-up DC voltage boosting applications. Both of them are packed with fault tolerance operation capability. The first topology is an asymmetrical flyback-forward converter, this topology is proposed for renewable power system that does not include reverse power flow function, such as PV panel and fuel cell system. The second topology is proposed for electric vehicles with low battery voltage and high motor voltage requirement, it is a modularized system.

All the modules in the systems are identical, which makes the system easy to be repaired. The more modules can boost the voltage into higher level, and with its bypass capability, the output voltage can be regulated in a large range with small duty ratio variation. This feature would avoid the extreme duty ratio situation, which would make it hard for controller to generate such PWM waveform. Moreover, each module can function as an output voltage source, for a multi-voltage system like electric vehicle, this new topology would be promising.

Chapter 2 Literature review

Step-up DC-DC converters (SUDCC) have numerous applications in daily life and industrial solutions. They variate from low-power devices as power conversion for control circuit to a megawatts-level system, such as High voltage DC (HVDC) power system. The principle of this kind of topology is to transfer energy to passive components (inductors and capacitors) and release the energy to the load. During the process, the passive components generate magnetic field (inductor) or electric field (capacitor) so that voltage drop can occur across the elements. In different combination, lower voltages can be boosted to higher voltages. The development of SUDCC has benefited from the breakthrough of semiconductor in 1950s and 1960s [18].

SUDCCs are originated from pulse-width modulation (PWM) boost converters. They inherit several features from PWM boost converters to make them suitable for application in a wide-range output solution. A SUDC-DC converter can operate at controllable wide range operation under continuous current mode (CCM) or discontinuous current mode (DCM) and controlling the duty ratio applied to the active switching devices [19], [20]. CCM is more preferable in most circumstances [158]. However, SUDC-DC converters have some drawbacks that have been studied to overcome in decades: hard switching causing overshot when switching the semiconductor, reverse recovery energy, non-minimum-phase, low power density due to the existence of passive components. Some disadvantages have been key aspects

to promote researchers to discover new topologies and control algorithms, especially for high performance inquiry is required [21]–[25].

When considering reliability, volume and efficiency of SUDCCs, some basic topologies are more than capable for lower requirement. They are discussed in this part of literature review, e.g. boost, single ended primary inductor converter (SEPIC). If galvanic isolation is necessary, fly-back, forward, push-pull and bridge circuits are still useful structure and also reviewed. In addition, review also contains techniques that fulfill higher operation demand such as: soft-switching, interleaved, voltage multiplier cells, switched capacitor, coupled inductor and so on [25-152].

The first part of the review will be structured based on the application and requirements, e.g., galvanic isolation capability, bidirectional power transmission capability, minimum phase feature. Second part is the discussion of different boosting techniques. Third part is the overview for the discussed topologies and techniques.

2.1 Categories of step-up DC-DC converters

This section is the classification in terms of topology. Fig 2-1 indicates the step-up DC-DC converter techniques classification in this thesis. Detailed descriptions of these categories are presented in following parts.

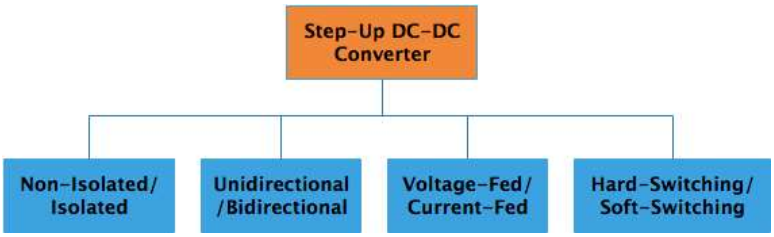


Fig 2-1. Technique of step-up DC-DC converter.

2.1.1 Unidirectional/bidirectional topologies

In general, unidirectional SUDCCs only allow energy transferring from the input end to output end, [25-53], they serve the purpose of only energy consumption such as control circuit on PCB board, sensors, battery-based household application and so on. One textbook layout of such SUDCC is illustrated in Fig 2-2 (a). As shown, the key elements those two types of converters are: one inductor, one active switching device (IGBT or MOSFET) and one diode. In such topology, the power flow is unidirectional because only one active switch is applied in the circuit. The present of diode would block any current that flow back from the output end. In this case, this kind of DC-DC converter is single-quadrant, i.e., the direct of voltage and current in unidirectional converter can only be positive. However, the bidirectional structure, shown in Fig 2-2 (d), consists of two semiconductors (IGBTs or MOSFETs) and one inductor. It can be treated as both buck and boost converter, which depends on the duty ratio of the semiconductors. In this case, bidirectional DC-DC converters are two-quadrant, i.e., the direction of the voltage is only positive, while current has an extra negative option. When bidirectional power follow is not necessary, unidirectional structure is always preferable, owing its less complicated structure and simpler control requirement.

The development of power system and renewable energy increase the demand of application of energy storage system (counter the power demand and power generation). Both unidirectional and bidirectional DC-DC converter are appreciated in numerous situations such as PV panel and fuel cell for the unidirectional DC-DC

converter; battery bank, automotive transportation, aerospace, uninterruptable applications, High voltage DC (HVDC) systems and so on [26]–[54]. Fig 2-3 shows the isolated version of those categories, there are two H-bridge in both kinds. The high frequency transformer in both of these further enhance the boosting capability owing to the turns ratio. The isolated unidirectional structure has a diode rectifier on the secondary end to limit the current direction, while bidirectional one has symmetry structure that would enable bidirectional power flow. The latter, so called dual active bridge (DAB) converters are preferable in high voltage/power application [37], [44]–[46]. The voltage of the isolated unidirectional DC-DC converter is uncontrollable while DAB is controlled by adjusting switching angle of the two H-bridge to control the phase of two AC voltage across both sides of the transformer.

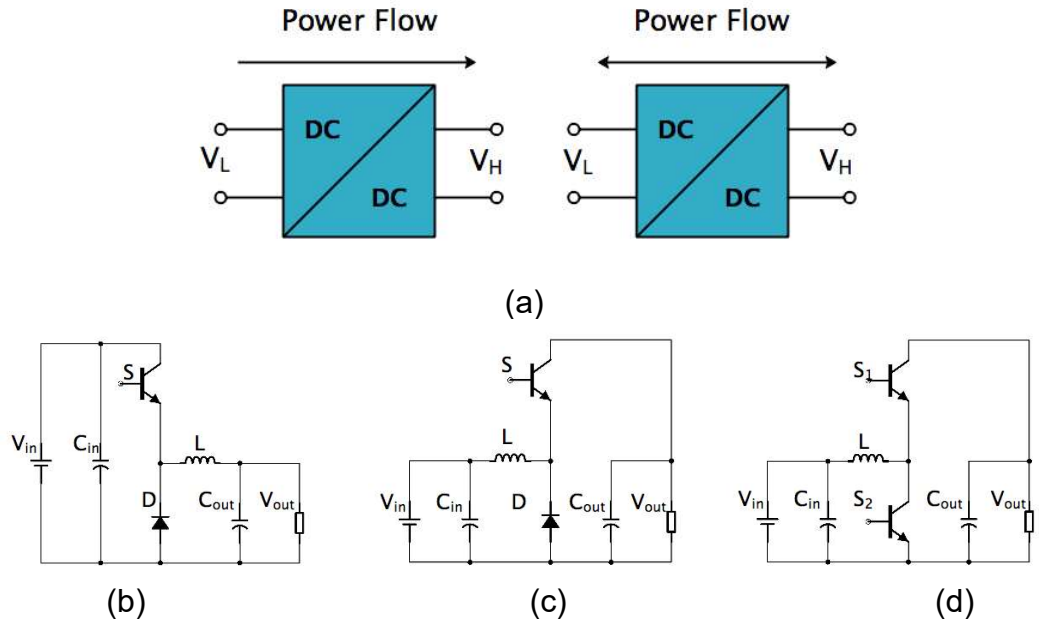
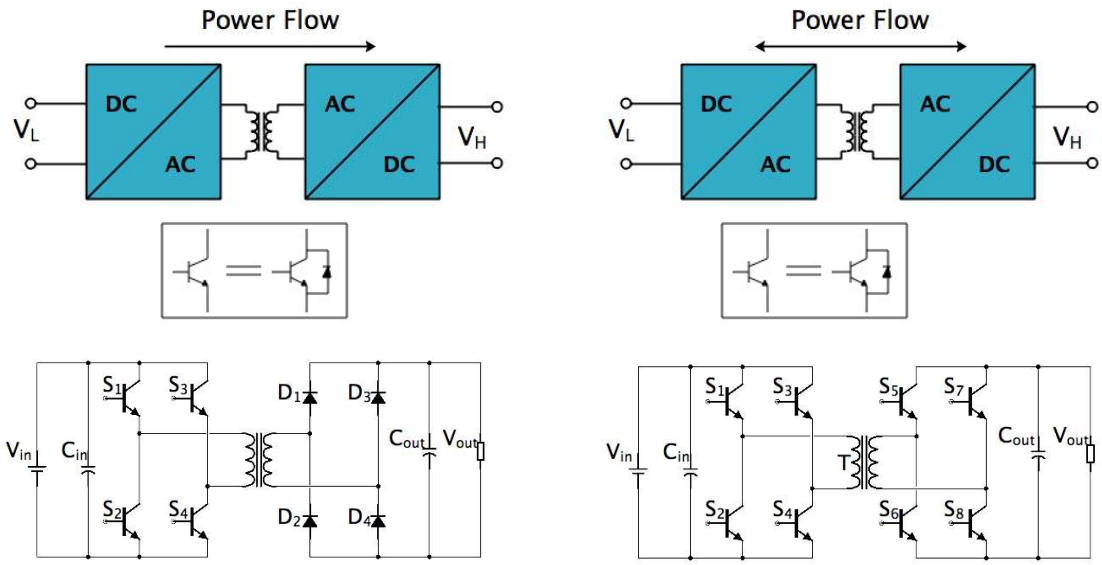


Fig 2-2. Indications of non-isolated unidirectional and bidirectional DC-DC converter
(a). Power flow indication of uni- and bi- directional DC-DC converter;
(b). unidirectional buck DC-DC converter;
(c). unidirectional boost DC-DC converter;
(d). bidirectional boost DC-DC converter.



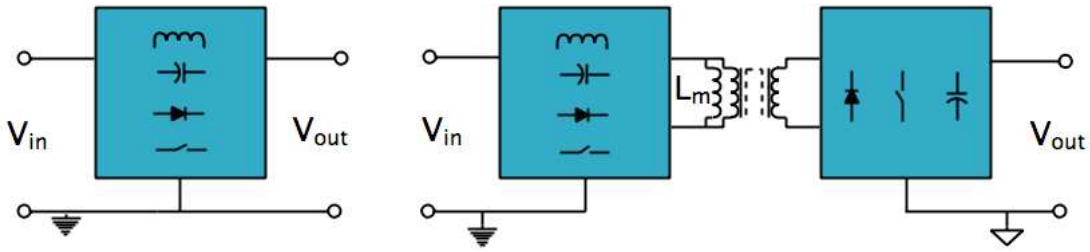
(a) (b)

Fig 2-3. Indications of isolated unidirectional and bidirectional DC-DC converter
(a). unidirectional DC-DC converter;
(b). bidirectional DC-DC converter.

2.1.2 Isolated/non-isolated topologies

This classification method is one of the basics, non-isolated converters are where from commercial product to industrial application. Fig 2-4 presents the structures of non-isolated and isolated DC-DC converters. The non-isolated converters are low-cost and efficient due to its simple structure and straight-forward control. They shine on the feature of low volume when compare to isolated DC-DC converters where magnetic component is necessary [24], [25]. Many studies on the non-isolated DC-DC converter have been carried out for lower cost, smaller volume, higher efficiency [25-91] since non-isolated DC-DC converter has many applications. However, when dealing with high power level with high voltage, basic non-isolated DC-DC converters are not working well. Because the voltage boosting is limited by the magnetic saturation of inductor. To acquire higher voltage boosting ratio from basic non-isolated converter,

more power will be dispatched in term of heat due to magnetic saturation. In order to overcome the drawback, coupled inductor (CI) is introduced in the circuit. CI can be employed in isolated and non-isolated DC-DC converter [25-91]. In the non-isolated converter, the features applied in turns ratio. The turns ratio can directly change the voltage ratio from windings on the same magnetic core. Once parameter of CI is finalized, the voltage ratio would not change, the voltage tuning process is still based on tuning duty ratio of the active switch. It introduces one dimensionality “N” into the voltage ration equation when designing the circuit. In this case, the voltage can be boosted to a higher level.



(a) (b)

Fig 2-4. General indication of non-isolated and isolated DC-DC converter.
(a) non-isolated DC-DC converter;
(b) isolated DC-DC converter.

In isolated DC-DC converter one more feature that is applied from the CI is electrical isolation. This feature in essential to the power grid and some other application that safety, reliability, low noise and low electromagnetic interference (EMI) are required. The power gird would require electrical isolation to protect the grid from the faulted parts to avoid entire system fault and other application that would not allow to be damaged from power failure also demand electrical isolation [38], [39], [45], [50], [55]–[73]. And specifically, in [39], [40], [68]–[71], [73]–[92], these literatures have reported the CI is applied for various applications. In such applications, DC voltages are

transformed into AC voltages to the primary ends of the coupled inductors. The secondary ends generate AC voltages and then rectified into DC voltages. These converters usually operate at high frequency to reduce the volume and loss of the converter by reducing current ripple.

The detailed classification of isolated converter is made in terms of topology, i.e., fly-back, forward, push-pull, half and full bridge converters. In all of these categories, fly-back converter is distinctive: energy transmission in other topologies from the primary end to secondary end is simultaneously with the charging stage of primary end, however, in fly-back converter, those two processes are separated, i.e., the inductor would store the energy and then release it to the secondary end. For this reason, fly-back converters are not capable for high power level, due to the limitation of inductor energy storage capability. However, because of the unique characteristic, the secondary ends of fly-back converters can be easily extended in parallel.

2.2 High Step-Up DC-DC converters

High step-up converters are always a challenge, due to its unique high voltage gain requirement. They have many applications from power grid system to automotive transportation. In PV system, the normal PV panel output voltage is from 10 to 42 V, in order to connect to the grid, the voltage should be first boosted to over 311-volt and then inverted to AC voltage. Normal DC-DC converters would not have the capability for that voltage gain. Different techniques are employed to achieve that function. Fig 2-5 shows the brief classification of the boost technique. Five major categories are

presented: switched capacitor, voltage multiplier, switched inductor, magnetic multi-stage/-level.

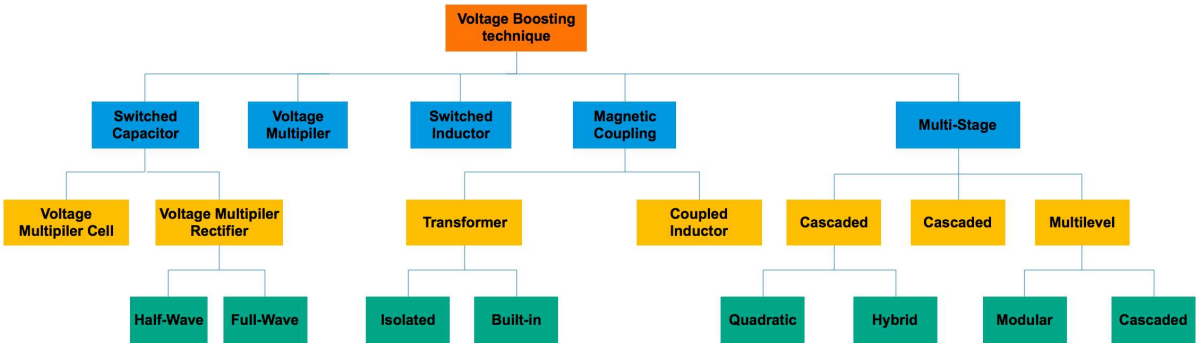


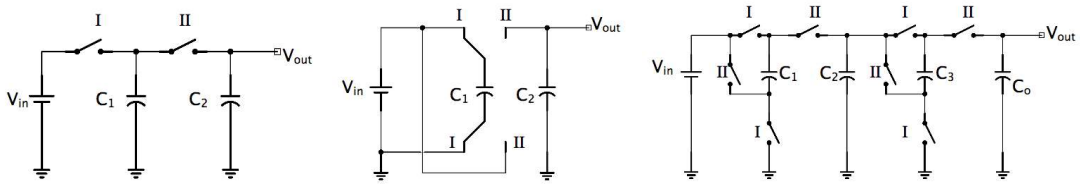
Fig 2-5. Classification of voltage boosting techniques.

2.2.1 Switched capacitor (charge pump)

The switched capacitor (SC) is one of the most popular voltage boosting technique, one of the common modification of charge pump (Fig 2-6(a)). The principle operation of the technique only involves electric energy transfer, it does not have electric-magnetic energy conversion. As shown in Fig 2-6 (a), the switch I and switch II complement each other. When capacitor C_1 is charged, C_2 is discharge. Until steady state, all the capacitor voltages would be the same with the input voltage, and so it is with the load voltage [93].

The charge pump circuit is only capable for energy transfer, other than any regulation on the output voltage. The idea of switched capacitor then is raised. SC structure also include the charging and discharging process of the capacitor as charge pump structure. In the first stage, the capacitor is charged. And in second stage, together with the input source, the capacitor is discharging, transferring energy to the load. As shown in Fig 2-6 (b), the voltage of the load would be N times of the input source (N is

the number of switched capacitor stages in the converter) [94]. However, the switches in the basic switched capacitor structure are all two-way switch, which is highly impractical for commercial product. So that the structure doubler switched capacitor is proposed [95]. The operation philosophy of the doubler as the same with the basic structure. The difference is that the function of two single pole double throw switches is realized by four single pole single throw switches. Since then, different topologies have been introduced to reduce the number of switches, shown in Fig 2-6(d)-(g) [94]–[96]. Taking the structure in Fig 2-6(g) for example, the structure is proposed by M. S. Makowski in 1997 [96]. The structures of each stage are identical; however, the control is complementary in adjacent stages. The voltages of each capacitor in different stage are different. In detailed analysis, voltage of C_1 is V_{in}, and V_{c2} is $2V_{in}$. When switch I is closed, C_1 is charged with V_{in} and the output voltage is equal to $V_{c2}+V_{in}$ and when switch II is closed, C_2 is charged with $V_{c1}+V_{in}$, which is $2V_{in}$. Concluding from above, the output voltage is $3V_{in}$. The output voltage would submit to Fibonacci number, respect the number of switched capacitor stages. Although this kind of SC has high voltage gain, the voltage stresses in the SC cells are problematic as they become high and vary from each other.



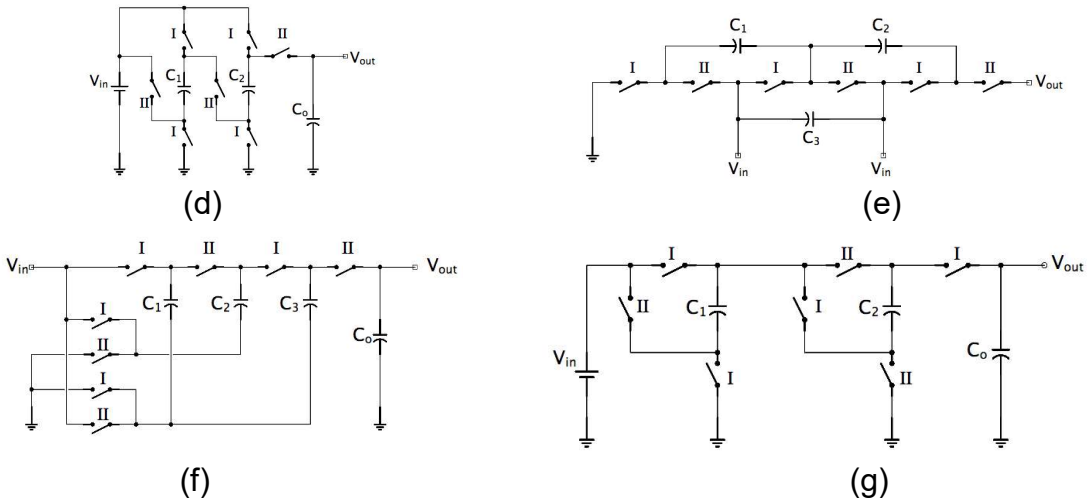
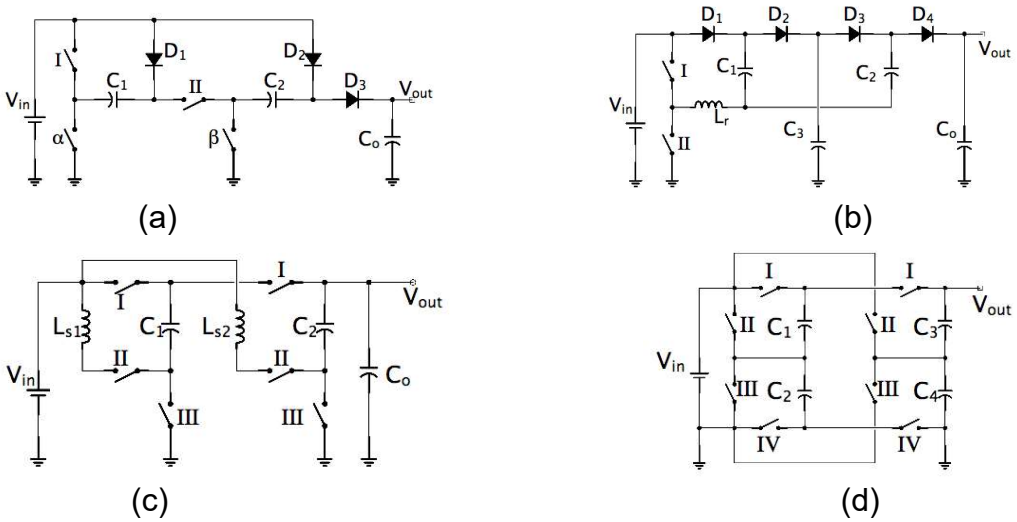
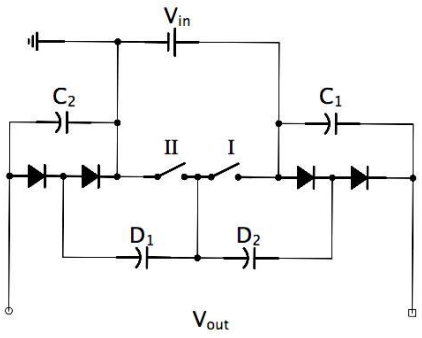


Fig 2-6. Structure of charge pump and switched capacitor.

High current gradient is the inherent drawback of this kind of SC structure, as they have no passive element to restrict the current variation. High current gradient would cause high current ripples, which would degrade power density and efficiency. Solution towards this kind of situation has been mentioned in [97], which is adding inductor into the circuit to achieve soft-charging.





(e)

Fig 2-7. Variant of different switched capacitor

In 1999, H. S. H. Chung present a switched capacitor DC-DC converter with continuous input current, as the input source is always connected in the circuit. In Fig 2-7(a), when S_1 turns off and all QS_n turn on, the input source is charging the capacitors through the diodes. And in the complementary phase, the input source, together with the capacitors, is transferring energy to the load [98]. And similar topology is reported in [99], in which, the diodes are replaced by active switches. In Fig 2-7(b), a small inductor is inserted into the circuit to minimized the current ripple and achieve ZCS. The voltage of C_{nb} is the sum of the voltages of C_{n-1b} and C_{na}. Fig 2-7(c) reveals modular multilevel switched capacitor DC-DC converters (MMSCC), the converters use a modular structure, and the control of each cell is identical. This type of DC-DC converters has fault tolerance operation potential [29], [30]. Fig 2-7(d) and (e) present two symmetrical MMSCC, which can be easily extended with more modules for higher voltage gain. In (d), the number of active and passive component is significantly larger than what is in (e). The former one has better performance regarding current stress, while and latter would be cost friendly since only two active components are applied. As conclusion, a summary of the reported SC converters is listed in Table 2-1.

Table 2-1. Summary of the reported SC converter

Converter in Fig. 8	No. of switches	No. of capacitors	No. of stages	Feature
(a)	*4*	*3*	*2*	*•Continuous input current*
(b)	*2*	*4*	*2*	*•ZCS* *•Less current ripple* *•Only two active switches*
(c)	*7*	*3*	*2*	*•Multiple input/output capability* *•Fault tolerance capability*
(d)	*8*	*5*	*2*	*•low current stress* *•Extension capability*
(e)	*2*	*5*	*2*	*•Only two active switches* *•Extension capability*

2.2.2 Voltage multiplier

Voltage multiplier is [100] a structure consists of only passive components (diodes and capacitors). It is a very efficient technique regarding voltage boosting for the simple structure and low cost. They can be divided into two categories in terms of structure: the first one is non-isolated voltage multiplier cell (VMC) and second one is isolated voltage multiplier rectifier (VMR). The VMCs are usually placed after the main switch to reduce the voltage stress of the main switch, while VMRs are placed in the secondary end of the coupled inductors/transformers. Due to the existence of the diodes, all converters that employ voltage multiplier is uni-directional. Voltage multiplier cell (VMC)

1. Voltage multiplier cell (VMC)

VMCs are widely applied for high voltage gain DC-DC converters for their simple structure and easy implementation [101]. Their operation relies on the bidirectional current follow to the SC cell. Fig 2-8(a) to Fig 2-8(c) present VMCs with only capacitors and diodes, known as switched capacitor (SC) VMCs [102]–[104]. Other topologies have more complicated structure, they can be implemented with active switches (Fig 2-8(d) [105]), or with inductors (Fig 2-8(e) and Fig 2-8(f) [102]–[104], [106], [107])

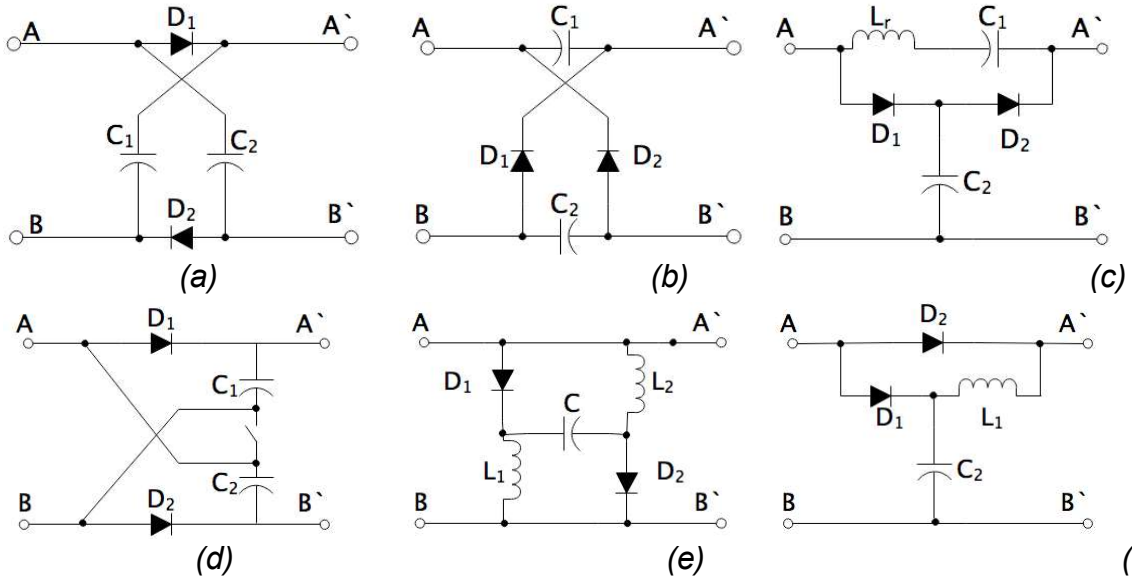


Fig 2-8. Different VMCs

The first three topologies in Fig 2-8 have the same voltage gain: *(1 + D)/(1 - D)*, where D is the duty ratio. The latter two structures (Fig 2-8(e)(f)) and the one shown in Fig 2-8(c), implemented with inductors, can achieve ZCS in the main circuit, for the LC oscillation circuit in the structures. The reported VMCs have similar function, and the principle of operation are similar as well, the Table 2-2 summaries the number of components required in each topology and their feature.

Table 2-2. Summary of reported VMCs

VMC	Voltage Gain	NO. Passive component	No. Active component	Feature
Fig 2-8(a)	*(1 + D)/(1 - D)*	*4*	*0*	*NA*
Fig 2-8(b)	*(1 + D)/(1 - D)*	*4*	*0*	*NA*
Fig 2-8(c)	*(1 + D)/(1 - D)*	*4*	*0*	*ZCS capability*
Fig 2-8(d)	*(1 + D)/(1 - D)*	*4*	*1*	*NA*
Fig 2-8(e)	*(2+ D)/(1 - D)*	*5*	*0*	*ZCS capability Higher voltage gain*
Fig 2-8(f)	*1/(1 - D)*	*4*	*0*	*ZCS capability*

2. Voltage multiplier rectifier (VMR)

Voltage multiplier rectifier is another classification of voltage multiplier. Unlike VMCs, the VMRs rectify sinusoidal or rectangular AC voltage into different capacitors and multiple the voltages together to achieve higher voltage gain. This kind of multiplier only boost input voltage to its integer multiple.

Fig 2-9(a), Fig 2-9(c) and Fig 2-9 (e) present three fundamental types of VMRs. In Fig 2-9(a), known as the half wave voltage multiplier (HW-VMR), the input voltage would charge C_1 in its negative period, and, together with C_1, charge C_2 in its positive period. Thus, the output voltage is 2 times of the input ones. Fig 2-9(b) reveals the extend capability of the HW-VMR [68], [108]–[111]. In the second one (in Fig 2-9(c)), known as full wave voltage multiplier rectifier (FW-VMR), the positive and negative periods of the input voltage charge C_1 and C_2 respectively and the voltages of C_1 and C_2 are the directly represent the output voltage [59], [72], [78], [79], [89], [112]–[114]. The last one (in Fig 2-9(e)) is a hybrid version of the previous converter. In the positive and negative

period of the input voltage charge C_1 and C_2 respectively, and in the next positive period, the input voltage charges the output capacitor with C_1 and C_2 [74], [90], [115], [116]. Fig 2-9(d) and Fig 2-9(f) are the extended version of Fig 2-9(c) and Fig 2-9(e)

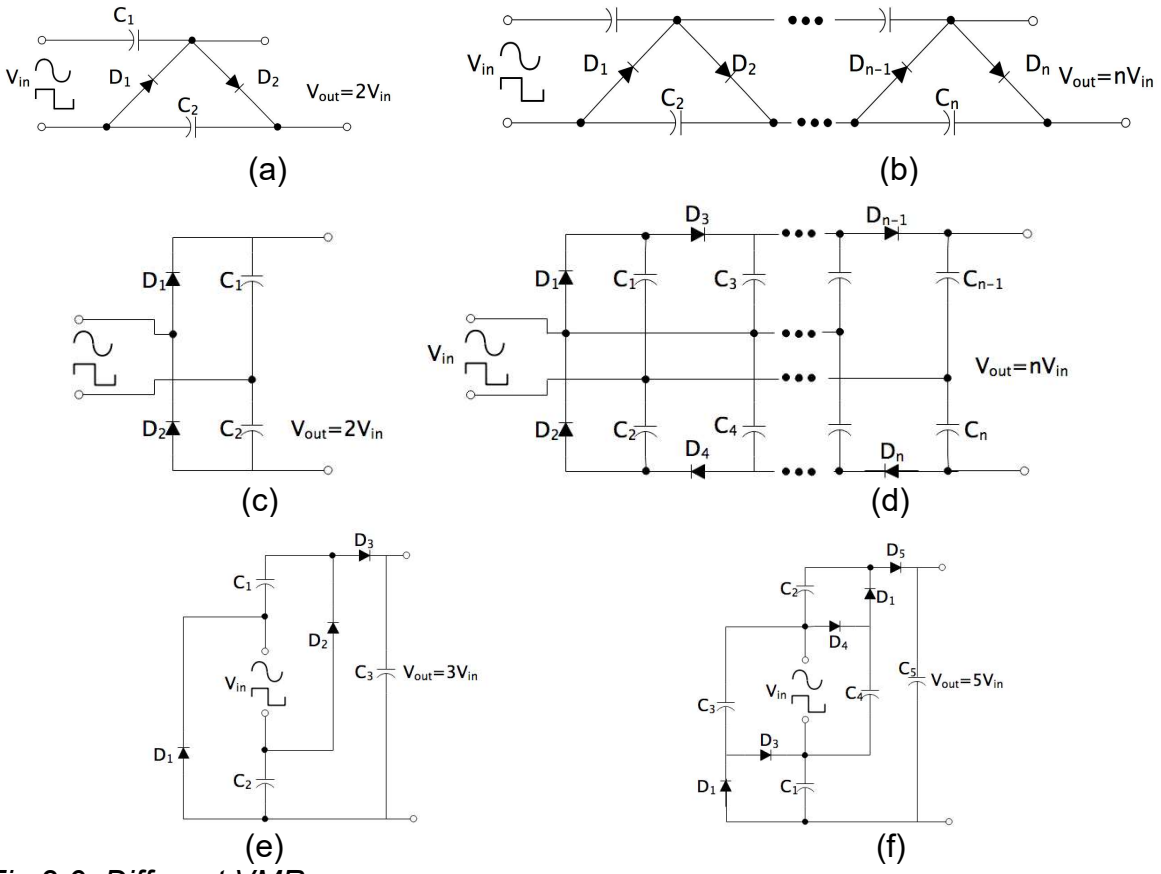


Fig 2-9. Different VMRs

The voltage gain ratio is based on the number of the capacitors applied in the system. There are some other modifications, which may reduce the voltage stress of the component by increasing the number of capacitors for the same voltage gain. the summary of the VMRs is presented in

Table 2-3.

Table 2-3. Summary of the VMRs

VMR	Output voltage	Output capacitor voltage stress	Output diode voltage stress
HW-VMR	$2V_{in}$	V_{out}	V_{out}
FW-VMR	$2V_{in}$	$V_{out}/2$	$V_{out}/2$
Hybrid	$3V_{in}$	V_{out}	V_{out}

2.2.3 Magnetic coupling

Magnetic coupling is a very popular voltage boosting method, it transfers energy regardless of the cable connection. The winding which convert magnetic energy to electric energy can be treated as a voltage source that can be convenient to boost voltage. Despite of the benefits, magnetic coupling is always facing the challenge of leakage inductance, no matter it is transformers or coupled inductors. The transformers and coupled inductors are basically the same things. The principle of these two are identical, apart from a few parameter differences. The transformers are meant to deliver energy from one winding to another, without any energy storing process. However, coupling inductors will have airgaps to increase the energy storing capacity, which can be useful in the converter that magnetic energy storage is necessary, i.e., flyback converter. In the following sections, papers regarding these two magnetic will be reviewed.

2.2.4 Transformer

Techniques of transformer is one of the popular research topic in the high-step up DC-DC converter, due to the introduction of the additional dimension known as turns ratio into the voltage gain function. However, the purpose of transformer is not necessary to be electric isolation. The technique itself then can be divided into two categories: isolated and non-isolated.

1. Isolated transformer-based DC-DC converter

Fig 2-10(a) has indicated the basic structure of isolated version. Generally speaking, the output of this type would require rectifier to converter AC voltage from the secondary end of transformer into DC voltage [19], [20]. Basic applications include bridge structure, forward structure, and push-pull structure, presenting in Fig 2-10(b)(c)(d) respectively. Researches are reported for boosting capabilities and optimizing features. Improvements such as soft-switching has been reported [67]. New topologies such as dual active bridge topologies, dual active half bridge and other topologies have been reported in [37]–[43], [52]–[54], [59], [80], [81], [114], [117]–[119].

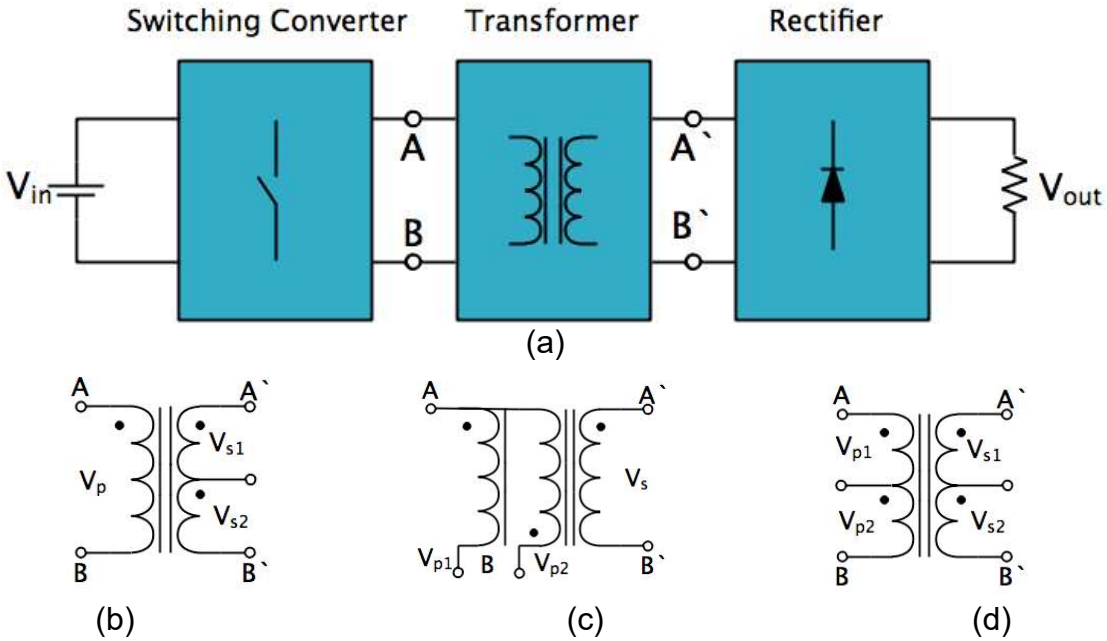


Fig 2-10. Configuration of isolated transformer-based DCF converter

2. Non-isolated transformer-based DC-DC converter

Non-isolated version to utilize transformer has more flexibility than the isolated version in terms of topology. The applications are usually implemented with capacitor to lift the

voltage. the ideal of the non-isolated circuit is derived from the isolated circuit. The energy transfer can be divided into direct energy transfer and magnetic coupling energy transfer. Some examples from the literature are shown in Fig 2-11 [113], [120]–[122].

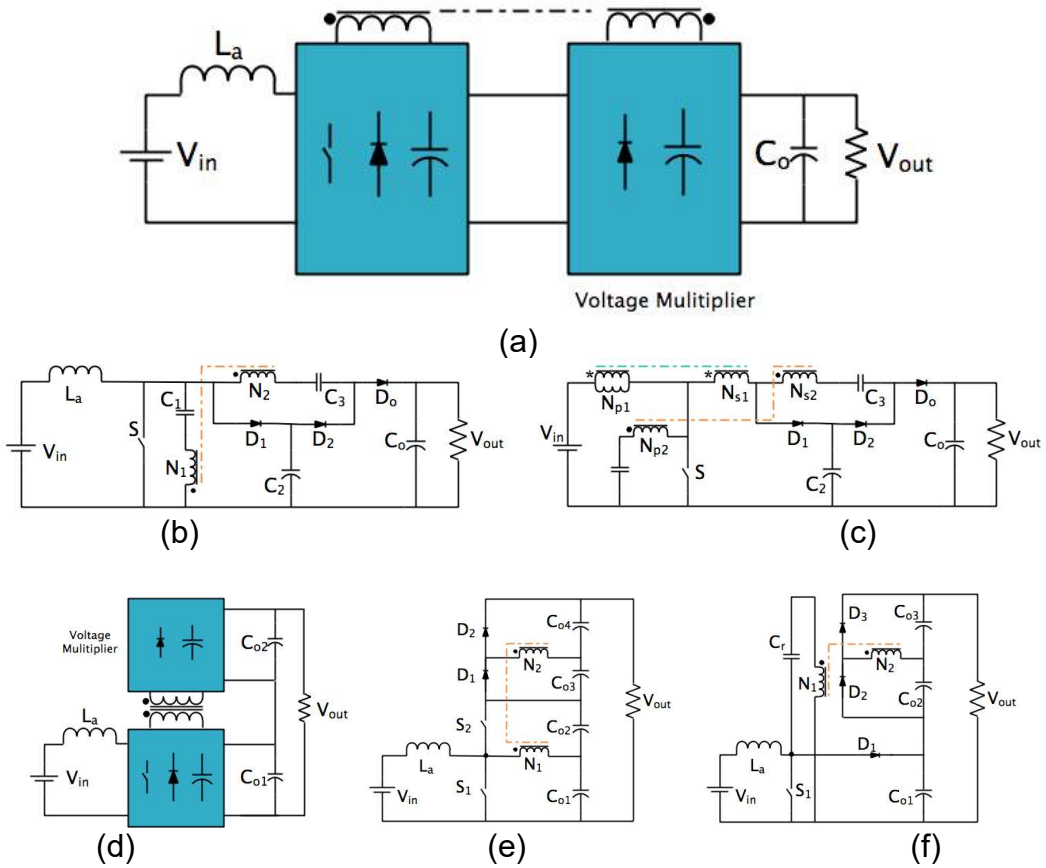


Fig 2-11. Non-isolated transformer-based DC-DC converter

2.2.5 Multi-stage

Multi-stage is a well-known technique for voltage boosting and eliminating harmonic. It can be realized by applying serval identical or similar module, alone with other voltage boosting techniques mentioned above. In this section, multilevel converters and interleave structure are introduced.

3. Cascaded converter

Cascaded converters utilize cascading connection for increasing voltage gain. In [123], schematic cascaded DC-DC converter has been introduced. Based on Fig 2-12, more than one DC-DC converters are connected front to end one another. The structures or types of these converters can be identical (quadratic boost) or different (hybrid boost).

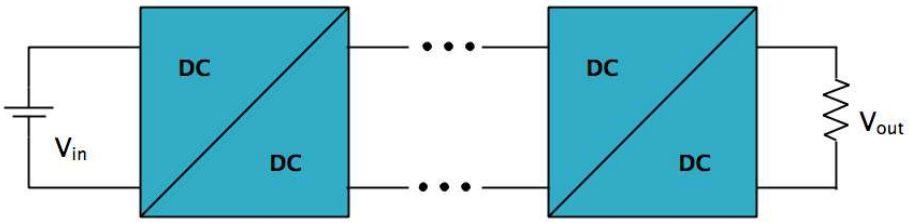


Fig 2-12. Schematic general cascaded DC-DC converter in [25]

a. Quadratic boost DC-DC converter (QBC)

Fig 2-13(a) presents a fundamental structure of the quadratic boost DC-DC converter reported in [124]. it consists of two identical boost DC-DC converters, which can be divided into two stages. The first stage can operate in high frequency for the lower voltage stress across the transistor. However, the voltage stress across the transistor in the second stage is higher. In order to limit the switching losses, the operation frequency in the second stage should be lower than the first stage. Fig 2-13(b) is an improved structure of the general structure. It integrates two switches into one switch and an extra diode. [125] presents the extended structure of Fig 2-13(b) and deduced buck converter version of this structure. To reduce the voltage stress of the semiconductors, [126] illustrates a three-level quadratic boost DC-DC converter shown in (c). With this feature, it can be applied in scenario where high voltage gain is required.

Other modifications of quadratic boost DC-DC converters are presented in Fig 2-13(d), (f), (g) and (h). The more DC-DC converters integrated in QBC, the wider the voltage various range it is capable of. QBC are preferred by lower power application where sophisticated magnetic designs are unnecessary. In general, quadratic boost converters contain one inductor and one capacitor in each module.

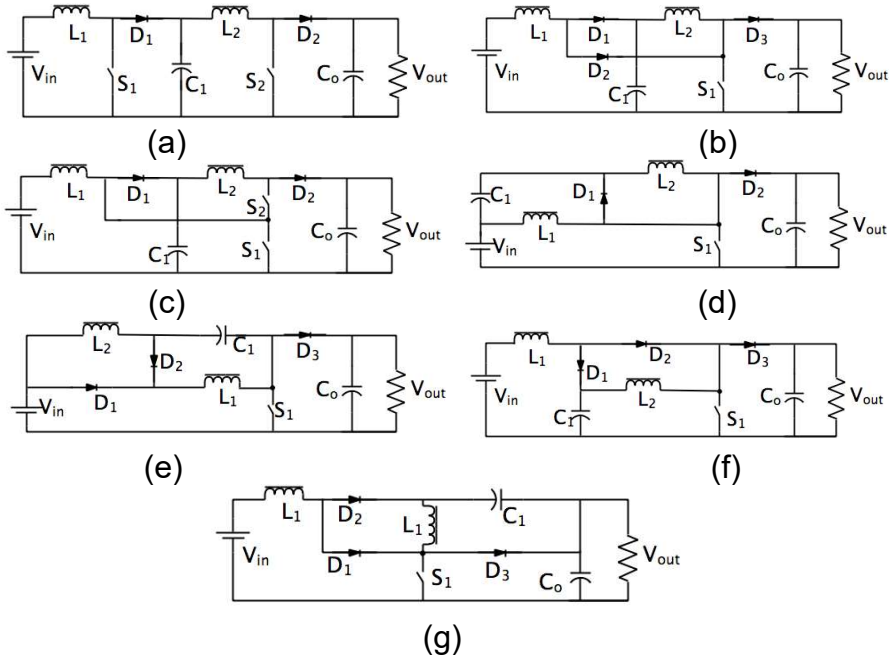


Fig 2-13. Quadratic boost DC-DC converters.
(a) two-level cascaded boost converter;
(b) quadratic boost converter;
(c) three-level quadratic boost converter;
(d) to (g)some basic quadratic boost DC-DC converter.

b. Hybrid boost DC-DC converter (HBC)

Fig 2-14 (a) is a general display of HBC, for quadratic boost structure combined with other voltage boosting techniques. In [127], apart from the quadratic boost structure, the output voltage is further boosted by coupled inductors, the second end of the coupled inductors is used to charge the extra output capacitor, which is connected in

series with the original one (shown in Fig 2-14 (b)). In [128], another structure utilizing coupled inductors is reported. As shown in Fig 2-14 (c), the primary end and secondary end of the coupled inductors are connected in series to increase the voltage of the original output capacitor. More layout of the HBCs are presented in Fig 2-14 (d) and (e). The former one consists of interleaved structure for the first stage and three-level boosting techniques in the second stage. And the later one is the combination of buck-boost converter and half-bridge converter. The HBCs have the potential of cascading different types of DC-DC converter structures or boosting techniques. Compared with traditional DC-DC converters, HBCs can be implemented with more components to gain high voltage ratio, however, increase the overall cost of the system.

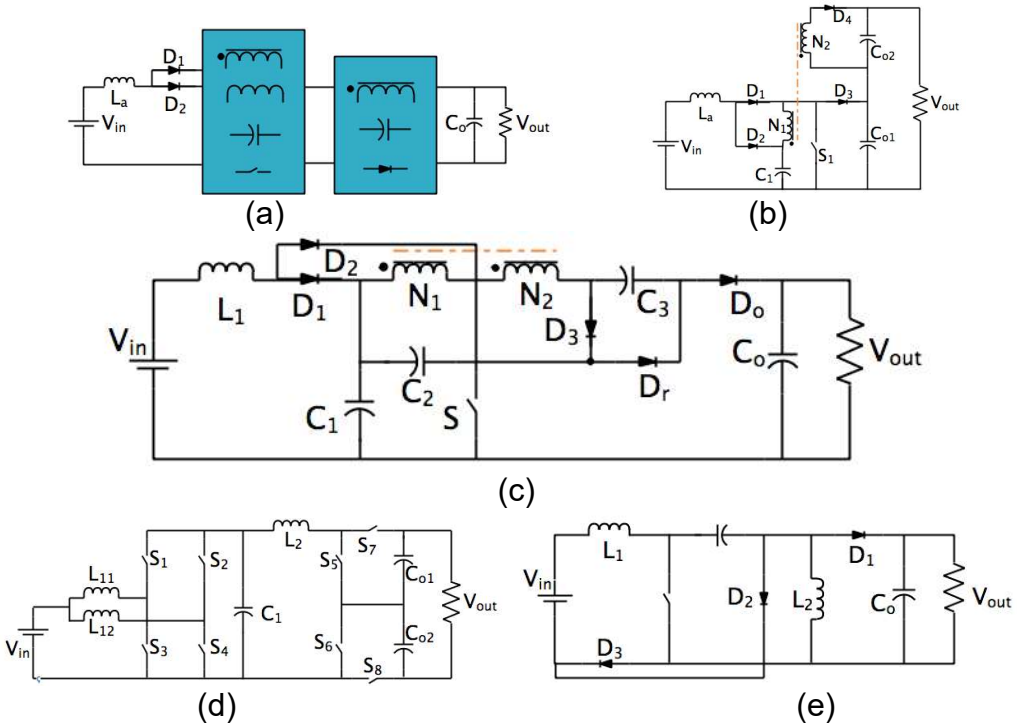
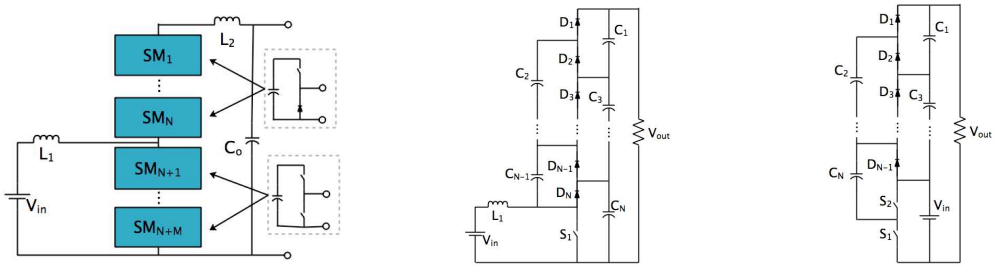


Fig 2-14. Hybrid boost DC-DC converter.
(a) General layout of HBC;
(b) HBC presented in [127];
(c) HBC presented in [128];
(d) HBC presented in [129];
(e) HBC presented in [130].

4. Multilevel converter

Multilevel technique is popular in both industry and academia due to its significance in high voltage application. By applying this structure, magnetic component can be decreased or eliminated. For single input structure, the mechanism of voltage boosting of general multilevel converters lies with capacitor. Unlike cascaded system, most module in multilevel converter only consists of semiconductors and capacitors. One particular structure is boost converter with multiple sub-modules shown in Fig 2-15 [131]–[133]. Fig 2-15(a) reveal the general structure of this kind of multilevel converters. Fig 2-15(b) presents a PWM boost converter based multilevel converter. As shown, the even number of the capacitors are used as voltage lift of the odd number capacitors. The odd number capacitors are connected in series as output capacitor group to provide output voltage. In Fig 2-15(c), similar structure is presented, the difference with the previous one is the absence of the inductor.



(a) (b) (c)

Fig 2-15. Layout multilevel converter.
(a) General layout the multilevel converter in [212];
(b) Multilevel converter shown in [160];
(c) Multilevel converter shown in [161].

Fig 2-16(a) indicates examples of the multilevel converter [28]. The sub-modules of this topology only consist of transistors and capacitors, thus, there is no magnetic component in the entire circuit. In Fig 2-16(b), this structure is the base of DC-DC

converter boosting function. Another module structure is revealed in Fig 2-16(c). This structure consists of two capacitors and four switches [30]. Due to the switched-capacitor structure, the features description and analysis are presented in previous section.

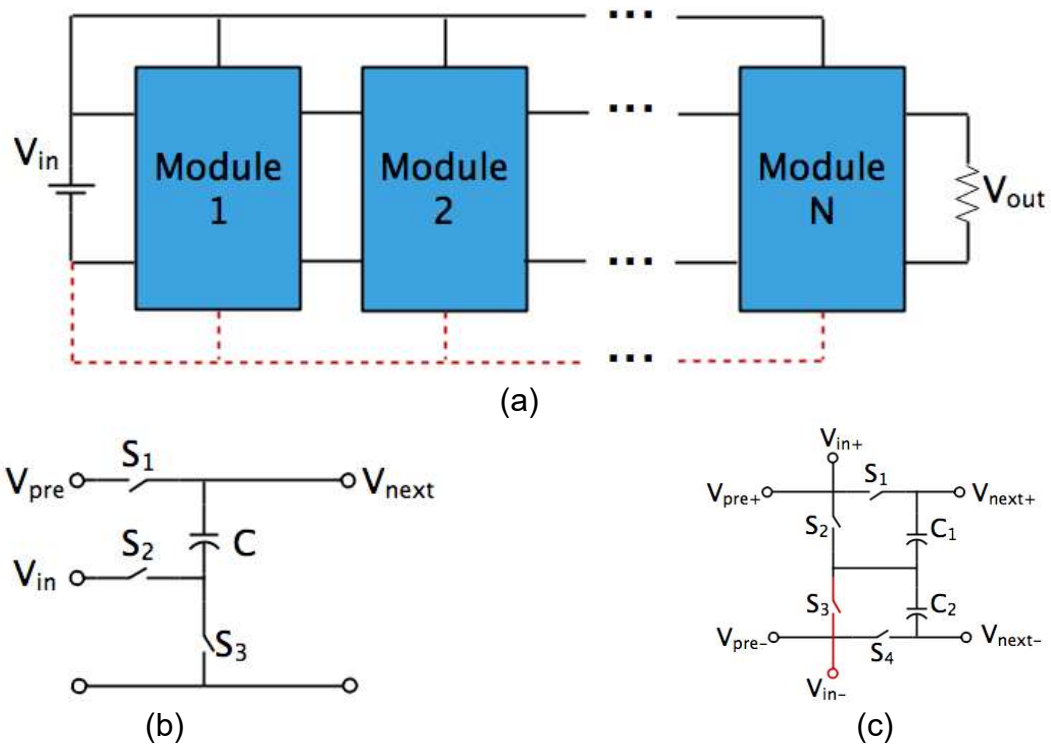


Fig 2-16. Multilevel switched-capacitor DC-DC converters.
(a) Overall structure of multilevel switched-capacitor DC-DC converter;
(b) Module structure in [215];
(c) Module structure in [217].

2.3 Hard/soft switching

Hard switching is that the active switch operates without any auxiliary circuit to deal with the switching losses and soft switching is the opposite. IGBTs and MOSFETs are still the most commonly used semiconductors, both of them have current and voltage overlap during switching period. The overlaps are the origins of switching losses. A main disadvantage of hard switching converters is the switching power losses,

especially when IGBTs are employed, due to their tail current in switching-off stage. Moreover, high EMI would be a potential issue as high *dv/dt* and *di/dt* occur in switching stage [22]. In order to limit the power losses of the hard-switching converter, switching frequency of the semiconductors is limited. However, Lower switching frequency would require larger volume of the passive component (i.e., inductors and capacitors) to achieve the same current and voltage ripple. These defects diminish the practical value of the converters.

On the other hand, soft switching technique can improve the above situations by reducing the switching losses in each switching cycle. It is achieved by means of utilizing auxiliary circuit (contains small inductors and capacitors) to generate resonance oscillation to force voltage or current become zero so that the overlap stage would be reduced as small as possible. If the voltage is forced to zero, then the process is called “zero voltage switching (ZVS)”. And if that is the current, it is called “zero current switching (ZCS)”. In the past decades, soft switching has been a hot topic, and literatures have been reported which often relate to the aspect of reducing volume, complexity and achieving controlled oscillation process [31], [32], [45]–[49], [52]–[54], [57]–[73], [78]–[84], [97], [97], [113], [120]–[122], [133]–[147].

Soft switching converters can be classified as passive resonant networks and active resonant auxiliary circuit. The passive resonant networks consist of only passive component, the parameter of the passive component is calculated so that the oscillation frequency would be fixed. In this case, the switching frequency of the entire

circuit would also be limited to a certain range to achieve soft switching. Fig 2-17(a) presents the different resonant network: LC series, LC parallel, LCC, LLC, CLLC, LCL. These networks have been reported in [31], [47], [57]–[59], [111], [148]. In these papers, the design and operation of the converters are tied to the certain power level, duty ratio and switching frequency, which make them, as mentioned above, not suitable for universal solutions for different circumstances. The active resonant auxiliary circuit is illustrated in Fig 2-17(b). The circuit that enable oscillation is not always connected to the circuit, they only applied when the main switch operates at switching stage. The parameter calculation is only based on the minimum switching frequency. So that the application of the active resonant auxiliary circuit would be feasible in a wide variety of converter [149]–[154].

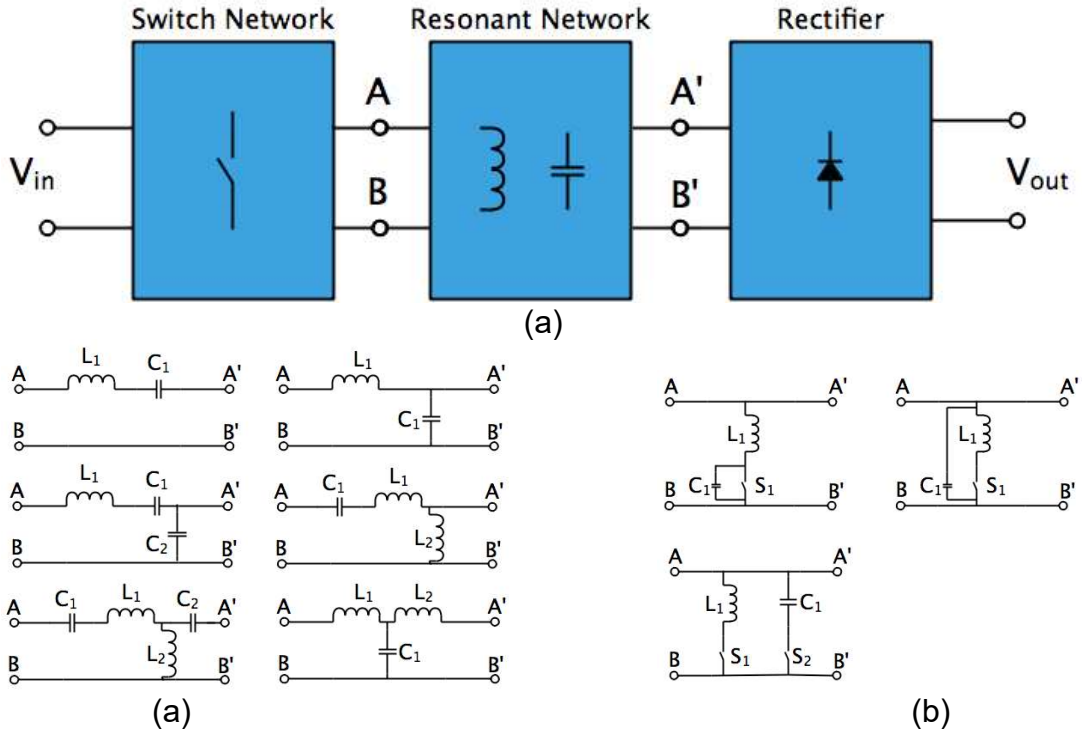


Fig 2-17. Soft-switching structure.
(a) resonant circuit diagram;
(b) passive resonant networks;
(c) active resonant auxiliary circuit.

2.4 Fault mechanism

Fault in power electronic system has always been a topic of interest in academia as well as in industry. The fault in power electronic system would cause series consequences in essential applications such as power grid or aircraft. Studying the mechanism and providing the solution for fault operation is significant in practical system.

2.4.1 Fault type

In power circuit, especially in DC-DC converter system, Fault can be classified as: power circuit fault and control/sensor fault. Power circuit fault includes all passive elements and transistors open circuit and short circuit fault. Control/sensor fault include any malfunction in control circuit and sensors inaccurate measurement as well as malfunction. In this thesis, power circuit fault is analyzed in detail.

The most common fault in power circuit is the transistors and capacitor. For different types of the transistors. The most likelihood fault occasions can be open circuit fault due to the overload of electrical and thermal stress. Various IGBT failures can be categorized as open circuit fault (OCF), short-circuit fault (SCF) and gate signal fault. And in DC-DC converter, most IGBT would suffer from OCF. The SCF on the IGBT in DC-DC converter has more destructive consequences that the OCF. SCF can cause high current flow to the DC-link capacitors and the

load, resulting damage to the DC-link capacitors and the load. The overcurrent damage to the DC-link capacitor can result in system break-down or even explosion. The OCF would just lead to system shut down, however, it still would be an issue when the DC-DC converters are supporting critical system, like aerospace or medical facility. DC-link capacitor open circuit fault also makes up 60% deviations[155].

Chapter 3 Research methodology

In this chapter, all the DC-DC topology mechanisms, system analysis methods, and control strategies are explained in detail.

3.1 Analysis of DC-DC converters

DC-DC converters, namely, switching converters, consist of semiconductor power devices, inductors and capacitors in the form of an electric network to transform electric energy. To stabilize the output voltage, negative closed-loop control is the most common and effective approach. Due to high efficiency feature of DC-DC converters, they have been widely accepted in power source management. In this section, several basic structures and characteristics of DC-DC converters are introduced.

3.1.1 System overview

DC-DC converter systems are usually combined with a power circuit and control circuit. The power circuit oversees the energy conversion and has a higher voltage and current rating than the control circuit. In contrast, the control circuit generates low level voltage and a current signal to trigger the power devices, and the signal contains information, such as the duty cycle and switching frequency.

Fig 3-1 shows an example of a buck converter. In the power circuit, the transistor periodically switches the inductor to connect between the input voltage Vg and the GND. The mean value of the voltage-second balance is determined by the duty cycle

D of the control signal. The inductor and the capacitor consist of an LC filter network to transform the square wave voltage from the positive end of the transistor to a DC voltage to supply the load. The voltage goes through DC to square wave to DC transform. From the control circuit point of view, the power circuit can be simplified as a system with an input signal D and an output signal Vout. The control circuit applies the feedback control with an error amplifier that detects and amplifies the feedback signal [156]. The amplifier output is compared with the saw-tooth wave to generate a PWM signal driving power switch, thus constituting a closed loop.

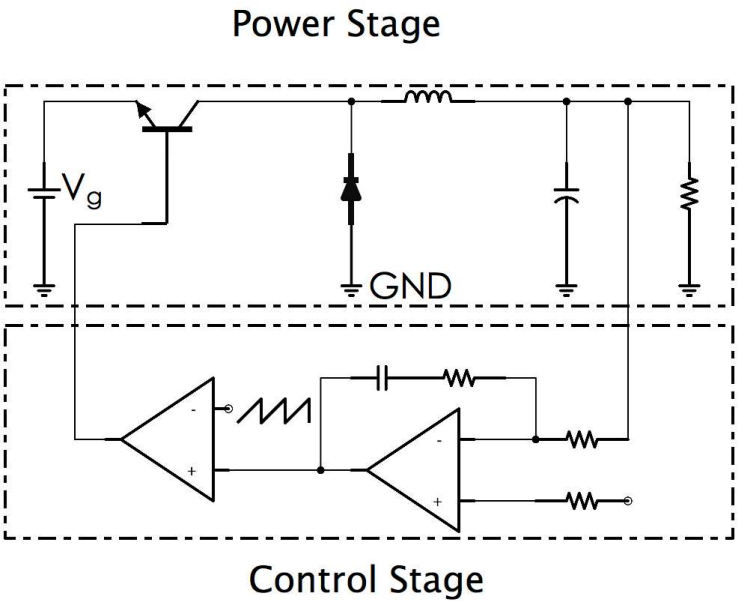


Fig 3-1. Example of a buck converter

As shown in the figure, the switch power supply is a linear feedback control system, and the feedback keeps the output voltage constant and is not affected by factors such as the power supply, load, and external environment. However, the feedback also causes system stability problems, so compensation is the key to the switch power supply system design.

Main parameter of the DC-DC converter:

- Efficiency: The percentage of output power and input power of conversion efficiency.
- Voltage gain: Voltage conversion ratio of output voltage to input voltage.
- Output ripple: Output voltage fluctuation amplitude when the output voltage ripple is in steady state.
- Output current capability: The output current capacity converter provides the current range for the load.
- Transient load response: After the load current changes, the time to regain the referenced output voltage represent the transient load response capability.

3.1.2 Power circuit structure

This section lists all the components that are used for energy transformation in the DC-DC converter and explains their mechanisms.

1. Non-consumption device

The switch power supply, the power level of processing in the form of energy transformation, is composed of a switch and inductance and capacitance components (sometimes including diodes, whose action can be used to switch to the equivalent). The basic power components are listed in Fig 3-2.

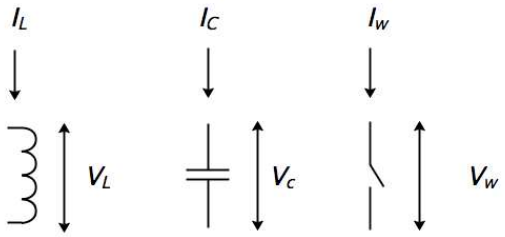


Fig 3-2. Basic power passive components

For the inductor component, the current gradient I_L is proportional to the voltage V_L across it; in the frequency domain, the relationship can be expressed as:

$$V_L = L\frac{dI_L}{dt} \qquad 3\text{-}1$$

For the capacitor component, the voltage gradient V_c is proportional to the current I_c charging or discharging it; in the frequency domain, the relationship can be expressed as:

$$I_C = L\frac{dV_c}{dt} \qquad 3\text{-}2$$

The voltage of the inductor is always orthogonal to the current signal of the capacitor, and the power consumed is the product of the voltage and current. Therefore, the ideal inductors and capacitors do not consume energy but only stores or releases energy.

For an ideal switch, there is no conductive resistance, and the voltage across it is 0 when it turns on. The conductive resistance is infinite, and the current passing through the switch is 0 when it turns off. Therefore, the voltage and current signal of the ideal switch are also orthogonal and do not consume energy. The ideal switching power level is a lossless transformation structure. Of course, the actual switch is realized by a semiconductor device, such as MOFET or IGBT, and there is certain conductive resistance and leakage current, which causes a loss. The real-world inductors capacitors also have parasitic series resistance, which causes a loss. With soft-

switching technique, the switching power supply can achieve a high energy conversion efficiency, and existing products can achieve more than 90% efficiency [3].

2. Topology structure

The combination of the switch, inductance and capacitance constitutes the switching power level. According to the voltage conversion range, the topological structure of the power level is mainly divided into the following types: Buck converter, Boost converter, buck boost converter, Cuk converter, Zeta converter, single ended primary inductor converter (SEPIC) converter, switched capacitor converter, Flyback converter and Forward converter.

a. Non-isolated DC-DC converter

The buck converter structure is shown in Fig 3-1 and consists of a pair of complementary switches, an inductor and capacitors. Fig 3-3 shows the schematic diagram of the buck converter power circuit structure. The left side of the inductor switches between the power supply and the ground, and the other end of the inductor is connected to the output. The output voltage V_{out} is lower than the input voltage V_g.

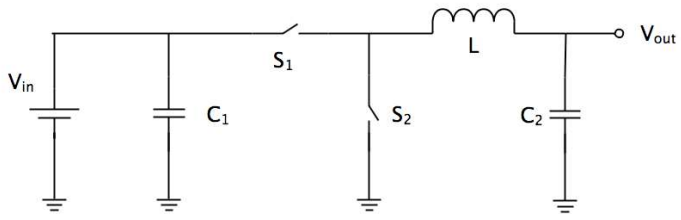


Fig 3-3. Buck converter power circuit

The booster converter structure can be treated as an input-output inverse version of the buck converter, as shown in Fig 3-4. The input end of the inductor is always connected to the input power supply, and the output end switches between the output end and the GND, i.e., the output voltage is equal to the mean value of the sum of the input voltage and the voltage across the inductor. The output voltage V_{out} is higher than the input voltage V_{in}.

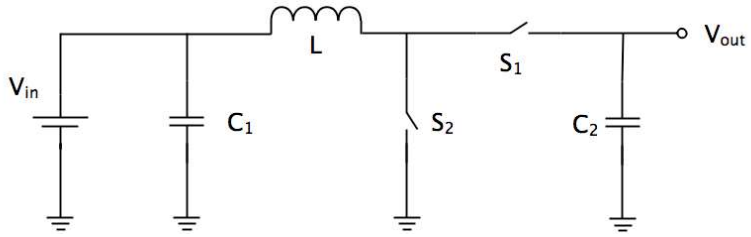


Fig 3-4. Boost converter power circuit

The buck converter is shown in Fig 3-5. it charges the inductor when S_1 turns on and the inductor support the load alone when S_1 turns off. In this case, the voltage would step down from input end to the output end.

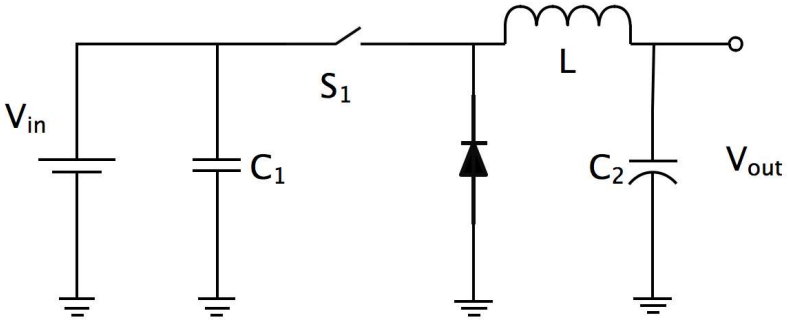


Fig 3-5. Buck converter power circuit

The Cuk chopper circuit, also known as the Cuk converter (Fig 3-6), was introduced by Slobodan Cuk at the California Institute of Technology. It was an improvement based on the buck/boost single-switch non-isolated DC-DC converter. The inductor participates in both the input and output of the system, which can significantly reduce the input and output current ripple. The polarity of the output voltage is the inverse of

that of the input voltage, and the output voltage can be either greater than or less than the input voltage. The Cuk converter can be treated as a series-connected boost and buck converter.

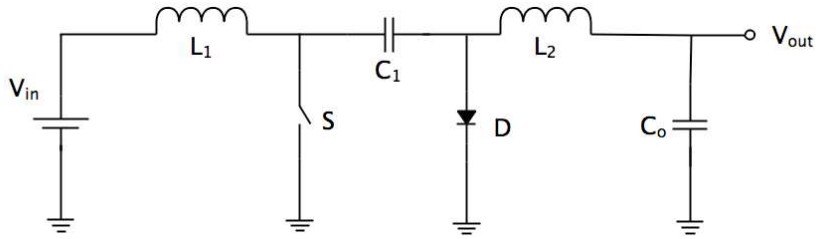


Fig 3-6. Cuk converter

Transistor *S* is in the pulse width modulation (PWM) control mode. The Cuk converter has two working modes: the continuous current mode (CCM) and the discontinuous current mode (DCM). These two modes indicate whether the current has continuous or discontinuous flow through the diode *D*. During the turn-off stage of transistor *S* in a switching cycle, if the diode current is always greater than zero, the current is in the CCM. If the diode current is zero for a period of time, then the current is in the DCM. If the diode current is reduced to zero at $t=T_s$, then it is in the critical continuous working mode. There are two inductors in the Cuk converter that can have no coupling or coupling, and the coupling inductance can reduce the current fluctuation.

Fig 3-7 shows the schematic diagram of a Zeta converter structure. The basic working principle of the Zeta circuit is that during the steady state of *S*, the power supply is switched on to the inductive *L* energy storage, while the power supply and *C* are powered by L_o to load *R*. After the closing of *S*, *L* is charged to 1 by *D*, and its stored energy is transferred to *C*; in addition, the current of L_o is continuous with *D*.

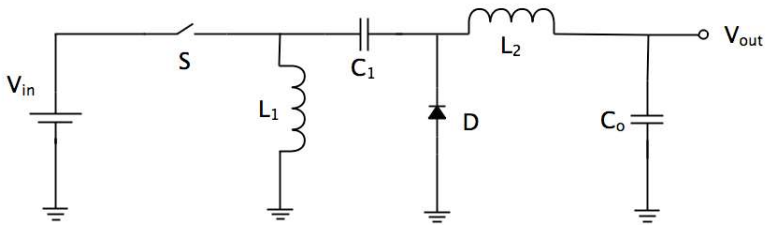


Fig 3-7. Zeta converter power circuit

The SEPIC is a DC-DC converter that allows the output voltage to be greater than or equal to the input voltage. The output voltage is controlled by the main control switch. The structure of the SEPIC converter is revealed in Fig 3-8. When S_W is in the on state, the V_{in} - L_1 - S circuit and C_p - L_2 - S loop simultaneously conducts, and L_1 and L_2 store energy. When S is in the off state, the V_{in} - L_1 - Cp - D_1 - load (C_{out} and V_{out}) circuit and L_2 - D_1 - load circuit conduct at the same time. In this stage, V_{in}, L_1 and L_2 supply power to the load and also charge C_1, and the energy stored in C_1 transfers to L_2 when S_W is in the on state.

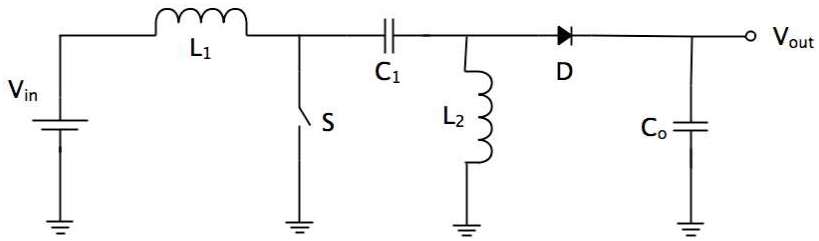


Fig 3-8. SEPIC converter power circuit

The greatest benefit of this circuit is that the input and output have the same polarity. This circuit is especially suitable for the use of battery power supply as it allows the battery voltage to be higher than or less than the required input voltage. Another benefit is the isolation of the input and output, which is achieved by capacitance C_1 on the main loop. The output voltage is 0 V when the transistor is turned on.

The switched capacitor is the last non-isolated topology mentioned in this paper. The basic principle of the switch capacitor converter is to transfer the charge from the input end to the output end by using the capacitance to transfer the current required by the load without any magnetic component.

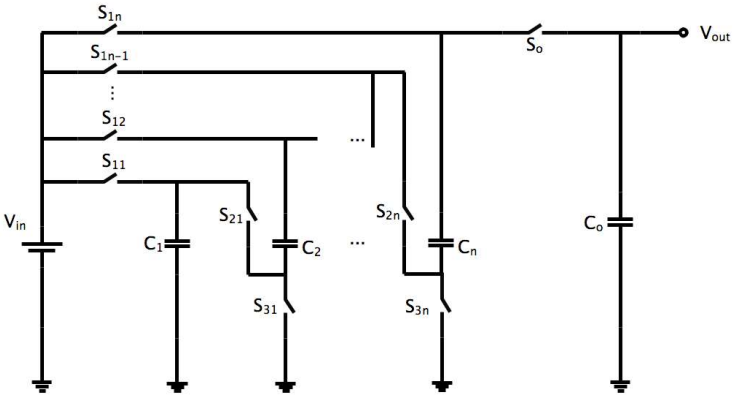


Fig 3-9. Switched capacitor DC-DC converter unified model

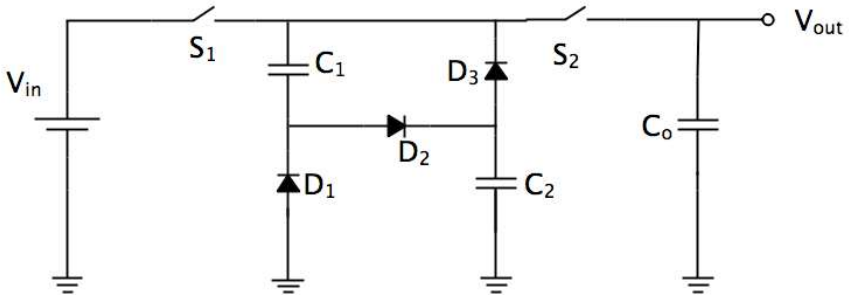


Fig 3-10. Second-order switched capacitor DC-DC converter

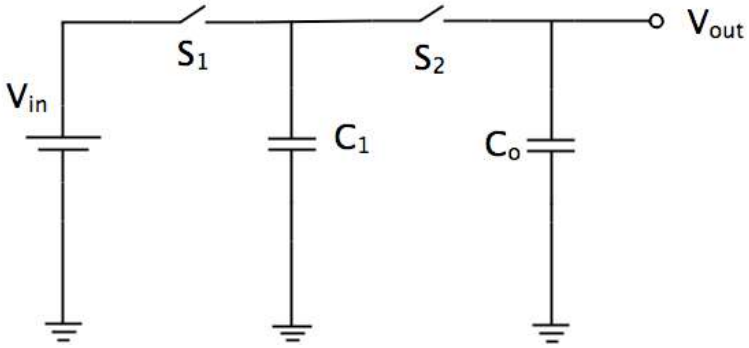


Fig 3-11. Basic switched capacitor DC-DC converter topology

The unified model of the switched capacitor DC-DC converter is shown in Fig 3-9, where *S* represents the power switch, C_i is the n_i order of the capacitance combination structure, n_i is the number of capacitors, and subscript *i* represents the *ith* string

capacitor combination structure. These structures are composed of the capacitors (usually the same capacitance) and diode, and these capacitors have the characteristics of series charging and parallel discharging, as shown in Fig 3-10. The dotted box indicates the second-order switched capacitor DC-DC converter, and Fig 3-11 shows the basic topology of the switched capacitor DC-DC converter.

As shown in Fig 3-9, the switched capacitor DC-DC converter generally has two states: the charging state and discharging state. In the charging state, S_{i1} and S_{i4} conduct, S_{i3} turns off, and C_1... C_m are charging in parallel. Similarly, in the discharging state, S_{i1} and S_{i4} turn off, S_{i3} conducts, and C_1... C_m are discharging in series. In the first state, C_o discharges to provide load current, while in the second state, C_1... C_m provide charge to C_o while C_O functions as an output filter to obtain a smooth output voltage.

In the industry, switched capacitor DC-DC converters have a considerable advantage over the other type of DC-DC converter due to its high modularization capability. By increasing the switched capacitor module, the output voltage can be boosted to a very high level without introducing any magnetic component. However, it has a fixed conversion ratio and a high transient current; other techniques are needed to address those issues, as discussed in a later section.

b. Isolated DC-DC converter

The forward converter is an isolated DC-DC converter that utilizes the transformer to transfer electric energy to magnetic energy and then back to electric energy to the load.

It provides galvanic isolation to protect the adjacent circuit from any faulty operation from the source and/or the primary end of the converter. The converter can provide higher or lower voltage, depending on the turns ratio of the transformer. The structure of a single-switch forward converter is shown in Fig 3-12.

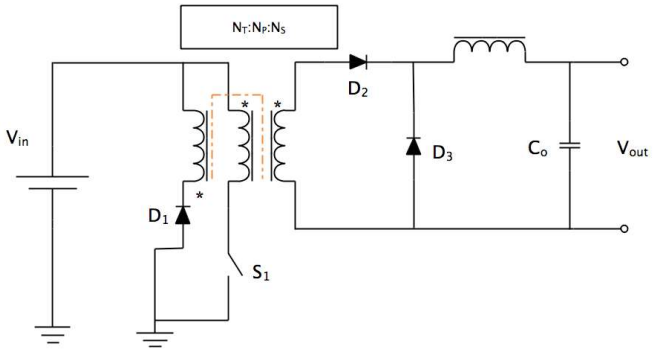


Fig 3-12. Structure of a single-switch forward converter

As shown in the figure, the transformer in the forward converter is same-polarity connected. The transformer itself lacks the capability to store the energy because the transformer has no air gap, and the maximum output voltage of the forward converter is limited by the transformer turns ratio N_s/N_p:

$$\frac{V_{out}}{V_{in}} = D \cdot \frac{N_s}{N_p} \qquad 3\text{-}3$$

where *D* is the duty cycle.

Push-pull is the output circuit of two different polar transistor connections. An example of a push-pull structure is shown in Fig 3-13. The push-pull circuit adopts two parameters of the same power, i.e., BJT or MOSFET. The term “push-pull” means that each transistor is in charge of the waveform amplification of the positive or negative half cycle. When the system is operating, only one of the two symmetrical power switches conducts at a time, the conduction losses reduced, resulting in an increase in efficiency.

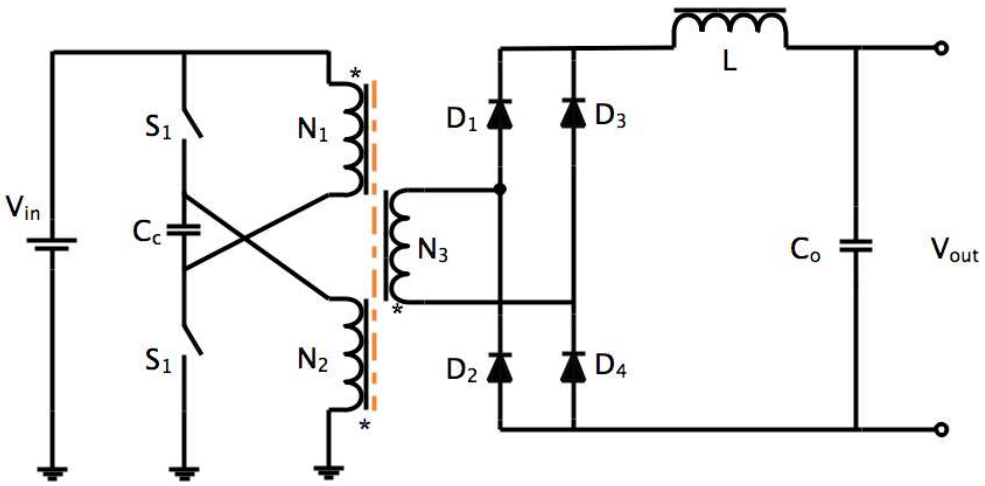


Fig 3-13. Structure of a push-pull DC-DC converter

A push-pull circuit is suitable for a low voltage–high current situation, and it can be widely applied in the power amplifier circuit and switching power supply. This type of circuit offers the following advantages: simple structure, high utilization of the magnetic core, and low conduction loss. However, it also has certain disadvantages, such as centre tap in the transformer, high voltage stress on the transistor, high voltage spike on the transistor when switching, and high input current ripple.

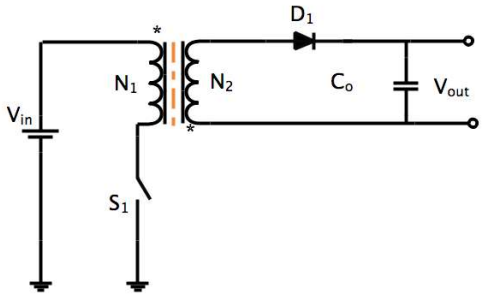


Fig 3-14. Structure of a flyback converter

A flyback converter (Fig 3-14) is commonly known as a single-ended flyback type DC-DC converter because the output end gains energy from the transformer when the primary end of the transformer is cut off. The flyback converter stores energy in the air gap of the transformer when the main switch turns on, and when the main switch turns off, the energy is delivered to the load.

3.1.3 Steady state performance

Steady state performance is a series of key indicators that determine the quality of the system. In this section, 4 criteria are introduced: average current, conversion ratio, output ripple and efficiency.

1. Average current and voltage

The power circuit of the power supply functions by switching the transistors. When the state of the inductive and capacitive components is periodically stable with the switch, the power circuit is considered to be in steady state. The stability of the switching power system is not a fixed concept, namely, the instantaneous state of the inductors and capacitors are constantly changing. To analyse the state of the switching power supply, the average value in periodic time is used to replace the value measured in instantaneous time. For example, taking the buck converter working in a fixed cycle, as shown in Fig 3-15, there are two states in the power circuit. The inductor current fluctuates, but the average cycle remains stable.

When S_1 turns on and S_2 turns off, the inductor current follows the equation:

$$L\frac{dI_L}{dt} = V_{in} - V_{out} \qquad 3\text{-}4$$

When S_1 turns off and S_2 turns on, the inductor current follows the equation:

$$\mathrm{L}\frac{\mathrm{dI_L}}{\mathrm{dt}} = 0 - \mathrm{V_{out}} \qquad 3\text{-}5$$

If in one switching cycle, the turn-on time of S_1 is DT and that of S_2 is $(1\text{-}D)T$, through the average voltage current method, the inductor current would be:

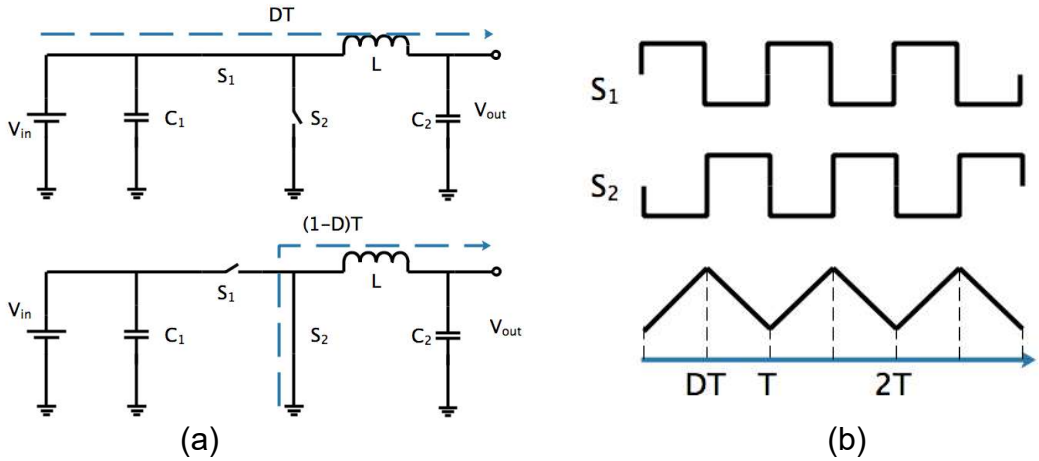
$$L\frac{dI_L}{dt} = DV_g - V_{out} \quad 3\text{-}6$$

When the system is in steady state, the average value of the inductor current in one switching cycle would be zero, which leads to:

$$DV_g = V_{out} \quad 3\text{-}7$$

For the analysis of the capacitor, a similar conclusion can be found in the current aspect:

$$I_g = DI_{out} \quad 3\text{-}8$$



(a) (b)

Fig 3-15. Buck converter switching state and its steady state time series
(a). switching state;
(b). time series.

The steady state voltage current relationship between the input and output of a buck converter can be analysed by means of the periodic average method. The method can be used to remove the switch function in the variable, and it is also applicable to other types of structures, which is the basic method of the switching power supply analysis.

2. Conversion ratio

According to the average analysis of the previous section, the input and output relationship of the power circuit in the steady state of the switching power supply can

be obtained. For the buck converter, the input and output relationships are described by equation 3-8, and the voltage conversion is determined by the control signal. The example in this section can be found in the topology section and is therefore not included here.

3. Output ripple

The DC-DC converter outputs DC current. However, in the switching power supply, DC output is obtained through the filter of the switching signal, and voltage fluctuation, namely, the output ripple, is inevitable. The output waveform originates from the charging and discharging of the output capacitor. For an ideal capacitor, the voltage ripple of the capacitor can be calculated by the changes in the charging and discharging current. For the actual capacitor parts, the existence of parasitic equivalent series resistance and equivalent series inductance can also generate voltage fluctuations during charging and discharging, which needs to be considered. Fig 3-16 shows an example of output ripple generation in a buck converter.

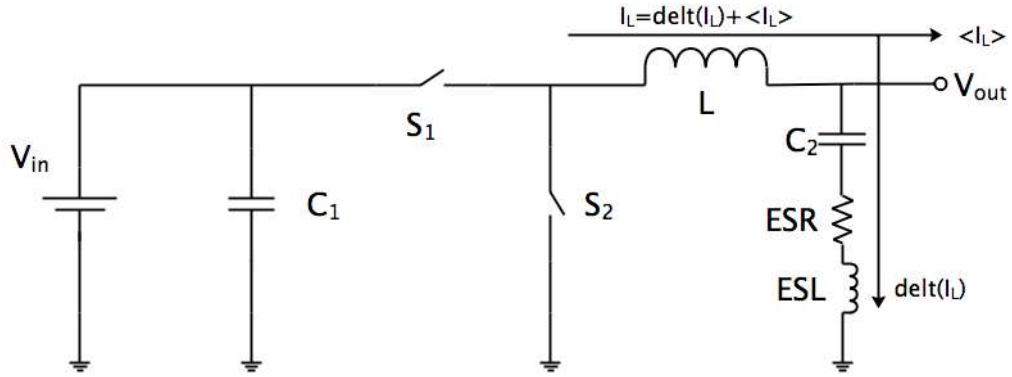


Fig 3-16. Indication of the output ripple generation of a buck converter

4. Efficiency

Energy transfer efficiency is the core factor of power management. High efficiency is the fundamental purpose of a switching power supply. Energy conversion must be accompanied by loss, and efficiency and loss are two representations of the same property. The loss of a switching power system mainly includes conduction losses, driving losses, switching losses and control losses.

As mentioned in section 3.1.2 of this chapter, an ideal switching power circuit is composed of inductors, capacitors and switches, which can achieve a lossless transformation. However, for the actual components, the inductors and capacitors have parasitic series resistance, and the resistivity component of all the power devices will cause conduction losses. If the switches are considered to be MOSFETs, when they turn on, the transistors work in the linear resistance area, and a certain conduction resistance exists, thus causing losses. When the MOSFETs are turned off, the reverse leakage current can also cause loss. The above losses caused by the resistivity components are collectively referred to as conductance losses.

For the switching operation of MOSFET, the fundamental process is to charge and discharge the gate capacitance. The capacitor itself is lossless, but it can cause conduction loss at the driving circuit, which is generally called driving loss. The driving loss is related to the power transistor effective sectional area, the switching frequency and the drive voltage.

According to the analysis in section 3.1.2, the voltage current signal of the ideal switch is orthogonal. However, for the actual MOSFET devices, there is a voltage current signal overlap in the switching process, causing loss. In addition, if the switch timing of two transistors is not properly controlled, there may be two transistors in the same half bridge conducting at the same time, leading to a large current, which could damage the device and cause loss. The losses caused during switching are collectively referred to as switching losses. The switching losses are related to the voltage current phase, so the parasitic inductance and capacitance of the power transistors greatly influence the loss. As the converter switch frequency increases, the problem of switching loss becomes more serious.

The above losses are power circuit losses; the control circuit also requires a certain power consumption, which is called a control loss. In the power management circuit, the power consumption of the control circuit is generally in the mW level, which has a slightly larger impact on efficiency when the system is under light load.

To decrease the conduction losses, low ESR inductive and capacitive components can be used to optimize the layout and connection of the power transistors in the circuit to minimize the parasitic conduction impedance. The switch conduction losses are inversely proportional to the effective sectional area, and the driving losses are proportional to this area. Thus, for a certain inductor current situation, there is an optimal transistor width value, making the total loss minimum. To reduce the driving loss, the switch frequency can be reduced depending on the load rate, the gate drive

voltage can be adjusted, and a resonant circuit can be used to reuse the gate charge energy. To decrease the switching loss, the dead zone time of power devices switching can be optimized, and soft-switching technology can be adopted to eliminate the overlap of voltage current signals when switching. In addition, the power level work mode also greatly impacts efficiency.

3.2 System modelling and dynamic features

A switching power supply is a negative feedback control system, and the basic structure is shown in Fig 3-1. To study the stability of the feedback system, a systematic mathematical model is needed to analyse the dynamic characteristics of the system. The following section derives the transfer functions of each type and analyses its dynamic characteristics.

The transfer function is a commonly used mathematical model of linear time-invariant systems. According to the analysis in the previous section, the simplified abstraction of the power level of switching power supply can be considered a linear time-invariant system. The transfer function applies the Laplace transform, which is the algebraic equation of the variable used to describe the dynamic characteristics of the system. The power circuit transfer function can be derived from the equivalent circuit or derived directly from the expression. According to the equivalent circuit derivation transfer function, the control transfer function of the booster converter can be conveniently obtained. The beginning of the expression involves directly writing the related differential equation, which is also an example of the fixed-duty cycle booster converter.

$$\begin{cases} L\frac{dI_L}{dt} = V_g - (1-D)\cdot V_{out} \\ C\frac{dV_{out}}{dt} = (1-D)I_L - \frac{V_{out}}{R} \end{cases} \quad 3\text{-}9$$

Adding interference gives:

$$\begin{cases} L\frac{d(I_L+i_L)}{dt} = V_g - (1-D-d)\cdot(V_{out}+v_{out}) \\ C\frac{d(V_{out}+v_{out})}{dt} = (1-D-d)(I_L+i_L) - \frac{(V_{out}+v_{out})}{R} \end{cases} \quad 3\text{-}10$$

Removing high order terms gives:

$$\begin{cases} L\frac{di_L}{dt} = -(1-D)v_{out} + dV_{out} \\ C\frac{dv_{out}}{dt} = (1-D)i_L - dI_L - \frac{v_{out}}{R} \end{cases} \quad 3\text{-}11$$

Using the Laplace transform gives:

$$\begin{cases} sLi_L = -(1-D)v_{out} + dV_{out} \\ sCv_{out} = (1-D)i_L - dI_L - \frac{v_{out}}{R} \end{cases} \quad 3\text{-}12$$

Then,

$$\frac{v_{out}(s)}{d(s)} = \frac{V_g}{(1-D)^2}\frac{1-s\frac{L}{(1-D)^2R}}{1+s\frac{L}{(1-D)^2R}+s^2\frac{LC}{(1-D)^2}} \quad 3\text{-}13$$

This method is based on the average value. Using the same principle, other transfer functions can also be obtained:

Buck:

$$\frac{v_{out}(s)}{d(s)} = V_g\frac{1}{1+s\frac{L}{R}+S^2LC} \quad 3\text{-}14$$

Buck-boost:

$$\begin{cases} \frac{v_{out}(s)}{d(s)} = (1+k)^2V_g\frac{1-sK(1+K)\frac{L}{R}}{1+s(1+k)^2\frac{L}{R}+S^2(1+k)^2LC} \\ K = \frac{V_{out}}{V_g} \end{cases} \quad 3\text{-}15$$

From the above expressions, the power level transfer function contains a pair of conjugate poles, whose position is mainly determined by the LC and is also related to the conversion ratio (except for the buck converter). To achieve the same conversion

ratio, the buck-boost converter needs a higher DC gain, and the conjugate poles are lower, which is detrimental to the system design.

Based on the above analysis, the power circuit can be abstracted as a linear time-invariant system, and its dynamic characteristics are described by the transfer function. The bode diagram gives the system's gain and zero pole distribution intuitively. Therefore, the power level of the switching power supply as the controlled object is clearly resolved and can be used to design the control parameters.

3.3 System control

From the analysis in the previous section, the output voltage is affected by the input voltage, load current and parasitic parameters. To maintain the stability of the output voltage, appropriate system control is necessary. The control method of the switching power supply systems can be divided into two categories: large signal control based on the comparator and small signal control based on modulation. Only small signal control is discussed here. An example of a buck converter for negative feedback is shown in Fig 3-1. The controller adjusts the duty ratio signal according to the detected feedback signal and drives the power transistors. If only the voltage signal is used for feedback, it is called voltage control mode, and if the feedback loop contains the current signal, it is called current control mode.

3.3.1 Voltage control mode

To obtain a stable output voltage, a direct method is used to detect and feedback the output voltage, which is the voltage control mode. The system diagram using the voltage control of a small signal converter system block diagram is shown in Fig 3-17. In this diagram, the feedback coefficient is reduced to 1, and the error between the output voltage and the reference voltage is amplified by a factor of $G_{vc}(S)$ and turns into the duty ratio signal by PWM to control the power circuit. Above all, it consists of a negative feedback loop. The transfer function of the power circuit $G_{vd}(S)$ is derived from the analysis in the last section. From equations 3-9 to 3-15, there are two conjugate poles that can be deduced. The boost converter and buck-boost converter both have a right half plane zero. Thus, the system design needs to consider bandwidth selection and compensation design.

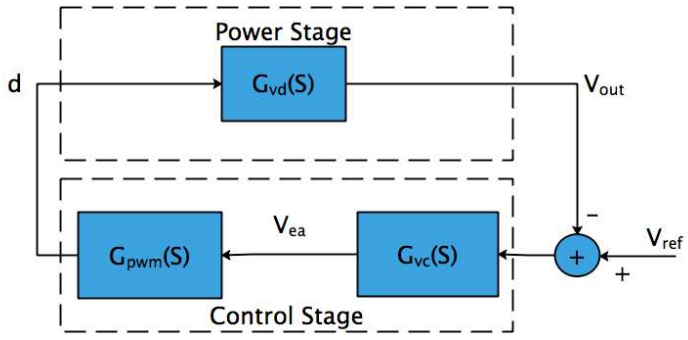
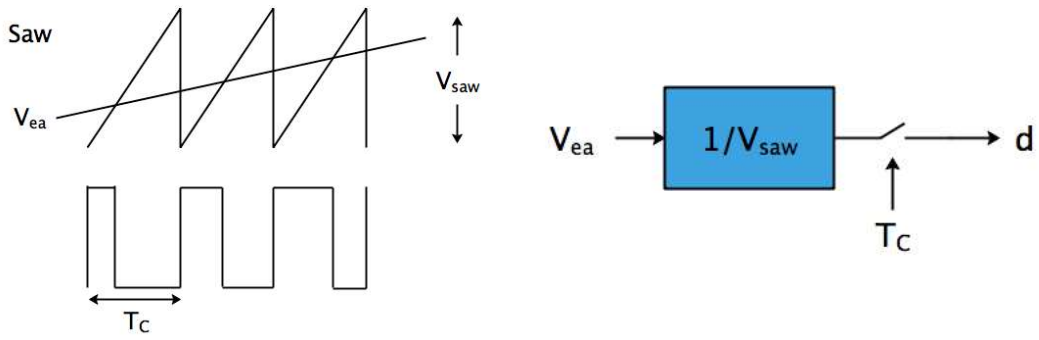


Fig 3-17. System diagram of voltage control



(a) I (b)

Fig 3-18. Indication of the PWM signal generation based on the saw-tooth waveform
(a). PWM time domain waveform
(b). PWM small signal model

The control level is mainly composed of two parts: error amplification compensation and PWM signal generation. The PWM module converts an analogue signal (such as an error signal) into a PWM signal where the duty ratio changes. Comparing PWM signals with saw-tooth signals is a common method for generating an PWM signal, as shown in Fig 3-18. If the periodic average method is used for analysis, the value of D can be expressed as:

$$D = \frac{V_{ea}}{V_{saw}} \qquad 3\text{-}16$$

The corresponding small signal expression is:

$$G_{pwm}(s) = \frac{d(s)}{V_{ea}(s)} = \frac{1}{V_{saw}} \qquad 3\text{-}17$$

The value of the duty ratio signal stays the same in one cycle, so it can be seen as a sampling process, as shown in Fig 3-18 (b), which is a complement to the linear model. The error amplification compensation module is the key to system stability, and it is also the key to design. The design of $G_{vc}(s)$ should meet the following criteria: a high DC gain to reduce the output voltage DC error and enough phase margin to make the system stable and the transient response fast. High DC gain means that $G_{vc}(s)$

contains at least one low-frequency pole; however, the transfer function of the converter contains two LC poles. In this case, compensation design is required. When the system bandwidth is within the conjugate poles, there is only one low-frequency pole, and the system does not need the extra zero compensation. When the bandwidth is low, usually for very high LC poles, the converter bandwidth is outside the conjugate poles, and the system has three poles. Therefore, two zero points are needed to compensate, and the zero point should be leading the conjugating pole. Generally, using a proportion-integral-derivative (PID) controller, its transfer function can be written as:

$$G_{vc}(s) = G_{vcm}\frac{(1+\frac{z_1}{s})(1+\frac{z_2}{s})}{(1+\frac{s}{p_1})(1+\frac{s}{p_2})} \quad 3\text{-}18$$

Its electric circuit can be achieved as shown in Fig 3-19.

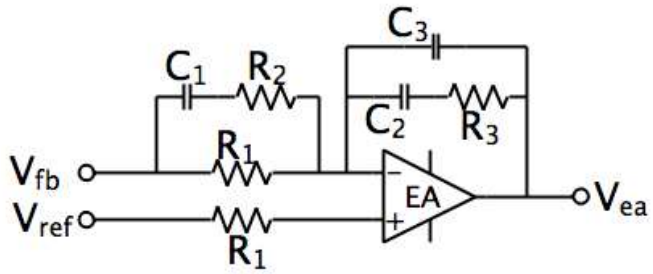


Fig 3-19. PID controller

3.3.2 Current control mode

The feedback signal of the converter in steady state is the voltage signal and the current signal. If only the voltage signal is tested for feedback, it considered to use voltage control mode. If the current signal is introduced into the control loop, it is called current control mode. The current signal is detected and amplified along with the

voltage error amplifier output to generate the PWM signal. The signal block diagram of the system is shown in Fig 3-20. In Fig 3-20, $G_{id}(s)$ is the transfer function of the inductor current, which can be expressed as:

$$G_{id}(s) = \frac{i_L(s)}{d(s)} = \frac{V_g}{R}\frac{1+sRC}{1+s\frac{L}{R}+s^2CL} \quad 3\text{-}19$$

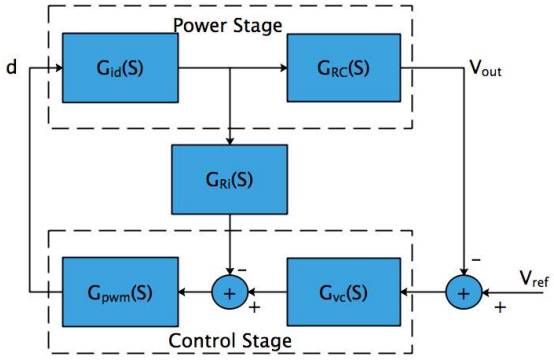


Fig 3-20. Signal diagram of the current control

$G_{RC}(s)$ is the output impedance, which can be expressed as:

$$G_{CR}(s) = \frac{R}{1+sRC} \quad 3\text{-}20$$

The gain from the feedback control to the output voltage is expressed as $G_{vd}(S)$, which can be divided into inductor current gain and output impedance gain:

$$G_{vd}(s) = G_{id}(s)G_{CR}(s) \quad 3\text{-}21$$

As with the current feedback module, the current signal can be transformed into a voltage signal, and the gain of the feedback module can be treated as a resistance:

$$G_{Ri}(s) = Ri \quad 3\text{-}22$$

Thus, all the gains from Fig 3-20 are deduced. This figure also indicates two control loops: the current control loop and voltage control loop. Their transfer function can be written as:

$$\begin{cases} T_i(s) = G_{id}(s)G_{Ri}(s)G_{pwm}(s) \\ T_v(s) = G_{vd}(s)G_{vc}(s)G_{pwm}(s) \end{cases} \quad 3\text{-}23$$

For a single loop control system, such as the voltage control mode described above, the system stability is determined by the dynamic characteristics of the loop. For a multiple loop control system, due to the interactions between the control loops, the system stability and dynamic characteristics of each loop do not affect one another directly; instead, all the effects of the control loops should be considered as a whole. Using the current control of the converter is a typical double loop system. Introducing the current loop to separate the LC resonant conjugate poles of the converter moves the secondary pole outside the bandwidth, and the primary pole is determined by the output capacitance. In this method, the current control loop causes the inductor to function as a current source, making the level of the transfer function of the converter by LC second-order downgraded to the RC first order, which in turn makes $G_{vc}(s)$ compensation easier to implement.

Based on the above analysis, due to the phase difference of the double closed-loop control objects, the current loop is usually considered to be the inner control loop of the system, and the voltage loop is considered the outer control loop. This consideration causes the current control loop to respond faster and be more stable than the voltage control loop. In reality, the current control loop needs to be 10 times faster than the voltage control loop [156]. The essence of the current control mode is to use the current closed-loop feedback to form the compensation phase, which can be considered a special zero-pole generation method.

3.3.3 Maximum power point tracking (MPPT)

1. Photovoltaic panel characteristic

Photovoltaic (PV) panels are essential components in a solar power system. The panel size is usually determined based on the output power of the panel. Taking a 4 W PV panel as an example, the panel size is 50 cm^2 [59]. The electric characteristic of PV panels can be described as in Fig 3-21.

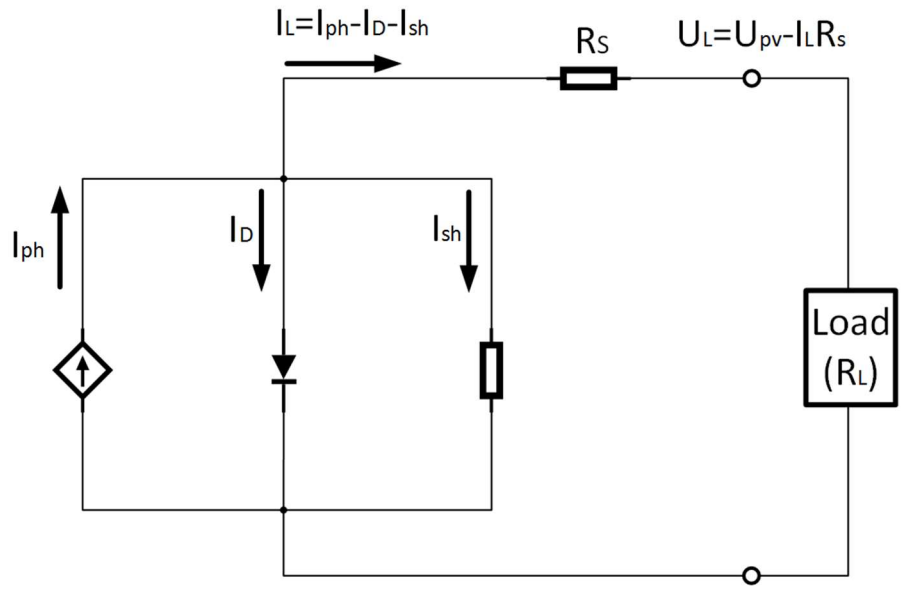


Fig 3-21. Equivalent circuit of the PV panel

In an ideal PV panel, $R_s = 0$ (no series connection losses) and $R_{sh} = \infty$ (no leakage current). In a classic lin[2] silicon PV battery, R_s is between 0.005 and 0.1 Ω, and R_{sh} is between 200 and 300 Ω. In this case, a tiny change in R_s would compromise the PV output power. In general, the ambient temperature changes in a short period of time are very tiny and can be neglected. The temperature has a considerable effect on the output voltage of the PV panel. Fig 3-22 indicates the I-U characteristic curve of the PV panel under different sunlight intensities.

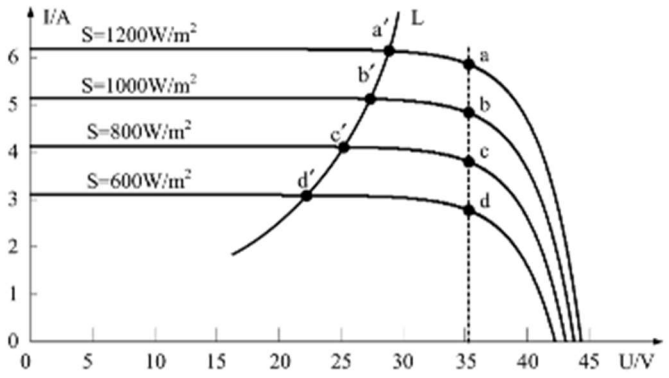


Fig 3-22. I-U characteristic curve of a PV panel under different sunlight intensities

2. Algorithm

A maximum power point tracking (MPPT) system is a system that consists of a DC-DC power converter and correlated control system. It functions by adjusting the working state of the electric module of the PV panels to maximize the energy output from the PV panel for storage in the battery system. It can effectively meet the residential and industrial electricity demands from remote and tourist areas that the regular power grid cannot cover while generating no additional environmental pollution. Unlike voltage control and current control, MPPT faces a current source rather than a voltage source, and its purpose is to achieve maximum power rather than to control the output voltage/current. Thus, different strategies are in place.

a. Constant voltage control

The constant voltage control method is used to fix the voltage of a solar panel to a certain value. According to Fig 3-20, when the effect of temperature is neglected, the

output voltage is relatively fixed at the maximum power point despite changes in the light intensity.

The constant voltage method to achieve MPPT is simple, and it functions without tracking the working voltage of the maximum power output of the solar panel. This method reduces the need for a current sensor and thus makes the system less expensive. The constant voltage method offers high control stability, is easy to achieve, and has good reliability. However, due to the unique temperature output characteristics of PV panels, as mentioned before, the temperature affects the PV panel performance. Taking monocrystalline battery cells as an example, when the environment temperature increases by 1 °C, the solar panels open circuit voltage of U_{oc} declines by 0.25%~0.45%. This result indicates that when the temperature changes, the maximum power point corresponding to the output voltage of the solar panel changes.

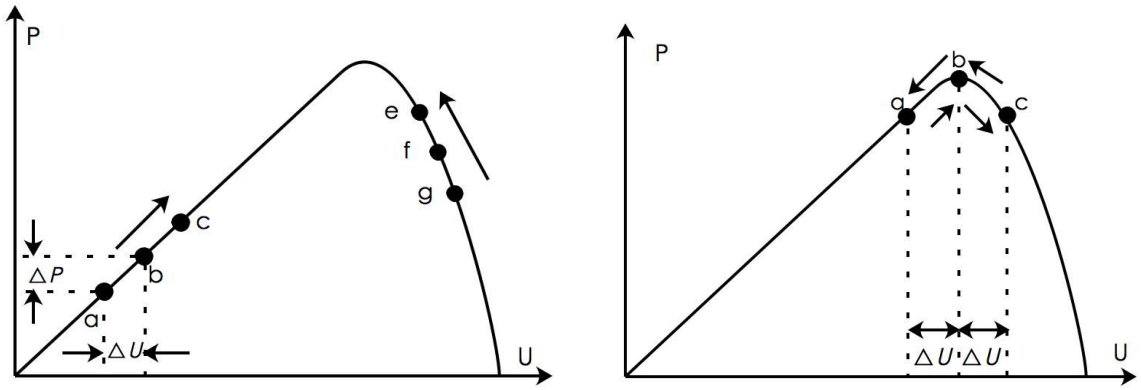
For regions where the temperature varies dramatically throughout the year or during a day, temperature changes would greatly impact the PV system. In these areas, using the constant voltage method to regulate the PV system is not efficient or stable for the system. With the development of digital signal processing technology, the method of using a constant voltage control for MPPT has gradually been eliminated.

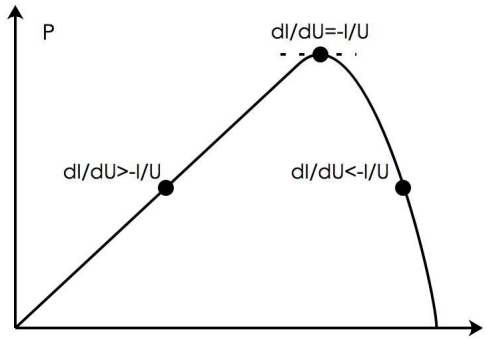
b. Perturbation and observation (P&O) method

The perturbation and observation (P&O) method is one of the most commonly used MPPT methods in the industry, as shown in Fig 3-23. From the PV panel P-U curve,

when the output voltage of solar panels is lower than the maximum output power point voltage, the power output will increase with increasing output voltage. When the output voltage of the solar panel is higher than the maximum output power point, the output power decreases with increasing output voltage.

The principle of P&O control is that the PV control system disturbs the output voltage of PV panels with a certain step change output voltage in each control cycle. Each step of the voltage disturbance is described as ΔU. The P&O algorithm compares the output power of the PV panel before and after the disturbance. If the PV panel output power increases after the disturbance, which means that the working point moves from a to b in Fig 3-23, then the P&O algorithm continues the disturbance in the same direction of the last control cycle. Then, the working point of the solar panel is moved from b to c. If the PV panel output power decreases after the disturbance, which means that the working point moves from f to g in Fig 3-23(a), then the P&O algorithm reverses the disturbance direction of the last control cycle. Then, the working point of the PV panel moves back from g to f. The P&O method controls the PV panel working point to move towards the direction of the maximum power point.





(c)

Fig 3-23. MPPT algorithm
(a). P&O method;
(b). oscillation near the maximum power point for the P&O method;
(c). INC method.

The disadvantage of P&O is that the output of the solar panels is continuously disturbed. When the PV panel reaches its maximum power point, the working point of the PV panel will move around the maximum power point due to the P&O method. As shown in Fig 3-23(b), when the working point of the PV panel moves from point e to point f, the output power of the PV panel is close to the maximum output power. Because the current output power P_f is higher than the output power from the last control cycle P_e, according to the P&O judgement criterion, the disturbance will be kept in the same direction as the last disturbance. Therefore, in the next control, the output voltage of the PV panel continues to rise, and the working point of the PV panel moves from f to g. At this time, the output power of the PV panels P_g is lower than P_f, which moves away from the maximum output power working point. The working point of the PV panel will move back to f after the control cycle when it moves to g. After arriving at point f, the working point of the PV panel at the next control cycle moves to e. Assuming that the environment does not change, the working point of the solar panels will constantly move from e to f to g and then from g to f to e, causing the output of the

PV panel to oscillate. The greater the disturbance step ΔU is in the P&O method, the greater the oscillation that occurs near the maximum power point, and the greater the output losses are.

c. Incremental conductance (INC) control

Incremental conductance (INC) control is another algorithm used in the MPPT control method. Fig 3-23(c) shows the INC control method based on the P-U characteristic curve. This diagram shows that the slope at the maximum power point is zero, such as in formula 2-24.

$$\frac{dP}{dU} = I + U\frac{dI}{dU} = 0 \qquad 3\text{-}24$$

Then, the following relationship can be deduced:

$$\frac{dI}{dU} = -\frac{I}{U} \qquad 3\text{-}25$$

Fig 3-23(c) shows that when the working point of the PV panel is to the right of the maximum power point, $dI/dU < -I/U$, and when the working point of the PV panel is to the left of the maximum power point, $dI/dU > -I/U$. When the negative value of the solar panel's electrical conductance is equal to its gradient, i.e., $dI/dU = -I/U$, the working point of the solar panel is at the maximum power point. By judging the relationship between dI/dU and $-I/U$, the INC method can be used to determine the working point of the solar panel, and then the working voltage of the solar panel can be adjusted accordingly.

In practice, to apply the INC method, the PV panel output current variation ΔI and PV panel output voltage variation ΔU are measured and divided to gain solar panels in the conductance gradient.

$$\frac{dI}{dU} \approx \frac{\Delta I}{\Delta U} \qquad 3\text{-}26$$

3.4 Switching technique

The DC-DC PWM power conversion technology, which has been developed and applied since the 1960s, is a hard switch technique. To enable the switching power to operate efficiently at high frequency, both industry professionals and academia have been studying and developing high frequency soft switching technology since the 1970s.

The characteristic of the soft switch is that the power device switches under a zero voltage condition or a zero current condition. Compared with a hard switch, the power device of the soft switch works under the zero voltage and zero current conditions, and the switching loss of the power device is small. In addition, the voltage and current gradient (dU/dt and dI/dt) are greatly reduced, which can eliminate the corresponding electromagnetic interference (EMI) and the radio frequency interference (RFI), thus improving the reliability of the converter. Furthermore, for the same switching losses, applying the soft-switching technique allows the system to operate at a higher frequency, thus reducing the weight and volume of the system. The switching losses are reduced to reduce the loss of the entire system. The way to reduce the switching loss is to realize soft switching, so soft switching has become an

important research direction for switching technology. In this paper, the working characteristics of the soft switch and hard switch are compared, and the soft switching technology is described in detail.

3.4.1 Hard switching

Fig 3-24 is the voltage and current waveform of the transistor for hard switching. In this discussion, the transistor is no longer an ideal device. During switching, the transistor generates turn-on losses and turn-off losses as the voltage current waveform overlaps in these durations; these losses are called the switching loss. The higher the switching frequency is, the higher the total switching loss is, and the lower the efficiency of the converter is. The switching losses limit the converter switching frequency, which limits the development of smaller and lighter converters.

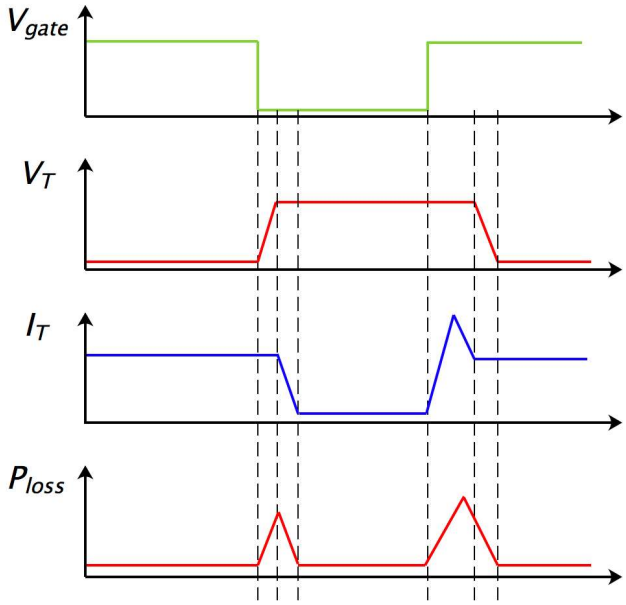


Fig 3-24. Voltage and current waveform of hard switching of the transistor and its switching power loss

The switching device in a traditional PWM converter works in hard switching. The four defects of hard switching hinder improvements of the working frequency of the switch device, which suffers from the following problems:

- Switching losses are large: When turning on, the current of the transistor rises, and the voltage drops simultaneously. When turning off, the voltage rises, and the current decreases simultaneously. The overlap of the voltage and current waveform leads to switching losses that are proportional to the switching frequency of the device.

- Back EMF is unavoidable: The back EMF occurs in the circuit due to the exitance of the inductive element (lead inductance, the leakage inductance of the transformer and other parasitic inductance). When the transistor is turning off, the current gradient in the transistor dI/dt is very large, resulting in large EMI. Moreover, based on the formula $U = L \cdot dI/dt$, the resulting peak voltage across the transistor is high, causing voltage breakdown.

- Capacitive turn-on issue: When turning on under high voltage, the electric charges stored in the junction capacitance of the switching device all dissipate in the switching devices, and overheating damage is caused by the switching devices. The formula is:

$$I = C \cdot dU/dt \qquad \text{3-27}$$

Large capacitive current and the conducting resistance of the transistor generate massive heat.

- Diode reverse recovery energy issue: When the diode state is converting from conduction into reverse cut-off, there is a reverse recovery period. During this period, the diode is still in the conducting state. If the series-connected transistor is immediately turned on, it easily causes the DC circuit to instantaneously short circuit. The DC power supply generates a large impact current for a short period of time, causing the transistor and diode device power consumption to increase dramatically or even cause damage.

3.4.2 Soft switching

From the previous analysis, the switching losses include the turn-on losses and the turn-off losses. Using soft switching technology can reduce the turn-on losses and turn-off losses of the converter. The turn-on and turn-off procedures of the soft switch are shown in Fig 3-25. There are several methods for opening a soft switch:

- Zero current turn-on: When the transistor is turning on, the current is kept at zero, or the current rate is limited, thus reducing the overlap region between the current and the voltage. As shown in Fig 3-25(a), the turn-on losses are greatly reduced.
- Zero voltage turn-on: Before the switch is opened, the voltage across the switch drops to zero. As shown in Fig 3-25(b), the opening loss is basically reduced to zero.

- Achieving A and B simultaneously, the turn-on losses are zero, which is the ideal situation.

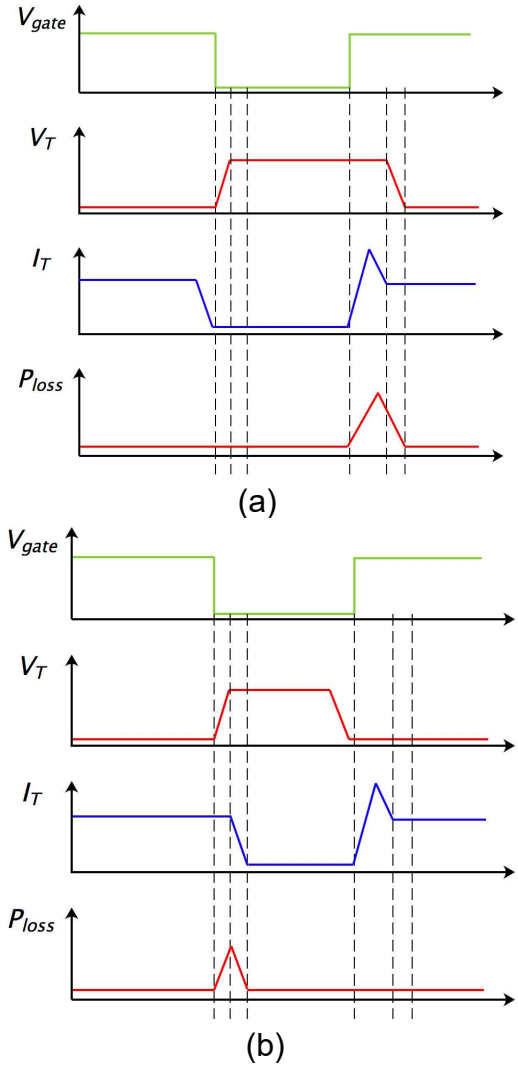


Fig 3-25. Indication of soft switching
(a) Zero current switching;
(b) Zero voltage switching

Similarly, there are several ways to turn off the soft switch:

- Zero current turn-off: Before the transistor turns off, the current is reduced to zero. Fig 3-25(a) shows that the turn-off losses are basically reduced to zero.

- Zero voltage turn-off: When the switch turns off, the voltage is kept at zero, or the upper rate of the voltage is limited, thus reducing the overlap region between the

current and the voltage. As shown in Fig 3-25(b), the turn-off is greatly reduced.

- Achieving A and B simultaneously, the turn-off losses are zero.

Chapter 4 Proposed Asymmetrical DC-DC converter for PV system

This chapter proposes an asymmetrical DC-DC converter for photovoltaic (PV) power systems. For modularized PV panels, a combination of the active clamping soft-switching technique is presented to achieve zero voltage switching ZVS and high-step-up features. The voltage boosting techniques, including turns-ratio boosting and voltage doubler, are carefully designed to be compatible with each other. The topology is not only capable of low voltage source boosting but can also be controlled by the MPPT algorithm to connect PV panels to high DC voltage bus and can achieve a high voltage gain with an efficiency of over 90% over a wide range of inputs by phase shift control. The entire system is simulated using the PSIM software and is tested experimentally. The key feature is its fault tolerance operation capability without the use of extra fault diagnosis circuitry. The innovation of the proposed converter is to combine the Flyback-forward operation, active clamping and voltage doubler in one topology as well as the capability of fault tolerance operation.

4.1 Circuit configuration and description

In Fig 4-1, the two main switching legs are composed of S_1, S_2, L_1 and L_2. S_1 and S_2 are the main switches connected in parallel to achieve an interleaved structure for coupled inductors L_1 and L_2, which can reduce the volume of the inductance for certain

input current ripple requirements. These coupled inductors have primary turns of N_1. The auxiliary reverse-connected switches are S_{c1} and S_{c2}. The clamping capacitors C_{c1} and C_{c2} are composed of the active-clamping circuit for the two main switching legs to recycle the leakage energy caused by leakage inductance and to realize ZVS for the primary power devices. The stray capacitors C_{s1} and C_{s2} of the main switches are also used to implement ZVS. The secondary windings L_{1b} and L_{2b}, which are in series with a leakage inductance L_{Lk1} and L_{Lk2}, with turns of N_2, are connected to the voltage double capacitor C_2. The marked end of L_{2b} is connected in the middle of the freewheel diodes D_{o2} and D_{o4}. The marked end of L_{1b} is connected to the voltage doubler C_1. D_{o1} and D_{o3} are the output diodes, and C_{o1} and C_{o2} are the output capacitors, which sustain one-third and two-thirds of the output voltage, respectively. V_{in} and V_{out} are the input and output voltages, respectively, and R is the load.

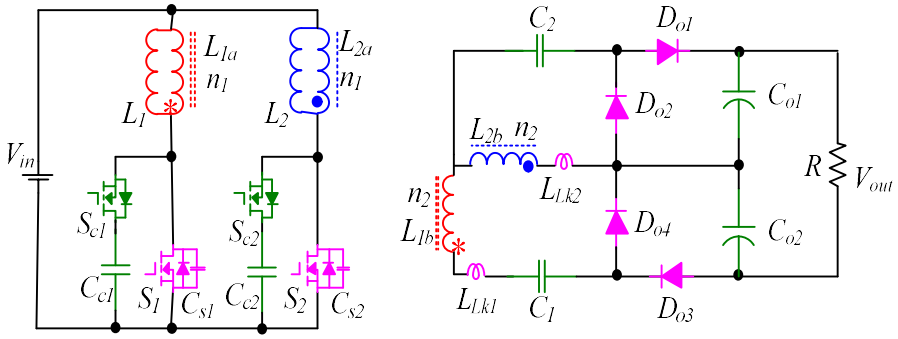


Fig 4-1. The proposed asymmetrical flyback-forward DC-DC converter

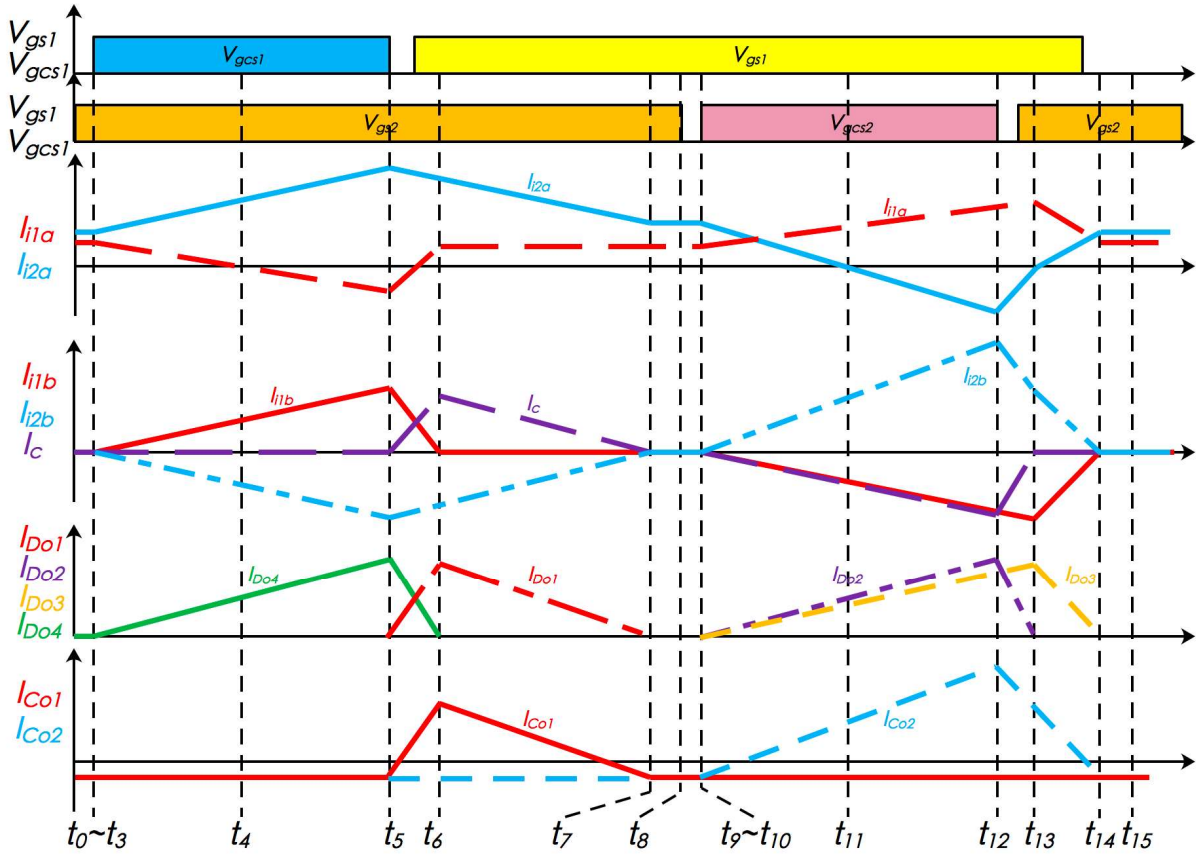


Fig 4-2. The waveform of the proposed converter

4.2 Operational analysis

Two signals with the same frequency and duty cycle are applied to the main switches S_1 and S_2. Due to the asymmetrical connection, the signal of S_1 leads the other by 160° (Fig 4-2). In contrast, the auxiliary switches are complementary with their corresponding main switches. Using steady state analysis, 15 stages can be classified as follows (Fig 4-3):

Stage 1 [t_0~t_1]: During this stage, both main switches S_1 and S_2 are in the turn-on state. The clamp switches S_{c1} and S_{c2} are in the turn-off state. In addition, the output diodes D_{o1} and D_{o2} are both reverse-biased. The two coupled inductors operate in the flyback mode to store energy. The primary winding currents I_{L1a} and I_{L2a} are stable, which

generates no current at the secondary side of the coupled inductor. The energy to the load is provided by the output capacitors C_{o1} and C_{o2}.

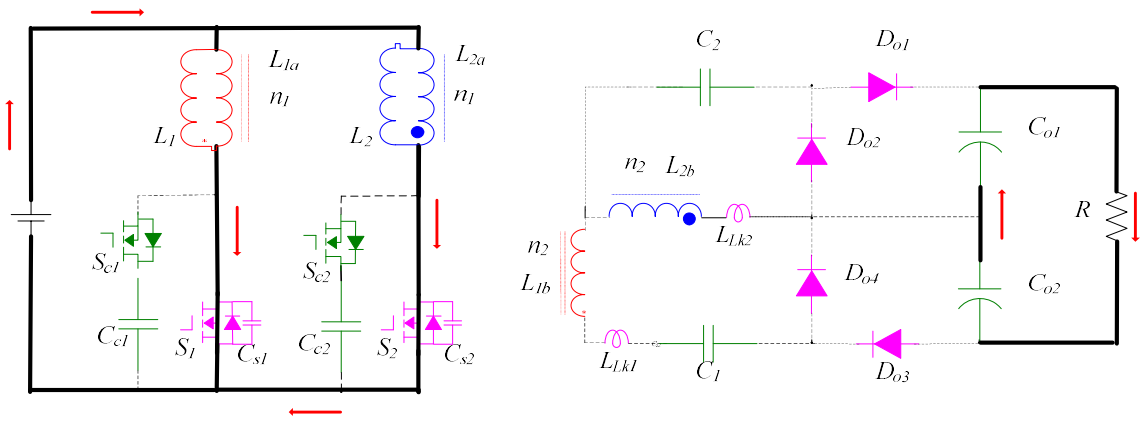
Stage 2 [t_1~t_2]: One of the main switches S_1 turns off at the beginning of this stage, resulting in nearly linear increasing voltage across the main switches and combining the existence of the parallel capacitor C_{s1}. This interval is very short because the primary winding current is large, and the stray capacitor is small.

Stage 3 [t_2~t_3]: The drain-source voltage of S_1 continues to increase until t_3. The drain-source voltage is larger than the voltage of clamp capacitor C_{c1}, which makes the parallel–reversed diode of the clamp switch conduct. The voltage of the clamp capacitor begins to increase for charging the primary winding current I_{1a}. From this stage, C_{c1} and L_{1a} begin to resonate.

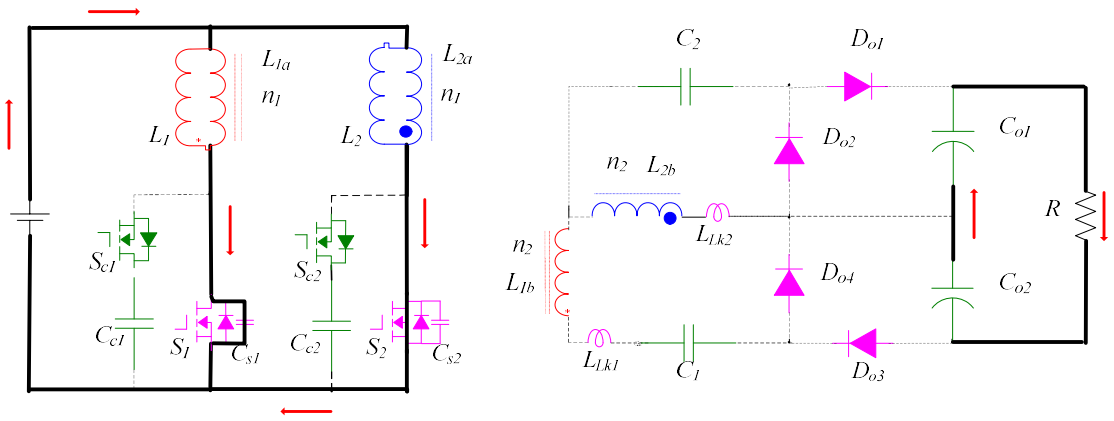
Stage 4 [t_3~t_4]: Due to the positive direction of the diode, the voltage across the clamp switch S_{c1} falls to zero at t_3. The turn-on signal is applied to the switch at the same time, which achieves ZVS turn-on operation. The current then quickly transfers from the diode to the switch. Increasing the voltage of C_1 leads to a decrease in the primary winding current I_{1a}, which increases the voltage on the secondary winding and generates the current I_{1b}. However, due to diodes D_{o3} and D_{o4}, the secondary winding current I_{1b} can flow only within the following path: L_{1b}-C_1-D_{o4}-L_{2b}-L_{1b}, namely, Path 1. In this stage, L_1 operates at the forward mode, and L_2 remains at the backward mode for the reverse direction increase of I_{2b}, leading to the increase in I_{2a}.

Stage 5 [t_4~t_5]: The primary winding current I_{1a} falls to zero at t_4. Because of the resonance, I_{1a} continues decreasing, which means that the capacitor also begins to discharge at the beginning of this stage.

Stage 6 [t_5~t_6]: At t_5, the turn-off signal is applied to the clamp switch S_{c1}. This is a ZVS turn-off operation condition because of C_{s1}. It restricts the increasing rate of the drain-source voltage of the main switch S_1, making the growth nearly linear. The primary winding current I_{1a} begins to increase, which decreases the secondary winding current I_{1b}. However, due to the existence of L_{2b}, the current through L_{2b} cannot decrease as fast as I_{1b}, so two new current paths appear in addition to Path 1. The other two paths are Path 2 (L_{2b}-C_2-D_{o1}-C_{o1}-L_{2b}) and Path 3 (L_{2b}-C_2-D_{o1}-R-C_{o2}-L_{2b}). In addition, it is obvious that Path 2 is charging C_{o1}, while Path 3 is discharging C_{o2}. L_{2b} begins to operate at the forward mode, and the primary side winding current of L_{2b} starts to decrease. One part of the leakage energy is delivered to the secondary winding L_{2b}, C_{o1} and R, while another part is recycled to the input source.



(a)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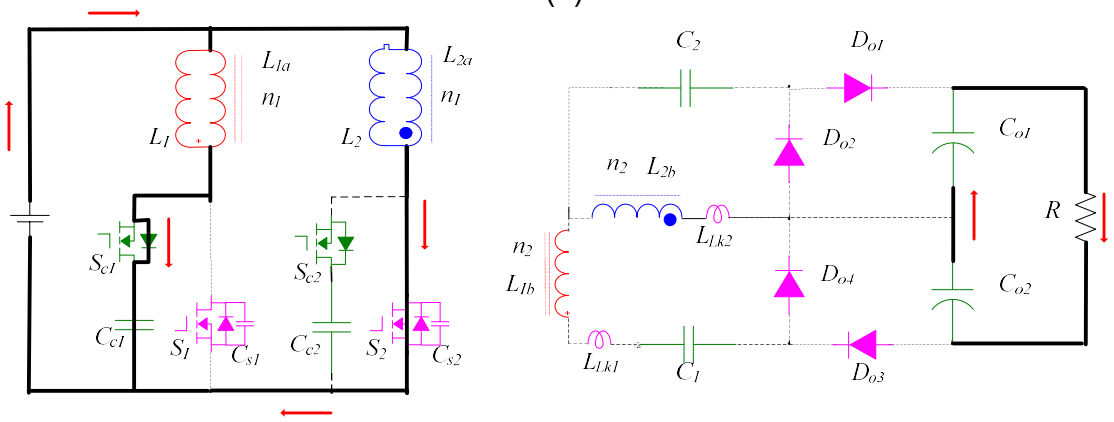
(b)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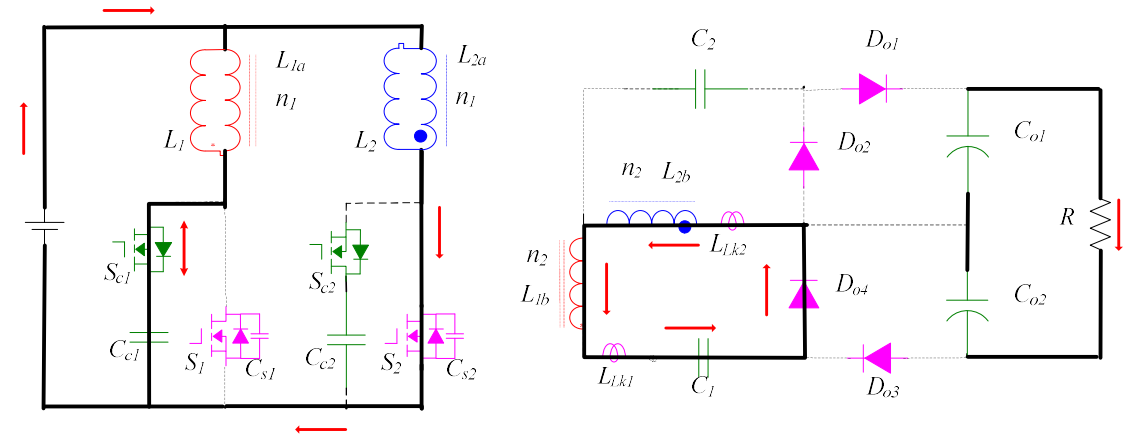
(c)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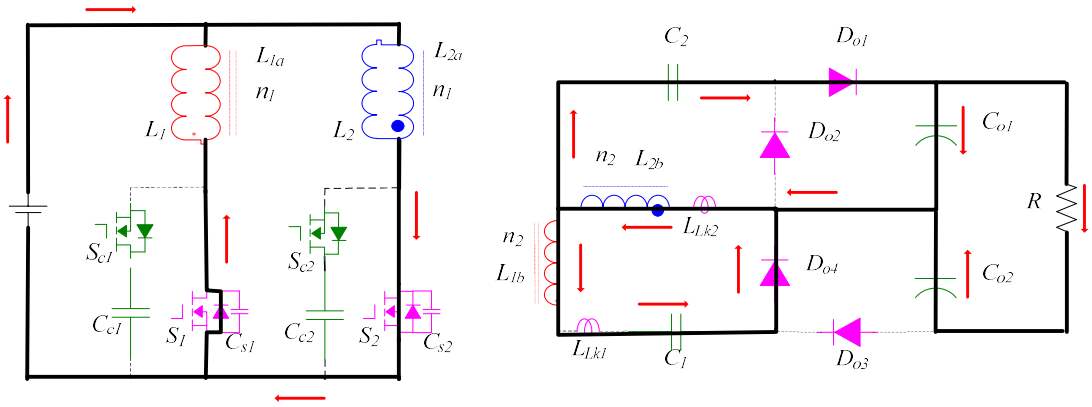
(d)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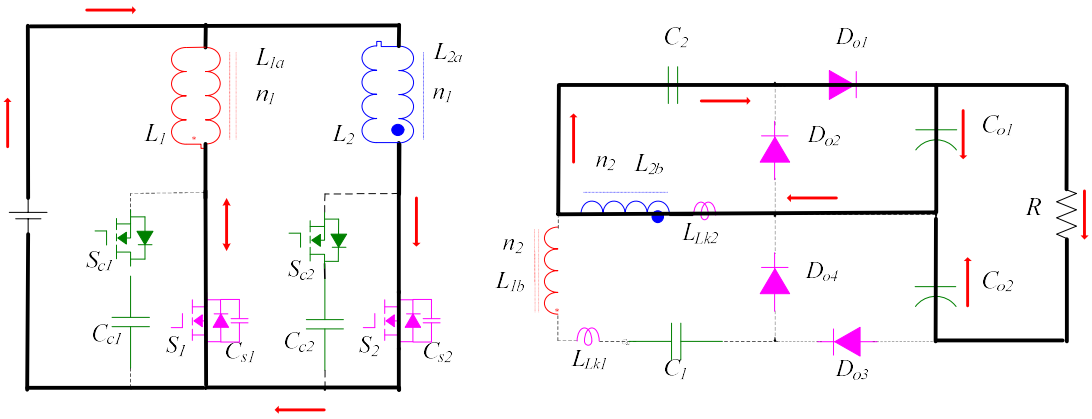
(e)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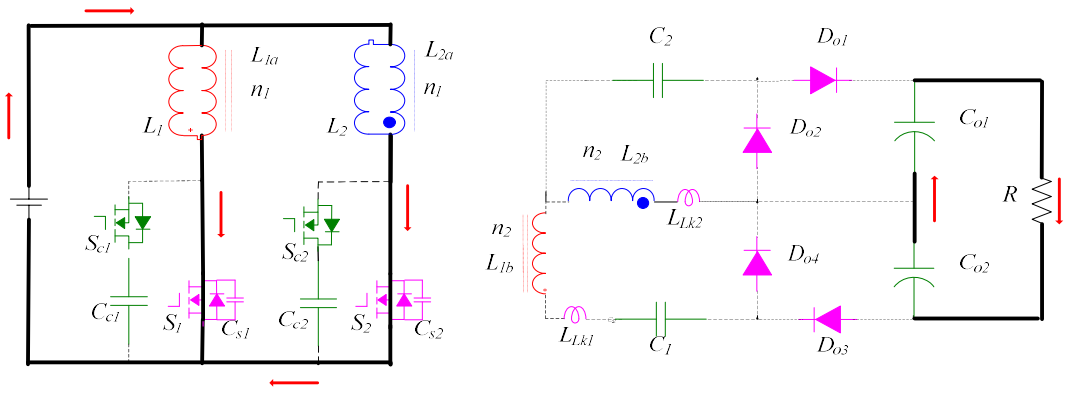
C_{o1}
n_2
L_{2b}
R
L_{Lk2}
n_2
L_{1b}
D_{o4}
C_{o2}
L_{Lk1}
C_1
D_{o3}

(f)


L_{1a}
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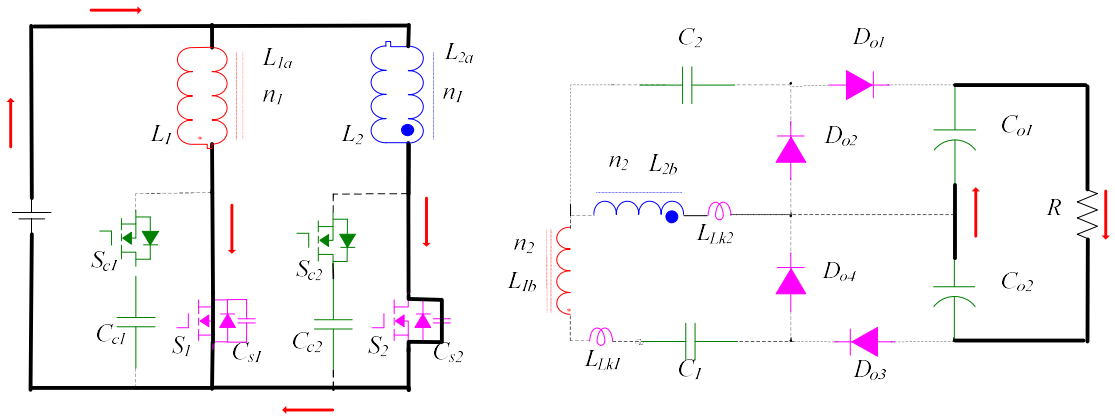
L_{2a}
n_1
L_1
L_2
S_{c1}
S_{c2}
C_{c1}
S_1
C_{s1}
C_{c2}
S_2
C_{s2}
C_2
D_{o1}
D_{o2}
C_{o1}
n_2
L_{2b}
R
L_{Lk2}
n_2
L_{1b}
D_{o4}
C_{o2}
L_{Lk1}
C_1
D_{o3}

(g)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C_{c2}
S_2
C_{s2}
C_2
D_{o1}
D_{o2}
C_{o1}
n_2
L_{2b}
R
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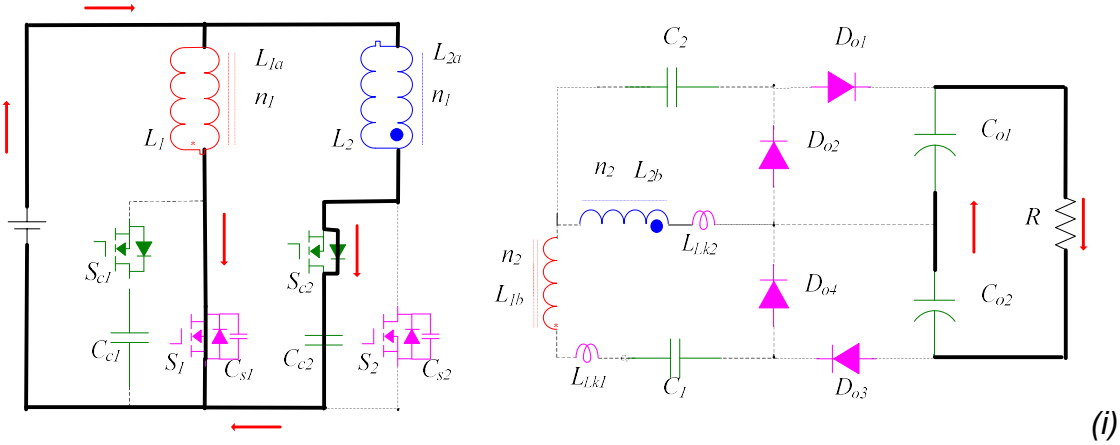
D_{o3}

(h)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C_{s2}
C_2
D_{o1}
D_{o2}
C_{o1}
n_2
L_{2b}
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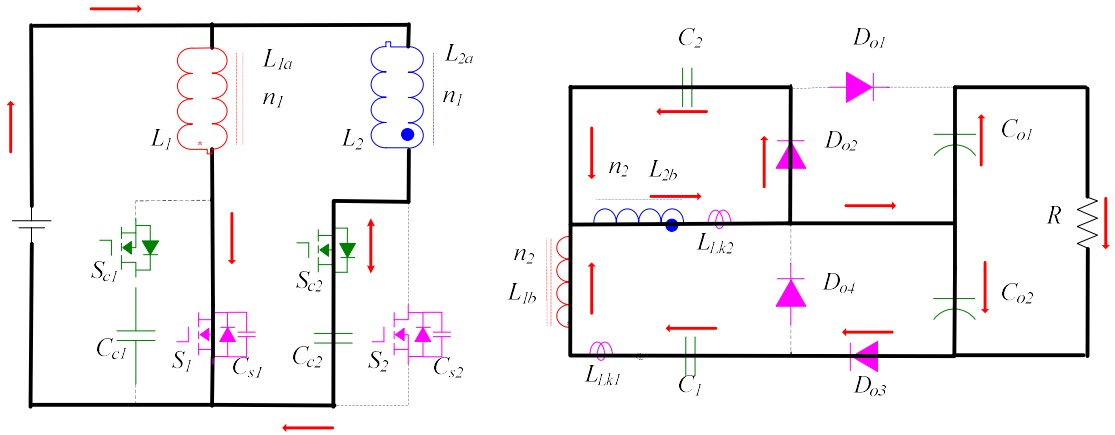
D_{o3}

(i)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C_{c2}
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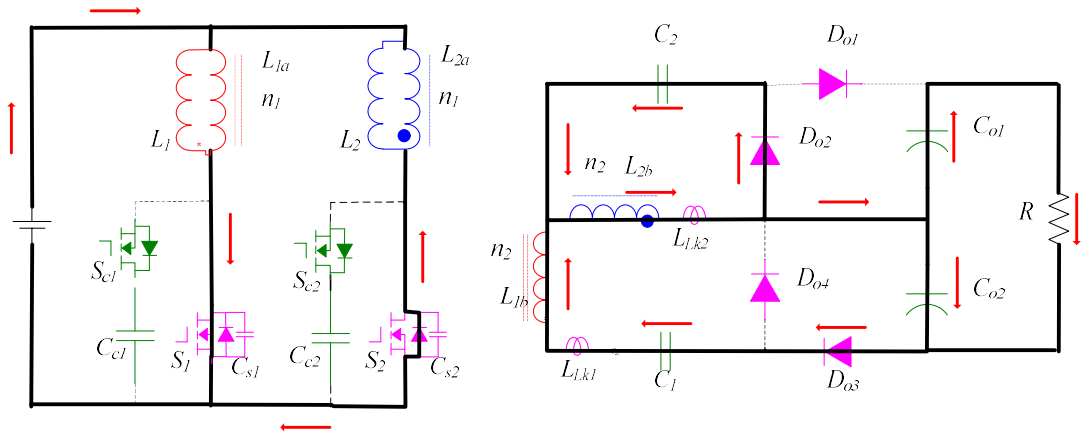
C_1
D_{o3}

(j)



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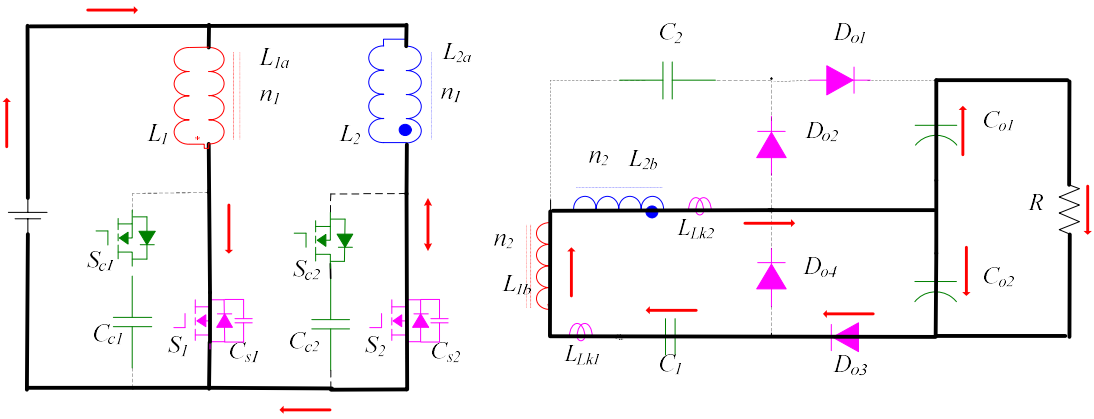
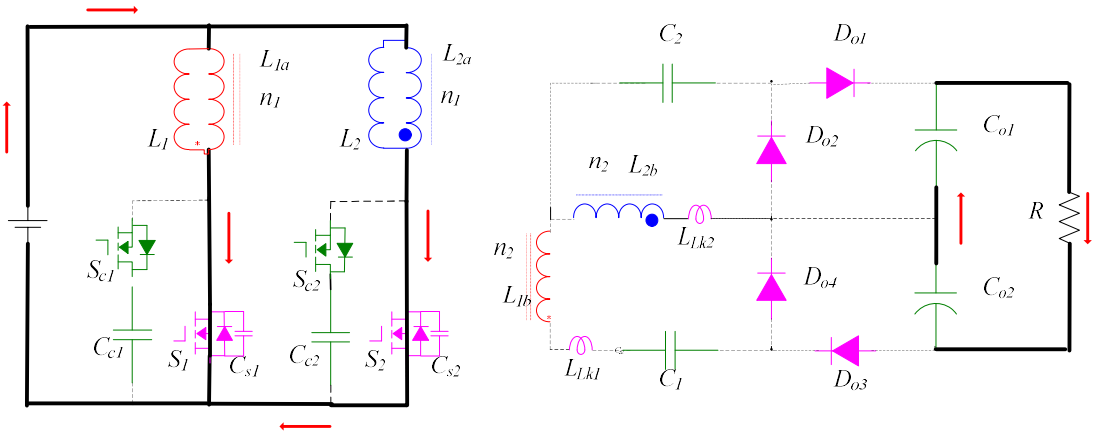


(l)



(m)

Fig 4-3. Circuit diagrams
(a) Stage 1 [t_0~t_1]; (b) Stage 2 [t_1~t_2]; (c) Stage 3 [t_2~t_3]; (d) Stage 4 [t_3~t_4] and Stage 5 [t_4~t_5]; (e) Stage 6 [t_5~t_6]; (f) Stage 7 [t_6~t_7]; (g) Stage 8 [t_7~t_8]; (h) Stage 9 [t_8~t_9]; (i) Stage 10 [t_9~t_{10}]; (j) Stage 11 [t_{10}~t_{11}] and Stage 12 [t_{11}~t_{12}]; (k) Stage 13 [t_{12}~t_{13}]; (l) Stage 14 [t_{13}~t_{14}]; and (m) Stage 15 [t_{14}~t_{15}].

Stage 7 [t_6~t_7]: At t_6, the primary winding current I_{1a} returns to the stable state, and the inductor L_{1a} operates at flyback-mode to store energy again. For the steady state of I_{1a}, the secondary winding current I_{1b} falls to zero. Then, the current paths have only Path 2 and Path 3 left. Without the source, the current of both paths continues to drop.

Stage 8 [t_7~t_8]: At the beginning of this stage, the currents in Path 2 and Path 3 fall to zero. The remaining part of this stage is the same as Stage 1.

Stage 9 [t_8~t_9]: The turn-off signal is applied to the main switch S_2. This stage is the same as Stage 2.

Stage 10 [t_9~t_{10}]: This stage is similar to Stage 3.

Stage 11 [t_{10}~t_{11}]: The primary end has a similar operation as Stage 4. Additionally, due to the reverse direction increasing of I_{1b}, the corresponding primary winding current I_{1a} begins to increase, similar to the behaviour of I_{1b} in Stage 3. However, for the secondary end, unlike in Stage 3, the secondary winding current splits into three different paths: Path 4 (L_{2b} - C_2- L_{2b}), Path 5 (L_{2b} - C_{o1} - R - D_{o3} - C_1 – L_{1b}) and Path 6 (L_{2b} - C_{o2} - D_{o3} - C_1 – L_{1b}). Moreover, the power for the load in this stage is provided by C_{o1} and the energy from the source, while the other output capacitor C_{o2} is charging.

Stage 12 [t_{11}~t_{12}]: This stage is similar to Stage 5.

Stage 13 [t_{12}~t_{13}]: The primary end of this stage is similar to that of Stage 7. The increase in I_{2a} leads to a decrease in I_{2b}. Because the current flow through C_2 is affected by only L_{2b}, the decrease rate of I_{c2} is fast, while the currents flowing through Path 5 and Path 6 decrease much slower than that in Path 4 due to the existence of L_{1b}.

Stage 14 [t_{13}~t_{14}]: At the beginning of this stage, the current of Path 4 falls to zero. The amplitudes of I_{2b} and I_{2a} are identical, and both continue to decrease, which leads to a change in the primary winding current value.

Stage 15 [t_{14}~t_{15}]: At t_{15}, the residual current of the secondary winding falls to zero. The rest of this stage is similar to Stage 1.

4.3 Steady-state circuit performance analysis

In this section, the following assumptions are made to simplify the analytical process:

- The two coupled inductors L_1 and L_2 are identical;
- The two clamping capacitors C_{s1} and C_{s2} are identical;
- The equivalent series resistance (ESR) is neglected;
- The two voltage doubler capacitors C_1 and C_2 are identical;
- The voltages of all capacitors are constant;
- The dead time effect is neglected;
- The voltage drop and the internal resistance of all devices are neglected.

These assumptions can be expressed as:

$$L_{m1} = L_{m2} = L_m \quad \text{4-1}$$

$$L_{Lk1} = L_{Lk2} = L_{Lk} \quad \text{4-2}$$

$$C_{c1} = C_{c2} = C_c \quad \text{4-3}$$

$$C_1 = C_2 = C \quad \text{4-4}$$

4.3.1 Voltage-gain derivation

The charging process of the first leg switching period can be calculated by I_c during t_5 and t_7. For the second leg, the process can be obtained by I_{L1b} during t_{10} and t_{14}. The charge of the load within a given period can be derived as:

$$Q_{load} = Q_{co1} + Q_{co2} = Q_{c1} + Q_{c2} \quad \text{4-5}$$

where Q_{co1} and Q_{co2} are the charges going through C_{o1} and C_{o2}, respectively, and Q_{c1} and Q_{c2} are for C_1 and C_2, respectively. Q_{c1} equals the integration of the current flows out of capacitor C_1, which means that the area of I_c is within [t_5~t_7]. By the same principle, Q_{c2} equals the area of I_{L1b} within [t_{10}~t_{14}]. However, due to the charging balance of the voltage doubling capacitors and the fact that C_2 is charged and discharged by only I_c, C_1 is affected by only I_{L1b}. These two currents can be transferred to I_c during [t_{10}~t_{13}] and to I_{L1b} during [t_3~t_6]. Then, 4-5 can be expressed as:

$$Q_{load} = A_{Il1b,3\sim6} + A_{Ic,10\sim13} \quad \text{4-6}$$

Then, the voltage gain of the output can be expressed as follows:

The time gap of [t_5~t_6] is known as:

$$t_5 - t_3 = (1 - D)T_s \quad \text{4-7}$$

where T_s is the switching period. The time gap of [t_6~t_7] can be calculated as:

$$t_6 - t_5 = \frac{I_{L1b}(t_5) - I_{L1b}(t_6)}{k_I`} = \frac{k_I(1-D)T_s}{k_I`} \quad \text{4-8}$$

where k_I and $k_I`$ represent the current slope rate of I_{L1b}, which is:

$$k_I = \frac{NV_{cc}-V_{c1}}{L_{Lk1}+L_{Lk2}} \quad 4\text{-}9$$

Substituting 4-2 into 4-9, k_I can be simplified as:

$$k_I = \frac{NV_{cc}-V_{c1}}{2L_{Lk}} \quad 4\text{-}10$$

Following a similar process for k_I`:

$$k_I` = \frac{V_{c1}}{2L_{Lk}} \quad 4\text{-}11$$

From 4-7 and 4-8, the time interval [t_3~t_6] can be obtained as:

$$t_6 - t_3 = \frac{(NV_{cc}-V_{c1})(1-D)T_s}{V_{c1}} \quad 4\text{-}12$$

In turn, $A_{Il1b,3\sim6}$ can be calculated as:

$$A_{Il1b,3\sim6} = \left(\frac{NV_{cc1}-V_{c1}}{V_{c1}}\right)\frac{NV_{cc1}-V_{c1}}{4L_{Lk}}(1-D)^2{T_s}^2 \quad 4\text{-}13$$

Similarly, the area of I_c within [t_{10}~t_{13}] $A_{Ic,10\sim13}$ can be expressed as:

$$A_{Ic,10\sim13} = \left(\frac{NV_{cc2}-V_{c2}}{V_{c2}}\right)\frac{NV_{cc2}-V_{c2}}{L_{lk}}(1-D)^2{T_s}^2 \quad 4\text{-}14$$

Then, the total amounts of charges to the load are:

$$\begin{cases} Q = A\frac{NV_{cc1}-V_{c1}}{L_{Lk1}+L_{Lk2}}F + B\frac{NV_{cc2}-V_{c2}}{L_{lk2}}F \\ F = (1-D)^2{T_s}^2 \\ A = \frac{NV_{cc1}-V_{c1}}{V_{c1}} + 1 \\ B = \frac{NV_{cc2}+NV_{cc1}-V_{c2}}{V_{c2}} + 1 \end{cases} \quad 4\text{-}15$$

For this asymmetrical connection of secondary side inductors, the voltage ratio of C_{o1} and C_{o2} is:

$$\frac{V_{co}}{V_{co}} = \frac{\left(\frac{NV_{cc}-V_{c1}}{V_{c1}}+1\right)\frac{NV_{cc}-V_{c1}}{L_{Lk}+L_{Lk2}}(1-D)^2{T_s}^2}{\left(\frac{NV_{cc}+NV_{cc}-V_{c2}}{V_{c2}}+1\right)\frac{NV_{cc}-V_{c2}}{L_{lk2}}(1-D)^2{T_s}^2} \quad 4\text{-}16$$

Based on the voltage-second balance principle, the voltage stress across the clamping capacitors V_{cc} is:

$$V_{cc1} = V_{cc2} = \frac{V_{in}}{1-D} \quad 4\text{-}17$$

In addition,

$$Q = \frac{V_{out}}{R} T_s \quad 4\text{-}18$$

$$V_{co2} = 2V_{c1} \quad 4\text{-}19$$

$$V_{co} = 2V_{c2} \quad 4\text{-}20$$

$$V_{out} = V_{co1} + V_{co2} \quad 4\text{-}21$$

Due to the complexity of the equation, from the simulation result, the voltage ratio of the two output capacitors is approximately 0.5. Therefore, the result of 4-16 is approximately 0.5.

Then, the voltage gain of the converter can be expressed as follows:

$$\begin{cases} M_{Lk} = \frac{V_{out}}{V_{in}} = \frac{-3K+\sqrt{9K^2+96NK}}{4} \\ K = \frac{N \cdot R \cdot (1-D) \cdot T_S}{L_{lk}} \end{cases} \quad 4\text{-}22$$

If L_{lk} is assumed to be very small for the proposed converter, then the gain expression can be simplified as:

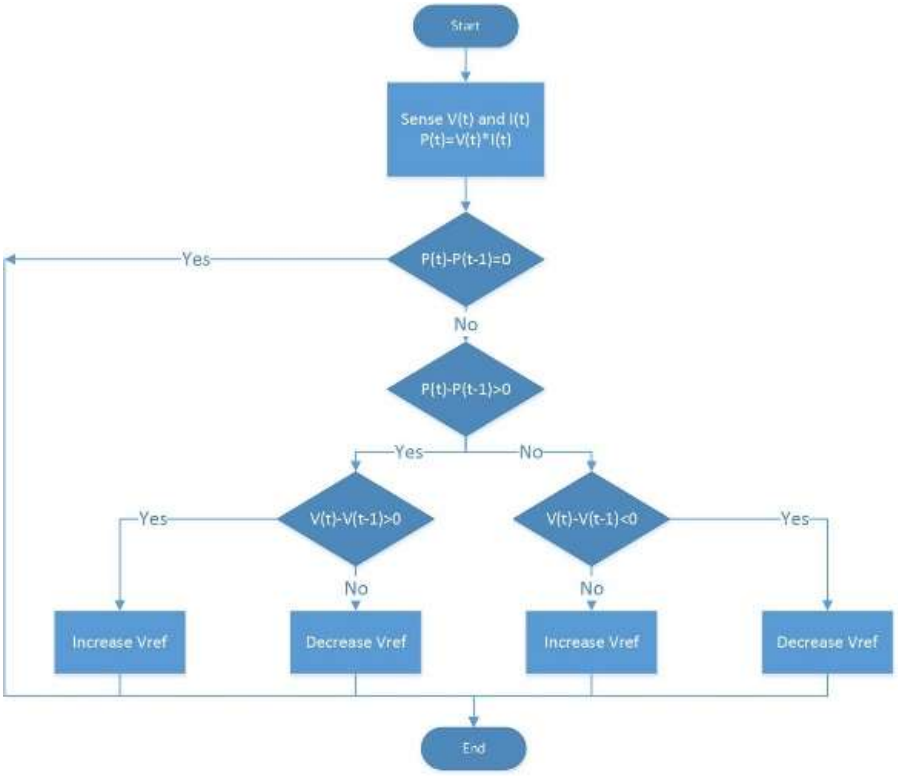
$$M_{Simp} = \frac{\sqrt{\left(\frac{N(1-D)RT_S}{L_{lk}}\right)^2 + \frac{32^{\ 2}RT_S}{L_{lk}}} - \frac{N(1-D)RT_S}{L_{lk}}}{4} \quad 4\text{-}23$$

From the above equations, it can be concluded that the voltage gain of the proposed converter is determined by the turn ratio of the coupled inductors, the duty ratio of the main switches, the leakage inductance, the switching frequency and the output load.

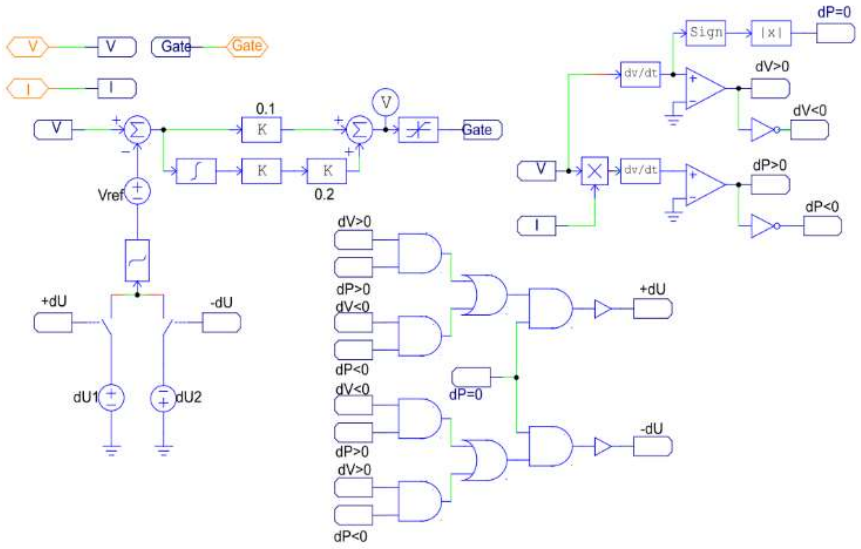
4.3.2 MPPT

Basic MPPT methods are applied in this paper, including constant voltage control (CVT), the perturb and observe (P&O) method and the incremental conductance

method. CVT has the advantages of simplicity and stability. However, the perfect voltage reference could be affected by temperature, sand on the panel and other environmental conditions. The P&O method can adjust the panel voltage to meet the maximum output power in any condition. The drawback is constant oscillation when reaching the maximum output, which causes energy losses. The incremental conductance method is better than the CVT method and P&O method in terms of accuracy, stability, efficiency and overall performance. Because of the requirements of the sensors and the complicated algorithm, the P&O method is not eco-friendly for residential or commercial PV panel groups, especially for modularized PV farms. In this paper, the P&O method is chosen to verify the converter for its simulation simplicity. Fig 4-4(a) is the flow chart of the P&O method.



(a)



(b)

Fig 4-4. P&O flow chart and simulation
(a) P&O flow chart;
(b) P&O method realization in PSIM

4.3.3 Voltage stress analysis

The voltage stress for the main switches is the voltage of the clamping capacitors:

$$V_{ds\_stress} = V_{cc} = \frac{V_{in}}{1-D} \approx \frac{V_{out}}{2N} \quad 4\text{-}24$$

The maximum voltage stresses of D_{o1}, D_{o2}, D_{o3} and D_{o4} are:

$$V_{Do1} = {}^{2}/_{3}\, V_{out} \quad 4\text{-}25$$

$$V_{Do2} = {}^{1}/_{6}\, V_{out} \quad 4\text{-}26$$

$$V_{Do3} = {}^{5}/_{6}\, V_{out} \quad 4\text{-}27$$

$$V_{Do4} = {}^{5}/_{6}\, V_{out} \quad 4\text{-}28$$

Clearly, to achieve a certain amount of voltage gain, the switching devices should be selected by considering the turns ratio of the coupled inductors and the resulting voltage stress.

4.4 Simulation results and analysis

A specific case study of the proposed DC-DC converter was performed. Using the PSIM software program, the converter was designed using certain parameters.

4.4.1 Simulation setup

An asymmetric isolated DC-DC converter was built using PSIM software. Fig 4-5indicates the configuration of the proposed converter.

In this case, a single PV panel is connected as an input source for the proposed converter, where there is a current or power limitation. For the purpose of topology testing, all the components are ideal except for the transformers, whose magnetizing inductance and leakage inductance are still taken into consideration. To simplify the circuit, the auxiliary capacitors parallel to the auxiliary switches are eliminated. The system is operated at a very high carrier frequency, and the two switches do not affect each other.

The system parameters are shown in Table 4-1, and the maximum power output of the PV panel is 156.1 W at 17.1 V. To present a clear waveform to analyse each switching period, the switching angle between the two main control legs is 165 degrees.

Table 4-1. Specifications of the simulated proposed converter

Parameter	*Value*
Clamping capacitor (μF)	*100*
Transformer turns ratio	*1:2*
Transformer magnetizing inductance (μH)	*50*
Transformer leakage inductance (pri)(μH)	*0.8*
Transformer leakage inductance (sec)(μH)	*0.2*
Voltage doubler capacitance (μF)	*4.2*
Output capacitance (each)(μF)	*100*
Load battery voltage (V)	*380*

4.4.2 MPPT simulation step-up

The proposed DC-DC converter was tested under a basic MPPT module based on PSIM software. The following table shows the parameters of the MPPT converter. The light intensity input is given by a square waveform from 70%-100% of its standard value, and the switching frequency was set to 10 kHz. Fig 4-4 shows the general P&O method flow chart and its simulation in PSIM. Due to the special operational routine, the output current is discontinuous, as shown in Fig 4-5(b). To optimize the output feature, a three-interleaved structure is also investigated (Fig 4-5(b)). The principle of the structure is to utilize the modularized topology, overlapping the output current waveform to minimize the current ripple at the output end. This structure requires an even distribution of the phase-shift angle. For residential and commercial PV systems, there are usually 20-30 PV panels with a rated power of 150 W for each PV panel. The performance of the actual system with an even distribution structure can be better than the simulated PV system.

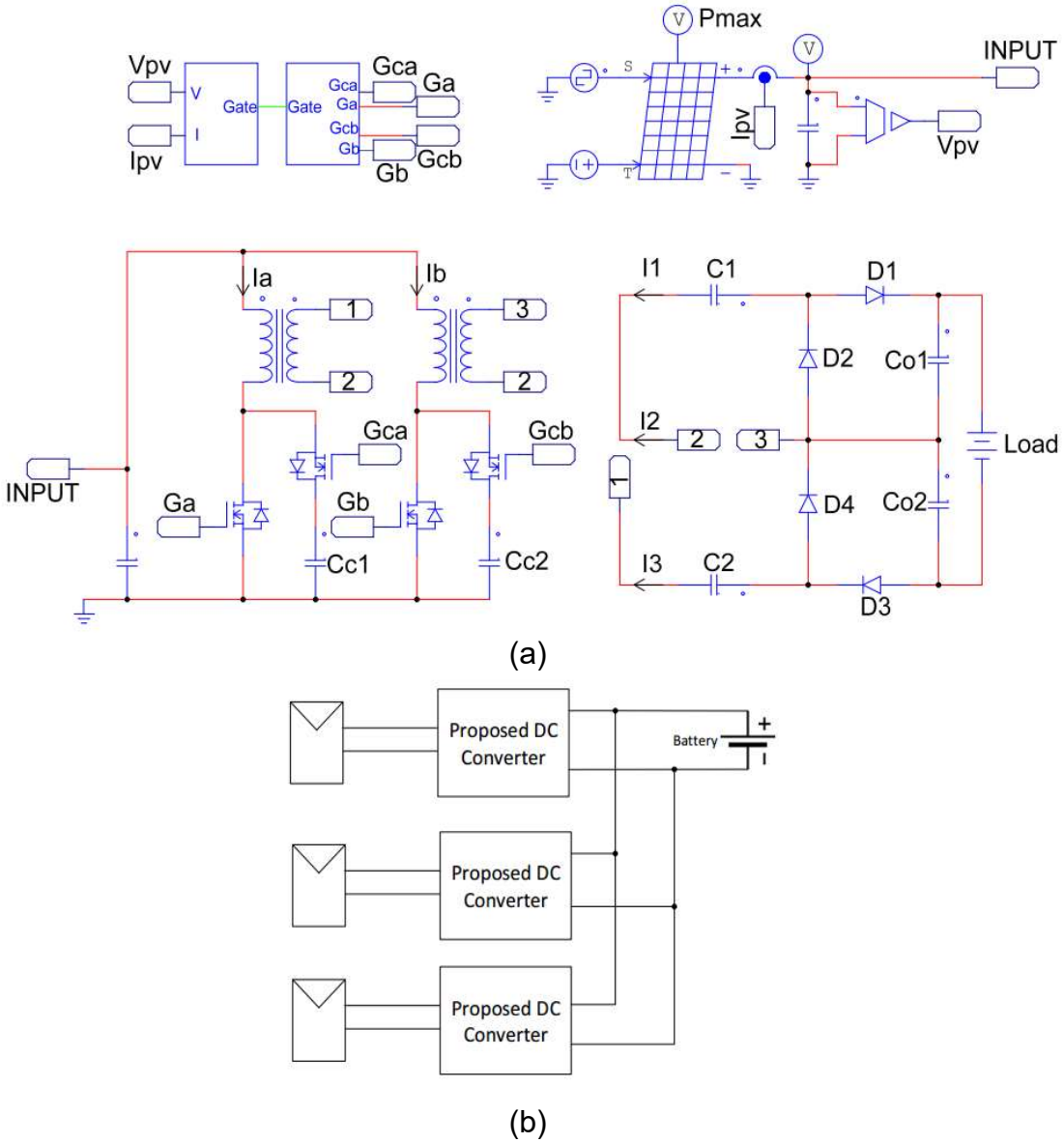


Fig 4-5. Simulation diagram
(a) Simulation diagram of the proposed converter;
(b) Three-interleaved topology structure.

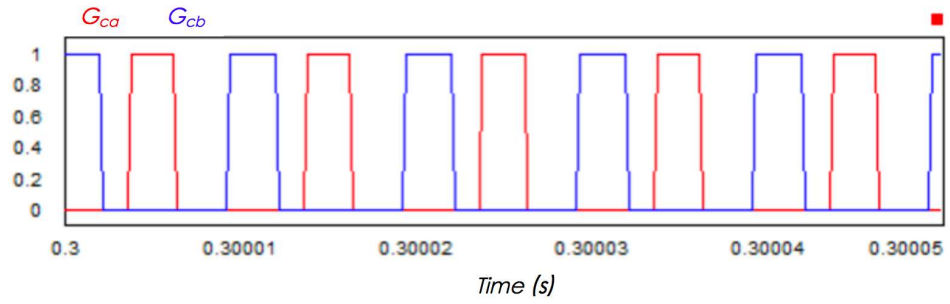
4.4.3 Fault tolerance and operation simulation

In this paper, only main switch open circuit faults are simulated and analysed. The primary side is an interleaved structure, and this topology allows the entire system to operate into two individual stages. The converter itself would still operate with one open circuit fault. However, the secondary side of the transformers are asymmetrically

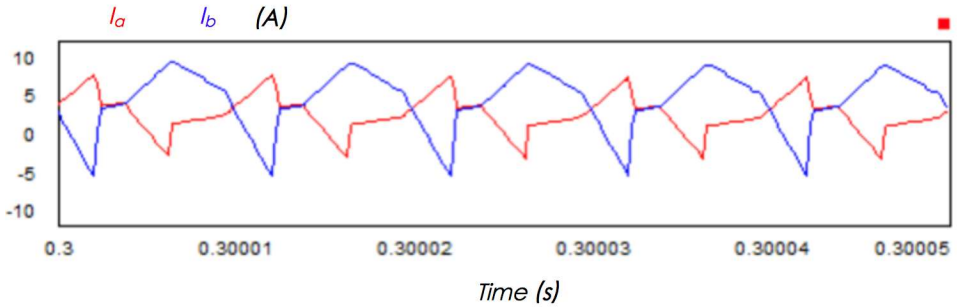
connected. For this case, Fig 4-11 and Fig 4-12 reveal the simulation results of the fault operation.

4.4.4 Simulation results

The configured converter was simulated based on the 100 kHz and 50 kHz carriers shown in Fig 4-6 and Fig 4-7, respectively, and with the sampling time step of 0.2 μs. Fig 4-8 indicates the phase-shift and non-phase-shift control reflection on the output current and diode current.



(a)



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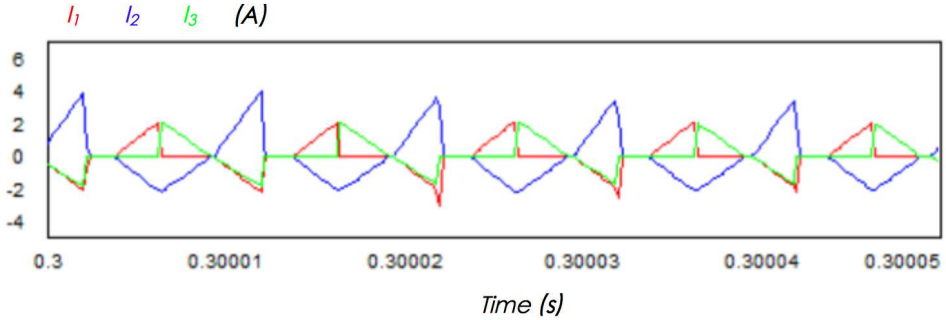

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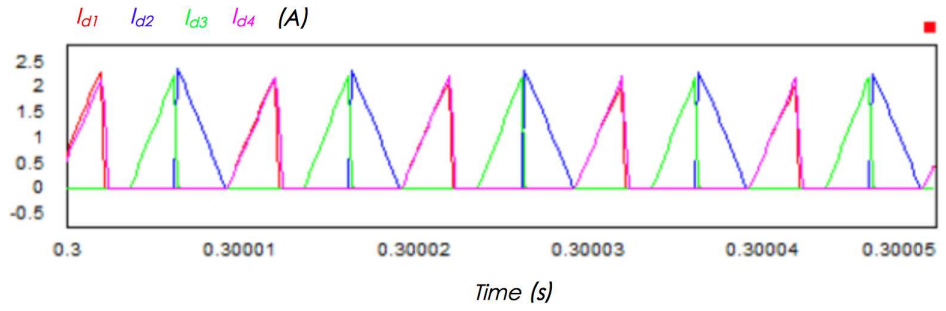

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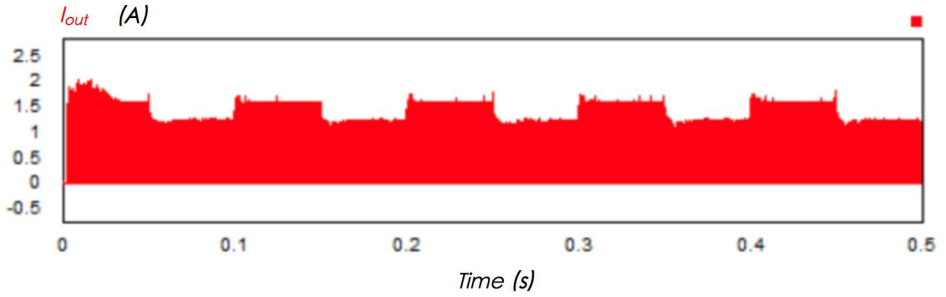
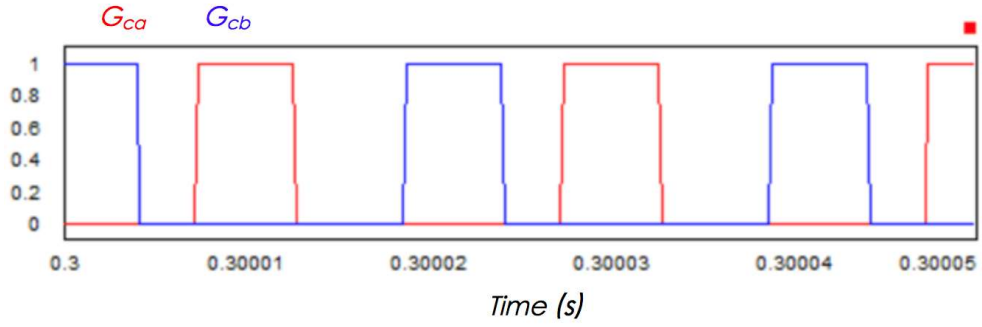
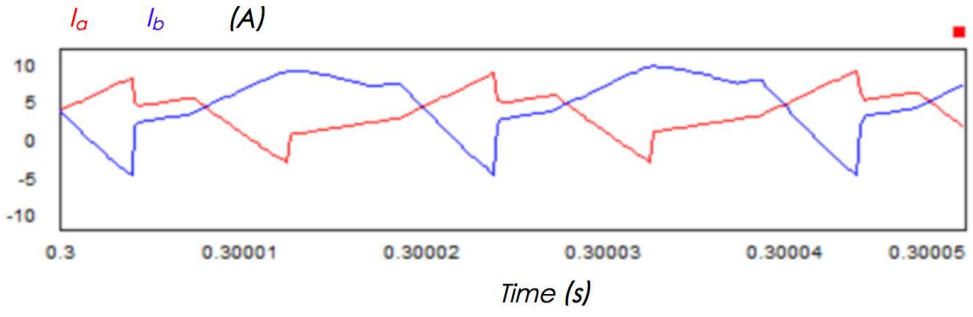


(e)

Fig 4-6. Simulation results from the PSIM software with the 100 kHz carrier waveform
(a) Carrier waveform;
(b) Current waveforms I_a and I_b of the primary side;
(c) Current waveforms I_a, I_b, and I_c of the secondary side;
(d) Current waveform of the four output diodes;
(e) Output current.



(a)



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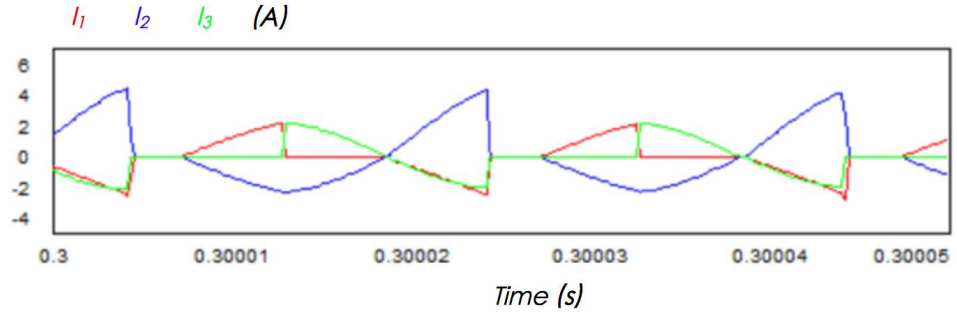

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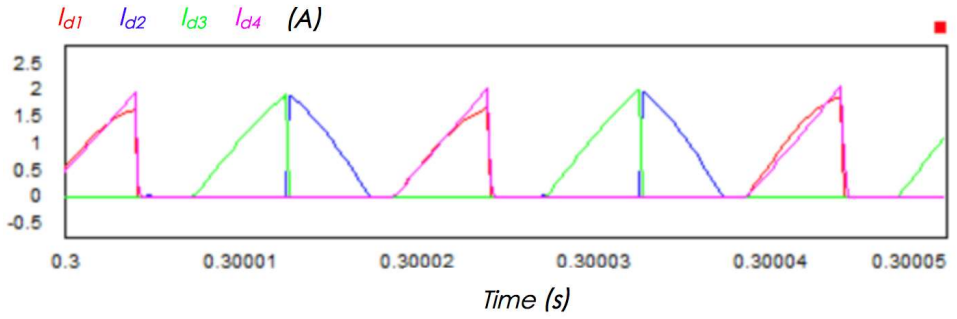

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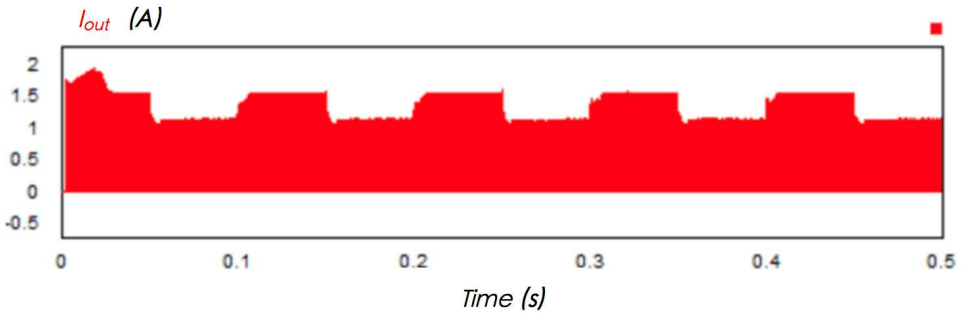
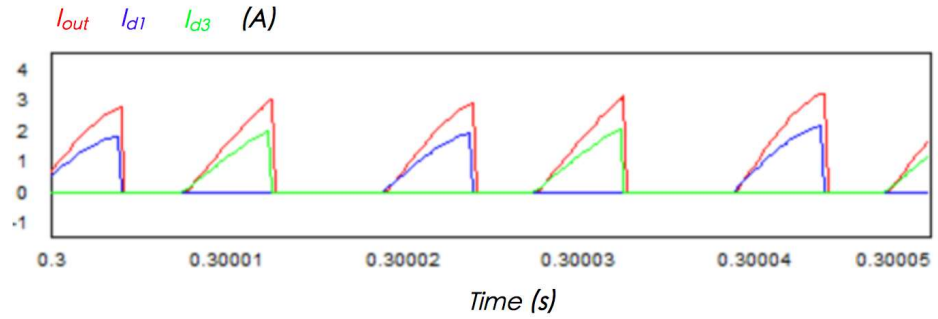
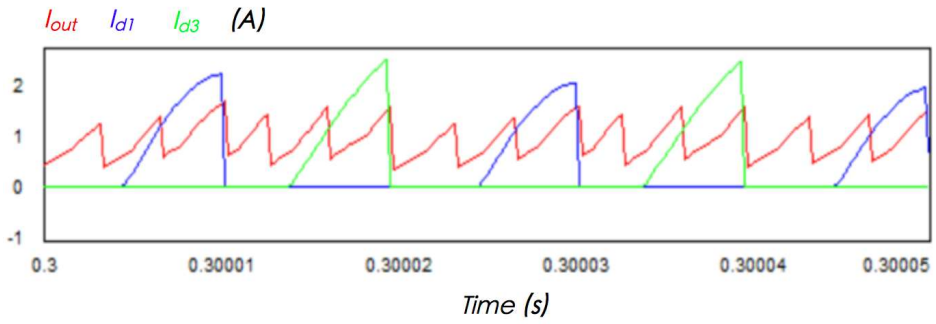


(e)

Fig 4-7. Simulation results from the PSIM software with the 50 kHz carrier waveform
(a) Carrier waveform;
(b) Current waveform I_a, I_b of the primary side;
(c) Current waveform I_a, I_b, I_c of the secondary side;
(d) Current waveform of four output diodes;
(e) Output current.



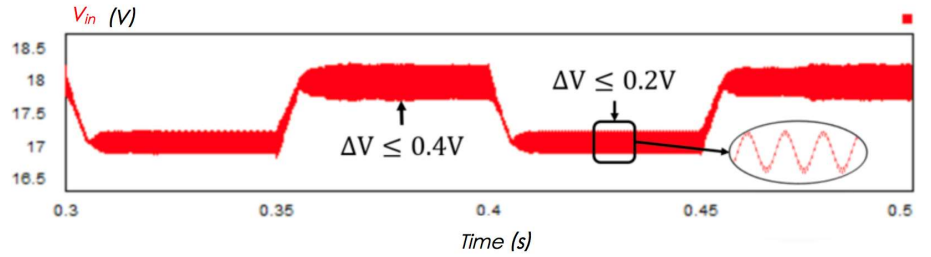
(a)



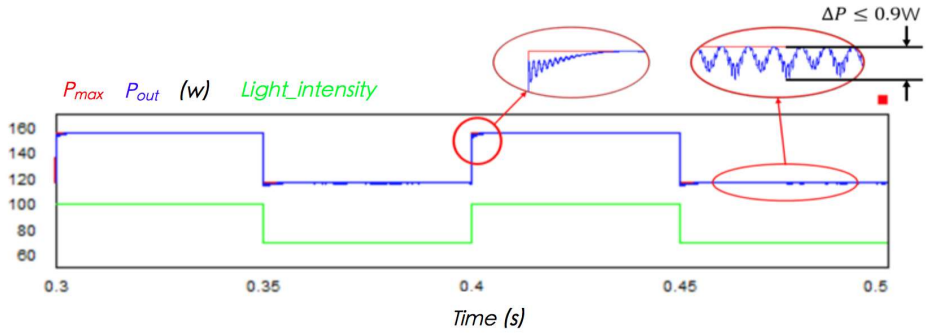
(b)

Fig 4-8. Fault model simulation results on output diodes
(a) Output current waveform compared with current waveform through output diodes D1 and D3 in three-interleaved topology (non-phase-shift);
(b) Output current waveform compared with current waveform through output diodes D1 and D3 in three-interleaved topology (phase-shift).

The results clearly indicate that the proposed converter is working properly, and the result waveform is very close to the theoretically deduced waveform presented in Fig 4-2. Fig 4-6(a) and Fig 4-7(a) present the switching signals of the main switches under 100 and 50 kHz, which are merely indications to show that the operations matched the theoretical analysis. Fig 4-6(b) and Fig 4-7(b) reveal the currents in the primary end of the proposed converters. As shown in Fig 4-6, the 100 kHz example has linear gradient currents, and under 50 kHz, the gradients have more curvy disturbances than the theoretical waveform. The same reactions also appear in Fig 4-6(c) and Fig 4-7(c) and in Fig 4-6(d) and Fig 4-7(e). This result is caused by the oscillation from the clamping capacitor and the inductance from the transformer. Fig 4-6(e) and Fig 4-7(e) suggest that the outputs of the converter would be close to each other. However, with the oscillation, the higher switching frequency would have a lower voltage and current ripple, leading to higher efficiency, as verified in a later subsection.

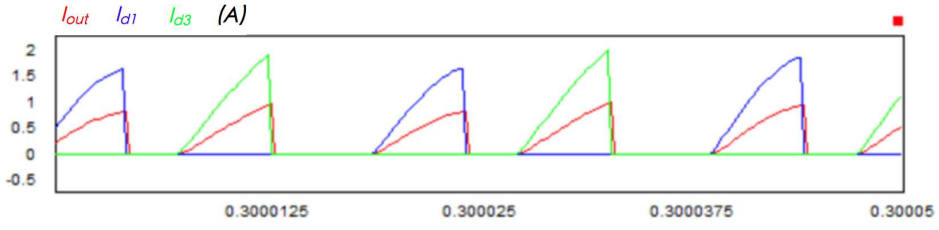


(a)

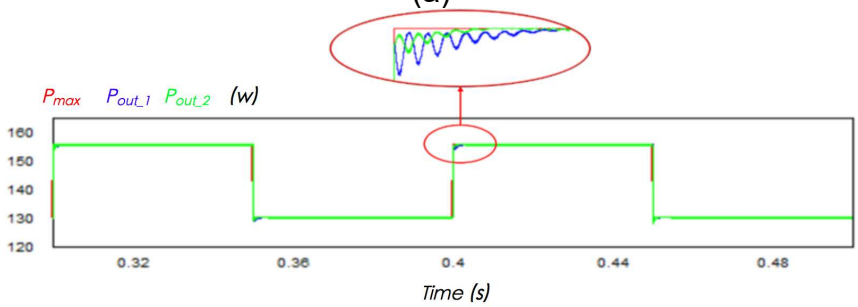


(b)

Fig 4-9. Simulation results for the PV output
(a) PV output voltage;
(b) Maximum power output and actual power output vs. light intensity input.



(a)

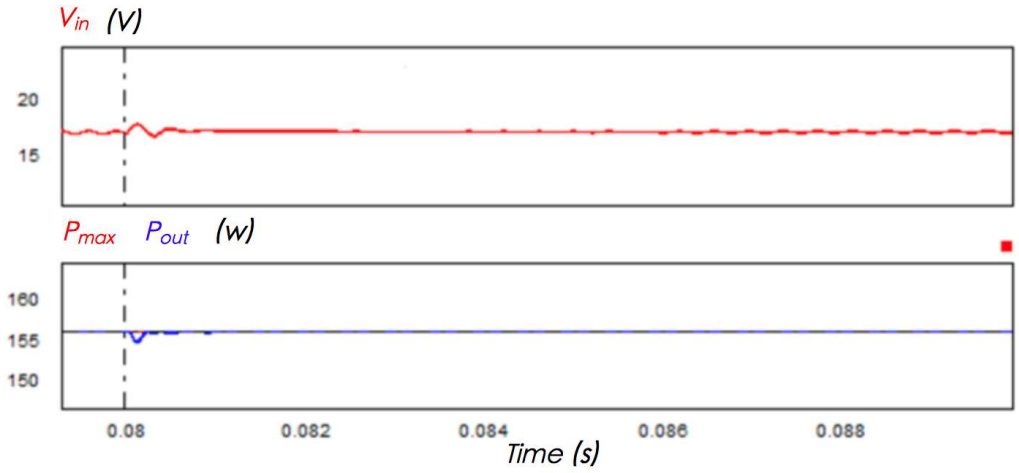


(b)

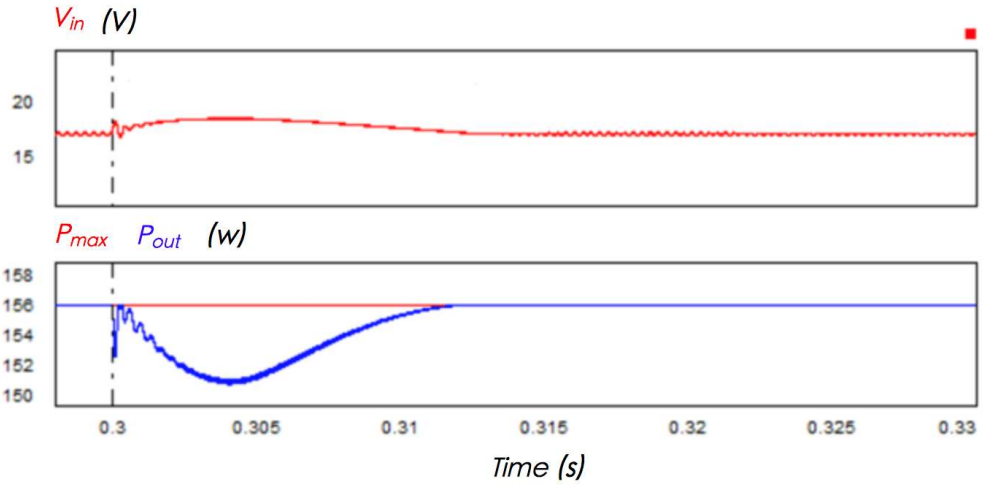
Fig 4-10. Fault model simulation results of PV output
(a) Output current waveform compared with the current waveform through output diodes D1 and D3, (b) Actual output power matching maximum power duration under different reference voltage steps: Po represents 0.1 V, and Po_1 represents 0.05 V.

Fig 4-9 shows the simulation results of the MPPT. The unmatched parts of the maximum PV output and the actual output are caused by the unbalanced input power and output power of the entire system.

Under the assumption of ideal circumstances, no energy consuming elements were included in this simulated system. However, with the existence of leakage inductance in the transformer, the power dissipates into the air. From equation 4-22, the leakage inductance, load resistance and carrier frequency affect the voltage gain, which in turn affects the efficiency. Fig 4-10(a) indicates that the efficiency decreases with decreasing carrier frequency. In addition, the high frequency brings more stability to the system, which is indicated by the input and output current ripple.

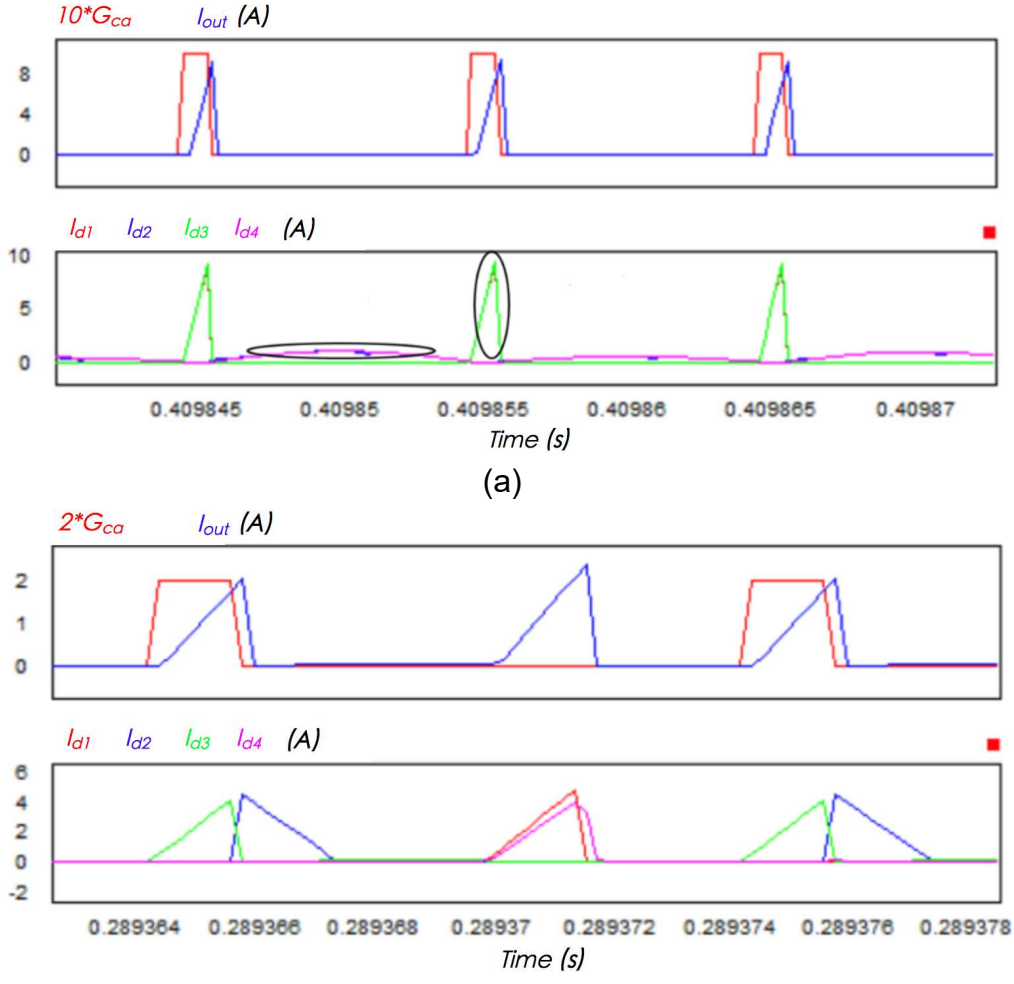


(a)



(b)

Fig 4-11. Main switch open circuit fault transit
(a) Ga open circuit fault;
(b) Gb open circuit fault.



(a)

(b)

Fig 4-12. Current waveform under fault tolerance operation
(a) Ga open circuit fault;
(b) Gb open circuit fault.

The phase-shift technique is an important control scheme for interleaved structures such as those proposed in this paper. With properly tuned PI control, the converter could achieve better output flexibility when small variations occur without undertaking major tuning of the duty ratio of the switches. In Fig 4-11 and Fig 4-12, the simulation results indicate the transit output power/voltage of the PV panel and the current waveforms of the load/output diodes. These figures show that under a S_1 and S_2 open circuit fault, the PV panel would suffer from different variations regarding the output voltage and power. The system can be tuned to its original outputs. The open circuit faults in S_1 and S_2 have different impacts because the system is asymmetrical; the transformer corresponding to S_2 has a larger current than S_1. This asymmetry explains why S_2 would have a larger impact on the system than S_1.

4.5 Experiment

The proposed topology is tested with a DC power supply as the input source. An ezdsp 28335 is used to generate the PWM waveform, and an 800 Ω resistive load is used for energy consumption. The IGBT is driven by an MCP1406E MOSFET/IGBT driver fed by an A3120 opto-coupler and, the entire drive system is powered by a TJ-IB2415LS DC-DC converter. The experimental platform is shown in Fig 4-13. The circuit is tested under an open circuit PWM control with a fixed duty cycle varying from 0.2 to 0.55. The switching frequency changes from 10 kHz to 30 kHz, and the input voltage is tuned from 5 V to 35 V. Fig 4-14 to Fig 4-20 show the experiment results regarding the relationship between the gain ratio and input voltage (and the switching frequency and

duty ratio) and between the efficiency and input voltage (and the switching frequency and duty ratio). Due to the fixed duty ratio and load resistance, increasing the input voltage means increasing the power flow through the converter. Because there are fixed power losses in a practical system and because of the oscillation effect mentioned in subsection 4.4.4, the system efficiency and voltage gain increase when the input power increases. As shown in Fig 4-14, the voltage gain ratio increases from 14 to 17.5 as the input voltage increases from 5 to 35 volts because the percentage of the inherent system power loess decreases while the total power of the system increases. Fig 4-15 tells the same story as Fig 4-14 from the efficiency point of view. However, there is a small distortion in Fig 4-14 and Fig 4-15, which could be caused by system error and sensor error. The voltage gain decreases from 17.89 to 17.20 when the switching frequency increases from 1 kHz to 4 kHz with the soft-switching technique (Fig 4-16(a)). However, without the soft-switching technique, the voltage gain increases from 17.81 to 16.76 with respect to the same switching frequency range (Fig 4-16(b)). These two figures demonstrate that the soft-switching technique increases the efficiency and voltage gain ratio by 2.63% at a switching frequency of 4 kHz, and the increased ratio increases at a higher frequency. Moreover, the voltage gains still decreased with the soft-switching technique, and the power loss could be caused by the reverse recovery energy loss of the diodes. Fig 4-19 and Fig 4-20 indicate that soft-switching is achieved for overlap turn-on and non-overlap turn-on in

two major switches. The highlighted circles in these two pictures are the interval of soft-switching, which occurs when the current is in the free-wheeling state.

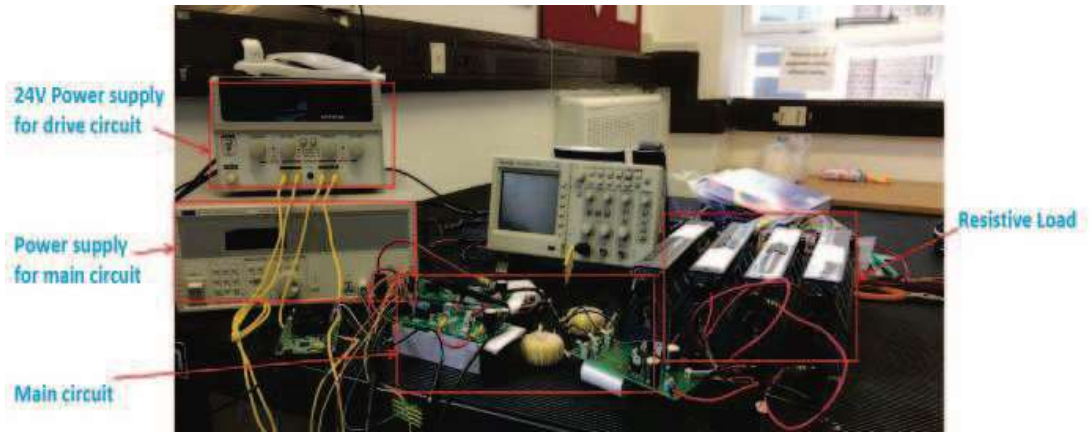


Fig 4-13. Experimental platform

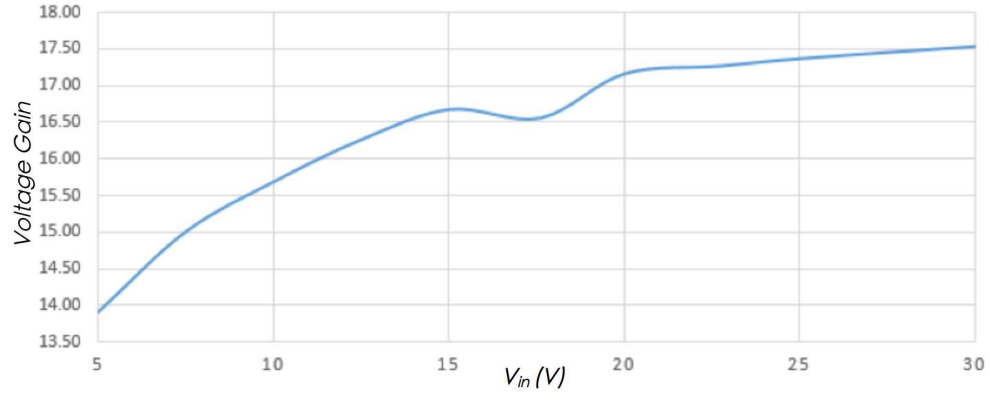


Fig 4-14. Voltage gain vs. V_{in}

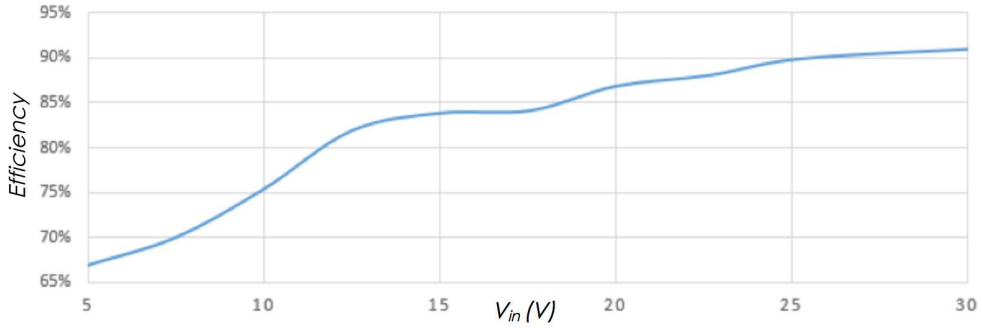
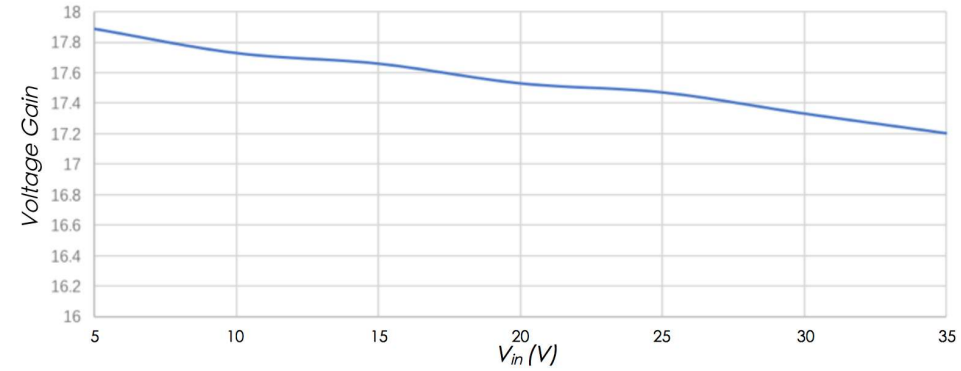
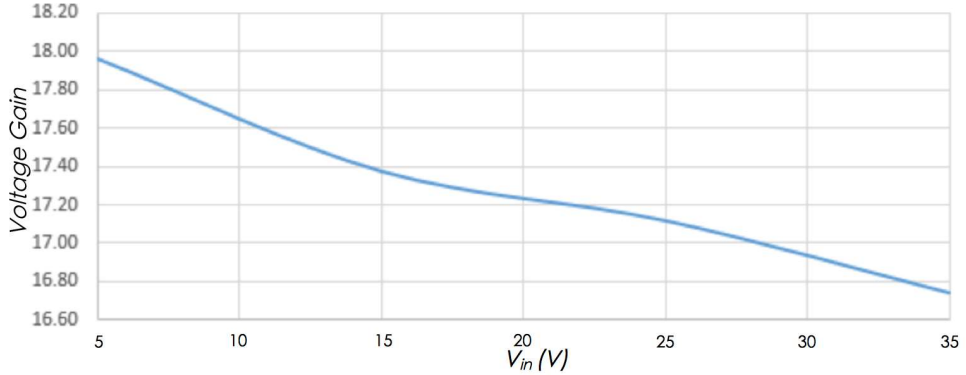


Fig 4-15. Efficiency vs. V_{in}



(a)



(b)

Fig 4-16. Voltage gain vs. switching frequency
(a). System with soft-switching technique;
(b). System without soft-switching technique.

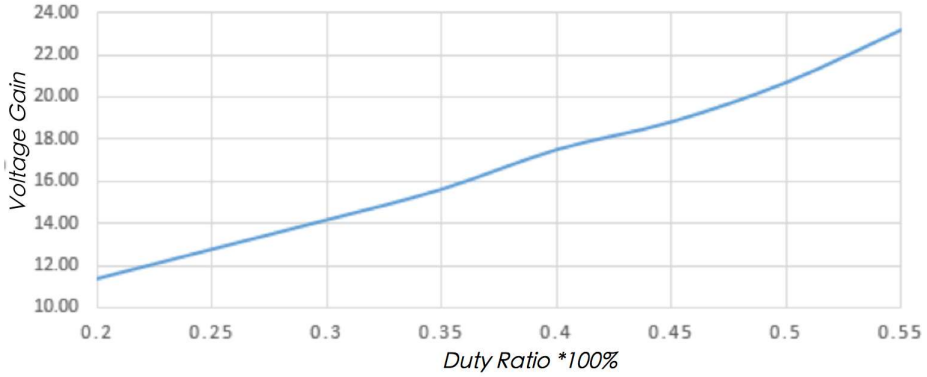


Fig 4-17. Voltage gain vs. duty ratio

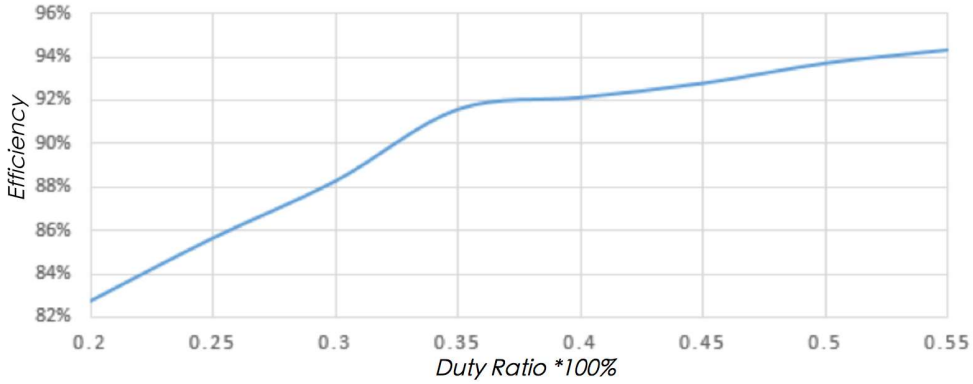


Fig 4-18. Efficiency vs. duty ratio

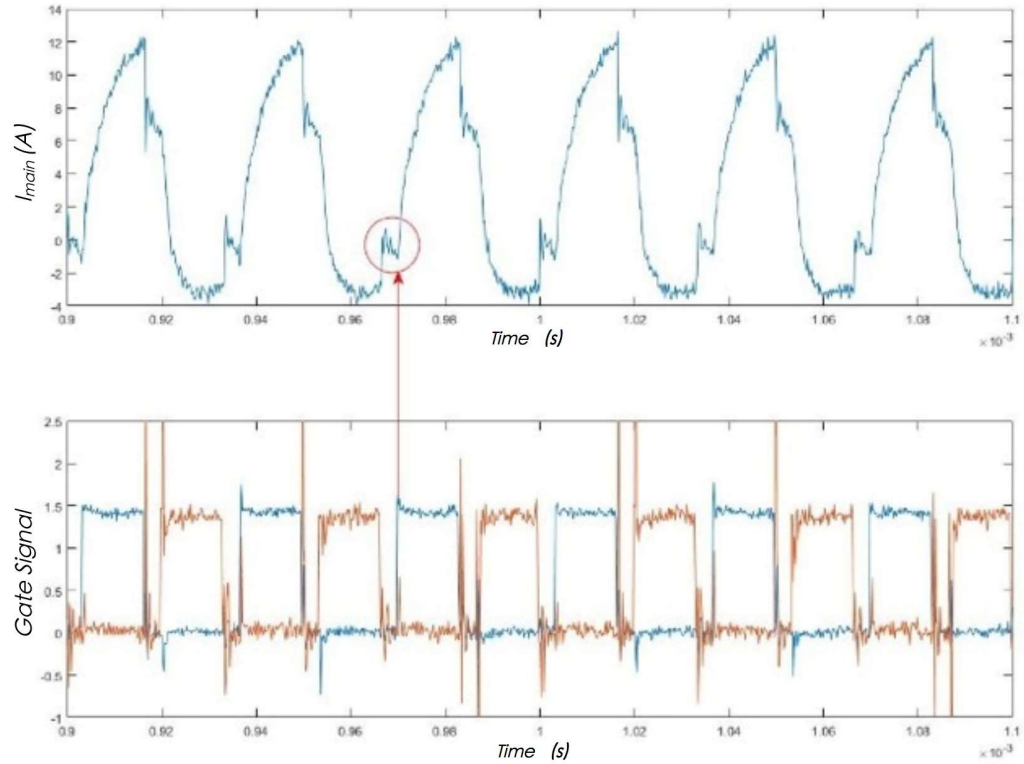


Fig 4-19. Main switch current indicating soft-switching for D=0.4

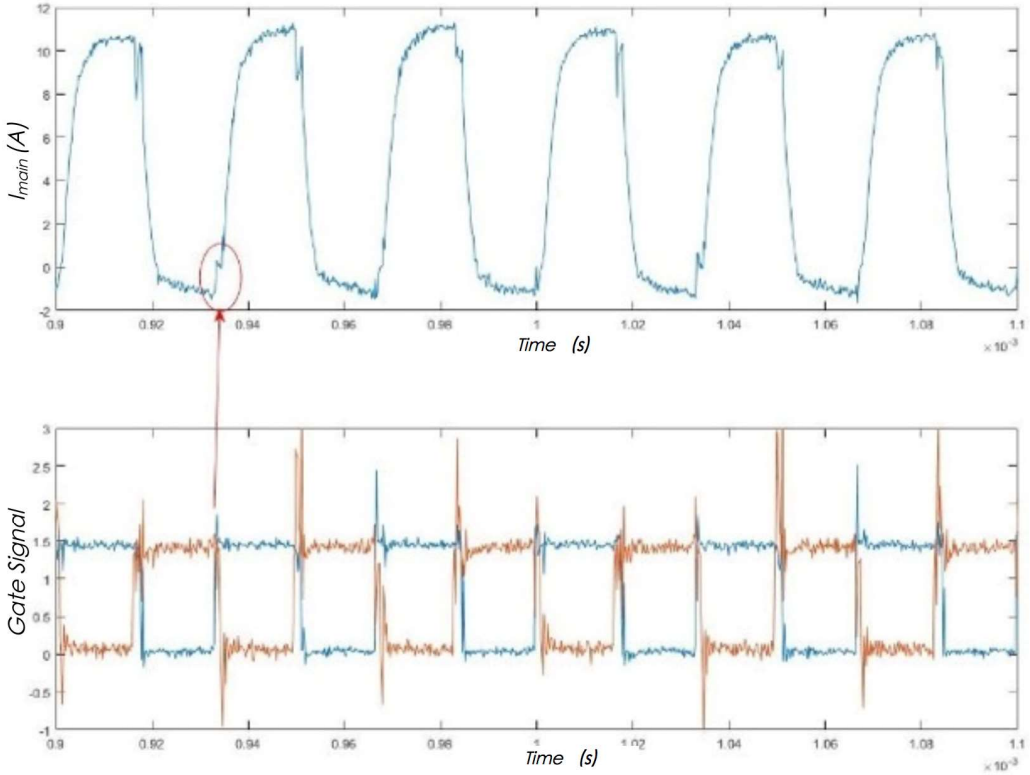


Fig 4-20. Main switch current indicating soft-switching for D=0.55

4.6 Conclusion

A high-step-up flyback-forward asymmetrical DC-DC converter with an active clamping circuit is introduced in this paper. This convertor pushes the current limits of voltage gain by employing a voltage multiplier and transformer. The flyback-forward structure avoids the drawback of the standalone flyback and forward topology. An interleaved connection at the primary end of the transformer reduces the voltage stress, and an active-clamp circuit achieves ZCS turn-off, increasing the circuit efficiency. The simulation results indicate that the system is controlled by the carrier frequency, output power demand and shift angle, thus proving that this topology could be applied to a PV-to-grid system. The practical experiment indicates that the topology can be properly operated. Compared to the symmetrical output system, the proposed topology can achieve a higher voltage gain. Future work could include phase shift control, hysteresis current control and practical experimentation.

Chapter 5 Switched-capacitor DC-DC converters

In the last chapter, an isolated asymmetric DC-DC converter was proposed, while in this section, a detailed description of a non-isolated high-step-up modular switched-capacitor DC-DC converter is presented along with an analysis of system performance. A modular switched-capacitor DC-DC converter (MSCC) is designed to boost the input voltage to a high voltage level and can be applied for photovoltaics and electric vehicles. This topology has high extensibility for high voltage gain output. The merits of the converters include fault tolerance operation and voltage regulation with a minimum change in the duty ratio. These features are built in when designing the modules and then integrated into the DC-DC converter. The converter performance, including voltage gain, voltage and current stresses, is determined and tested. The converter is modelled analytically, and its control algorithm is analysed in detail. Both a simulation and experiment are performed to verify the topology under normal operation and fault mode operation. The innovation of the proposed converter is modularization with fault tolerance capability. This convertor can overcome open circuit faults of both the transistors and capacitors.

5.1 Circuit architecture

Fig 5-1(a) illustrates the topology of the proposed MSCC. The convertor contains 3 identical modules, as shown in Fig 5-1(b). The insulated gate bipolar transistors

(IGBTs) S_1 and S_2 as well as S_3 and S_4 control the current flow to and from the capacitors; capacitor C_1 is connected between the collector end of S_1 and the middle point of the half bridge formed by S_3 and S_4, while capacitor C_2 is connected to the collector end of S_2 and shares the other end with C_1. The collector end of S_3 is connected only to V_{pre} (representing the output end of the previous module). The emitters of S_1 and S_2 are connected to the input source, and the emitters of S_4 are connected to the ground. As previously mentioned, the collector ends of S_1 and S_2 are connected to V_{next} (representing the output of this module).

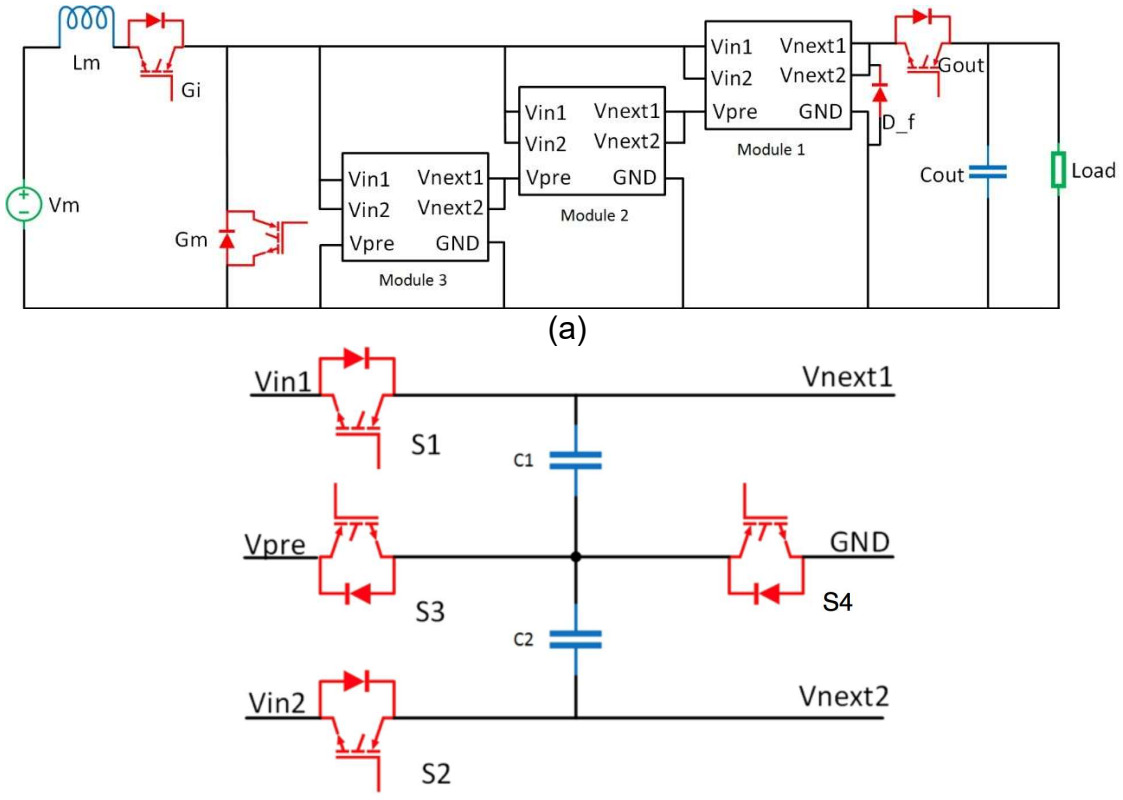


Fig 5-1. Proposed MSCC DC-DC converter
(a) Overall structure;
(b) Module structure.

The module of the proposed converter is similar to that of a traditional MSCC. A traditional MSCC requires an output capacitor that has a larger capacitance as the number of modules increases. In the proposed converter, all the component parameters are identical, so it can be very easy to maintain and replace the faulted module. In addition, with the voltage regulation capability, even with the faulted module remaining in the system, the entire voltage could be tuned to the rated level.

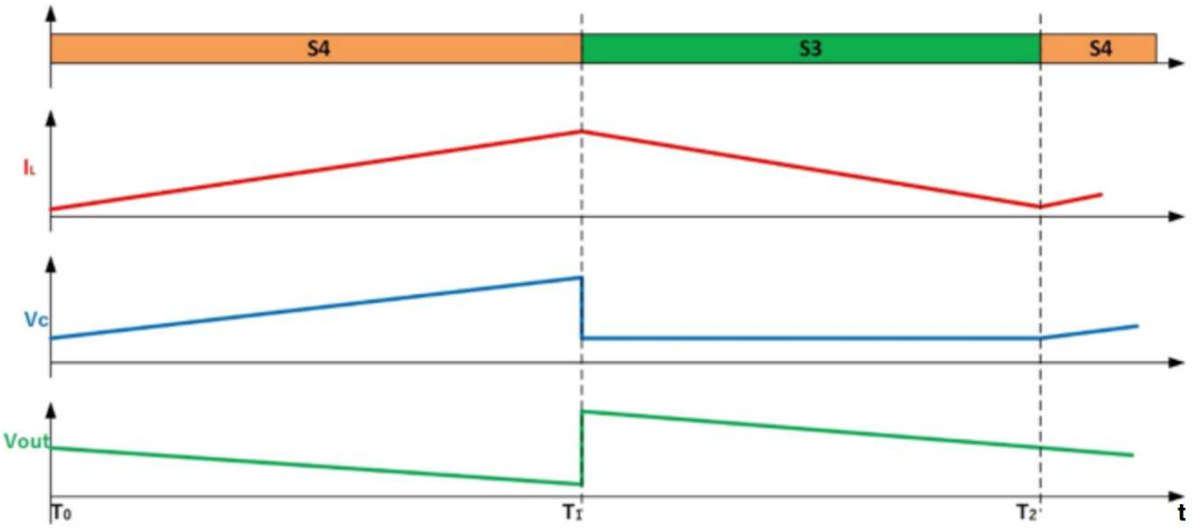


Fig 5-2. The waveform of the proposed converter

5.2 Principles of operation

The normal operation of this converter requires transistor G_{out} turning off and G_i turning on during the entire procedure. In the reverse directional operation, turning on G_{out} is necessary, while when the first module needs to be bypassed for fault isolation, turning off G_i is required. The normal function of the entire system is based on proper control of the transistors in all modules. The control for each module is identical. There are only two stages in the system, as presented in Fig 5-2. In the first stage, S_4 is switched on, and S_3 is switched off. The input voltage is charging the module capacitors along

with the input inductor, and the module detail is shown in Fig 5-3. The second stage (shown in Fig 5-4) is the input voltage charging the input inductor and all the output capacitors starting to transfer energy to the load. In this case, S_3 is switched on, and S_4 is switched off. The energy is transferred from all the submodule capacitors to the load. In the normal operation mode, S_1 and S_2 can be turned off for the entire procedure by using the freewheeling diode to charge the module capacitors. The signals for these transistors are required only when fault isolation or bidirectional operation is used. In this paper, only fault isolation is discussed.

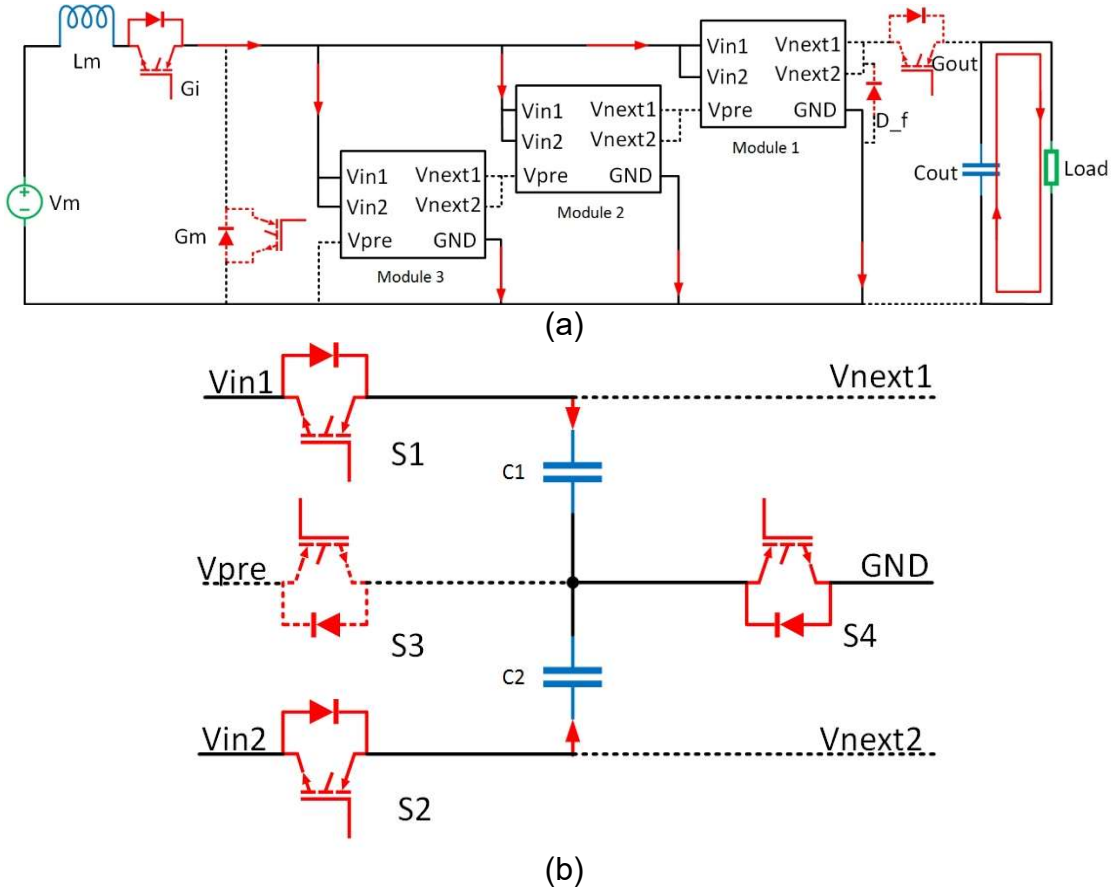


Fig 5-3. Charging mode of the proposed converter
(a) Route of the overall circuit;
(b) Route of the modules.

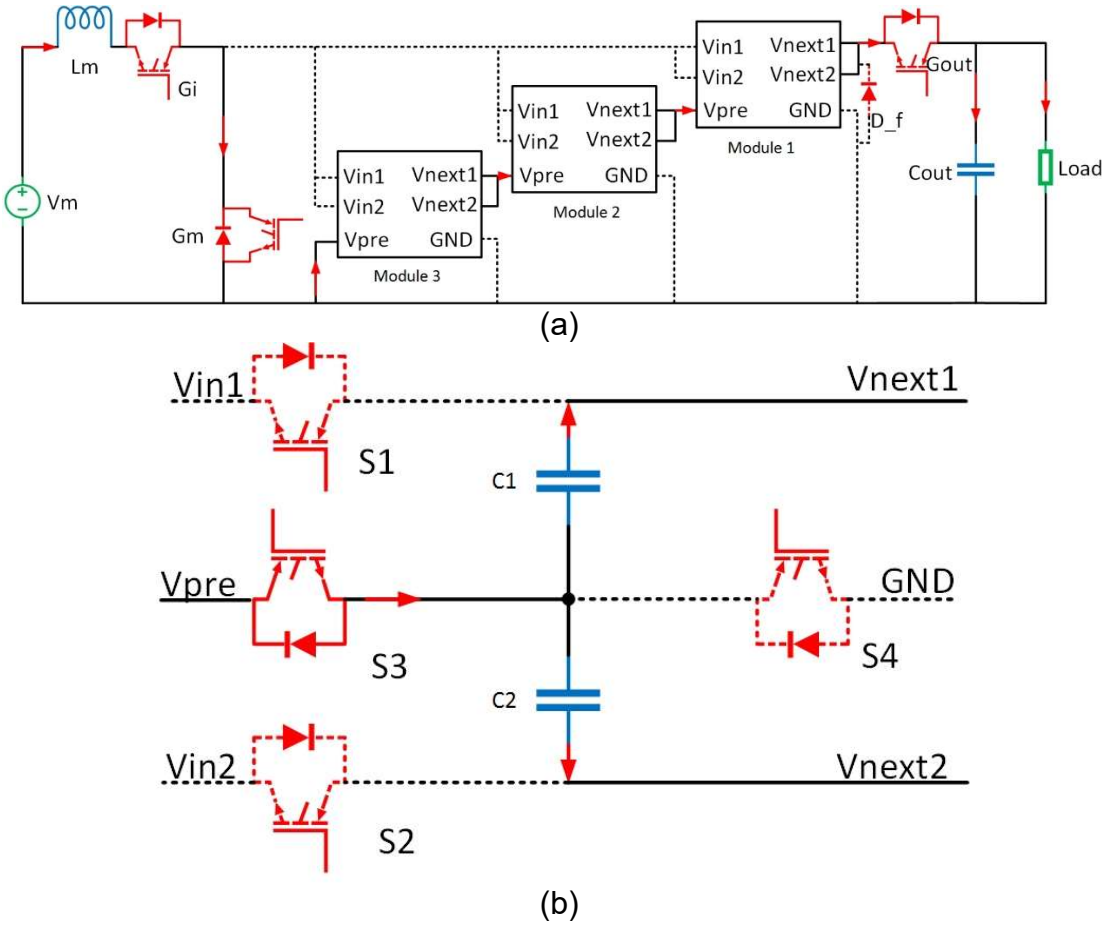


Fig 5-4. Discharging mode of the proposed converter
(a) Route of the overall circuit;
(b) Route of the modules.

5.3 Circuit analysis

To analyse the proposed DC-DC converter circuit, this section uses S-domain system modelling to determine the system stability and studies the voltage ratio range, voltage/current stress and ripple to test the normal operation performance in the steady state. Similar to the previous section, some assumptions are made to simplify the mathematical model and analysis:

- The capacitors in all modules are identical;
- All transistors are ideal; and

- The dead time effect is neglected.

5.3.1 System modelling

In the charging stage, the system differential equations can be obtained by using the volt-time balance principle:

$$\begin{cases} (1-D)\cdot(v_{in}-v_c) = (1-D)\cdot L\cdot\frac{di_L}{dt} \\ (1-D)\cdot i_L = (1-D)\cdot C_n\cdot\frac{dv_c}{dt} \end{cases} \quad 5\text{-}1$$

In the discharging stage:

$$\begin{cases} D\cdot v_{In} = D\cdot L\cdot\frac{di_L}{dt} \\ D\cdot i_s = \frac{D\cdot N\cdot v_c}{R} = D\cdot C_n\cdot\frac{dv_c}{dt} \end{cases} \quad 5\text{-}2$$

Combining the two stages:

$$\begin{bmatrix} \frac{di_L}{dt} \\ \frac{dv_C}{dt} \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1-D}{L} \\ \frac{1-D}{C} & \frac{ND}{RC} \end{bmatrix} \begin{bmatrix} i_L \\ v_c \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} v_{IN} \quad 5\text{-}3$$

$$\begin{cases} A = \begin{bmatrix} 0 & -\frac{1-D}{L} \\ \frac{1-D}{C} & \frac{N\cdot D}{R\cdot C} \end{bmatrix} \\ B = \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} \end{cases} \quad 5\text{-}4$$

Using the Laplace transform:

$$\begin{bmatrix} i_L(s) \\ v_c(s) \end{bmatrix} = (I\cdot s - A)^{-1}\cdot B = det(I\cdot s - A)\cdot \begin{bmatrix} \frac{1}{L}\cdot(s-\frac{N\cdot D}{R\cdot C}) \\ \frac{1-D}{CL} \end{bmatrix} \quad 5\text{-}5$$

The output voltage small-signal transfer function of the proposed modularized switched capacitor converter can be expressed as:

$$G_{vd}(s) = \frac{b}{s^2+a_1 s+a_2} \quad 5\text{-}6$$

where:

$$\begin{cases} a_1 = -\frac{ND}{RC} \\ a_2 = \frac{(1-D)^2}{CL} \\ b = \frac{1-D}{CL} \end{cases} \quad 5\text{-}7$$

The bode diagrams of the proposed converter are presented in Fig 5-5. The system slop inclination is approximately -20 dB/dec. The magnitude analysis of the converter indicates an unstable state of the converter when encountering a low frequency input noise. In contrast, the system has high stability against high frequency input noise. The phase angle is -180 degrees, indicating the stability of the converter. Based on the above analysis, a closed loop is necessary to address any low frequency input disturbance. The control loop for this topology can be easily implemented, as shown in Fig 5-6.

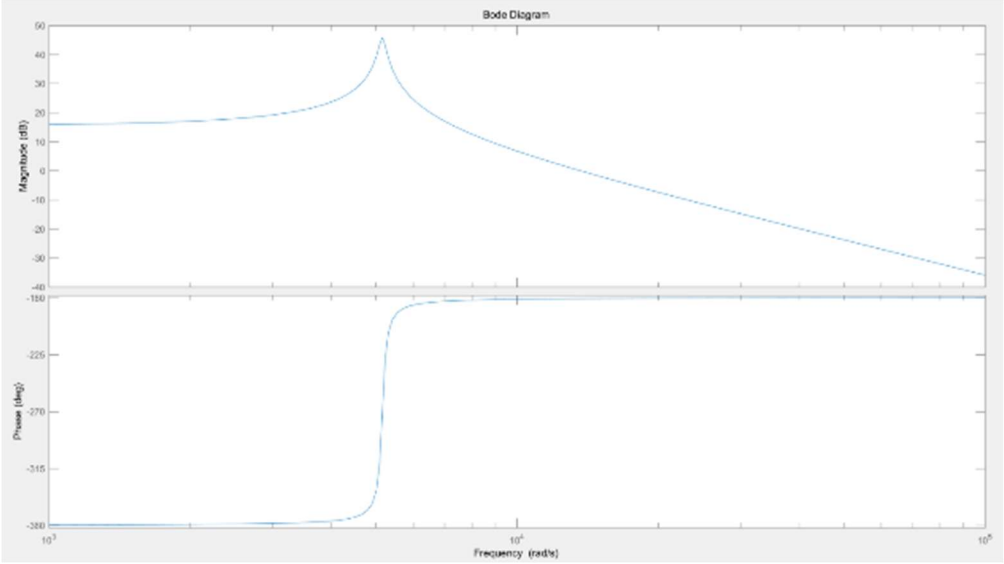


Fig 5-5. Bode analysis of the open-loop of the proposed converter

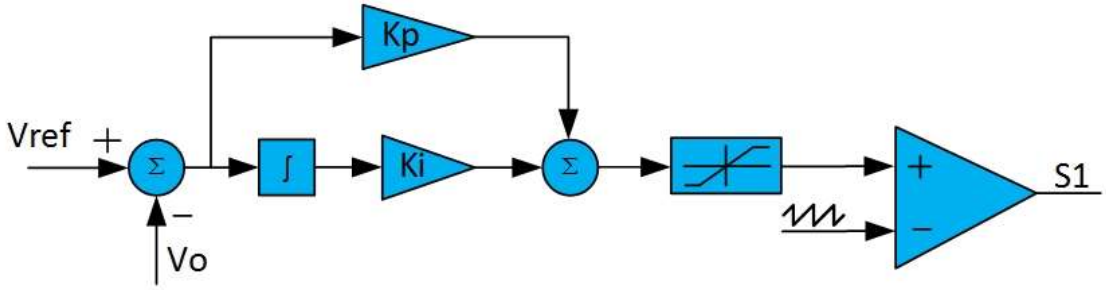


Fig 5-6. PI controller of the proposed converter

5.3.2 Voltage ratio range

The capacitor voltage for each module can be express as:

$$V_c = \frac{V_{in}}{1-D} \tag{5-8}$$

Because the load is connected in series with all the output capacitors in the submodule at the second stage, the entire output voltage is:

$$V_{out} = \frac{N \cdot V_{in}}{1-D} \tag{5-9}$$

The relationship between the output voltage gains of the proposed converter and the module number is presented in Fig 5-7.

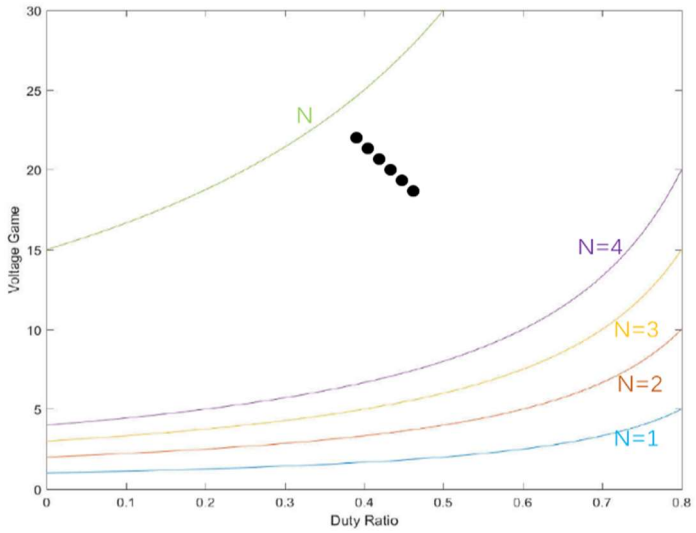


Fig 5-7. Voltage gains of the proposed converter

5.3.3 Current stress

The inductor is in series with the input voltage source, which means that the inductor's current stress is larger than the maximum current output of the DC voltage source. As with the switches, *N* modules would divide the input current into *1/N*. Moreover, S_2 and

S_3 are switched on at the same time. Thus, for L, S_1, S_2 and S_4, the current stresses are:

$$\begin{cases} I_{stress,L} = I_{in} = I_l \\ I_{stress,S1} = \frac{DI_l}{2N} \\ I_{stress,S2} = \frac{DI_l}{2N} \\ I_{stress,S4} = \frac{DI_l}{N} \end{cases} \quad 5\text{-}10$$

For S_3, the switch carries the current to charge the output capacitor for the entire system. The maximum current flow through S_3 is:

$$I_{stress,S3} = \ （1 - D）I_l \quad 5\text{-}11$$

5.3.4 Voltage stress

For each module, the voltage stress for S_3 is identical to the module capacitors:

$$V_{stress,S3} = V_c \quad 5\text{-}12$$

The rated voltages for S_1 and S_2 are the same for its symmetrical connection. They block the positive end of the current module capacitors; thus, the voltage stresses for S_1 and S_2 are:

$$V_{stress,S1} = V_{stress,S2} = N \cdot V_c \quad 5\text{-}13$$

The voltage stress for S_4 can be deduced from the following analysis: due to the series connection of the output module capacitors, in the N^{th} module, S_4 needs to block the voltage from all the output former module capacitors in the series connection, so the voltage stress for S_4 is:

$$V_{stress,S4} = (N - 1) \cdot V_c \quad 5\text{-}14$$

The common maximum stress voltages for commercial IGBTs are 600 V, 1200 V and 6.5 kV. In this project, a 600 V stress voltage level is sufficient.

5.3.5 Current ripple

All the submodule structures are identical, and so are all the capacitor parameters. One module is analysed to represent the entire system. As the input voltage regulator, the current ripple should be written as:

$$V_{in} = L\frac{dI_l}{dt} \quad \text{5-15}$$

where V_{in} is the input source voltage and I_l is the input current. To maintain the continuous operation mode and decrease the current ripple, the input current ripple should be limited to a certain level. To fulfil all the criteria, the inductance should obey:

$$L \geq \frac{V_{in} \cdot dt}{dI_l} \quad \text{5-16}$$

when the system switching frequency is limited to less than 20 kHz and the output voltage is set to 20 V. If the rated system power is set to 160 W, the inductance for continuous operation can be calculated as:

$$L \geq 15.625\ uH \quad \text{5-17}$$

For this project, a 47 *u*H inductor is selected to minimize the oscillation in the circuit. Small inductance would cause the module capacitor voltage to oscillate for a half cycle in the discharging mode. When the duty ratio is set to 0.5, the current ripple can be derived as:

$$\Delta I_l = 1.5625\ A \quad \text{5-18}$$

5.3.6 Voltage ripple

In each module, the voltage ripple is determined by the capacitance of the module capacitor, input current and switching frequency:

$$\Delta V_c = \int_0^T \frac{I_c}{C} dt \qquad 5\text{-}19$$

The capacitance is then calculated as:

$$\mathrm{C} = \frac{k \cdot V_c \cdot f_s}{I \cdot D} \qquad 5\text{-}20$$

where *K* is the error ratio of the output voltage, f_s is the switching frequency and *D* is the duty ratio of S_1, S_2 and S_4.

If there are 4 modules in the system, a 5% voltage ripple is allowed, and the rest of the system setup is the same as mentioned before, then the minimum capacitance is:

$$C \geq 25uF \qquad 5\text{-}21$$

For this project, a 47 *uF* capacitor is selected, and the current ripple can be derived as:

$$\Delta V_c = 1.064\ \mathrm{V} \qquad 5\text{-}22$$

5.4 Fault tolerance operation

Fault tolerance operation has become a crucial aspect for PWM DC-DC power converter, especially for modern industrial applications, such as electric vehicles, HVDC power transmission, island DC power networks and even military applications. Ensuring normal function is important to the aforementioned system in terms of economic damage and safety issues. Two categories of components have higher risk of damage due to electrical and thermal stress than other components:

semiconductors and capacitors. In this module, three fault scenarios are discussed: open circuit faults (OCFs) of the IGBTs and capacitors.

5.4.1 Capacitor open circuit fault

The capacitor in each module is used to deliver energy from the source to the load in a series connection. When one module has a capacitor OCF without fault isolation, the entire system would shut down gradually. The M^{th} module is taken as an example to demonstrate the fault isolation principle.

When C_{mn} is detected as a fault element (n represents the capacitor), the Sn switch from the current module continues to turn off for the entire fault operation stage, thus isolating the faulted capacitor from the capacitor charging stage. In contrast, in the capacitor discharging stage, the Sn switch from the next module is switched off to eliminate any disturbances from the faulted capacitor to the converter. The current path is indicated as shown in Fig 5-8. However, this would increase the current stress of the other capacitor's corresponding transistor.

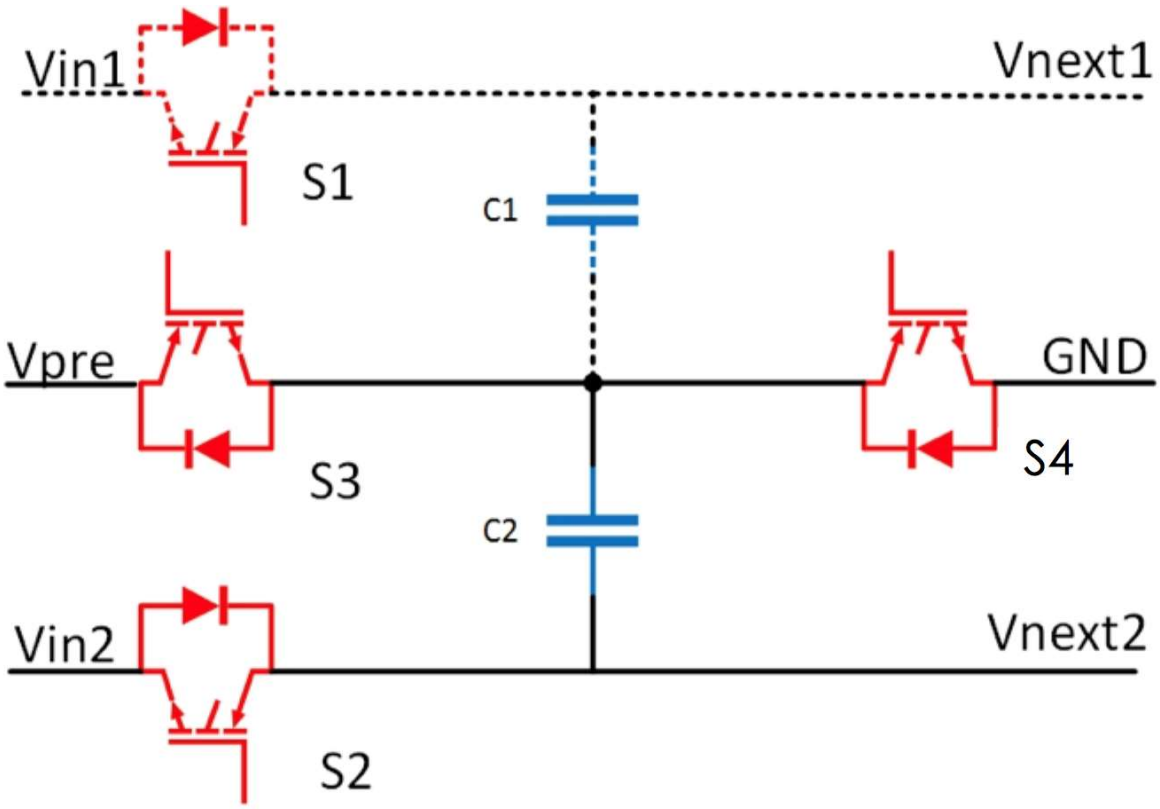


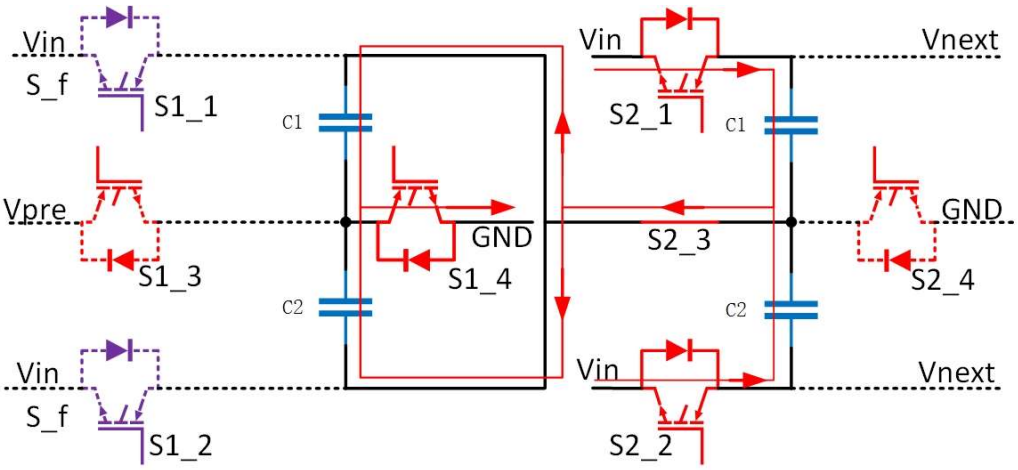
Fig 5-8. Fault isolation in the module for signal transistor or capacitor fault

In this situation, the output voltage for the system would be the same as that in the normal operation mode.

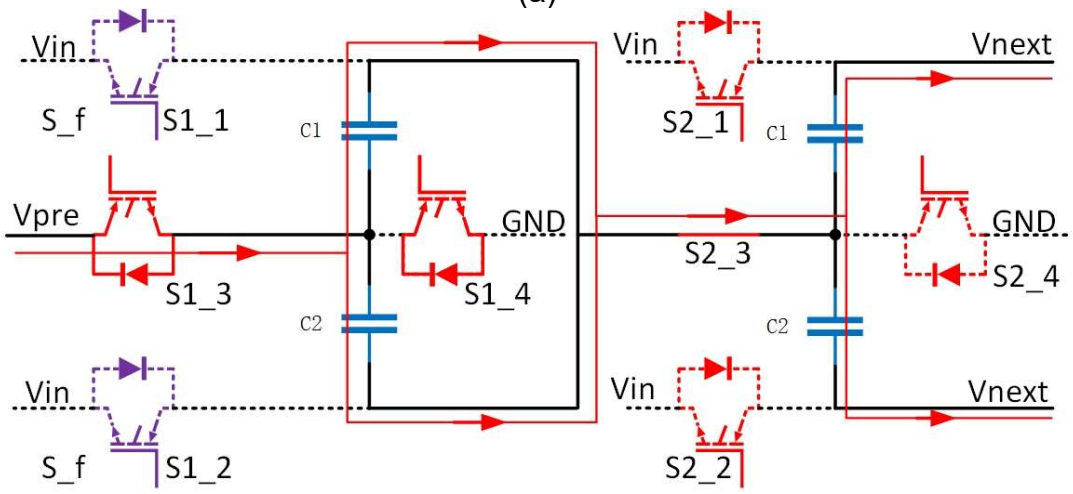
5.4.2 S_1 and S_2 open circuit fault (OCF)

The S_1 and S_2 OCF is very convenient to address. For each individual with an OCF, the consequences would be the same as that of the corresponding capacitor OCF. If S_1 and S_2 have an OCF at the same time, the entire faulty module needs to be bypassed. The circuit would react in the following state (Fig 5-9). In these two diagrams, the faulted transistors S_{1_1} and S_{1_2} are marked as $S_{\_f}$. To maintain the output capacitor chain, the capacitor in the next module is charged alone with the ones in the faulted module in series. To differentiate between the switches in different modules, sub-labels

are introduced in the following. As presented in Fig 5-9(a), S_{2_1}, S_{2_2}, S_{2_3} and S_{1_4} turn on, and the rest are off. In addition, as shown in Fig 5-9(b), S_{2_3} and S_{1_3} are turned on, and the rest are off. However, the connection would decrease the output voltage level, and compensation would occur by tuning the duty ratio. These steps would increase the voltage stress on the capacitors in the remaining modules. When this type of fault occurs in the last module, there is no next module to help bypass the fault. As shown in Fig 5-1, a bypass diode (d_f) is introduced between the ground and the output end of the last module to bypass the fault, which would not influence normal operation.



(a)



(b)

Fig 5-9. S_1 and S_2 Fault isolation mode
(a)Charging mode;
(b) Discharging mode.

5.4.3 S_3 and S_4 OCF

Addressing S_3 and S_4 OCF individually or together is identical. Both faulty switches would be treated as open circuited in both scenarios. S_1 and S_2 switch from the previous module to charge the corresponding capacitors; therefore, these switches would also be used to discharge the capacitors. In this way, the entire faulty module is bypassed, as shown in Fig 5-10. The duty ratio is modified to minimize the effect.

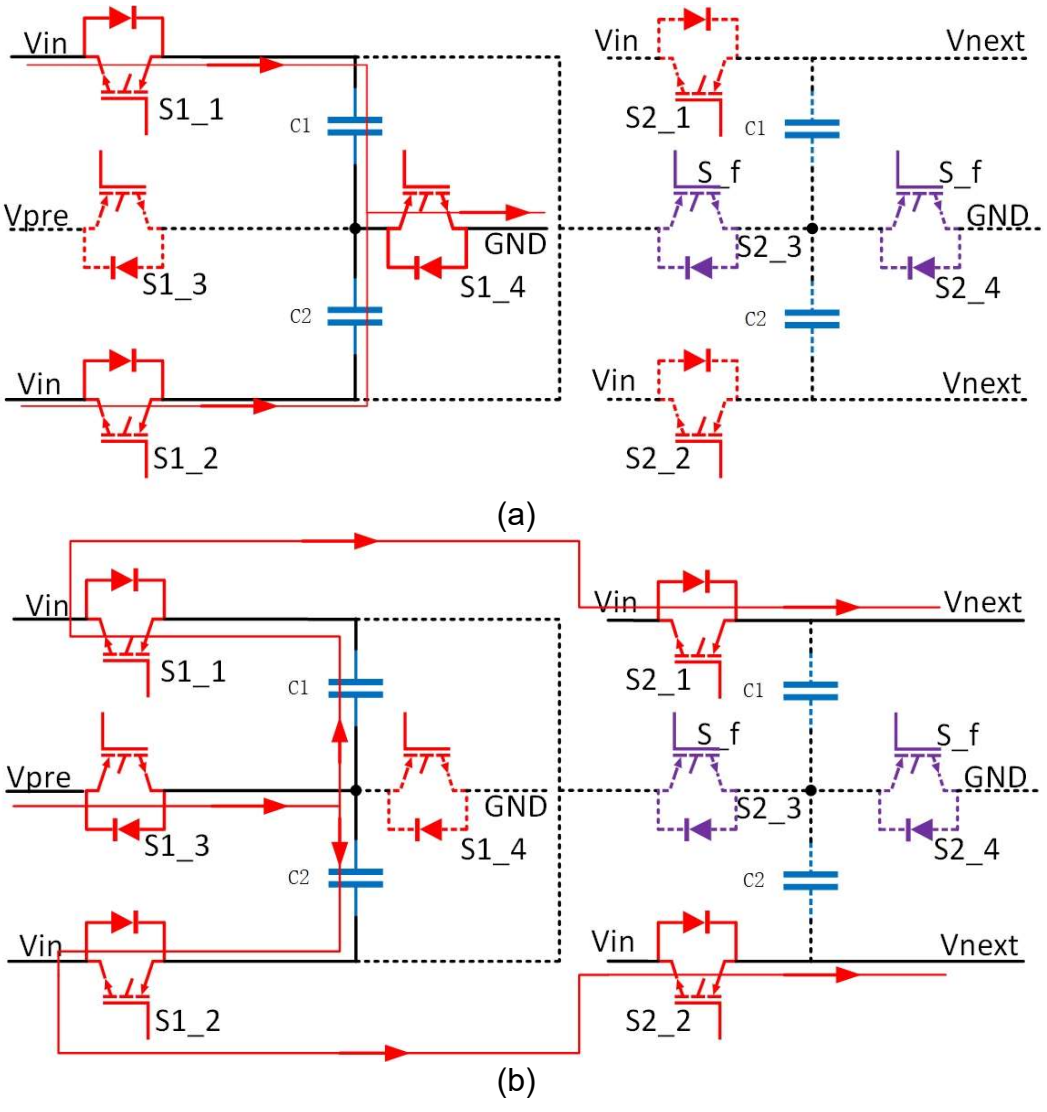


Fig 5-10. S_3 and S_4 Fault isolation mode
(a) Charging mode;
(b) Discharging mode.

5.5 Simulation and experimental results

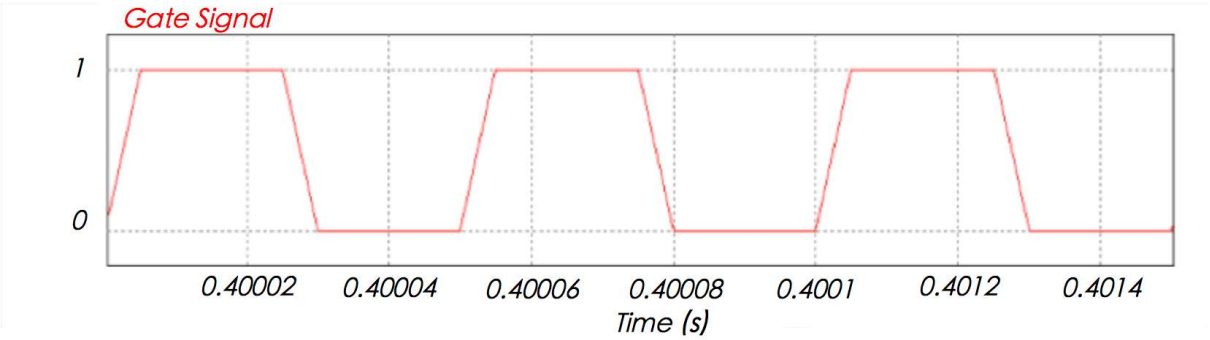
The proposed converter was simulated with a large input voltage for a high power system. However, due to lab limitations, the practical experiment was carried out for a low power system. The detailed expression is presented in the following section.

5.5.1 Simulation results

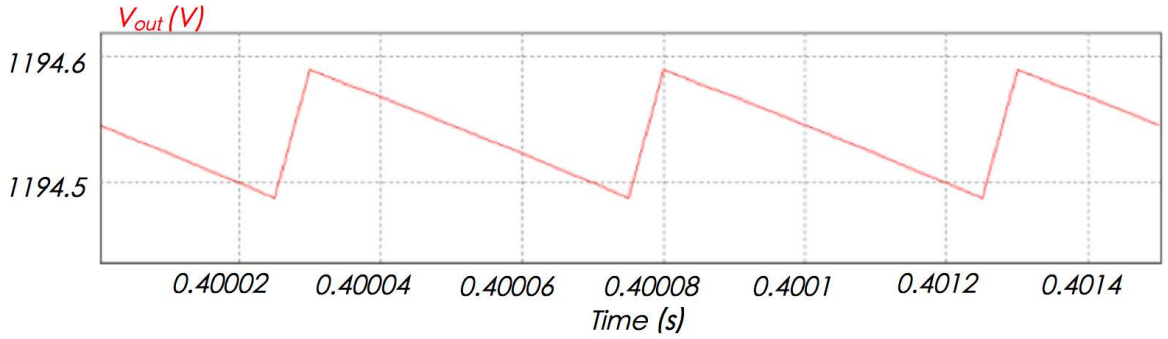
A detailed simulation was performed for the proposed DC-DC converter. The simulation was conducted using PSIM software, and the system parameters are presented in Table 5-1. Only the closed loop is carried out in the simulations in this paper.

Table 5-1. Specifications of the simulated proposed converter

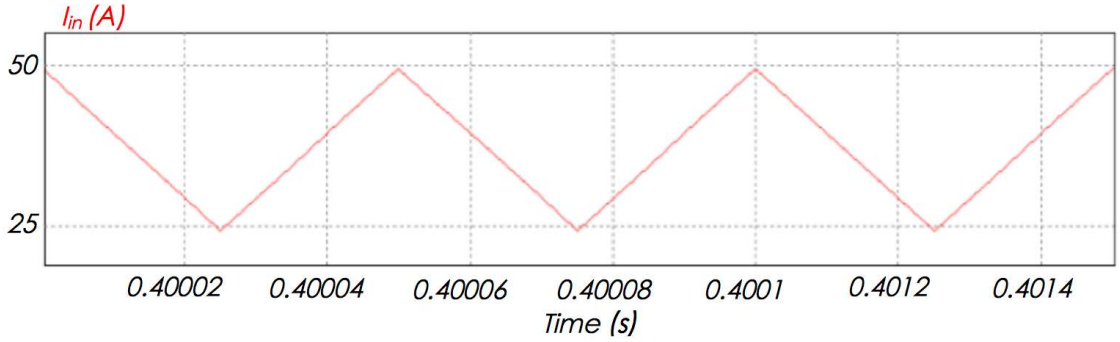
Parameter	*Value*
Module capacitor (μF)	*47*
Switching Frequency (kHz)	*20*
Input inductor (μH)	*50*
Input voltage (V)	*200*
Output capacitance (each) (μF)	*470*
Load resistance (Ω)	*200*



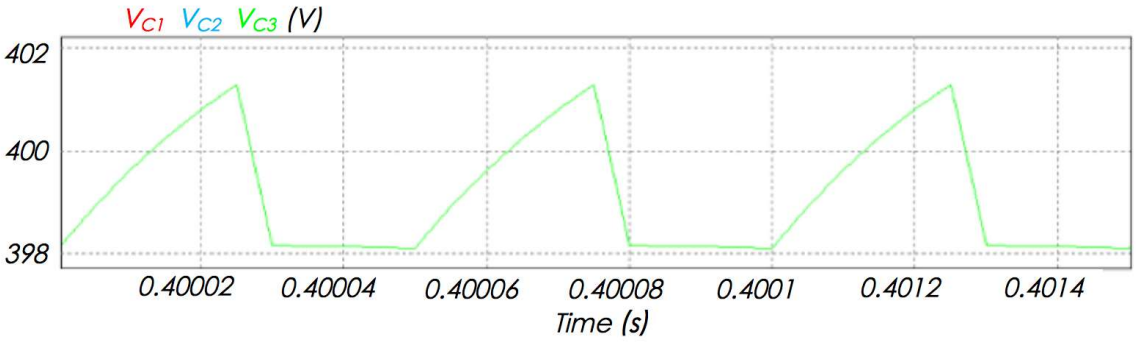
(a)



(b)



(c)

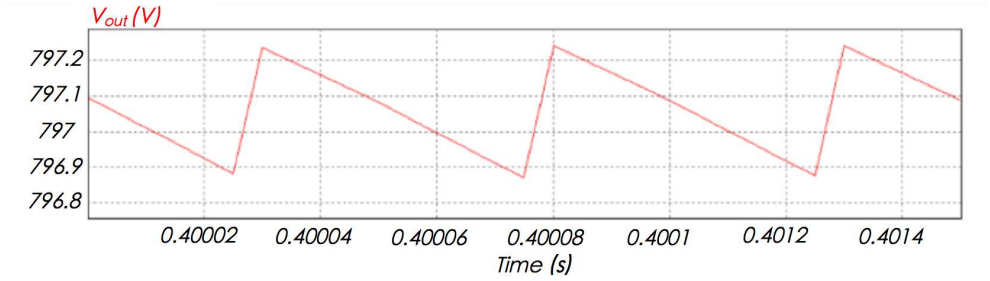


(d)

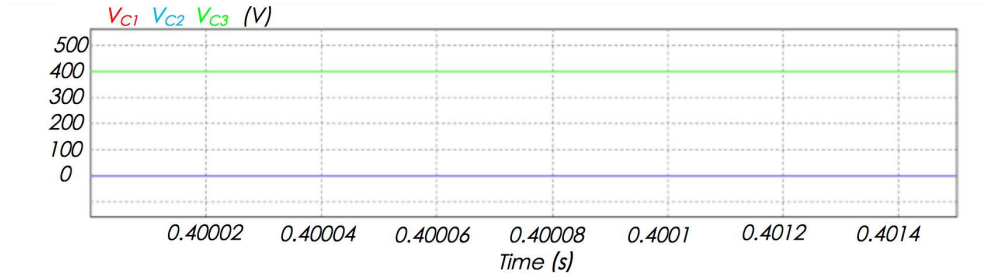
Fig 5-11. Simulation results of the proposed converter
(a) S_1 switching signal;
(b) Input current waveform;
(c) Output voltage waveform;
(d) Capacitor voltage waveform.

Fig 5-12 and Fig 5-13 demonstrate the S_1 and S_2 module capacitor OCF and S_3 and S_4 OCF, respectively, in open circuit tests. The former situations require the entire module to be bypassed. Therefore, one of the module capacitor voltages drops to zero, and the others are intact. Thus, the output result is composed of two-thirds of the original output. In the scenario shown in Fig 5-13, the voltages of the capacitors

participating in fault isolation drop to half of those in the normal function mode because of the series connection in the fault isolation procedure. The closed-loop results are identical to the open circuit operation in the steady state.

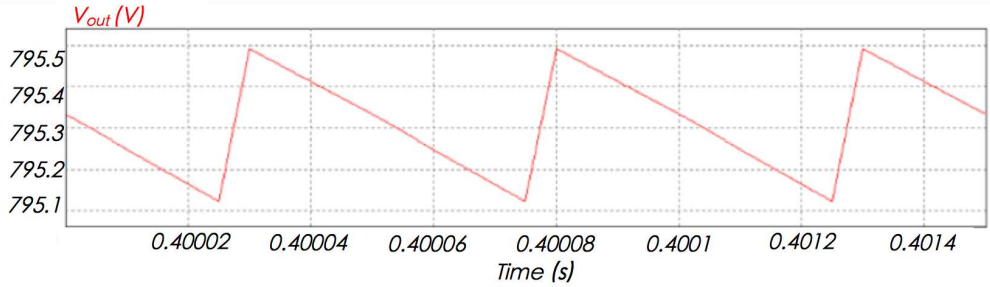


(a)

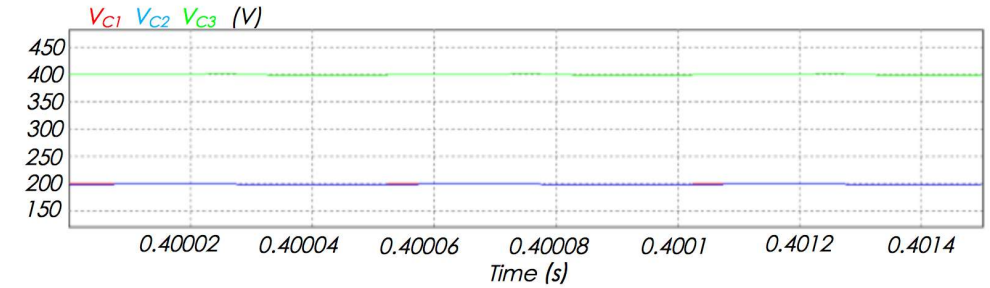


(b)

Fig 5-12. Simulation results of the proposed converter (S_1 and S_2 OCF)
(a) Output voltage;
(b) Module capacitor voltages.



(a)

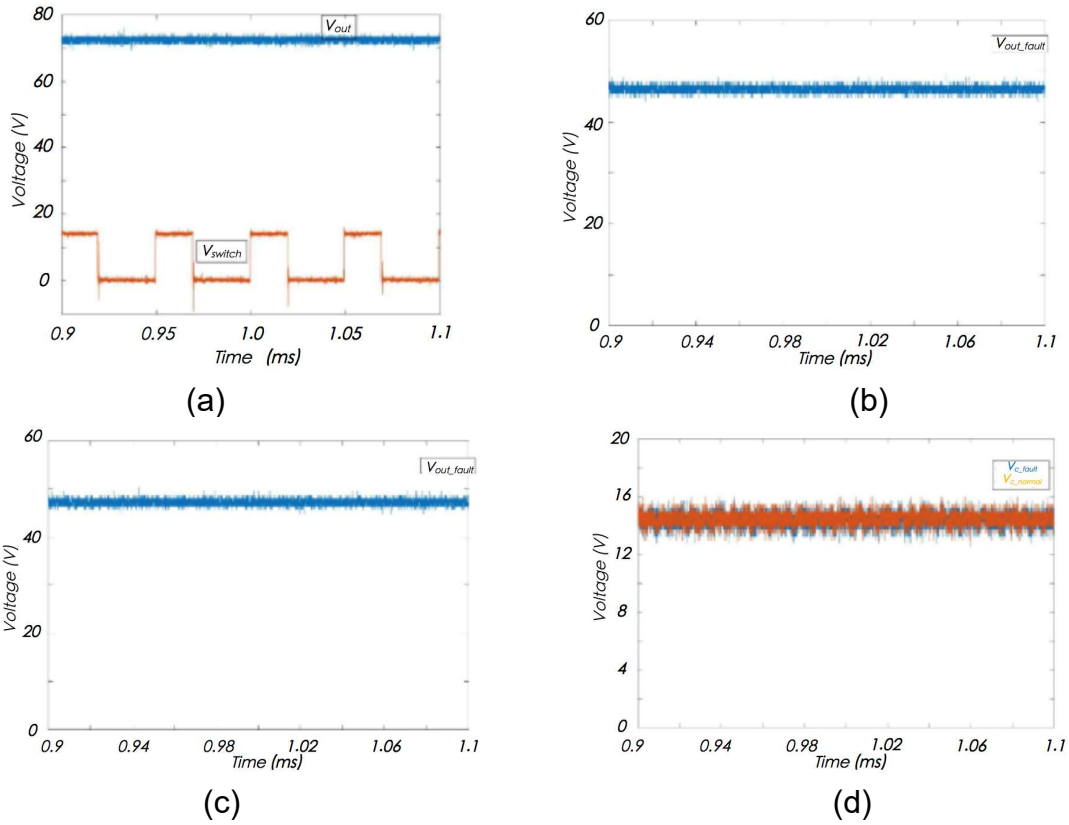


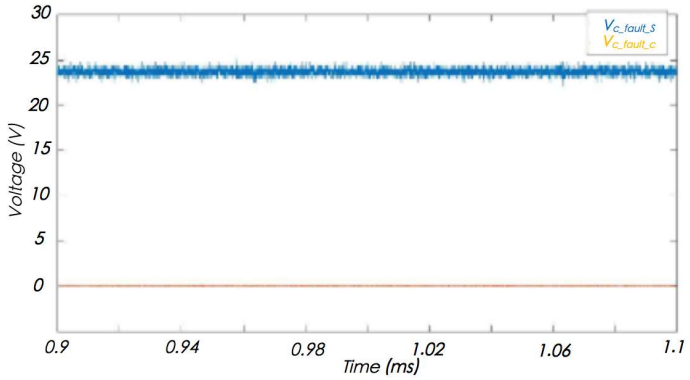
(b)

Fig 5-13. Simulation results of the proposed converter (S_3 and S_4 OCF)
(a) Output voltage;
(b) Module capacitor voltages.

5.5.2 Experimental results

An experimental platform was established for normal and fault operations. Due to lab limitations, a low voltage and power system was tested. Table 5-2 includes the specifications of the experimental parameters. The following diagrams indicate the normal and fault operations. The faulty scenarios were implemented by manual toggle switches, which simulate the OCF of the transistors and capacitors. All the experiments utilized open circuit tests to prove the concept.





(e)

Fig 5-14. Experimental results
(a). Normal operation output voltage;
(b) Output voltage for S_1 and S_2 fault operation;
(c) Output voltage for S_3, S_4, and capacitor fault operation;
(d) Fault module and normal capacitor voltages for S_1 and S_2 OCF;
(e) Fault module capacitor voltages for S_3, S_4, and capacitor OCF.

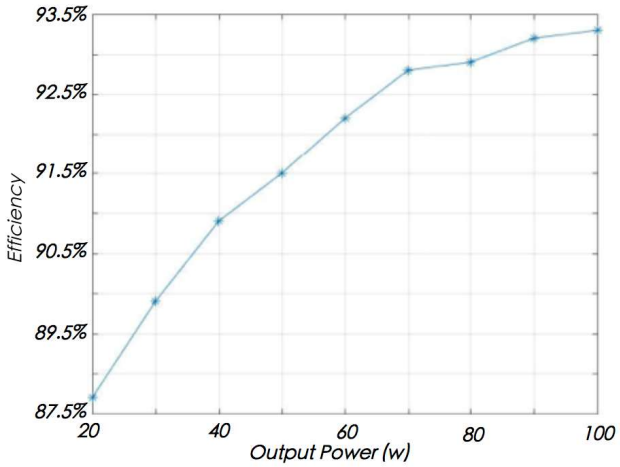


Fig 5-15. Efficiency of the proposed converter

Fig 5-14 presents the experimental results. Fig 5-14(a) shows the normal operation output voltage. According to (8), the output voltage should be 75 V, and the experimental result shows that the actual output voltage is 72.12 V. The difference is caused by the diode voltage drop and losses. The output voltages for the fault operations are presented in Fig 5-14(b) and (c). From the fault analysis and simulation, one N^{th} of the output voltage would be compromised due to a fault bypass. The practical results show close output voltages: 46.46 and 47.17 V. These values are

consistent with the analytical and simulation results. Fig 5-14(d) and (e) show the faulty module capacitor voltages from two faulty scenarios, which also support the analytical and simulation results. Fig 5-15 shows the efficiency of the system.

Table 5-2. Specifications of the experiment of the proposed converter

Parameters	*Value*
Module capacitor (μF)	*47*
Switching frequency (kHz)	*20*
Input inductor (μH)	*200*
Input voltage (V)	*15*
Output capacitance (each) (μF)	*47*
Load resistance (Ω)	*100*
Duty ratio	*0.4*

5.6 Conclusion

This paper presented and analysed a modularized switch capacitor DC-DC converter that has high extensibility for high voltage gain output and fault tolerance under OCFs in capacitors and transistors. Due to the ability to bypass modules, the voltage can be regulated with a minimum duty ratio change. The circuit architecture, operation principle, voltage/current stress and fault tolerance operation are explained in detailed. The voltage regulation method is also presented. Finally, the simulations and experimental results verified the effectiveness of the proposed converter and output with satisfactory fault tolerant operation and energy efficiency.

Chapter 6 Conclusion and future work

In this chapter, the conclusions of the entire PhD project are given, and areas of future study are proposed.

6.1 Conclusion

This thesis studies high-step-up DC-DC converter topology, which is built on the application background of a renewable energy system, especially PV systems, fuel cell systems and electric vehicles. Based on isolated and non-isolated categories, an asymmetric flyback-forward DC-DC converter and a switched-capacitor DC-DC converter with voltage regulation and fault tolerance capability are proposed to satisfy the requirements of recent developments of renewable energy systems.

The first chapter of the thesis introduces the importance of high-step-up DC-DC converters and their fault tolerance capability in industrial applications. The second chapter reviews DC-DC topologies for high-step-up boosting, including several boosting techniques. The third chapter explains the DC-DC converter system in detail, introduces the system architecture along with the common control strategies, and presents the steady state performance to measure system performance. Additionally, small signal mathematic modelling is used to determine the system performance. Furthermore, an MPPT algorithm is mentioned for the PV application for the topology introduced in the following chapter. Finally, the soft-switching technique is explained in

advance for the proposed DC-DC converter. The fourth chapter introduces a new flyback-forward DC-DC converter. Its new topology overcomes the limitation of the flyback converter, i.e., the energy storage limitation in the air gap of the transformer. With this new topology, the transformer can alternatively work in the flyback mode and forward mode, so that the transformer becomes magnetic-flux-saturated less easily. With this feature, the heat dissipated from the transformer dramatically decreases when the DC-DC converter is working under a heavy load. The fourth chapter discusses an isolated topology, and the fifth chapter discusses a new non-isolated DC-DC converter. The switched-capacitor DC-DC converter overcomes the limitation of the traditional switched capacitor, which is the lack of ability to regulate the output voltage, by introducing an inductor into the switched-capacitor system and a bypassing mechanism to minimize the alteration of the duty cycle. The proposed converter is also packed with transistors and a capacitor open circuit fault (OCF). With certain transistor and capacitor OCFs, this new topology can minimize the system performance compensation.

6.2 Future work

Due to the limitations of research skill and time, this topic still has numerous problems worth exploring. The assessment for the cost of the proposed DC-DC converter has yet to be performed. The soft-switching technique used in the switched-capacitor converter can be covered in the future. In addition, more combinations for the high-

step-up technique and utilization of the topology to increase the system power density will be discovered continuously.

1. In a PV system, the MPPT algorithm can be improved to achieve better performance. The practical experiment can be conducted with a PV panel in the future.

2. More isolated high-step-up DC-DC converters for PV systems can be developed in the future.

3. Future research can study the impact of different drive circuits in the electric vehicle system on the proposed converter.

List of References

[1] "IEA Report." [Online]. Available: http://www.iea.org/statistics/statisticssearch/report/?country=WORLD&product=electricityandheat&year=2013. [Accessed: 05-May-2017].

[2] F. Blaabjerg, Z. Chen, and S. B. Kjaer, "Power electronics as efficient interface in dispersed power generation systems," IEEE Trans. Power Electron., vol. 19, no. 5, pp. 1184–1194, 2004.

[3] W. Li and X. He, "Review of Nonisolated High-Step-Up DC/DC Converters in Photovoltaic Grid-Connected Applications," IEEE Trans. Ind. Electron., vol. 58, no. 4, pp. 1239–1250, Apr. 2011.

[4] W. Li, W. Li, X. He, D. Xu, and B. Wu, "General Derivation Law of Nonisolated High-Step-Up Interleaved Converters With Built-In Transformer," IEEE Trans. Ind. Electron., vol. 59, no. 3, pp. 1650–1661, 2012.

[5] Y. J. A. Alcazar, D. D. S. Oliveira, F. L. Tofoli, and R. P. Torrico-Bascopé, "DC–DC Nonisolated Boost Converter Based on the Three-State Switching Cell and Voltage Multiplier Cells," IEEE Trans. Ind. Electron., vol. 60, no. 10, pp. 4438–4449, 2013.

[6] R. J. Wai and R. Y. Duan, "High-efficiency power conversion for low power fuel cell generation system," IEEE Trans. Power Electron., vol. 20, no. 4, pp. 847–856, 2005.

[7] O. Garcia et al., "Boost-Based MPPT Converter Topology Trade-Off for Space Applications," vol. 661, 2008.

[8] L. J. Shu, T. J. Liang, L. S. Yang, and R. L. Lin, "Transformerless high step-up DC-DC converter using cascode technique," in Power Electronics Conference, 2010, pp. 63–67.

[9] C. M. Lai, C. T. Pan, and M. C. Cheng, "High-Efficiency Modular High Step-Up Interleaved Boost Converter for DC-Microgrid Applications," IEEE Trans. Ind. Appl., vol. 48, no. 1, pp. 161–171, 2012.

[10] K. B. Park, C. E. Kim, G. W. Moon, and M. J. Youn, "Non-isolated high step-up converter based on boost integrated half-bridge converter," in Telecommunications Energy Conference, 2009. Intelec 2009. International, 2009, pp. 1–6.

[11] B. Axelrod, Y. Berkovich, and A. Ioinovici, "Switched Coupled-Inductor Cell for DC-DC Converters with Very Large Conversion Ratio," Iet Power Electron., vol. 4, no. 3, pp. 309–315, 2006.

[12] Z. Amjadi and S. S. Williamson, "Digital Control of a Bidirectional DC/DC Switched Capacitor Converter for Hybrid Electric Vehicle Energy Storage System Applications," IEEE Trans. Smart Grid, vol. 5, no. 1, pp. 158–166, 2014.

[13] Z. Zhang, Z. Ouyang, O. C. Thomsen, and M. A. E. Andersen, "Analysis and Design of a Bidirectional Isolated DC–DC Converter for Fuel Cells and Supercapacitors Hybrid System," IEEE Trans. Power Electron., vol. 27, no. 2, pp. 848–859, 2012.

[14] N. M. L. Tan, T. Abe, and H. Akagi, "Design and Performance of a Bidirectional Isolated DC–DC Converter for a Battery Energy Storage System," IEEE Trans. Power Electron., vol. 27, no. 3, pp. 1237–1248, 2012.

[15] A. S. Samosir and A. H. M. Yatim, "Implementation of Dynamic Evolution Control of Bidirectional DC–DC Converter for Interfacing Ultracapacitor Energy

Storage to Fuel-Cell System," IEEE Trans. Ind. Electron., vol. 57, no. 10, pp. 3468–3473, 2010.
[16] R. Barrero, J. Van Mierlo, and X. Tackoen, "Energy savings in public transport," Veh. Technol. Mag. IEEE, vol. 3, no. 3, pp. 26–36, 2008.
[17] A. Khaligh and Z. Li, "Battery, Ultracapacitor, Fuel Cell, and Hybrid Energy Storage Systems for Electric, Hybrid Electric, Fuel Cell, and Plug-In Hybrid Electric Vehicles: State of the Art," IEEE Trans. Veh. Technol., vol. 59, no. 6, pp. 2806–2814, 2010.
[18] T. G. Wilson, "The evolution of power electronics," IEEE Trans. Power Electron., vol. 15, no. 3, pp. 439–446, May 2000.
[19] M. Kazimierczuk, "Pulse-width modulated DC-DC power converters," John Wiley Sons, 2015.
[20] R. W. Erickson and D. Maksimović, "Fundamentals of Power Electronics," Green Energy Technol., vol. 35, no. 1, p. 1.1–1.9, 2001.
[21] M. M. Jovanovic, "A technique for reducing rectifier reverse-recovery-related losses in high-power boost converters," IEEE Trans. Power Electron., vol. 13, no. 5, pp. 932–941, Sep. 1998.
[22] H. Chung, S. Y. R. Hui, and K. K. Tse, "Reduction of power converter EMI emission using soft-switching technique," IEEE Trans. Electromagn. Compat., vol. 40, no. 3, pp. 282–287, Aug. 1998.
[23] B. W. Williams, "DC-to-DC Converters With Continuous Input and Output Power," IEEE Trans. Power Electron., vol. 28, no. 5, pp. 2307–2316, May 2013.
[24] R. D. Middlebrook, "Transformerless DC-to-DC converters with large conversion ratios," IEEE Trans. Power Electron., vol. 3, no. 4, pp. 484–488, Oct. 1988.
[25] F. L. Tofoli, D. d C. Pereira, W. J. de Paula, and D. d S. O. Júnior, "Survey on non-isolated high-voltage step-up dc-dc topologies based on the boost converter," IET Power Electron., vol. 8, no. 10, pp. 2044–2057, 2015.
[26] Y. Du, X. Zhou, S. Bai, S. Lukic, and A. Huang, "Review of non-isolated bi-directional DC-DC converters for plug-in hybrid electric vehicle charge station application at municipal parking decks," in 2010 Twenty-Fifth Annual IEEE Applied Power Electronics Conference and Exposition (APEC), 2010, pp. 1145–1151.
[27] N. Jabbour and C. Mademlis, "Improved Control Strategy of a Supercapacitor-Based Energy Recovery System for Elevator Applications," IEEE Trans. Power Electron., vol. 31, no. 12, pp. 8398–8408, Dec. 2016.
[28] F. H. Khan and L. M. Tolbert, "Bi-directional power management and fault tolerant feature in a 5-kW multilevel dc-dc converter with modular architecture," IET Power Electron., vol. 2, no. 5, pp. 595–604, Sep. 2009.
[29] F. H. Khan and L. M. Tolbert, "Multiple-Load-Source Integration in a Multilevel Modular Capacitor-Clamped DC-DC Converter Featuring Fault Tolerant Capability," IEEE Trans. Power Electron., vol. 24, no. 1, pp. 14–24, Jan. 2009.
[30] F. H. Khan and L. M. Tolbert, "A Multilevel Modular Capacitor-Clamped DC-DC Converter," IEEE Trans. Ind. Appl., vol. 43, no. 6, pp. 1628–1638, Nov. 2007.
[31] B.-M. Han, "Grid-tied power converter for battery energy storage composed of 2-stage DC-DC converter," in 2013 IEEE Power Energy Society General Meeting, 2013, pp. 1–5.

[32] Y. M. Chen, A. Q. Huang, and X. Yu, “A High Step-Up Three-Port DC-DC Converter for Stand-Alone PV/Battery Power Systems,” IEEE Trans. Power Electron., vol. 28, no. 11, pp. 5049–5062, Nov. 2013.
[33] W. Qian, H. Cha, F. Z. Peng, and L. M. Tolbert, “55-kW Variable 3X DC-DC Converter for Plug-in Hybrid Electric Vehicles,” IEEE Trans. Power Electron., vol. 27, no. 4, pp. 1668–1678, Apr. 2012.
[34] Z. Li, S. Hoshina, N. Satake, and M. Nogi, “Development of DC/DC Converter for Battery Energy Storage Supporting Railway DC Feeder Systems,” IEEE Trans. Ind. Appl., vol. 52, no. 5, pp. 4218–4224, Sep. 2016.
[35] P. Garcia, L. M. Fernandez, C. A. Garcia, and F. Jurado, “Energy Management System of Fuel-Cell-Battery Hybrid Tramway,” IEEE Trans. Ind. Electron., vol. 57, no. 12, pp. 4013–4023, Dec. 2010.
[36] A. K. Rathore and U. Prasanna, “Comparison of soft-switching voltage-fed and current-fed bi-directional isolated Dc/Dc converters for fuel cell vehicles,” in 2012 IEEE International Symposium on Industrial Electronics, 2012, pp. 252–257.
[37] B. Zhao, Q. Song, W. Liu, and Y. Sun, “Overview of Dual-Active-Bridge Isolated Bidirectional DC-DC Converter for High-Frequency-Link Power-Conversion System,” IEEE Trans. Power Electron., vol. 29, no. 8, pp. 4091–4106, Aug. 2014.
[38] P. Asfaux and J. Bourdon, “Development of a 12kW isolated and bidirectional DC-DC Converter dedicated to the More Electrical Aircraft: The Buck Boost Converter Unit (BBCU),” in PCIM Europe 2016; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management, 2016, pp. 1–8.
[39] P. Thummala, D. Maksimovic, Z. Zhang, and M. A. E. Andersen, “Digital Control of a High-Voltage (2.5 kV) Bidirectional DC–DC Flyback Converter for Driving a Capacitive Incremental Actuator,” IEEE Trans. Power Electron., vol. 31, no. 12, pp. 8500–8516, Dec. 2016.
[40] R. J. Wai and J. J. Liaw, “High-Efficiency-Isolated Single-Input Multiple-Output Bidirectional Converter,” IEEE Trans. Power Electron., vol. 30, no. 9, pp. 4914–4930, Sep. 2015.
[41] Y. Du, S. Lukic, B. Jacobson, and A. Huang, “Review of high power isolated bi-directional DC-DC converters for PHEV/EV DC charging infrastructure,” in 2011 IEEE Energy Conversion Congress and Exposition, 2011, pp. 553–560.
[42] M. Jain, M. Daniele, and P. K. Jain, “A bidirectional DC-DC converter topology for low power application,” IEEE Trans. Power Electron., vol. 15, no. 4, pp. 595–606, Jul. 2000.
[43] L. Roggia, L. Schuch, J. E. Baggio, C. Rech, and J. R. Pinheiro, “Integrated Full-Bridge-Forward DC-DC Converter for a Residential Microgrid Application,” IEEE Trans. Power Electron., vol. 28, no. 4, pp. 1728–1740, Apr. 2013.
[44] Y. Xie, J. Sun, and J. S. Freudenberg, “Power Flow Characterization of a Bidirectional Galvanically Isolated High-Power DC/DC Converter Over a Wide Operating Range,” IEEE Trans. Power Electron., vol. 25, no. 1, pp. 54–66, Jan. 2010.
[45] R. T. Naayagi, A. J. Forsyth, and R. Shuttleworth, “High-Power Bidirectional DC-DC Converter for Aerospace Applications,” IEEE Trans. Power Electron., vol. 27, no. 11, pp. 4366–4379, Nov. 2012.

[46] F. Krismer and J. W. Kolar, “Efficiency-Optimized High-Current Dual Active Bridge Converter for Automotive Applications,” IEEE Trans. Ind. Electron., vol. 59, no. 7, pp. 2745–2760, Jul. 2012.
[47] W. Chen, P. Rong, and Z. Lu, “Snubberless Bidirectional DC #x2013;DC Converter With New CLLC Resonant Tank Featuring Minimized Switching Loss,” IEEE Trans. Ind. Electron., vol. 57, no. 9, pp. 3075–3086, Sep. 2010.
[48] Z. Zhang, O. C. Thomsen, M. A. E. Andersen, J. D. Schmidt, and H. R. Nielsen, “Analysis and Design of Bi-directional DC-DC Converter in Extended Run Time DC UPS System Based on Fuel Cell and Supercapacitor,” in 2009 Twenty-Fourth Annual IEEE Applied Power Electronics Conference and Exposition, 2009, pp. 714–719.
[49] B. Zhao, Q. Yu, and W. Sun, “Extended-Phase-Shift Control of Isolated Bidirectional DC #x2013;DC Converter for Power Distribution in Microgrid,” IEEE Trans. Power Electron., vol. 27, no. 11, pp. 4667–4680, Nov. 2012.
[50] L. Rubino, B. Guida, F. Liccardo, P. Marino, and A. Cavallo, “Buck-boost DC/DC converter for aeronautical applications,” in 2010 IEEE International Symposium on Industrial Electronics, 2010, pp. 2690–2695.
[51] “A bidirectional DC-DC converter for fuel cell electric vehicle driving system,” IEEE Trans. Power Electron., vol. 21, no. 4, pp. 950–958, Jul. 2006.
[52] F. Z. Peng, H. Li, G.-J. Su, and J. S. Lawler, “A new ZVS bidirectional DC-DC converter for fuel cell and battery application,” IEEE Trans. Power Electron., vol. 19, no. 1, pp. 54–65, Jan. 2004.
[53] G. Ma, W. Qu, G. Yu, Y. Liu, N. Liang, and W. Li, “A Zero-Voltage-Switching Bidirectional DC-DC Converter With State Analysis and Soft-Switching-Oriented Design Consideration,” IEEE Trans. Ind. Electron., vol. 56, no. 6, pp. 2174–2184, Jun. 2009.
[54] A. K. Rathore, D. R. Patil, and D. Srinivasan, “Non-isolated Bidirectional Soft-Switching Current-Fed LCL Resonant DC/DC Converter to Interface Energy Storage in DC Microgrid,” IEEE Trans. Ind. Appl., vol. 52, no. 2, pp. 1711–1722, Mar. 2016.
[55] A. H. Weinberg and J. Schreuders, “A High-Power High-Voltage DC-DC Converter for Space Applications,” IEEE Trans. Power Electron., vol. PE-1, no. 3, pp. 148–160, Jul. 1986.
[56] E. Rotman and S. S. Ben-Yaakov, “Rapid push pull resonant charger for high power, high voltage applications using low input voltage,” in 2013 IEEE Energy Conversion Congress and Exposition, 2013, pp. 2325–2332.
[57] V. Garcia, M. Rico, J. Sebastian, M. M. Hernando, and J. Uceda, “An optimized DC-to-DC converter topology for high-voltage pulse-load applications,” in , 25th Annual IEEE Power Electronics Specialists Conference, PESC ’94 Record, 1994, pp. 1413–1421 vol.2.
[58] J. Sun, X. Ding, M. Nakaoka, and H. Takano, “Series resonant ZCS-PFM DC-DC converter with multistage rectified voltage multiplier and dual-mode PFM control scheme for medical-use high-voltage X-ray power generator,” IEE Proc. - Electr. Power Appl., vol. 147, no. 6, pp. 527–534, Nov. 2000.
[59] H. Wu, T. Xia, Y. Xing, P. Xu, H. Hu, and Z. Zhang, “Secondary-side phase-shift-controlled high step-up hybrid resonant converter with voltage multiplier for high efficiency PV applications,” in 2015 IEEE Applied Power Electronics Conference and Exposition (APEC), 2015, pp. 1428–1434.

[60] H. Mao, J. Abu-Qahouq, S. Luo, and I. Batarseh, “Zero-voltage-switching half-bridge DC-DC converter with modified PWM control method,” IEEE Trans. Power Electron., vol. 19, no. 4, pp. 947–958, Jul. 2004.
[61] S. J. Jeon, F. Canales, P. M. Barbosa, and F. C. Lee, “A primary-side-assisted zero-voltage and zero-current switching three-level DC-DC converter with phase-shift control,” in APEC. Seventeenth Annual IEEE Applied Power Electronics Conference and Exposition (Cat. No.02CH37335), 2002, vol. 2, pp. 641–647 vol.2.
[62] S.-J. Jeon and G.-H. Cho, “A zero-voltage and zero-current switching full bridge DC-DC converter with transformer isolation,” IEEE Trans. Power Electron., vol. 16, no. 5, pp. 573–580, Sep. 2001.
[63] J. Zhang, X. Xie, X. Wu, G. Wu, and Z. Qian, “A novel zero-current-transition full bridge DC/DC converter,” IEEE Trans. Power Electron., vol. 21, no. 2, pp. 354–360, Mar. 2006.
[64] H.-S. Choi, J.-W. Kim, and B. H. Cho, “Novel zero-voltage and zero-current-switching (ZVZCS) full-bridge PWM converter using coupled output inductor,” IEEE Trans. Power Electron., vol. 17, no. 5, pp. 641–648, Sep. 2002.
[65] J.-G. Cho, C.-Y. Jeong, and F. C. Y. Lee, “Zero-voltage and zero-current-switching full-bridge PWM converter using secondary active clamp,” IEEE Trans. Power Electron., vol. 13, no. 4, pp. 601–607, Jul. 1998.
[66] T. Song, N. Huang, and A. Ioinovici, “A family of zero-voltage and zero-current-switching (ZVZCS) three-level DC-DC converters with secondary-assisted regenerative passive snubber,” IEEE Trans. Circuits Syst. Regul. Pap., vol. 52, no. 11, pp. 2473–2481, Nov. 2005.
[67] E. Chu, X. Hou, H. Zhang, M. Wu, and X. Liu, “Novel Zero-Voltage and Zero-Current Switching (ZVZCS) PWM Three-Level DC/DC Converter Using Output Coupled Inductor,” IEEE Trans. Power Electron., vol. 29, no. 3, pp. 1082–1093, Mar. 2014.
[68] W. Li, D. Xu, B. Wu, Y. Zhao, H. Yang, and X. He, “Zero-voltage-switching dual-boost converter with multi-functional inductors and improved symmetrical rectifier for distributed generation systems,” IET Power Electron., vol. 5, no. 7, pp. 969–977, Aug. 2012.
[69] J. H. Lee, T. J. Liang, and J. F. Chen, “Isolated Coupled-Inductor-Integrated DC-DC Converter With Nondissipative Snubber for Solar Energy Applications,” IEEE Trans. Ind. Electron., vol. 61, no. 7, pp. 3337–3348, Jul. 2014.
[70] D. Wang, Y. Deng, and X. He, “Isolated ZVT boost converter with switched capacitors and coupled inductors,” in 2008 34th Annual Conference of IEEE Industrial Electronics, 2008, pp. 808–814.
[71] W. Li and X. He, “A Family of Isolated Interleaved Boost and Buck Converters With Winding-Cross-Coupled Inductors,” IEEE Trans. Power Electron., vol. 23, no. 6, pp. 3164–3173, Nov. 2008.
[72] Y. Hu, W. Xiao, W. Li, and X. He, “Three-phase interleaved high-step-up converter with coupled-inductor-based voltage quadrupler,” IET Power Electron., vol. 7, no. 7, pp. 1841–1849, Jul. 2014.
[73] J. Elmes, C. Jourdan, O. Abdel-Rahman, and I. Batarseh, “High-Voltage, High-Power-Density DC-DC Converter for Capacitor Charging Applications,” in 2009 Twenty-Fourth Annual IEEE Applied Power Electronics Conference and Exposition, 2009, pp. 433–439.

[74] T. J. Liang, J. H. Lee, S. M. Chen, J. F. Chen, and L. S. Yang, “Novel Isolated High-Step-Up DC-DC Converter With Voltage Lift,” IEEE Trans. Ind. Electron., vol. 60, no. 4, pp. 1483–1491, Apr. 2013.
[75] D. Y. Kim, J. K. Kim, and G. W. Moon, “A Three-Level Converter With Reduced Filter Size Using Two Transformers and Flying Capacitors,” IEEE Trans. Power Electron., vol. 28, no. 1, pp. 46–53, Jan. 2013.
[76] Y. K. Cheng and K. W. E. Cheng, “General Study for using LED to replace traditional lighting devices,” in 2006 2nd International Conference on Power Electronics Systems and Applications, 2006, pp. 173–177.
[77] V. K. Chinnaiyan, J. Jerome, J. Karpagam, and S. S. Mohammed, “Design and implementation of high power DC-DC converter and speed control of DC motor using TMS320F240 DSP,” in 2006 India International Conference on Power Electronics, 2006, pp. 388–392.
[78] W. J. Lee, C. E. Kim, G. W. Moon, and S. K. Han, “A New Phase-Shifted Full-Bridge Converter With Voltage-Doubler-Type Rectifier for High-Efficiency PDP Sustaining Power Module,” IEEE Trans. Ind. Electron., vol. 55, no. 6, pp. 2450–2458, Jun. 2008.
[79] M. Nymand and M. A. E. Andersen, “High-Efficiency Isolated Boost DC-DC Converter for High-Power Low-Voltage Fuel-Cell Applications,” IEEE Trans. Ind. Electron., vol. 57, no. 2, pp. 505–514, Feb. 2010.
[80] J. Y. Lee, Y. S. Jeong, and B. M. Han, “An Isolated DC/DC Converter Using High-Frequency Unregulated LLC Resonant Converter for Fuel Cell Applications,” IEEE Trans. Ind. Electron., vol. 58, no. 7, pp. 2926–2934, Jul. 2011.
[81] S. S. Dobakhshari, J. Milimonfared, M. Taheri, and H. Moradisizkoohi, “A Quasi-Resonant Current-Fed Converter With Minimum Switching Losses,” IEEE Trans. Power Electron., vol. 32, no. 1, pp. 353–362, Jan. 2017.
[82] J. F. Chen, R. Y. Chen, and T. J. Liang, “Study and Implementation of a Single-Stage Current-Fed Boost PFC Converter With ZCS for High Voltage Applications,” IEEE Trans. Power Electron., vol. 23, no. 1, pp. 379–386, Jan. 2008.
[83] H. Wang, Q. Sun, H. S. H. Chung, S. Tapuchi, and A. Ioinovici, “A ZCS Current-Fed Full-Bridge PWM Converter With Self-Adaptable Soft-Switching Snubber Energy,” IEEE Trans. Power Electron., vol. 24, no. 8, pp. 1977–1991, Aug. 2009.
[84] A. Mousavi, P. Das, and G. Moschopoulos, “A Comparative Study of a New ZCS DC-DC Full-Bridge Boost Converter With a ZVS Active-Clamp Converter,” IEEE Trans. Power Electron., vol. 27, no. 3, pp. 1347–1358, Mar. 2012.
[85] P. J. Wolfs, “A current-sourced DC-DC converter derived via the duality principle from the half-bridge converter,” IEEE Trans. Ind. Electron., vol. 40, no. 1, pp. 139–144, Feb. 1993.
[86] L. Yan and B. Lehman, “An integrated magnetic isolated two-inductor boost converter: analysis, design and experimentation,” IEEE Trans. Power Electron., vol. 20, no. 2, pp. 332–342, Mar. 2005.
[87] W. Song and B. Lehman, “Current-Fed Dual-Bridge DC ndash;DC Converter,” IEEE Trans. Power Electron., vol. 22, no. 2, pp. 461–469, Mar. 2007.

[88] J. Wen, T. Jin, and K. Smedley, “A new interleaved isolated boost converter for high power applications,” in Twenty-First Annual IEEE Applied Power Electronics Conference and Exposition, 2006. APEC ’06., 2006, p. 6 pp.-.
[89] Y. Zhao, X. Xiang, W. Li, X. He, and C. Xia, “Advanced Symmetrical Voltage Quadrupler Rectifiers for High Step-Up and High Output-Voltage Converters,” IEEE Trans. Power Electron., vol. 28, no. 4, pp. 1622–1631, Apr. 2013.
[90] K. C. Tseng, C. C. Huang, and C. A. Cheng, “A High Step-Up Converter With Voltage-Multiplier Modules for Sustainable Energy Applications,” IEEE J. Emerg. Sel. Top. Power Electron., vol. 3, no. 4, pp. 1100–1108, Dec. 2015.
[91] I. Barbi and R. Gules, “Isolated DC-DC converters with high-output voltage for TWTA telecommunication satellite applications,” IEEE Trans. Power Electron., vol. 18, no. 4, pp. 975–984, Jul. 2003.
[92] M. Chen, K. K. Afridi, S. Chakraborty, and D. J. Perreault, “Multitrack Power Conversion Architecture,” IEEE Trans. Power Electron., vol. 32, no. 1, pp. 325–340, Jan. 2017.
[93] G. Palumbo and D. Pappalardo, “Charge Pump Circuits: An Overview on Design Strategies and Topologies,” IEEE Circuits Syst. Mag., vol. 10, no. 1, pp. 31–45, First 2010.
[94] J. A. Starzyk, Y.-W. Jan, and F. Qiu, “A DC-DC charge pump design based on voltage doublers,” IEEE Trans. Circuits Syst. Fundam. Theory Appl., vol. 48, no. 3, pp. 350–359, Mar. 2001.
[95] M. D. Seeman and S. R. Sanders, “Analysis and Optimization of Switched-Capacitor DC-DC Converters,” in 2006 IEEE Workshops on Computers in Power Electronics, 2006, pp. 216–224.
[96] M. S. Makowski, “Realizability conditions and bounds on synthesis of switched-capacitor DC-DC voltage multiplier circuits,” IEEE Trans. Circuits Syst. Fundam. Theory Appl., vol. 44, no. 8, pp. 684–691, Aug. 1997.
[97] Y. Lei and R. C. N. Pilawa-Podgurski, “A General Method for Analyzing Resonant and Soft-Charging Operation of Switched-Capacitor Converters,” IEEE Trans. Power Electron., vol. 30, no. 10, pp. 5650–5664, Oct. 2015.
[98] H. S.-H. Chung, “Design and analysis of a switched-capacitor-based step-up DC/DC converter with continuous input current,” IEEE Trans. Circuits Syst. Fundam. Theory Appl., vol. 46, no. 6, pp. 722–730, Jun. 1999.
[99] R. Guo, Z. Liang, and A. Q. Huang, “A Family of Multimodes Charge Pump based DC-DC Converter With High Efficiency over Wide Input and Output Range,” IEEE Trans. Power Electron., vol. 27, no. 11, pp. 4788–4798, Nov. 2012.
[100] M. Abbasi and J. Lam, “A Step-Up Transformerless, ZV-ZCS High-Gain DC/DC Converter With Output Voltage Regulation Using Modular Step-Up Resonant Cells for DC Grid in Wind Systems,” IEEE J. Emerg. Sel. Top. Power Electron., vol. 5, no. 3, pp. 1102–1121, Sep. 2017.
[101] M. Prudente, L. L. Pfitscher, G. Emmendoerfer, E. F. Romaneli, and R. Gules, “Voltage Multiplier Cells Applied to Non-Isolated DC-DC Converters,” IEEE Trans. Power Electron., vol. 23, no. 2, pp. 871–887, Mar. 2008.
[102] E. H. Ismail, M. A. Al-Saffar, A. J. Sabzali, and A. A. Fardoun, “A Family of Single-Switch PWM Converters With High Step-Up Conversion Ratio,” IEEE Trans. Circuits Syst. Regul. Pap., vol. 55, no. 4, pp. 1159–1171, May 2008.
[103] B. Axelrod, Y. Berkovich, and A. Ioinovici, “Switched-Capacitor/Switched-Inductor Structures for Getting Transformerless Hybrid DC #x2013;DC PWM

Converters," IEEE Trans. Circuits Syst. Regul. Pap., vol. 55, no. 2, pp. 687–696, Mar. 2008.
[104] M. Prudente, L. Pfitscher, and R. Gules, "A Boost Converter With Voltage Multiplier Cells," in 2005 IEEE 36th Power Electronics Specialists Conference, 2005, pp. 2716–2721.
[105] S. Rivera, S. Kouro, B. Wu, J. I. Leon, J. Rodríguez, and L. G. Franquelo, "Cascaded H-bridge multilevel converter multistring topology for large scale photovoltaic systems," in 2011 IEEE International Symposium on Industrial Electronics, 2011, pp. 1837–1844.
[106] A. A. Fardoun and E. H. Ismail, "Ultra Step-Up DC-DC Converter With Reduced Switch Stress," IEEE Trans. Ind. Appl., vol. 46, no. 5, pp. 2025–2034, Sep. 2010.
[107] B. Axelrod, Y. Berkovich, and A. Ioinovici, "Transformerless DC-DC converters with a very high DC line-to-load voltage ratio," in Proceedings of the 2003 International Symposium on Circuits and Systems, 2003. ISCAS '03, 2003, vol. 3, p. III-435-III-438 vol.3.
[108] I. C. Kobougias and E. C. Tatakis, "Optimal Design of a Half-Wave Cockcroft-Walton Voltage Multiplier With Minimum Total Capacitance," IEEE Trans. Power Electron., vol. 25, no. 9, pp. 2460–2468, Sep. 2010.
[109] S. Lee, P. Kim, and S. Choi, "High Step-Up Soft-Switched Converters Using Voltage Multiplier Cells," IEEE Trans. Power Electron., vol. 28, no. 7, pp. 3379–3387, Jul. 2013.
[110] L. Müller and J. W. Kimball, "High Gain DC-DC Converter Based on the Cockcroft-Walton Multiplier," IEEE Trans. Power Electron., vol. 31, no. 9, pp. 6405–6415, Sep. 2016.
[111] C. M. Young, M. H. Chen, T. A. Chang, C. C. Ko, and K. K. Jen, "Cascade Cockcroft-Walton Voltage Multiplier Applied to Transformerless High Step-Up DC-DC Converter," IEEE Trans. Ind. Electron., vol. 60, no. 2, pp. 523–537, Feb. 2013.
[112] J.-W. Baek, M.-H. Ryoo, T.-J. Kim, D.-W. Yoo, and J.-S. Kim, "High boost converter using voltage multiplier," in 31st Annual Conference of IEEE Industrial Electronics Society, 2005. IECON 2005., 2005, p. 6 pp.-.
[113] K. B. Park, G. W. Moon, and M. J. Youn, "High Step-up Boost Converter Integrated With a Transformer-Assisted Auxiliary Circuit Employing Quasi-Resonant Operation," IEEE Trans. Power Electron., vol. 27, no. 4, pp. 1974–1984, Apr. 2012.
[114] M. Forouzesh and A. Baghramian, "Galvanically isolated high gain Y-source DC-DC converters for dispersed power generation," IET Power Electron., vol. 9, no. 6, pp. 1192–1203, 2016.
[115] T. J. Liang, S. M. Chen, L. S. Yang, J. F. Chen, and A. Ioinovici, "Ultra-Large Gain Step-Up Switched-Capacitor DC-DC Converter With Coupled Inductor for Alternative Sources of Energy," IEEE Trans. Circuits Syst. Regul. Pap., vol. 59, no. 4, pp. 864–874, Apr. 2012.
[116] Y. P. Hsieh, J. F. Chen, T. J. P. Liang, and L. S. Yang, "Novel High Step-Up DC-DC Converter With Coupled-Inductor and Switched-Capacitor Techniques for a Sustainable Energy System," IEEE Trans. Power Electron., vol. 26, no. 12, pp. 3481–3490, Dec. 2011.

[117] A. Chub, D. Vinnikov, F. Blaabjerg, and F. Z. Peng, “A Review of Galvanically Isolated Impedance-Source DC #x2013;DC Converters,” IEEE Trans. Power Electron., vol. 31, no. 4, pp. 2808–2828, Apr. 2016.
[118] D. Vinnikov and I. Roasto, “Quasi-Z-Source-Based Isolated DC/DC Converters for Distributed Power Generation,” IEEE Trans. Ind. Electron., vol. 58, no. 1, pp. 192–201, Jan. 2011.
[119] Y. P. Siwakoti, F. Blaabjerg, P. C. Loh, and G. E. Town, “High-voltage boost quasi-Z-source isolated DC/DC converter,” IET Power Electron., vol. 7, no. 9, pp. 2387–2395, Sep. 2014.
[120] Y. Lu, H. Liu, H. Hu, H. Wu, and Y. Xing, “Single-switch high step-up converter with coupled-inductor and built-in transformer,” in 2015 IEEE 10th Conference on Industrial Electronics and Applications (ICIEA), 2015, pp. 1181–1186.
[121] Y. Deng, Q. Rong, W. Li, Y. Zhao, J. Shi, and X. He, “Single-Switch High Step-Up Converters With Built-In Transformer Voltage Multiplier Cell,” IEEE Trans. Power Electron., vol. 27, no. 8, pp. 3557–3567, Aug. 2012.
[122] K. B. Park, G. W. Moon, and M. J. Youn, “Nonisolated High Step-Up Stacked Converter Based on Boost-Integrated Isolated Converter,” IEEE Trans. Power Electron., vol. 26, no. 2, pp. 577–587, Feb. 2011.
[123] S. Poshtkouhi, A. Biswas, and O. Trescases, “DC-DC converter for high granularity, sub-string MPPT in photovoltaic applications using a virtual-parallel connection,” in 2012 Twenty-Seventh Annual IEEE Applied Power Electronics Conference and Exposition (APEC), 2012, pp. 86–92.
[124] T.-F. Wu and T.-H. Yu, “Unified approach to developing single-stage power converters,” IEEE Trans. Aerosp. Electron. Syst., vol. 34, no. 1, pp. 211–223, Jan. 1998.
[125] M. G. Ortiz-Lopez, J. Leyva-Ramos, E. E. Carbajal-Gutierrez, and J. A. Morales-Saldana, “Modelling and analysis of switch-mode cascade converters with a single active switch,” IET Power Electron., vol. 1, no. 4, pp. 478–487, Dec. 2008.
[126] Y. R. de Novaes, A. Rufer, and I. Barbi, “A New Quadratic, Three-Level, DC/DC Converter Suitable for Fuel Cell Applications,” in 2007 Power Conversion Conference - Nagoya, 2007, pp. 601–607.
[127] N. Zhang, D. Sutanto, K. M. Muttaqi, B. Zhang, and D. Qiu, “High-voltage-gain quadratic boost converter with voltage multiplier,” IET Power Electron., vol. 8, no. 12, pp. 2511–2519, 2015.
[128] K. D. Kim, J. G. Kim, Y. C. Jung, and C. Y. Won, “Improved non-isolated high voltage gain boost converter using coupled inductors,” in 2011 International Conference on Electrical Machines and Systems, 2011, pp. 1–6.
[129] A. Shahin, M. Hinaje, J. P. Martin, S. Pierfederici, S. Rael, and B. Davat, “High Voltage Ratio DC-DC Converter for Fuel-Cell Applications,” IEEE Trans. Ind. Electron., vol. 57, no. 12, pp. 3944–3955, Dec. 2010.
[130] J. Fu, B. Zhang, D. Qiu, and W. Xiao, “A novel single-switch cascaded DC-DC converter of Boost and Buck-boost converters,” in 2014 16th European Conference on Power Electronics and Applications, 2014, pp. 1–9.
[131] X. Zhang and T. C. Green, “The Modular Multilevel Converter for High Step-Up Ratio DC-DC Conversion,” IEEE Trans. Ind. Electron., vol. 62, no. 8, pp. 4925–4936, Aug. 2015.

[132] J. C. Rosas-Caro, J. M. Ramirez, F. Z. Peng, and A. Valderrabano, “A DC-DC multilevel boost converter,” IET Power Electron., vol. 3, no. 1, pp. 129–137, Jan. 2010.
[133] W. Li, W. Li, Y. Deng, and X. He, “Single-Stage Single-Phase High-Step-Up ZVT Boost Converter for Fuel-Cell Microgrid System,” IEEE Trans. Power Electron., vol. 25, no. 12, pp. 3057–3065, Dec. 2010.
[134] D. Wang, X. He, and R. Zhao, “ZVT Interleaved Boost Converters with Built-In Voltage Doubler and Current Auto-Balance Characteristic,” IEEE Trans. Power Electron., vol. 23, no. 6, pp. 2847–2854, Nov. 2008.
[135] W. Li and X. He, “A Family of Interleaved DC-DC Converters DeducedFrom a Basic Cell With Winding-Cross-CoupledInductors (WCCIs) for High Step-Upor Step-Down Conversions,” IEEE Trans. Power Electron., vol. 23, no. 4, pp. 1791–1801, Jul. 2008.
[136] W. Li and X. He, “ZVT interleaved boost converters for high-efficiency, high step-up DC-DC conversion,” IET Electr. Power Appl., vol. 1, no. 2, pp. 284–290, Mar. 2007.
[137] D. Cao and F. Z. Peng, “Zero-current-switching multilevel modular switched-capacitor dc-dc converter,” in 2009 IEEE Energy Conversion Congress and Exposition, 2009, pp. 3516–3522.
[138] K. K. Law, K. W. E. Cheng, and Y. P. B. Yeung, “Design and analysis of switched-capacitor-based step-up resonant converters,” IEEE Trans. Circuits Syst. Regul. Pap., vol. 52, no. 5, pp. 943–948, May 2005.
[139] S. R. Sanders, E. Alon, H. P. Le, M. D. Seeman, M. John, and V. W. Ng, “The Road to Fully Integrated DC-DC Conversion via the Switched-Capacitor Approach,” IEEE Trans. Power Electron., vol. 28, no. 9, pp. 4146–4155, Sep. 2013.
[140] T. F. Wu, Y. S. Lai, J. C. Hung, and Y. M. Chen, “Boost Converter With Coupled Inductors and Buck-Boost Type of Active Clamp,” IEEE Trans. Ind. Electron., vol. 55, no. 1, pp. 154–162, Jan. 2008.
[141] Y. Tang, D. Fu, J. Kan, and T. Wang, “Dual Switches DC/DC Converter With Three-Winding-Coupled Inductor and Charge Pump,” IEEE Trans. Power Electron., vol. 31, no. 1, pp. 461–469, Jan. 2016.
[142] M. Forouzesh, K. Yari, A. Baghramian, and S. Hasanpour, “Single-switch high step-up converter based on coupled inductor and switched capacitor techniques with quasi-resonant operation,” IET Power Electron., vol. 10, no. 2, pp. 240–250, 2017.
[143] L. H. S. C. Barreto, E. A. A. Coelho, V. J. Farias, J. C. de Oliveira, L. C. de Freitas, and J. J. B. Vieira, “A quasi-resonant quadratic boost converter using a single resonant network,” IEEE Trans. Ind. Electron., vol. 52, no. 2, pp. 552–557, Apr. 2005.
[144] W. Li, W. Li, and X. He, “Zero-voltage transition interleaved high step-up converter with built-in transformer,” IET Power Electron., vol. 4, no. 5, pp. 523–531, May 2011.
[145] W. Li, X. Xiang, C. Li, W. Li, and X. He, “Interleaved High Step-Up ZVT Converter With Built-In Transformer Voltage Doubler Cell for Distributed PV Generation System,” IEEE Trans. Power Electron., vol. 28, no. 1, pp. 300–313, Jan. 2013.
[146] H. L. Do, “A Soft-Switching DC/DC Converter With High Voltage Gain,” IEEE Trans. Power Electron., vol. 25, no. 5, pp. 1193–1200, May 2010.

[147] W. Li, W. Li, X. He, D. Xu, and B. Wu, “General Derivation Law of Nonisolated High-Step-Up Interleaved Converters With Built-In Transformer,” IEEE Trans. Ind. Electron., vol. 59, no. 3, pp. 1650–1661, Mar. 2012.
[148] S. D. Johnson, A. F. Witulski, and R. W. Erickson, “Comparison of resonant topologies in high-voltage DC applications,” IEEE Trans. Aerosp. Electron. Syst., vol. 24, no. 3, pp. 263–274, May 1988.
[149] C. M. C. Duarte and I. Barbi, “A family of ZVS-PWM active-clamping DC-to-DC converters: synthesis, analysis, design, and experimentation,” IEEE Trans. Circuits Syst. Fundam. Theory Appl., vol. 44, no. 8, pp. 698–704, Aug. 1997.
[150] H.-S. Choi and B. H. Cho, “Novel zero-current-switching (ZCS) PWM switch cell minimizing additional conduction loss,” IEEE Trans. Ind. Electron., vol. 49, no. 1, pp. 165–172, Feb. 2002.
[151] C.-M. Wang, “Novel zero-Voltage-transition PWM DC-DC converters,” IEEE Trans. Ind. Electron., vol. 53, no. 1, pp. 254–262, Feb. 2005.
[152] D.-Y. Lee, M.-K. Lee, D.-S. Hyun, and I. Choy, “New zero-current-transition PWM DC/DC converters without current stress,” IEEE Trans. Power Electron., vol. 18, no. 1, pp. 95–104, Jan. 2003.
[153] A. Elasser and D. A. Torrey, “Soft switching active snubbers for DC/DC converters,” IEEE Trans. Power Electron., vol. 11, no. 5, pp. 710–722, Sep. 1996.
[154] J. Y. Zhu and D. Ding, “Zero-voltage- and zero-current-switched PWM DC-DC converters using active snubber,” IEEE Trans. Ind. Appl., vol. 35, no. 6, pp. 1406–1412, Nov. 1999.
[155] V. Smet et al., “Ageing and Failure Modes of IGBT Modules in High-Temperature Power Cycling,” IEEE Trans. Ind. Electron., vol. 58, no. 10, pp. 4931–4941, Oct. 2011.
[156] Erickson. Fundamentals of Power Electronics[M]. Kluwer Academic Publishers, 2001.
[157] C. C. Chan, "The State of the Art of Electric, Hybrid, and Fuel Cell Vehicles," in Proceedings of the IEEE, vol. 95, no. 4, pp. 704-718, April 2007.
[158] L. Huber, Y. Jang and M. M. Jovanovic, "Performance Evaluation of Bridgeless PFC Boost Rectifiers," in IEEE Transactions on Power Electronics, vol. 23, no. 3, pp. 1381-1390, May 2008.