

# High Step-up Converter without Electrolytic Capacitors for Renewable Energy Applications

Yihua Hu, *Member, IEEE*, Wenping Cao, *Senior Member, IEEE*, Bing Ji, *Member, IEEE*, Xiangning He, *Fellow, IEEE*, James Kirtley, *Fellow, IEEE*

**Abstract**—Traditional electrolytic capacitors used in power converters are bulky, unreliable and short in their service life. This paper proposes the use of film capacitors in a high step-up DC-DC converter for renewable energy applications including photovoltaics and fuel cells. The converter is of a three-phase modular structure and six pulse rectifiers are employed to reduce the output voltage ripple. The primary side of the converter includes three interleaved inductors, three main switches and an active clamp circuit. Therefore, the input capacitor can be eliminated and the input current is greatly reduced. The zero voltage switching is achieved during the switching transition for all the active switches so that the switching losses can be reduced greatly. Magnetic energy stored in the leakage inductance is recovered and the reverse-recovery issue associated with diodes is effectively addressed by the leakage inductance of a built-in transformer. The proposed converter is justified by simulation and experimental tests on a 1000W prototype.

**Index Terms**—DC-DC converter, electrolytic capacitor, fuel cells, modularization, photovoltaics, power loss.

## I. INTRODUCTION

RENEWABLE energy is high on the international and national agendas. Photovoltaics (PVs) and fuel cells are two prominent examples and their output is typically low voltage direct current (DC). In these applications, high step-up DC-DC converters with low cost and high reliability are highly desired [1]-[5]. However, large electrolytic capacitors are generally used at the front-end and the output terminal of the converter [2], in order to minimize the current and voltage ripples. These capacitors require galvanic isolation [7] and provide only a limited service life, especially in the PV micro-inverter at outdoor conditions [6].

Voltage gain is also a key performance indicator for DC-DC converters. In the literature, a variety of isolated high step-up topologies to increase the voltage gain are reported [8]-[14]. Among these is an interesting concept of isolating inter-cell transformer and interleaved technology [14]. Nonetheless, due to its multi-cell structure, the bridge circuit suffers from a breakthrough risk and the voltage stress of switching devices is high on the high voltage side. In [15], a group of interleaved Flyback converters with three winding coupled inductors are developed but their current ripples are also high. Thereby new topologies are proposed in [16]-[17] to lower input current ripples while still achieving a high voltage gain. Their

drawback lies in a need for an input capacitor (small) and an output capacitor (large). On the contrary, a symmetrical rectifier configuration is used [18] to decrease the output current ripple but the current ripple on the primary side structure is high. This work is set out to achieve the high voltage gain and low output ripples without the use of electrolytic capacitors, by proposing a new topology which combines the features of electrical isolation and modular structure so as to improve the reliability and cost-effectiveness.

## II. PRINCIPLE OF OPERATION

The proposed three-phase interleaved converter without electrolytic capacitors is presented in Fig. 1, where  $S_1, S_2, S_3$  are the main switch devices,  $S_{c1}, S_{c2}$  and  $S_{c3}$  are clamp switches. The switch devices also form a three-phase bridge.

The capacitor  $C_c$  and the switches  $S_{xxx}$  are employed to clamp the switch devices and to realize soft switching. For the three coupled inductors  $L_1, L_2$  and  $L_3$ , their primary windings are interleaved connected with each other and their secondary windings are star connected for a high output voltage gain. The winding turns of the coupled inductors are represented by  $n_1$  (primary) and  $n_2$  (secondary), respectively, and the turns ratio  $N$  is derived from  $n_2/n_1$ . The coupling reference of  $L_1, L_2$  and  $L_3$  are marked with “\*”, “o” and “□”, respectively.  $L_{LK1}, L_{LK2}$  and  $L_{LK3}$  denote the leakage inductances of the coupled inductors;  $D_{o1}-D_{o6}$  are the rectifier diodes;  $C_o$  is the output filter capacitor.

There are six operating stages during one switching period. The equivalent circuits for each stage are presented in Fig. 3 and explained in detail as follows.

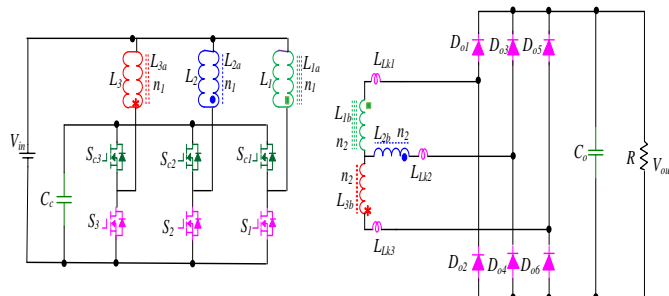


Fig. 1 The proposed DC-DC converter without electrolytic capacitors.

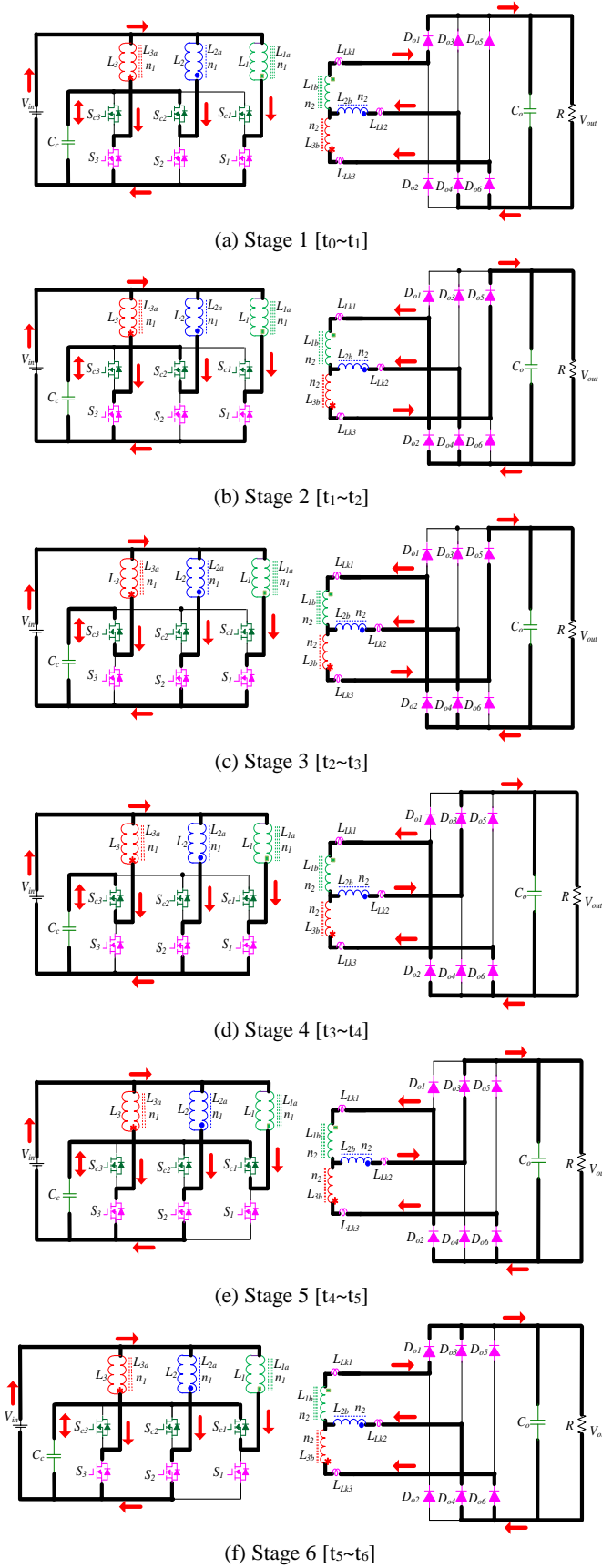


Fig. 3 Six operating stages of the proposed converter.

### A. Stage 1

Before  $t_0$ , the main switch  $S_1$  and the clamp Switch  $S_{c1}$  are in off state and the common clamp capacitor  $C_c$  is resonant with the leakage inductance of  $L_1$ . From  $t_0$  onwards, the voltage of  $S_{c1}$  increases from zero and zero voltage switching (ZVS) is realized on the clamp switch  $S_{c1}$ . The turn-on signal of the main switch  $S_1$  is given in this period when its parasitic diode is in on state, and  $S_1$  turns on with ZVS. Meanwhile, the main switch  $S_2$  turns off and its parasitic capacitor  $C_{s2}$  is charged by the magnetizing current of  $L_2$ . Due to its parasitic capacitance, the main switch  $S_2$  turns off with ZVS. In this period, the switching voltage of the main switch  $S_2$  reaches the level of  $C_c$  and the parasitic diode of  $S_{c2}$  conducts. The voltage of the main switch  $S_2$  is clamped to the voltage of  $C_c$ . The primary-side current of  $L_2$  begins to decrease and that of  $L_1$  begins to increase.  $L_2$  and  $L_3$  work in forward condition and  $L_1$  in flyback condition. Corresponding rectifier diodes  $D_{01}$ ,  $D_{04}$  and  $D_{06}$  conduct.

### B. Stage 2

In this stage, the main switches  $S_1$  and  $S_3$  turn on and the active clamp switch  $S_{c2}$  is in on state. At  $t_1$ , the current in the primary of  $L_1$  and  $L_3$  increases whilst that of  $L_2$  falls below zero. During this stage,  $L_1$  and  $L_2$  work in forward mode,  $L_3$  works in flyback mode, and the rectifier diodes  $D_{02}$ ,  $D_{04}$  and  $D_{05}$  conduct. The secondary windings of  $L_1$  and  $L_3$  are series connected to charge the output for high voltage gain; these of  $L_2$  and  $L_3$  are also series connected to charge the output for lowering the output voltage ripple.

The current in the secondary windings of  $L_1$  and  $L_2$  can be expressed by Eqs. 1 and 2.

$$i_{LK1} = -\frac{N}{L_{LK1}} \frac{V_{in} - V_{out}}{1-D} (t - t_1) \quad (1)$$

$$i_{LK2} = i_{LK2(t_2)} - \frac{N}{L_{LK2}} \frac{V_{in} - V_{out}}{1-D} (t - t_1) \quad (2)$$

By Kirchhoff's current law (KCL), the current on the secondary side of  $L_3$  is given by (rewrite i3=)

$$i_{LK3} + i_{LK1} + i_{LK2} = 0 \quad (3)$$

### C. Stage 3

At  $t_2$ ,  $S_{c2}$  turns off and the clamp capacitor  $C_{s2}$  is resonant with the leakage inductance of  $L_2$ . While the voltage across the parasitic capacitance of the main switch decreases, the voltage of  $S_{c2}$  increases from zero, and ZVS is realized on  $S_{c2}$ . The turn-on signal of  $S_2$  is given when its parasitic diode is in on state and  $S_2$  turns on with ZVS. The main switch  $S_3$  turns off, and then its parasitic capacitor  $C_{s3}$  is charged by the magnetizing current of  $L_3$ . In this period, the voltage of the main switch  $S_3$  reaches the voltage of  $C_c$  and that of the main switch  $S_3$  is clamped to the voltage of  $C_{c3}$ .  $L_1$  and  $L_2$  work in forward mode and  $L_3$  works in flyback mode. The antiparallel diode of  $S_{c3}$  and  $D_{02}$ ,  $D_{04}$  and  $D_{05}$  all conduct. The secondary windings of  $L_1$  and  $L_3$  are series connected to charge the output for a high voltage gain and these of  $L_2$  and  $L_3$  also series connected to charge the output and to reduce the output voltage ripple.

#### D. Stage 4

In this stage,  $S_1$  and  $S_2$  turn on; the active clamp switch  $S_{c3}$  is in on state. At  $t_3$ , the primary current of  $L_1$  and  $L_2$  increases while that of  $L_3$  decreases. The antiparallel diode of  $S_{c3}$  conducts. In this interval,  $L_1$  and  $L_3$  are in forward mode and  $L_2$  in flyback mode. The secondary windings of  $L_1$  and  $L_2$  are series connected to charge the output capacitor  $C_o$  through  $D_{o2}$  and  $D_{o3}$  and these of  $L_3$  and  $L_2$  are series connected to charge  $C_o$  through  $D_{o3}$  and  $D_{o6}$ . The secondary currents of  $L_1$ ,  $L_3$  and  $L_2$  are thus given by Eqs. 4,5 and 3, respectively.

$$i_{LK1} = i_{LK1(t_3)} - \frac{N}{L_{LK1}} \frac{V_{in} - V_{out}}{1-D} (t - t_3) \quad (4)$$

$$i_{LK3} = \frac{N}{L_{LK3}} \frac{V_{in} - V_{out}}{1-D} (t - t_3) \quad (5)$$

#### E. Stage 5

The clamp switch  $S_{c3}$  turns off at  $t_4$ . Then  $C_c$  is resonant with the leakage inductance of  $L_3$ . The voltage across  $S_{c3}$  increases from zero and ZVS is achieved on  $S_{c3}$ .  $S_3$  is turned on when its parasitic diode is on and  $S_3$  is on with ZVS. At  $t_4$ ,  $S_1$  turns off, and then its parasitic capacitor is charged from the magnetizing current of  $L_1$ . In this period, the switching voltage of  $S_1$  is clamped by  $C_c$ ;  $L_1$  and  $L_3$  are in forward mode; and  $L_2$  is in flyback mode. Furthermore, the second sides of  $L_1$  and  $L_2$  are series connected to charge  $C_o$  through  $D_{o2}$  and  $D_{o3}$  and these of  $L_2$  and  $L_3$  are also series connected to charge  $C_o$  through  $D_{o3}$  and  $D_{o6}$ .

\*\*\*\*\*

According to the voltage balance law,

$$DV_{PV} = (1-D)V_B \quad (1)$$

$$V_{ab} = N \frac{1-D}{D} V_B - N(-V_B) = \frac{NV_B}{D} \quad (2)$$

*State 3* [ $t_2$ - $t_3$ ]: At  $t_2$ ,  $S_2$  turns ON, which makes the two coupled inductors work in the Flyback state to store energy again, and  $D_{o2}$  is reverse-biased. The energy stored in  $C_{o1}$  and  $C_{o2}$  transfers to the load. At  $t_3$ , the leakage inductor current decreases to zero and diode  $D_{o1}$  turns off with zero-current switching operation.

(a) [ $t_0$ - $t_1$ ]

(b) [ $t_1$ - $t_2$ ]

(c) [ $t_2$ - $t_3$ ]

(d) [ $t_3$ - $t_4$ ]

Fig. 2 Four operating states of the proposed converter in mode 1.

*State 4* [ $t_3$ - $t_4$ ]: At  $t_3$ ,  $S_1$  turns OFF and  $S_3$  turns ON, which turns  $D_{o2}$  ON. The primary side of coupled inductor  $L_1$  charges the battery by  $S_3$ . During this state,  $L_2$  operates in the Forward mode and  $L_1$  operates in the Flyback mode to transfer energy to the load. When  $S_1$  turns ON and  $D_{o2}$  turns OFF, a new switching period begins.

In mode 2, the battery transfers energy to the load, as shown in Fig. 44(a). It indicates the nighttime operation of the standalone system. The circuit works as the Flyback-Forward converter, where  $S_3$  and  $S_4$  are the main switches,  $C_c$ ,  $S_1$  and  $S_2$  form an active clamp circuit. When the load is disconnected, the standalone system enters into mode 3. The PV array charges battery without energy transferred to the load due to the opposite series connected structure of coupled inductor, as shown in Fig. 4(b).  $S_1$  and  $S_2$  work simultaneously and the topology is equivalent to two paralleled buck-boost converters.

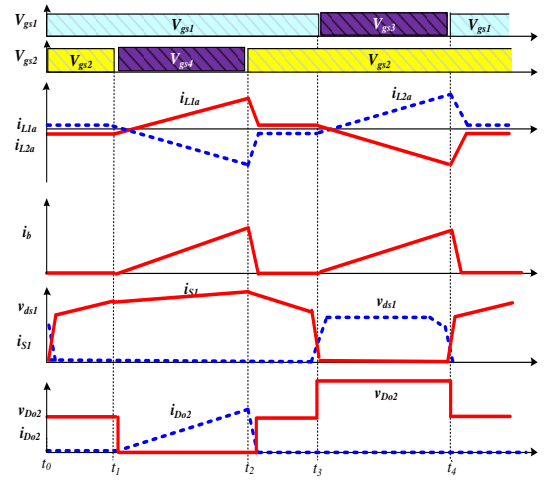


Fig. 3 Signal waveforms of the proposed converter under mode 1.

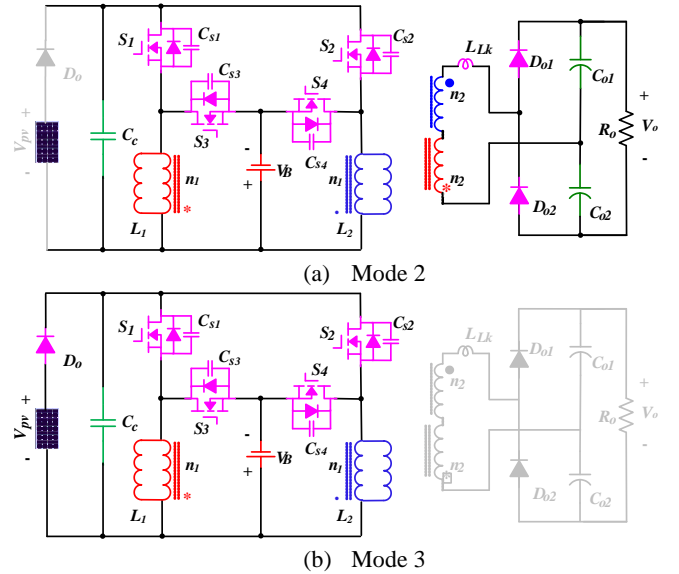


Fig. 4. Converter operating modes.

### III. PERFORMANCE ANALYSIS AND FEEDBACK LOOP DESIGN

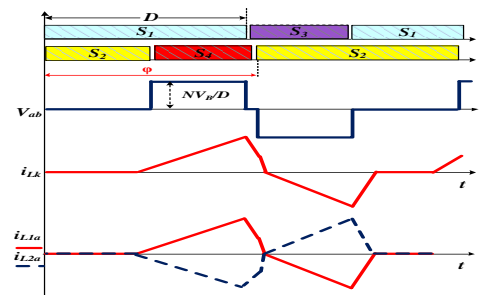
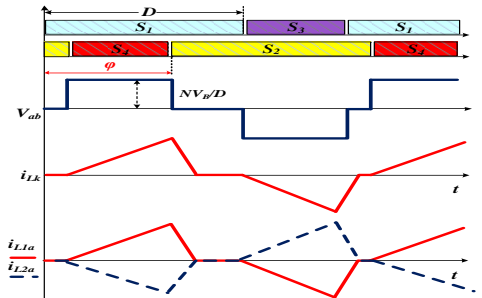
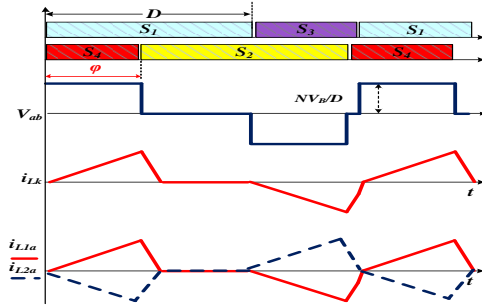
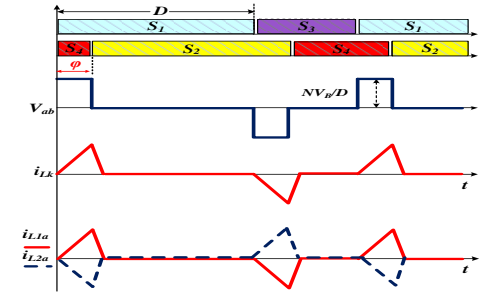
In order to realize flexible energy flow, the modulation strategy is proposed by combing PWM with PS. Firstly, the

relationship of voltage gains with duty ratio and FS needs to be researched. In the following analysis,  $S_1$  and  $S_2$  share the same duty ratio,  $D$ , meanwhile,  $S_3$  and  $S_4$  are applied to the same duty ratio. The gate signals for  $S_1$  and  $S_3$  are complementary, as well as for  $S_2$  and  $S_4$ .

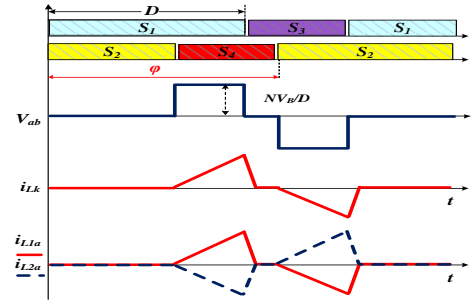
#### A. Analysis of Circuit Performance ( $D > 0.5$ )

When the duty cycle  $D > 0.5$ , there are five operating cases for analysis, as shown in Fig. 5.

In case 1, the phase shift angle is between  $0$  and  $\varphi_{crit1}$ . From the waveform of the leakage inductor current, the secondary side of the coupled inductor is equivalent to a discontinuous conduction mode (DCM) of a Buck converter. When  $\varphi = \varphi_{crit1}$ , the current pulses A and B is in a boundary conduction mode.



(d) Case 4



(e) Case 5

Fig. 5. Five operational cases for  $D > 0.5$ .

For pulse A, the current decreases to the minimum value and increases to zero during the time period of  $(1-D)T_s$ . The decrement time is equal to  $T_s \varphi_{crit1} / 2\pi$  and the increment time is  $(1-D - \varphi_{crit1} / 2\pi)T_s$ . Following the voltage-second balance (3), the critical phase angle can be determined in (4).

$$\frac{NV_B}{D} \cdot \frac{\varphi_{crit1}}{2\pi} \cdot T_s = \frac{V_o}{2} (1-D - \frac{\varphi_{crit1}}{2\pi}) T_s \quad (3)$$

$$\varphi_{crit1} = \pi \cdot D \cdot (1-D) \cdot \frac{V_{out}}{N \cdot V_B} \quad (4)$$

The secondary side of the coupled inductor is equivalent to two Buck converters connected in parallel at the DCM operational condition. The corresponding equivalent duty ratio of the buck converter is  $\varphi/2\pi$ . According to the equation of voltage gain of Buck converter in DCM, the output voltage can be expressed as:

$$V_o = 2 \cdot \frac{2}{1 + \sqrt{1 + \frac{4 \cdot 2L_k}{R_o \cdot T_s \cdot (\varphi/2\pi)^2 / 2}}} \cdot \frac{NV_B}{D} \quad (5)$$

In case 2, the phase shift angle is between  $\varphi_{crit1}$  and  $\varphi_{crit2}$ . The phase shift angle  $\varphi_{crit2}$  is the boundary point from continuous conduction mode (CCM) to DCM, which can be determined by (6). The voltage equation at  $\varphi_{crit1}$  and  $\varphi_{crit2}$  can be expressed as (7) and (8).

$$\varphi_{crit2} = \frac{4\pi \cdot (1-D)}{D} \cdot \frac{N \cdot V_B}{V_{out}} \quad (6)$$

$$\frac{NV_B}{DL_k} (1-D) = \frac{V_o}{2L_k} \frac{\varphi_{crit2}}{2\pi} \quad (7)$$

$$\frac{NV_B}{DL_k} \frac{\varphi_{crit1}}{2\pi} = \frac{V_o}{2L_k} (1-D) \quad (8)$$

In case 3, the PS angle ranges from  $\varphi_{crit2}$  to  $\varphi_{crit3}$ . The duty ratio of the secondary side equivalent Buck converter stays constant at the value of  $1-D$ , and the voltage gain stands the highest, therefore, the critical point,  $\varphi_{crit3}$ , and the corresponding voltage can be expressed as Eqs. 9 and 10. With the increase in PS angle, the voltage declines.  $\varphi_{crit3}$  is the boundary point between DCM and CCM. In this case, the output voltage cannot be controlled by PS angle, as shown in Eq.11.

$$\varphi_{crit3} = 2\pi - \varphi_{crit2} \quad (9)$$

$$\frac{NV_B/D}{L_k}(1-D) = \frac{V_o}{2L_k} \left(1 - \frac{\varphi_{crit3}}{2\pi}\right) \quad (10)$$

$$V_o = 2 \cdot \frac{2}{1 + \sqrt{1 + \frac{4 \cdot 2L_k}{R_o \cdot T_s \cdot (1-D)^2 / 2}}} \cdot \frac{NV_B}{D} \quad (11)$$

In case 4, the PS angle ranges from  $\varphi_{crit3}$  to  $\varphi_{crit4}$ . The leakage inductor current is still higher than zero before next voltage pulse.  $\varphi_{crit4}$  is the boundary point between DCM and CCM. The voltage gain stands as the highest, therefore, the critical point, the critical point, and the corresponding voltage can be expressed as Eqs. 12 and 13.

$$\varphi_{crit4} = 2\pi - \varphi_{crit1} \quad (12)$$

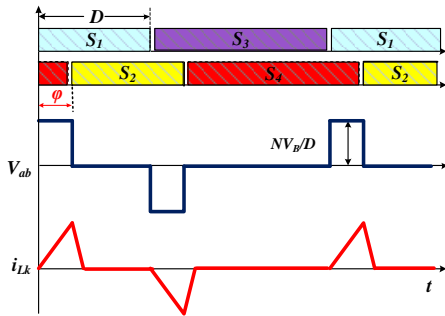
$$\frac{NV}{DL_k} \left(1 - \frac{\varphi_{crit4}}{2\pi}\right) = \frac{V_o}{2L_k} (1-D) \quad (13)$$

In case 5 ( $\varphi_{crit4} < \varphi < 2\pi$ ), the duty ratio of secondary side equivalent Buck converter is  $1 - \varphi/2\pi$ . The output voltage can be expressed as

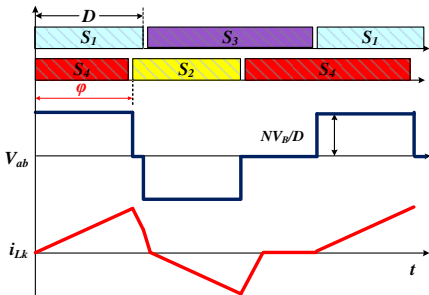
$$V_o = 2 \cdot \frac{2}{1 + \sqrt{1 + \frac{4 \cdot 2L_k}{R_o \cdot T_s \cdot (1 - \varphi/2\pi)^2 / 2}}} \cdot \frac{NV_B}{D} \quad (14)$$

### B. Analysis of Circuit Performance ( $D < 0.5$ )

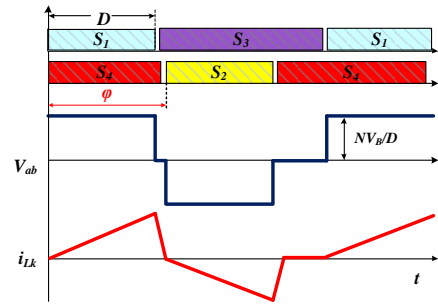
Similarly, there are five operating cases when the duty cycle  $D < 0.5$ . The respective waveforms are shown in Fig. 6.



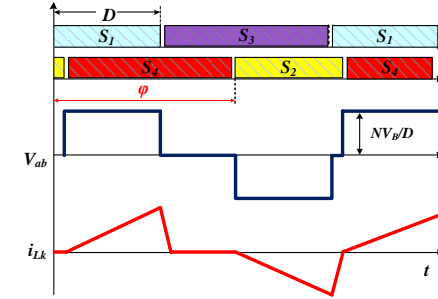
(a) Case 1



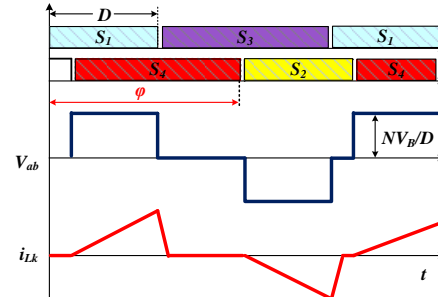
(b) Case 2



(c) Case 3



(d) Case 4



(e) Case 5

Fig. 6. Five operating cases under  $D < 0.5$ .

For case 1 ( $0 < \varphi < \varphi_{crit1}$ ), considering the waveform of the leakage inductor current, the secondary side of coupled inductor is equivalent to a DCM Buck converter, the corresponding duty ratio is  $D = \varphi/2\pi$ .

$$\varphi_{crit1} = \pi \cdot D^2 \cdot \frac{V_o}{N \cdot V_B} \quad (15)$$

$$V_o = 2 \cdot \frac{2}{1 + \sqrt{1 + \frac{4 \cdot 2L_k}{R_o \cdot T_s \cdot (\varphi/2\pi)^2 / 2}}} \cdot \frac{NV_B}{D} \quad (16)$$

In case 2 ( $\varphi_{crit1} < \varphi < \varphi_{crit2}$ ), the current of leakage inductor is still above zero before next pulse coming. The system equations can be expressed as

$$\varphi_{crit2} = 4\pi \cdot \frac{N \cdot V_B}{V_o} \quad (17)$$

$$\frac{NV_B}{DL_k} \cdot \frac{\varphi_{crit1}}{2\pi} = \frac{V_o}{2L_k} \cdot D \quad (18)$$

$$\frac{NV_B}{DL_k} \cdot D = \frac{V_o}{2L_k} \cdot \frac{\varphi_{crit2}}{2\pi} \quad (19)$$

In case 3 ( $\varphi_{crit2} < \varphi < \varphi_{crit3}$ ), the duty ratio of secondary winding equals to  $D$ . The system equations are

$$\varphi_{crit3} = 2\pi - \varphi_{crit2} \quad (20)$$

$$\frac{NV_B}{DL_k} \cdot D = \frac{V_o}{2L_k} \cdot \left(1 - \frac{\varphi_{crit3}}{2\pi}\right) \quad (21)$$

$$V_o = 2 \cdot \frac{2}{1 + \sqrt{1 + \frac{4 \cdot 2L_k}{R_o \cdot T_s \cdot D^2 / 2}}} \cdot \frac{NV_B}{D} \quad (22)$$

In case 4 ( $\varphi_{crit3} < \varphi < \varphi_{crit4}$ ), the current of leakage inductor is still above zero. The system equations can be expressed as

$$\varphi_{crit4} = 2\pi - \varphi_{crit1} \quad (23)$$

$$\frac{NV_B}{DL_k} \cdot \left(1 - \frac{\varphi_{crit4}}{2\pi}\right) = \frac{V_o}{2L_k} \cdot D \quad (24)$$

In case 5 ( $\varphi_{crit4} < \varphi < 2\pi$ ), the duty ratio of secondary winding can be expressed as  $1 - \varphi / 2\pi$ . The output voltage is

$$V_o = 2 \cdot \frac{2}{1 + \sqrt{1 + \frac{4 \cdot 2L_k}{R_o \cdot T_s \cdot (1 - \varphi / 2\pi)^2 / 2}}} \cdot \frac{NV_B}{D} \quad (25)$$

From the above analysis, the duty cycle  $D$  is the control variable to balance the PV voltage and battery voltage, and  $\varphi$  is employed to control secondary output voltage. The two-freedom control approach makes the solar energy, battery and load fully controllable. One condition should be applied to achieve decoupled control performance, which can be expressed as  $0 < \varphi < \varphi_{crit2}$  and  $\varphi_{crit3} < \varphi < 2\pi$ . If the condition is not satisfied, the secondary output voltage is determined by the switching duty cycle rather than the phase shift angle, as presented in Eqs. 11 and 22. In mode 1, the primary side is equivalent to an interleaved Buck-Boost, which operates in the continuous conduction mode due to the asymmetrical complementary operation of the switching devices ( $S_1, S_3$ ) and ( $S_2, S_4$ ), and the operation of the second side follows Buck converter, where the corresponding duty ratio can be controlled by phase shift angle except for case 3.

### C. Feedback Loop Design ( $D > 0.5$ )

In mode 1,  $S_1$  and  $S_3$  complementarily conduct, and the on/off operation of  $S_2$  and  $S_4$  is complementary. When the output energy of PV array is lower than the load power, the battery should supply the required energy to sustain output power. The primary side of the proposed converter can be equivalent to a bidirectional buck-boost converter, while the secondary side can be equivalent to a Buck converter in discontinuous conduction mode. The maximum power point tracking (MPPT) can be implemented by adjusting duty cycle of switching devices. The output voltage can be controlled by PS of the primary side bridge arm, which can be approximated to adjust the duty cycle of Buck converter of secondary side to realize output voltage regulation. The control block diagram of the proposed three-port converter for PV-battery hybrid power generation system is illustrated in Fig. 7.

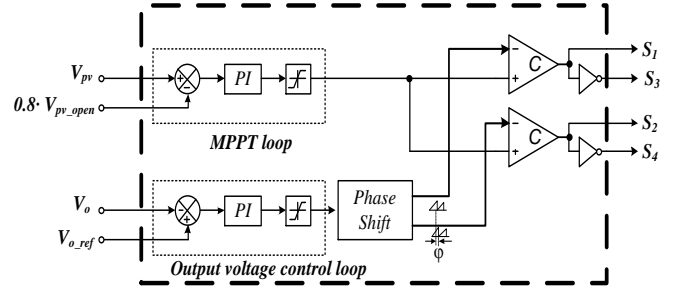


Fig. 7. Diagram of the proposed control scheme.

In the MPPT loop, the PV voltage can be regulated to follow the optimal operating point, which is initially assigned to 80% of the open circuit voltage of the PV array. The optimal operating point can be determined by the outer MPP Tracker, which has been broadly investigated in prior works [34]. The PV voltage regulation loop is an effective feature to improved MPPT performance as claimed in [35]. In the output voltage control loop in Fig. 7, the phase angle is the control variable. The phase angle of the carrier waveform for modulation is shifted to realize output voltage loop control. The mode can be switched smoothly by the proposed control method because of the block diode of PV input, mode 1 can be transferred to mode 2 by changing  $D > 0.5$  to  $D < 0.5$ , furthermore, the mode can be switched from 1 to 3 by controlling the phase shift angle between  $S_1$  and  $S_2$ .

## IV. SIMULATION AND EXPERIMENTAL RESULTS

Both simulation and experimental test are conducted to evaluation the proposed system and control scheme. The system parameters for evaluation are listed in Table I.

TABLE I  
PARAMETERS OF THE PROTOTYPE CONVERTER

Parameter	Product/Value
$D_{o1}$ - $D_{o2}$	BYW99W200
$S_1$ - $S_4$	FDP047AN
$N = n_1:n_2$	1:2
$C_c$	100V/100 $\mu$ F
Switching Frequency	20KHz
Battery voltage	12V
Load resistance	90 $\Omega$
$C_{o1}$ - $C_{o2}$	250V/470 $\mu$ F
Step-up ratio	6.25

### A. Simulation Results

Simulation is carried out in PSIM environment to establish the relationship of phase shift angle and output voltage, and to testify the proposed control strategy in MPPT and output voltage control.

Fig. presents the simulation results indicating the phase shift angle control and output voltage response at  $D > 0.5$  and  $D < 0.5$ . The voltage gain can be divided into five cases which coincide with the theoretical analysis. In case 1, 2, 4, and 5, the output voltage is controllable by the phase shift while in case 3, the output voltage cannot be controlled by phase angle, as in



Eqs. 11 and 22. When  $D < 0.5$ , the relation becomes more linear than that for  $D > 0.5$ .

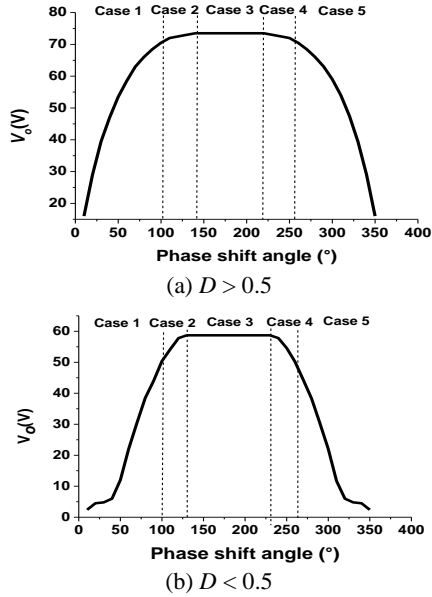


Fig. 8. Simulation results for phase shift angle control.

### B. Experimental Results

The proposed inverter topology and control scheme are implemented in a 250W prototype (see Fig. 9) with a Texas Instruments TMS320F28335 controller.

Experimental tests are conducted with a PV array simulator (Agilent Technology E4360A) to obtain the steady-state waveforms of the proposed converter in different operating cases. Fig. 10 illustrates waveforms of the input current ( $i_{in}$ ), battery current ( $i_B$ ) and the second side of the coupled inductor current ( $i_{LK}$ ), for the phase angle shift under different cases. Fig. 11 shows the regulation performance of the converter. Using the phase shift modulation, the output voltage is controlled at the constant 80V level. Meanwhile, the duty cycle control of PWM regulates the PV voltage at 12.8V, which represents the operating point of MPP of the PV array simulator.

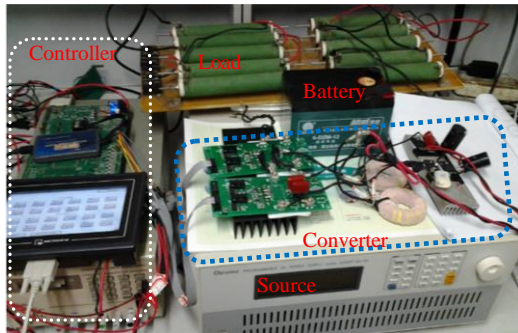


Fig. 9. Experimental setup of the proposed converter test system.

Modes 2-3 are also tested with the results presented in Figs. 12 and 13. Fig. 12 shows the current waveforms with the phase shift for different cases when  $D < 0.5$ . Under this condition, the battery discharges energy to the load and the blocking diode prevents the reverse current into the PV array. The converter

operation enters mode 2. In mode 3 (Fig. 13),  $S_1$  and  $S_2$  are applied with the same duty ratio without a phase shift angle. Therefore, the energy is transferred only from the PV array to the battery. The output voltage becomes zero due to the reverse series connection of the second side of the coupled inductor. Fig. 14 illustrates the measured converter efficiency. It can be seen that the maximum efficiency of this converter is 91.3% at 200W and the rated efficiency is approximately 90%.

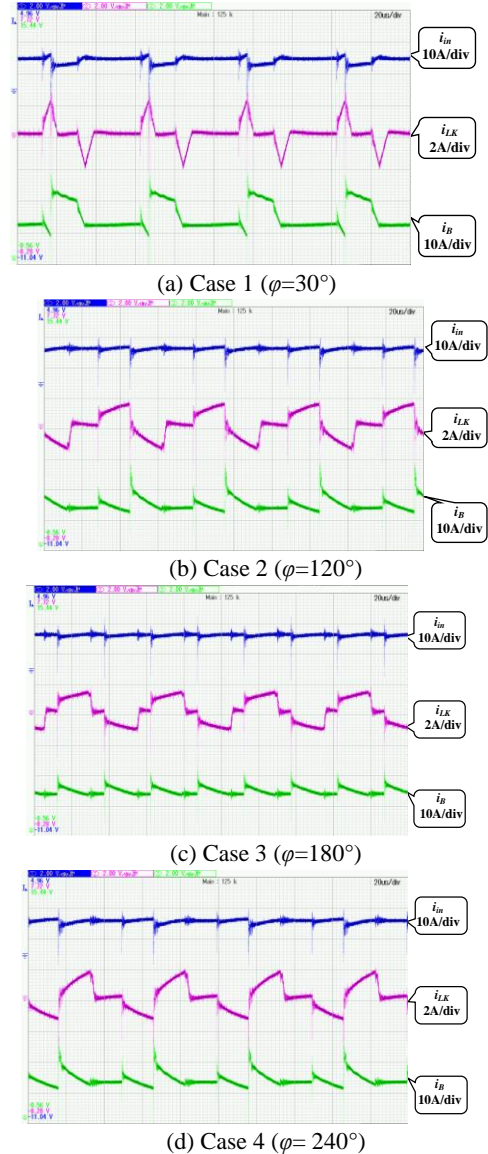
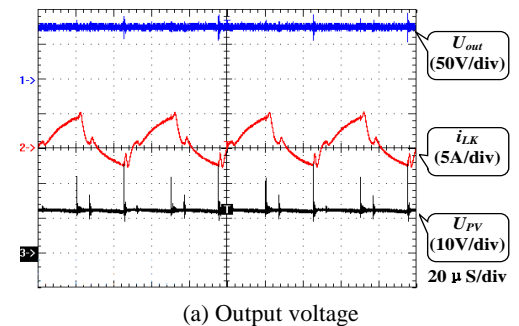


Fig. 10. Current waveforms for different cases ( $D > 0.5$  mode 1).



(a) Output voltage

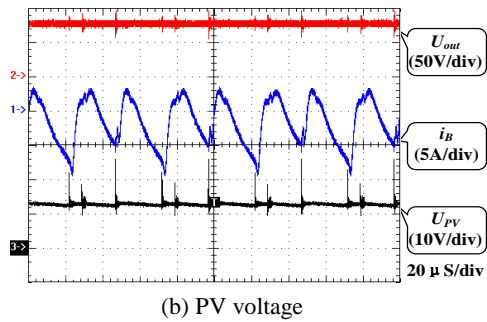


Fig. 11. Experiment results of voltage regulation performance.

## V. CONCLUSIONS

This paper has presented an isolated three-port DC-DC converter for standalone PV systems, based on an improved Flyback-Forward topology. The converter can provide a high

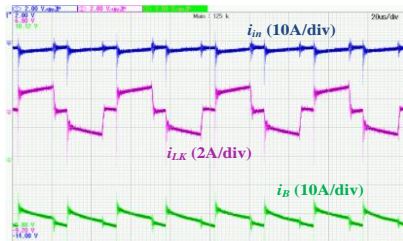
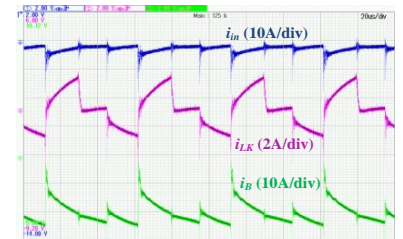
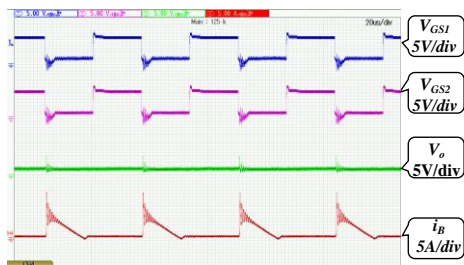

 Fig. 12. Current waveforms for different cases ( $D < 0.5$  mode 2).


Fig. 13. Steady-state waveforms under mode 3.

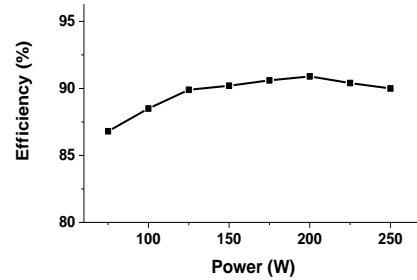


Fig. 14. Experimental results for the converter efficiency.

step-up capability interfacing the PV array, the battery storage, and the isolated consumption. Three operating modes are analyzed and have shown the effective operation of the proposed topology for PV applications.

From simulation and experimental test results, it can be seen that the output voltage and the PV voltage can be controlled independently by the phase shift and PWM respectively. The decouple control approach is a simple and effective way to achieve the regulation of output voltage and PV voltage, which is important for the MPPT operation of standalone PV power systems. In addition to developing simulation models, a 250W converter is prototyped and tested to verify the effectiveness of the proposed converter topology and control scheme.

The developed technology is capable of achieving MPPT, high conversion ratio and multiple operating modes whilst making the converter relatively simple, light, efficient and cost-effective.

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