Multi-Objective Design of IGBT Power Modules Considering Power Cycling and Thermal Cycling

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***Abstract*— Insulated gate bipolar transistor (IGBT) power modules find widespread use in numerous power conversion applications where their reliability is of significant concern. Standard IGBT modules are fabricated for general-purpose applications while little has been designed for bespoke applications. However, conventional design of IGBTs can be improved by the multi-objective optimization technique. This paper proposes a novel design method to consider die-attachment solder failures induced by short power cycling and baseplate solder fatigue induced by the thermal cycling which are among major failure mechanisms of IGBTs. Thermal resistance is calculated analytically and the plastic work design is obtained with a high-fidelity FE model, which has been validated experimentally. The objective of minimizing the plastic work and constrain functions is formulated by the surrogate model. The non-dominated sorting genetic algorithm-II (NSGA-II) is used to search for the Pareto optimal solutions and the best design. The result of this combination generates an effective approach to optimize the physical structure of power electronic modules, taking account of historical environmental and operational conditions in the field.**

***Index Terms*—Aging, fatigue, finite element methods, insulated gate bipolar transistors, multi-objective, optimization methods, power cycling, reliability, thermal cycling**

I. INTRODUCTION

POWER semiconductor devices are an enabling technology to convert energy between different forms. In the last two decades, they are playing an increasingly important role in safety-critical aerospace and automotive applications where stringent reliability constraints are placed on power electronic systems. As a result, there is a pressing need to improve power electronic systems by optimized design, advanced manufacturing and packaging, as well as system integration.

Insulated gate bipolar transistor (IGBT) power modules find widespread use in various applications including renewable energy, transport and space, industry, utility and home appliances. They have been manufactured in large quantities and have dominated a large portion of the medium- and high-power conversion market for decades. Field experience shows that power electronic converters were responsible for 37% of the unscheduled maintenance for photovoltaic (PV) generation systems [1], 13% for wind turbines [2] and 38% for industrial variable speed ac drives [3]. Their failures determine the system downtime and increase the operational cost [4][5]. Power semiconductor devices were rated as the most fragile component of a power electronic system from a recent industrial survey, followed by capacitors and gate drives [6]. The device and package-related failures account for 35% of the faults in the power electronics system [7]. The constantly growing need for power semiconductor devices coupled with important roles they have played in the system has led to corresponding reliability and robustness concerns, especially for safety-critical systems that may incur life security risks or enormous additional overall system operating cost (including maintenance, downtime, capital investment, etc).

In General, an IGBT module is comprised of one or more semiconductor chips and its package, which are equally important in providing high performance service. It is constructed with different materials (e.g. silicon, aluminum, copper, ceramics and plastics), package designs (e.g. layout, geometry and size) and properties (e.g. electrical, thermal and mechanical). These components/layers are mostly bonded together by soldering and bond wires (See Fig. 1). The assembly is then covered with an insulating gel and enclosed in a polymer housing from which only the metal connectors of the device terminals emerge. The base plate of the assembly is mounted onto a heat sink or other cooling devices with thermal interface material (TIM) greased between them for improved thermal contact.

Current, voltage, power dissipation and lifetime are the traditional design specifications, of IGBT power modules. In practice, they undergo harsh operational conditions (i.e. high temperature, frequent temperature cycles and intensive vibrations) that generate repetitive stresses leading to fatigue and wear-out failures, particularly at the interconnections between different layers. Numerous accelerated aging tests have been conducted by different researchers to evaluate wear-out failures [8]-[10]. The dominant wear-out mechanisms, for example bond wire lift-off, die-attach solder fatigue and baseplate solder fatigue, are mainly driven by thermo-mechanical stress that is induced by cyclic temperature swings and exposure to extreme temperatures.

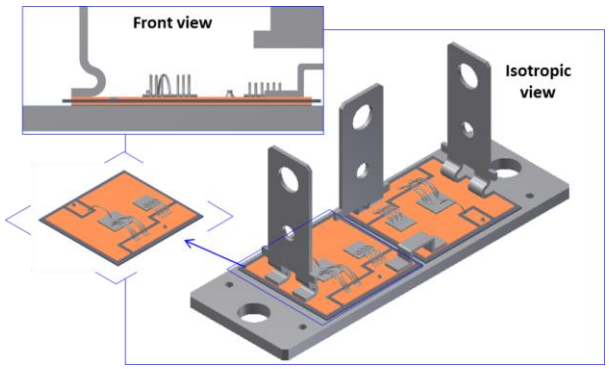

Fig. 1. typical multi-layered IGBT power module

The power dissipation path through the multilayered structure is constructed from different materials, characterized with individual coefficient of thermal expansion (CTE). Thermo-mechanical stress is generated in service at various layers and their interfaces under cyclic loadings. Power cycling (PC) and thermal cycling (TC) tests, as shown in Fig. 2, are the typical methods to evaluate the robustness and reliability [8]-[11]. The PC is exerted by the heat dissipation of power semiconductor devices when they are actively controlled. As the power loss requires finite time to conduct due to the thermal capacitance, each layer will be subject to different temperature swings dependent on the length of the dissipated power. PC can be further discriminated as short and long power cycling. Short power cycles are caused by the heat dissipation in relatively short intervals (e.g. a few seconds) that allow semiconductors and their direct vicinity undergoing frequent temperature changes with sizable amplitudes. However, the temperature variation in the distant baseplate solder layer is sufficiently alleviated by the large thermal capacities of substrate and baseplate. Short power cycling is mainly carried out to evaluate the lifetime of the bond wires and the die-attach solder layer [11]. Long power cycles normally indicate power pulses with long enough intervals (e.g. exceeding 10 seconds) to cause effective temperature swings and stresses in the baseplate solder layer. TC normally indicates the device temperature changes passively accompanying the ambient temperature variations. The focus of short PCT is normally the bond wire connections and the die attach solder while the baseplate solder fatigue is considered to be a dominant wear-out mechanism during long PC and TCT [11]. The device junction temperature was also factored in, showing accelerated wear-out with the raised temperature [8]. Moreover, the maximum junction temperature specified by the manufacturer (e.g. 150°C or 175°C for silicon devices) must not be exceeded under any conditions, since it may result in sudden failures such as hot spots and latch-up.

In order to achieve a robust design, numerous solutions to reduce the cyclic thermo-mechanical stress and junction temperature have been developed from all aspects, from design to in-field operation and from the system all the way down to the power semiconductor modules [12-17]. On the one hand, the thermal cycles are relieved with advanced structure design and optimized thermal management. The copper baseplate is replaced by AlSiC in some power modules to reduce the CTE mismatch between substrate and baseplate [18]. Active cooling methods were presented using coolant temperature as a feedback for flow control to reduce the temperature variation [19]. Generally, the temperature of the heat sink (either air or liquid cooled) can only be slowly regulated compared to the dynamic power loss variations from power modules due to its large thermal time constant. A thermal management technique is proposed to regulate the power losses with advanced gate control and PWM control algorithm [20]. On the other hand, methods to solve the junction temperature limitation have also been developed which fall into three categories – semiconductor, packaging and assembly, and thermal management algorithm. Semiconductor technological advancement has been observed over the past two decades thanks to the novel materials [21]-[23], improved fabrication technology[24] and optimized structures [25] that are able to sustain higher junction temperature. Advanced packaging and cooling designs have also been developed[26]-[28] to improve the thermal performance of the power assembly. The thermal conductivity of die attachment has been increased by about three times with enhanced electrical conductivity and mechanical properties [26] by replacing the solder alloy with sintered nanosilver paste. The techniques of integrating the cooling system into the power module by removing the base plate [26], or a more ambitious attempt to implement direct chip cooling [25][27], have been proposed to minimize the thermal resistance as well as the number of interconnections, thus reducing the number of potential sources of failure. The maximum temperature is also reduced with specific modulation strategies to minimize power losses [29].

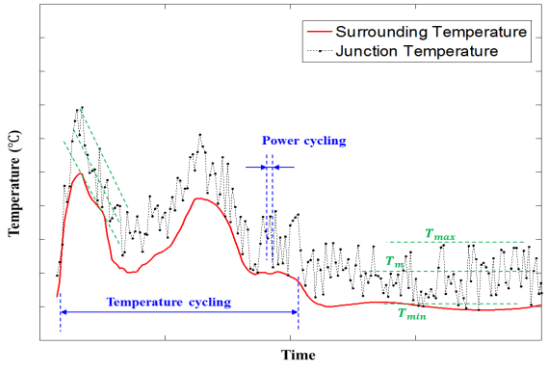

Fig. 2. Thermal cycling and Power cycling for IGBT module

Although advances in power module techniques have contributed to improved reliability and prolonged lifetime, there is little research on the optimization of IGBT modules [30][31]. Power modules are generally designed and manufactured to meet their typical operational and lifetime requirements. By following the engineering requirement (i.e. electrical, thermal, mechanical, cost, dimensions, etc.), it is typical to resolve the problem with a single-objective optimization target, i.e., maximizing the lifetime of IGBT modules under only one specific failure mode. In practice, an IGBT module is usually subjected to a combined fatigue loading such as power cycling, thermal cycling and vibration, and the requirements of the optimal design can be inconsistent or even conflicting with each other. This means that any further

lifetime improvement caused by addressing one fatigue mode can worsen the lifetime caused by other modes or increase the manufacturing complexity. For this reason, multi-objective optimization (MOO) strategy is desirable in the design of IGBT modules. In this paper, the objective is to explain why a MOO strategy is needed for IGBT power module design and to demonstrate the implementation of a MOO considering power cycling and thermal cycling in practice.

II. Multi-objective Optimization of IGBT Modules

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A common single-objective optimization problem of a power module is to maximize its lifetime:

$$\begin{cases} Max.: N_f \\ s.t.: X_L \le X \le X_U \end{cases} \tag{1}$$

where X is the matrix of design variables, X_U and X_L are the upper and lower bounds of X, respectively. N_f is the lifetime of the power module, which may be caused by one of the general failure modes, written in separate form as follows:

$$\begin{cases} Max.: {N_f}^d \otimes {N_f}^t \otimes {N_f}^p \otimes {N_f}^v \\ s.t.: X_L \le X \le X_U \end{cases} \tag{2}$$

where N_f^d is the lifetime of module due to material degradation [32], N_f^t is the lifetime of module due to the thermal cycling fatigue [33], N_f^p is the lifetime due to the power cycling fatigue [8] and N_f^v represents the lifetime due to the vibration fatigue [34]. The improvement of individual lifetime expectancy seems to be advantageous for the overall product lifetime. However, it does not necessarily increase the effective lifetime since different failure mechanisms are responsible for the four lifetime targets and they each play different roles in the aging process of power modules and require elaborated studies.

In terms of the thermal cycling fatigue mechanism, attempting to improve N_f^t requires thicker solder layers, thinner base plate and thinner ceramics layers to reduce the thermal stress induced by the mismatch of the CTE. And in terms of structural vibration theory, attempting to improve N_f^v requires all of the layers to be as thick as possible to reduce the static stress during vibration. On the contrary, attempting to improve the N_f^d and N_f^p demands most layers to be as thin as possible, since the junction temperature of the module as well as the resultant degradation will be alleviated with reduced total thermal resistance from the die to the base plate, as the failure and degradation is proportional to the junction temperature. Therefore, the lifetime optimization of power module needs considering the failure modes separately, as different failure modes need different treatment methods. In addition, as the price of modern lead-free solder goes up, minimizing the manufacturing cost (especially the material cost) becomes necessary as well. Therefore, the single-objective optimization needs to be transformed to a multi-objective optimization as shown below:

$$\begin{cases} Max.: [{N_f}^d, {N_f}^t, {N_f}^p, {N_f}^v] \\ s.t.: \begin{cases} X_L \le X \le X_U \\ N_f^i \ge N_{\min}^i \end{cases} \end{cases} \tag{3}$$

where, N_{min}^i means the required minimum lifetime of the module due to the *i*-th type of failure (material degradation, thermal cycling, powering cycling and vibration). Eq (3) can be solved as a single-objective optimization problem by retaining one objective while changing the other three objectives to constraints or by incorporating all the objectives into a single-objective by the use of arbitrary weighting factors. Such two types of approaches are easy to calculate and can provide quantitative insights into the sole objective, and restrict other constrains to some extent. However, most power module applications are rather sensitive to environmental and operational conditions, and it is thus difficult to select the most appropriate objective, define reasonable constraint levels or choose the most appropriate weighting factors. Consequently, conventional single-objective optimization is subject to a set of constraints which makes it impractical for the design optimization of power modules. As an alternative, introduction and application of a multi-objective optimization strategy becomes necessary to manage more information.

III. Lifetime Prediction Models

In this work, only two types of fatigue are taken into account: thermal cycling fatigue and power cycling fatigue.

A. Lifetime Prediction Model Subjected to Power Cycling

For the lifetime analysis due to the power cycling fatigue, there is a widely used analytical lifetime model, known as the power-law model [8]. The power-law model defines the relationship between the lifetime and the junction temperature of the power module, assuming that a small power cycle has the same effect on the lifetime irrespective of whether it occurred before or after a large temperature cycle, and is given as:

$$N_f^p = C_1 \cdot \left(\Delta T_j\right)^{C_2} \cdot e^{\frac{Q}{R \cdot T_m}} \tag{4}$$

where C_1 is a curve fitting constant of 640, exponent constant C_2 is approximately equal to -5, ΔT_j is the junction temperature, T_m is the mean temperature, Q is the activation energy of 7.8×10^4 J/mol, i.e. the smallest energy required to start the reaction, assumed to be independent of the temperature. R is the gas constant $8.314\ \mathrm{J/mol \cdot K}$ [8]. With this model, the lifetime due to the power cycling can be easily estimated. For a power module used in specific condition, ΔT_j and T_m can be described as

$$T_m = T_{\min} + \frac{1}{2}\Delta T_j \tag{5}$$

$$T_{\min} = T_{amb} + R_{th} \cdot P_{\min} \tag{6}$$

$$\Delta T_j = T_{\max} - T_{\min} = R_{th} \cdot \left(P_{\max} - P_{\min}\right) \tag{7}$$

Therefore, (4) can be transformed to

$$N_f^p = C_1 \cdot \left((P_{\max} - P_{\min}) \cdot R_{th}\right)^{C_2} \cdot \exp\left(\frac{Q}{R \cdot \left(T_{amb} + \frac{1}{2}(P_{\max} - P_{\min}) \cdot R_{th}\right)}\right) \quad (8)$$

For a specific power module under complex conditions, P_{max} and P_{min} are difficult to evaluate and thus the lifetime is impossible to predict. However, if the P_{max} and P_{min} are assumed to be known, for example, for a typical power electronic module with $R_{th} = 0.1K/W$ and undergoing a recorded temperature difference $\Delta T_j = 30℃$, the power loss difference ΔP is equal to $\frac{\Delta T_j}{R_{th}} = 300W$. Therefore the lifetime will be easily obtained, as N_f^p is then only related to the total thermal resistance R_{th}, which can be calculated as

$$R_{th} = \sum_{i=1}^{n=6} \frac{t_i}{k_i A_i} + \sum_{j=1}^{m=2} R_j^{sp} \quad (9)$$

where t_i, k_i, and A_i are the thickness, thermal conductivity, and the effective area of the i^{th} layer, respectively. R_j^{sp} is the j-th spreading thermal resistance, which can be approximately calculated as follows [35]:

$$R_j^{sp} = \frac{\Psi_{\max}}{k_j \cdot r_j \cdot \sqrt{\pi}} \quad (10)$$

where $\Psi_{\max}$ is the dimensionless constriction resistance, k_j is the thermal conductivity of the j-th layer, r_j is the source radius of the j-th layer. See Fig. 3.

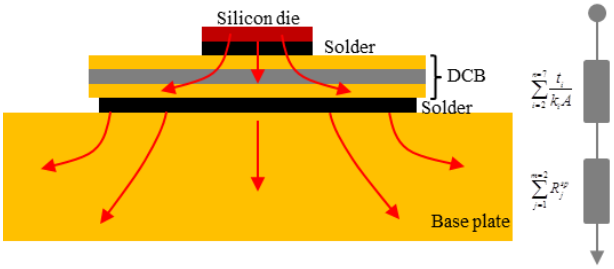


Fig. 3 Conductive and spreading thermal resistance in IGBT module

B. Lifetime Prediction Model Subjected to Thermal Cycling

As the real IGBT module test subjected to thermal cycling is very time consuming and costly, finite element analysis (FEA) is widely accepted in analyzing the failure mechanisms and predicting lifetime of the module especially during the design stage. The FE method provides a valuable insight into evolution characteristics of internal states in the solder joint and low cycle fatigue deformation and failure prediction of the solder [36]. Modeling an IGBT module subjected to thermal cycling involves five aspects: the life prediction model, the constitutive model, the material property, the finite element model and the thermal loading. These main steps form the basis of lifetime prediction of IGBT module subjected to thermal cycling.

1) Lifetime prediction model

Baseplate solder fatigue is the dominant failure mechanism under thermal cycling of the IGBT module. There exist many lifetime prediction models for determining the lifetime of solder layer in power modules and other types of electronic packages, in accordance to their own merits [37]. One of the widely accepted failure criteria was introduced by Darveaux for low cycle thermal fatigue life prediction [38]. This model describes the relationship between the volume-averaged inelastic work density increment ΔW, and the number of cycles to crack initiation N_0 and the crack propagation rate da/dN.

$$N_0 = K_1 \Delta W^{K_2} \quad (11)$$

$$\frac{da}{dN} = K_3 \Delta W^{K_4} \quad (12)$$

where K_1, K_2, K_3, K_4 are the empirical constants as shown in Table I and a is the characteristic crack length. So the characteristic lifetime N_f^t can be obtained as

$$N_f^t = N_0 + \frac{a}{da/dN} \quad (13)$$

The parameter ΔW is defined as:

$$\Delta W = \frac{\sum_{i=1}^{n} \Delta W_i \cdot V_n}{\sum_{i=1}^{n} V_n} \quad (14)$$

where ΔW_i designates the inelastic work density in the i^{th} element in FEA, whose volume is denoted by V_n.

TABLE I. EMPIRICAL CONSTANTS USED FOR LIFETIME PREDICTION [38]

constant	K_1	K_2	K_3	K_4
Value	71000 cycles/psi^{K_2}	-1.62	2.76× 10^{-7} in./cycles/psi^{K_4}	1.05

2) Constitutive model

To accurately calculate ΔW in (14), a high-fidelity finite element model with a precise description of the solder behavior is extremely critical. Therefore, the time- and temperature-dependent deformation behavior of the solder is one of the most important properties in the FEA. Among the various time-dependent and temperature-dependent constitutive models for solder in power modules, the viscoplastic constitutive model introduced by Anand is frequently adopted. The Anand model was originally developed for metal forming applications and quickly became popular to applications that involve strain and temperature effect including solder layer and high temperature creep. The model does not require an explicit yield condition and loading /unloading criteria because it assumes that plastic flow occurs at all non-zero stress values [39].

The Anand model consists of two coupled differential equations that relate the inelastic strain rate to the rate of deformation resistance. The strain rate equation is

$$\dot{\varepsilon}_P = A\left[\sinh\left(\frac{\xi\sigma}{s}\right)\right]^{\frac{1}{m}} e^{-Q/RT} \quad (15)$$

where $\dot{\varepsilon}_P$ is the inelastic strain rate, A is a constant, ξ is the stress multiplier, σ is the stress, s is the deformation resistance,

R is the gas constant, m is the strain rate sensitivity, Q is the activation energy and T is absolute temperature. And the rate of deformation resistance equation is

$$\dot{s} = \left\{ h_0 \left(|B| \right)^{\alpha} \frac{B}{|B|} \right\} \dot{\varepsilon}_P \tag{16}$$

where

$$B = 1 - \frac{s}{s^*} \tag{17}$$

$$s^* = \hat{s} \left[\frac{1}{A} \dot{\varepsilon}_P e^{-Q/RT} \right]^n \tag{18}$$

where s* is the saturation value of s, $\hat{S}$ is the coefficient for deformation resistance saturation value and n is the strain rate sensitivity. From the development of the above equations there are 9 material parameters that need to be defined in the Anand model. Table II shows these parameters for SAC305 alloy used in this work.

TABLE II. PARAMETERS OF SAC305 IN THE ANAND MODEL [40]

Parameter (unit)	Description	Values for SAC305
so (MPa)	Initial value of deformation resistance	1.0665×10^{6}
Q/R (1/K)	Activation energy/Boltzmann's constant	10.4133×10^{3}
A (1/s)	Pre-exponential factor	8.265×10^{7}
ξ (dimensionless)	Stress multiplier	2.55
m (dimensionless)	Strain rate sensitivity of stress	0.141446
h_0(MPa)	Hardening/softening constant	5023.9×10^{6}
$\hat{s}$(MPa)	Coefficient for saturation value of deformation resistance	20.2976×10^{6}
n (dimensionless)	Strain rate sensitivity of the saturation value	3.2472×10^{-2}
a (dimensionless)	Strain rate sensitivity of the hardening/softening	1.120371

3) *Material properties*

The IGBT module consists of a total of seven layers of materials. The solder layers are modelled with linear elastic coupled with viscoplastic material properties. The rest including the silicon die, the two copper layers, along with the ceramic layer and the base plate are assumed to be linear elastic in the FEAs. Table III shows the material properties of the seven layers from top to bottom.

TABLE III. MATERIAL PROPERTIES OF LAYERS FROM TOP TO BOTTOM

Layer/Material	ρ (kg/m^3)	E (MPa)	v	CTE (10^{-6}/K)	k (W/(mK))	σ_{allow} (MPa)
Silicon die	2,328	113,000	0.28	3	90	107
Solder (SAC305)	7,400	47	0.4	20	40	-
DCB copper	8,900	115,000	0.34	17	380	140
Ceramic (Al_2O_3)	3,900	370,000	0.22	6.3	20	55
DCB copper	8,900	115,000	0.34	17	380	140
Solder (SAC305)	7,400	47	0.4	20	40	-
Copper of baseplate	8,900	115,000	0.34	17	380	140

4) *Thermal cycling load*

The choice of thermal loads to evaluate the reliability of the IGBT module is important as the relative performance of the solders could change with the thermal load parameters such as maximum temperature and temperature range. This FEA was carried out using a typical thermal cycle as shown in Fig. 4, which includes beginning temperature, reference temperature, maximum temperature of 125℃, minimum temperature of -40℃, as well as the duration for ramp-up, ramp down, and dwell at the maximum and minimum temperatures. The beginning temperature as well as the reference temperature is assumed to be 25℃, since any residual stress in solder will relax due to the creep characteristic of the solder [41] and there is a good agreement between the FEAs and experiments by starting the simulation at reference temperature of 25℃ [42]. Each Dwell takes 15 minutes, which is same as the ramp up/down with ramp rate of $10℃/min$, so one thermal cycle lasts 60 minutes. Four thermal cycles in the simulation are usually sufficient to ensure the stability of the hysteresis loop and test semiconductors in automotive applications [43].

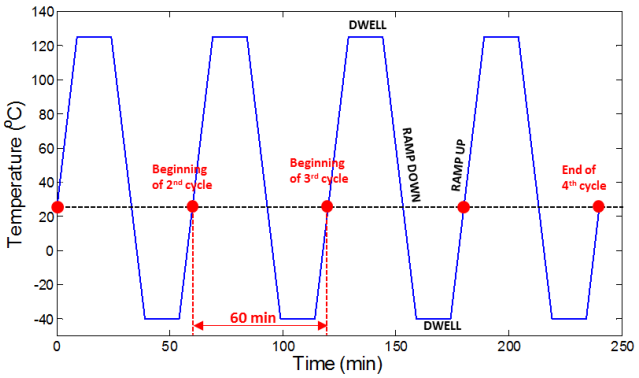


Fig. 4 Thermal cycles for fatigue analysis

5) *Finite element model*

The FE model in this work was conducted in Ansys 14.5, where the Ansys Parametric Design Language (APDL) was used to develop a generic model with a robust mesh, despite the variation of various design. To reduce the computational time and resources used, a two-dimensional (2-D) symmetrical FE model with one IGBT die was used as shown in Fig. 5 [44], which has been verified to be as accurate as a 3-D FE model for fatigue analysis of solder joints subject to thermal cycling [45]. The layers from 0 to 6 in Fig, 5 represent the silicon die, solder, DCB copper, Ceramic, DCB copper, solder and baseplate layers, respectively. VISCO106 element type with 4 nodes was used to model the solder layers because of its highly nonlinear behavior, and Plane 182 element type was used to model other linear elastic layers. Fig. 5(b) and (c) show the enlarged view of the FE model. It can be seen that fine mesh pattern is maintained in the model especially in the solder layer as the value of ΔW is dependent on the thickness s of the elements

[46]. In particular, the maximum element thickness of the solder layers is 17.5μm which are adequately accurate for the calculation of ΔW [38]. In total, 15405 nodes and 15040 elements have been generated for the model. Some assumptions are also made in the model, namely all seven layers are assumed homogenous, the process variations along with the manufacturing defect are not taken into account, and the inter-metallic growth in the solder layers is ignored.

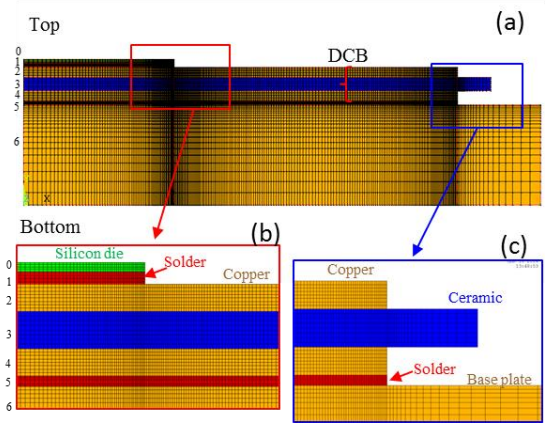


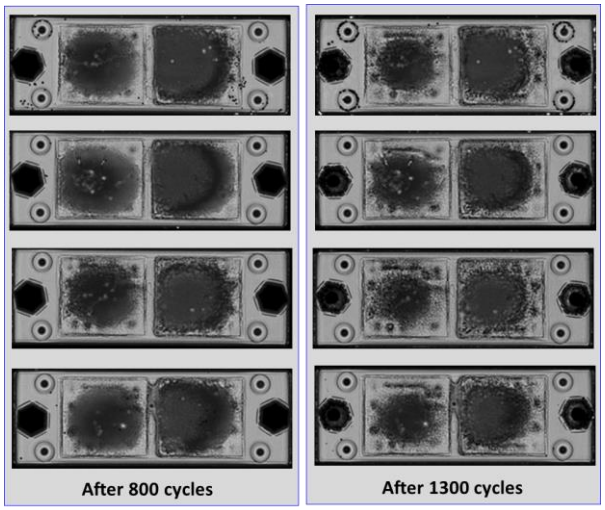
Fig. 5 2-D symmetrical FE model of multi-layered IGBT module

6) Experimental validation of FE models

The FE model was validated with thermal cycling test results prior to the MOO process. To accelerate the aging process of IGBT modules, a harsh thermal cycling profile was applied with the maximum and minimum temperature set to be 160℃ and −50℃, respectively. The ramp up/down time was set to be 2 min with the dwell time set to be 10 min. The thermal cycling test was interrupted at 800 and 1300 cycles for inspection. Fig. 6 shows the degradation of the solder layer between the DCB substrate and the base plate with a C-mode scanning acoustic microscope (SAM) from the bottom view as shown in Fig. 7. These figures clearly show that the failure initiates around the solder edges and propagates inwards to the centre.

Fig. 8 compares the lifetime vs. remaining area ratio between the experiments and the corresponding FEAs. The FEA results are in a good agreement with experiments, which demonstrates that the developed FE model as well as the lifetime prediction model are adequately accurate for the lifetime prediction of the IGBT module and proper for the subsequent design optimization.

The solder layers deform plastically when subjected to temperature cycling loads. The CTE mismatch of the different bonded materials induces thermo-mechanical stresses in the module which is critical at the interfaces of the assembled layers. Fig. 9 presents the stress and plastic strain contour of the IGBT module at the end of the 4th thermal cycle. The deformation in Fig. 9 is scaled up by 20 times to better illustrate the bending of each layer. As shown in Fig. 9(a), the maximum elastic stress of 54.07MPa occurs at the central interface of the ceramic layer and the copper layer, which is attributed to the mismatch in length of different layers. Silicon die and base plate also suffer evident stress of 49.06 MPa and 41.82 MPa, respectively.



(a) (b)

Fig. 6 Remaining effective solder areas in % observed by the SAM (a)after 800 cycles (b) after 1300 cycles

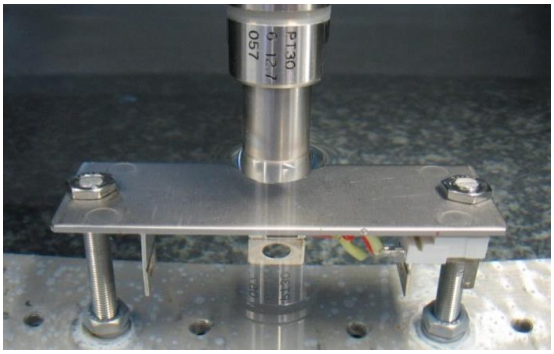


Fig. 7 C-mode SAM detection of IGBT modules

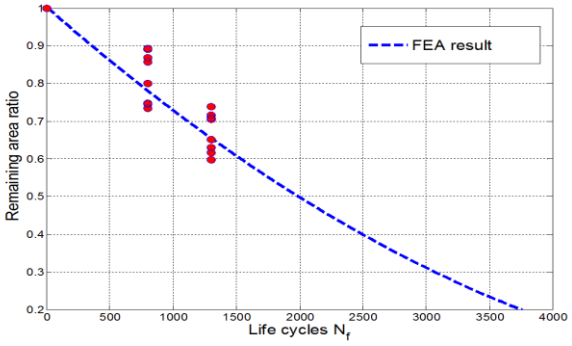


Fig. 8 Comparison of life cycles between FEAs and experiments

As shown in Fig. 9(b)-(d), the maximum plastic strain is located at the baseplate solder layer near the edge. The plastic strain in the first solder layer is modest compared with that of the baseplate solder layer, which is in agreement with the experimental result. It should be noted that the plastic work is only the output of viscoplastic elements, thus in the figures only solder layers are seen with plastic work and the rest corresponds to zero plastic work masked in blue. Fig. 10 plots the change of the strain energy density at the outmost node of the two solder layers over the four thermal cycles. The curve shows that strain energy density increases during the dwell period though the change is relatively small compared with that during the ramp up/down period. This is because the creep

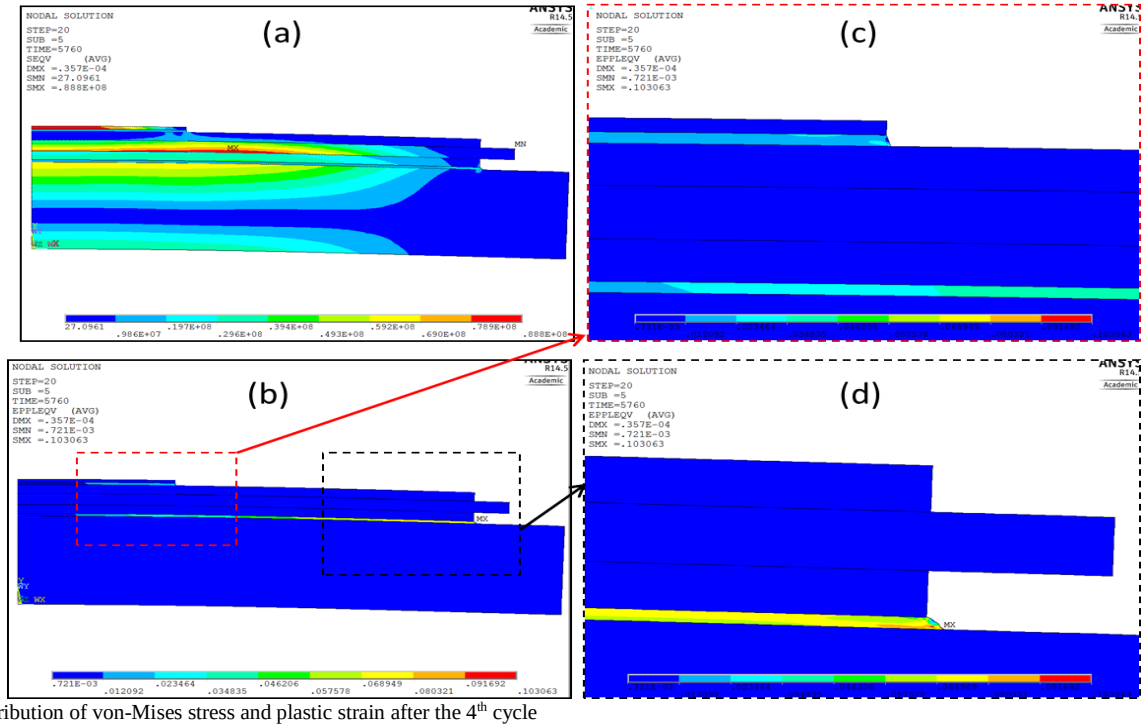


Fig. 9. Distribution of von-Mises stress and plastic strain after the 4th cycle

phenomenon exists during the dwell period and its effect is included in the plastic strain in Anand model.

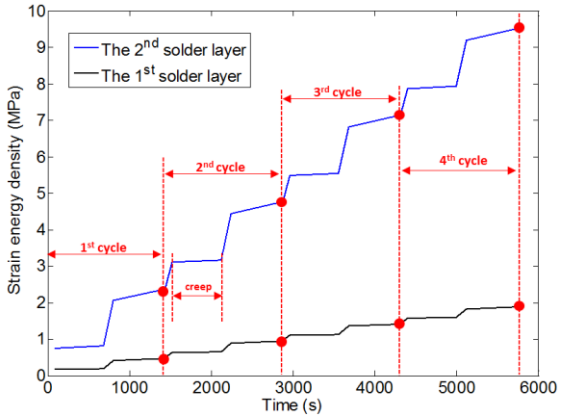


Fig. 10. Strain energy density histories of the two solder layers during thermal cycling

IV. Problem Definition

The objective of this work is to improve the lifetime of the module subject to both power cycling and thermal cycling by varying the thickness of the six layers. Therefore the objective functions can be expressed as

$$objective: \begin{cases} Maximize \ N_f^t(\mathbf{t}) \\ Maximize \ N_f^p(\mathbf{t}) \end{cases} \tag{19}$$

As mentioned above, for a specific power module used in specific conditions, N_f^p is a function of total thermal resistance R_{th}. The smaller R_{th} is, the larger N_f^p is. For the lifetime subject to thermal cycling N_f^t, it is beneficial to decrease ΔW as much as possible to increase N_f^t. Therefore, to reduce the equation transform, the objective function can be altered to

$$objective: \begin{cases} Minimize \ \Delta W_{solder2} \\ Minimize \ R_{th} \end{cases} \tag{20}$$

Since there are other elastic layers in the module, the reliability of these layers under the repeated thermal loads is mandatory as well. Therefore, five constraints are defined as shown below.

$$s.t.: \begin{cases} \sigma^i \le \sigma_{allow}^i \\ \Delta W_{solder1} \le \eta \cdot \Delta W_{solder2} \end{cases} \tag{21}$$

where σ^i and σ_{allow}^i are the maximum von-Mises stress and the allowed stress of the i^{th} elastic layer, respectively. $\Delta W_{solder1}$ and $\Delta W_{solder2}$ are the inelastic work density in the die-attach and baseplate solder layers, respectively, and η is a constant ensuring less inelastic work density (i.e. longer life) of the former compared to the latter. As the width of the die-attach solder layer and baseplate layer are 9mm and 26mm, resulting in a ratio of $9/26 \approx 0.35$, η is set to be 0.25 in this work to ensure a high reliability. It should be noted that total 4 layers from the silicon die to the base plate excluding these two solder layers have the elastic stress constraints as shown in Table I. The six design variables are the thickness of the six layers excluding the silicon die which is considered fixed. The layer thicknesses have constraints in terms of upper and lower limits which the variables can take. Specifically, the lower bound in Table IV is defined in terms of a commercially available power module in which the thickness of solder layers is the thinnest thickness the company can manufacture, and the upper bound is specified by the authors to make a reasonable search domain for the optimization.

TABLE IV. DESIGN SPACE FOR THE 6 DESIGN VARIABLES FROM TOP TO BOTTOM (UNIT: MM)

	t_1	t_2	t_3	t_4	t_5	t_6
Upper bound	0.15	0.4	0.46	0.4	0.2	4
Lower bound	0.08	0.2	0.36	0.2	0.08	2

V. Surrogate Based Multi-objective Optimization

During the optimization process, ΔW and R_{th} are iteratively calculated in terms of the possible combination of the six design variables. The calculation of R_{th} is easy and fast because the analytical solution in (11) and (12) is straightforward. However, the calculation of each ΔW and σ^i is more difficult and costly, penalizing optimization searches as it requires a costly and lengthy non-linear FEA. Hence, an efficient optimization method is essential for the optimization using finite element model. In this work, the surrogate based multi-objective optimization (SBMOO) is adopted, whose goal is to reduce computational iterations while obtaining desirable results. The SBMOO consists of an interpolation function developed based on a design of experiments (DoE) and multi-objective optimization (MOO) algorithm for a Pareto-optimal search. The entire workflow is illustrated in Fig. 11 and consists of the following steps.

1. Define objectives, constraints, design variables and design space for the optimization;
2. Produce the DoE using Latin Hypercube sampling method;
3. Calculate ΔW and σ^i at each design points with the FE model;
4. Build surrogate model for the objective and constrains (Kriging model);
5. Minimize errors of the surrogate models;
6. Output the surrogate models for the thermal cycling along with the analytical model for the power cycling;
7. Perform multi-objective optimization using MOO algorithm (NSGA-II);
8. Select optimal candidates and plot results.

A. *Kriging Surrogate Model [47][48]*

This work uses a widely used surrogate models, namely a Kriging (KRG) model to evaluate the approximation models of the objective and constraint functions for the thermal cycling. Kriging model was originally developed for mining and geostatistical application involving spatially and temporally correlated data.

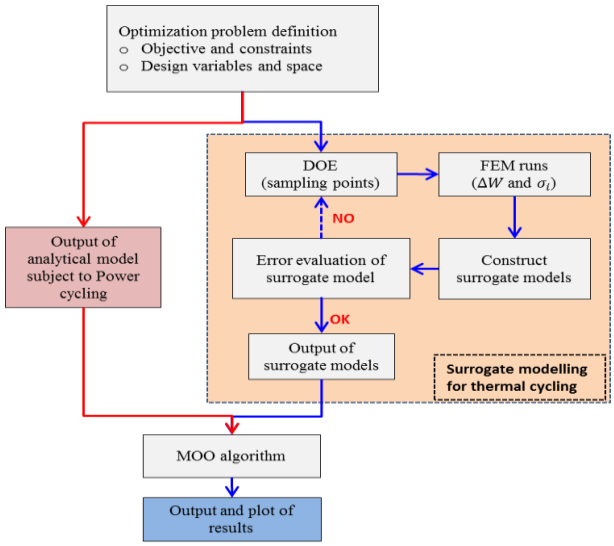


Fig. 11 Structure of SBMOO algorithm for IGBT module optimization

In general, the Kriging model combines a global model plus a localized departure, and can be formulated as:

$$f(x)=\beta+z(\mathbf{x}) \tag{22}$$

where f(x) is the unknown function of interest, β denotes a known approximation function (usually polynomial), and z(x) stands for a stochastic component in terms of zero mean and variance s^2 with the Gaussian distribution. Letting $\hat{f}(\mathbf{x})$ be an approximation function to the true function f(x), by minimizing the mean squared error between f(x) and $\hat{f}(\mathbf{x})$, $\hat{f}(\mathbf{x})$ can be calculated as

$$\hat{f}(\mathbf{x})=\hat{\beta}+\mathbf{r}^{\mathbf{T}}(\mathbf{x})\mathbf{R}^{-1}(\mathbf{f}-\hat{\beta}\mathbf{q}) \tag{23}$$

where R^{-1} is the inverse of correlation matrix R, r is the correlation vector, f is the observed data at n_s sample points, and $\mathbf{q}$ is the unity vector with n_s components. The random variables are correlated to each other using the basis function of

$$R(\mathbf{x}^j,\mathbf{x}^k)=Exp\left[-\sum_{i=1}^{m}\theta_i\left|x_i^{\,j}-x_i^{\,k}\right|^2\right],\ (j=1,\cdots,n_s,\ k=1,\cdots,n_s) \tag{24}$$

where θ_i is the i^{th} parameter corresponding to the i-th variable. The Kriging model is built with an assumption that there is no error in f; the likelihood can therefore be expressed in terms of the sampling data as

$$L=\frac{1}{(2\pi s^2)^{n/2}|\mathbf{R}|^{1/2}}\exp\left[-\frac{(\mathbf{f}-\beta\mathbf{q})^{\mathrm{T}}\mathbf{R}^{-1}(\mathbf{f}-\beta\mathbf{q})}{2s^2}\right] \tag{25}$$

To simplify the maximization of likelihood, (25) can be replaced by (26) by taking a natural logarithmic transformation as

$$\ln(L)=-\frac{n}{2}\ln(2\pi)-\frac{n}{2}\ln(s^2)-\frac{1}{2}\ln|\mathbf{R}|-\frac{(\mathbf{f}-\beta\mathbf{q})^{\mathrm{T}}\mathbf{R}^{-1}(\mathbf{f}-\beta\mathbf{q})}{2s^2} \tag{26}$$

By conducting the derivatives of the ln-likelihood function in (26) with respect to β and s, respectively, and setting them to zero, the maximum likelihood estimators (MLEs) of β and s^2 are determined in (27) and (28), respectively,

$$\hat{\beta}=(\mathbf{q}^{\mathrm{T}}\mathbf{R}^{-1}\mathbf{q})^{-1}\mathbf{q}\mathbf{R}^{-1}\mathbf{f} \tag{27}$$

$$\hat{s}^2=\frac{(\mathbf{f}-\hat{\beta}\mathbf{q})^{\mathrm{T}}\mathbf{R}^{-1}(\mathbf{f}-\hat{\beta}\mathbf{q})}{n_s} \tag{28}$$

These MLEs can now be substituted back into (26) by removing the constant terms to give what is known as the concentrated ln-likelihood function, and the unknown parameters of θ_i ($\theta_i > 0$) can be calculated by maximizing the formula as follows

$$maximize\quad -\frac{n_s}{2}\ln(\hat{s}^2)-\frac{1}{2}\ln|\mathbf{R}| \tag{29}$$

In this study, the method of modified feasible direction is utilized to determine the optimum values of parameter θ_i. And the estimated mean squared error (MSE) of the predictor is derived as (30).

$$\hat{e}^2=\hat{s}^2\left[1-\mathbf{r}^{\mathrm{T}}\mathbf{R}^{-1}\mathrm{r}+\left[\frac{(1-\mathbf{q}^{\mathrm{T}}\mathbf{R}^{-1}\mathbf{r})^2}{\mathbf{q}^{\mathrm{T}}\mathbf{R}^{-1}\mathbf{q}}\right]\right] \tag{30}$$

B. *Non-dominated Sorting Genetic Algorithm II (NSGA-II)*

Genetic algorithms are a form of search heuristic which takes

inspiration from natural evolutionary processes to identify optimal solutions to the problem being addressed. A solution exists in two domains, namely the solution space as well as objective space. In the former domain, a solution is described by its characteristics in terms of the variables, i.e. the various layer thicknesses. This takes this form of a string of code where each element defines the thickness of one layer. In keeping with the biological analogy, this string is termed a chromosome. Each solution is also associated with its value in objective space, i.e. the resultant ΔW and R_{th} for each chromosome. The set of chromosomes is termed a population, and by considering the correlation between a chromosome's location in population space and its location in objective space (fitness), a search can be steered towards locating better solutions.

The optimization process is an iterative one, whereby new chromosomes are created, evaluated in objective space, and in turn used to help identify better solutions to create a new generation. This is done by randomly selecting solutions, ranking according to fitness and mixing elements between chromosomes in order to generate offspring solutions. This process is repeated for a preset number of generations (or until a predetermined accuracy is reached) [49]. The definition of a 'better' solution is slightly different in the case of multiple objectives, and is handled by the concept of Pareto-dominance.

A solution is said to Pareto-dominate another, if and only if it is strictly better in all objectives. If a solution is only worse off in one objective, but better in another, then the two solutions form a Pareto-front, giving a set of equally optimum, compromise solutions. The final solution is then chosen from this Pareto-set [50].

A popular genetic algorithm which handles multiple objectives using the concept of Pareto dominance is the Non-dominated Sorting Genetic Algorithm II (NSGA-II) which is able to handle constraints as well as requiring a minimum amount of external parameters [51]. This makes it suited for robustly handling a range of different problems. The pseudo code for the NSGA-II is given below:

1. Create initial random population of size N;
2. Evaluate ΔW and R_{th} for each solution;
3. Use binary tournament selection, recombination and mutation operators to create offspring population of N;
4. Sort combined parent and offspring population (of size 2N) into Pareto ranks using fast non-dominated sorting;
5. Create new generation population by selecting the first N population members;
6. Repeat from step 3.

Constraints are handled in the selection operation, where chromosomes are selected for reproduction based on their Pareto-fitness. If both are in the same rank, a solution which does not violate the constraints is selected, and if both solutions are infeasible then the one with the least degree of constrain violation is selected. Finally if both are feasible and do not dominate each other, then the solution in the least crowded region of objective space is selected in order to focus the search towards sparser regions [51].

The above process is repeated for a set number of iterations and finally gives a set of Pareto-optimal solutions. The diversity operator ensures that the solutions are spread out in order to explore all areas of the search space to ensure better location of a global (as opposed to local) optimum.

VI. Test Results

To ensure that the surrogate models reach the accuracies required, a total of 124 sampling points, (i.e., 124 FEA runs) were generated, where 60 are the initial LHS (Latin hypercube sampling) points and the other 64 are the sequential infill points near the regions or interest. NSGA-II was then used with the parameters as defined in Table V to identify the Pareto solutions.

Fig. 12 indicates the sampling points and the Pareto-optimal solutions for the two objective functions after 100 generations of the search algorithm. It is observed that many sampling designs are infeasible designs in terms of the constrained condition, though they seem to be better than the Pareto optimal. For the Pareto optimal, ΔW can be decreased from 2MPa to 0.4MPa, while the total thermal resistance R_{th} can be reduced from 0.11 to 0.09. ΔW and R_{th} are strongly competing with each other and cannot reach an optimum simultaneously. In other words, any further improvement of the lifetime during power cycling must worsen that during the thermal cycling and vice versa. Therefore, it can be suggested from this result that it is better for the designer or engineer of IGBT module to comprehend the practical operational conditions (i.e. cooling ambient conditions and mission profiles).

TABLE V. Details of the NSGA-II parameters used in this study

NSGA-II Parameter name	value
Population size	100
Number of Generations	100
obability of Crossover	0.5
Mutation Probability	0.5

Optimums 1-3 in Fig. 12 are all feasible solutions and it is difficult to choose the best one without knowing the power/thermal cycling information of an specific application. Since the results in Fig. 12 are all equally-optimal solutions, it is difficult to choose the best one. Therefore, a process of decision-making for selection of the final optimal solution from the available solutions is needed. One of the classical decision-making processes is performed with the aid of a hypothetical point, named as Equilibrium Point (EP), i.e., the optimum 2 as shown in Fig. 12, for which both objectives have their optimal values independent of the other objective. The other widely used process is to select a better value for each objective than its initial value from the base design. In terms of these two methods, three optimum solutions are selected among all the possible solutions as shown in Fig. 12 and Table VI. Optimum 1 has the minimum ΔW and the longest lifetime during thermal cycling, solution 3 has the minimum R_{th} and the longest lifetime during power cycling. Solution 2 seems to be a good compromise with respect to the two objectives, i.e., higher reliability during both thermal and power cycling. With

regard to the lifetime, the assumption is that they are put in the same environments and operation conditions with power loss of 300W in the power cycling (see section 3.1),temperature variation of 175℃ in the thermal cycling (see section 3.2.4), and with the failure criteria defined as failure length reaching 10% total length. In terms of the equations derived above, optimum 1 will have 3.5 times lifetime during thermal cycling than the based design, however its lifetime during power cycling will decrease to half of the base design's. These are summarized in Table VI, which compares the three optimized solutions with the base design (typical solution), clearly showing the conflicting nature of the optimization objectives.

It is easily understood that the thickness reduction of any layer will decrease the thermal resistance and thus the lifetime during power cycling. For the thermal cycling, it can be concluded that the second solder layer should be designed a little thicker than the first solder layer to prevent the thermal cycling failure, as it is the most significant layer to prevent the solder fatigue. The same phenomenon can also be observed in the two copper layers of DCB substrate. Conventional designs make them equal, however, it is shown in this work that different thicknesses will not only help decrease the thermal resistance but also decrease the stress and strain in the layers. Concern of ceramic layer should be addressed more closely, because decreasing this layer will significantly decrease the thermal resistance and help decrease the energy accumulated in the second solder layer, however, the elastic stress will be likely to reach the allowed value as well.

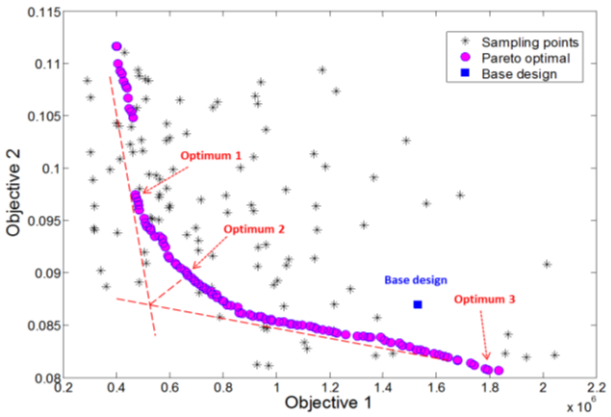


Fig. 12 Pareto solutions of multiple-objective optimization

TABLE VI. OPTIMAL SOLUTIONS AND BASE DESIGN COMPARISONS.

	Base design	Optimum 1	Optimum 2	Optimum 3
t_1 (mm)	0.090	0.0095	0.0093	0.0080
t_2 (mm)	0.300	0.0315	0.0335	0.040
t_3 (mm)	0.400	0.0453	0.0390	0.036
t_4 (mm)	0.300	0.0373	0.0339	0.0266
t_5 (mm)	0.090	0.0152	0.0101	0.0080
t_6 (mm)	3.000	0.2200	0.2205	0.3161
$\Delta W_{solder2}$	1530539	470258	665488	1793800
		-69.28%	-56.52%	+17.20%
R_{th}	0.087	0.0975	0.09	0.0807
		+12.07%	3.45%	-7.24%
N_f^t	1.29×10^3	4.48×10^3	4.43×10^3	1.09×10^3
		+247.29%	+243.41%	-15.50%
N_f^p	5.47×10^8	2.67×10^8	4.43×10^8	8.73×10^8
		-51.19%	-19.01%	+59.60%

VII. CONCLUSIONS

This paper has presented a multi-objective optimization for multi-layered IGBT power modules considering both thermal cycling and power cycling with the thickness of the constituent layers as the optimization targets. Two objectives of maximizing the lifetime under power cycling and thermal cycling are simultaneously considered by minimizing the total thermal resistance and the plastic work accumulated in the solder layer through equation transformation.

Thermal resistance is calculated analytically and the plastic work is obtained with a high-fidelity FE model, which has been experimentally validated. The objective of minimizing the plastic work and constrain functions is formulated by the surrogate model, which reduces computational time and cost. The NSGA-II is used to search for the Pareto optima in the last step. The results indicate that: (1) The optimization objectives determined by power cycling and thermal cycling are conflicting. This is due to the different failure mechanisms induced by power cycling and thermal cycling, so a multi-objective optimization considering both effects simultaneously is necessary. (2) During multi-objective optimization, Pareto optimal solutions could be identified and selected effectively in accordance to various environmental and operational conditions.

In summary, this work presents a novel and efficient way different from existing ones to optimize the structure of power electronic modules, especially for the power modules under special environmental and operational conditions.

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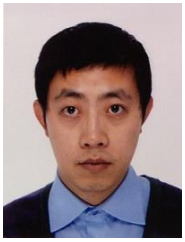

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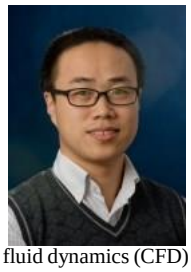

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