Optimized PDPWM Strategy for Hybrid-Clamped Multilevel Inverters Using Switching State Sequences

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***Abstract*—This paper describes an optimized modulation strategy based on switching state sequences for the hybrid-clamped multilevel converter. Two key control variables defined as *phase shift angle* and *switching state change* for a five-level hybrid-clamped inverter are proposed to improve all switches' operation, and by changing their values, different control methods can be obtained for modulation optimization purposes. Two example methods can solve the voltage imbalance problem of the DC link capacitors and furthermore avoid two switches' simultaneous switching transitions and improve the inverter's performance as compared to the traditional phase disposition PWM (PDPWM) strategy. A 6 kW prototype inverter is developed and a range of simulation and experiments are carried out for validation. It is found that simulation and experimental results are in a good agreement and the proposed modulation strategy is verified in terms of low order harmonic reduction.**

***Index Terms*— hybrid-clamped multilevel systems, PDPWM strategy, switching state sequence, modulation, switching loss.**

I. Introduction

MULTILEVEL voltage-source inverters are widely used in high-voltage and high-power applications [1-7] because the multilevel structure leads to low voltage stress on the switching devices, low switching frequency and reduced harmonic contents in the output voltage. But separated dc sources or complex control methods are generally required in order to deliver active power for high level outputs or high modulation indices cases [1]. In the literature, there are three common topologies: the diode-clamped (also termed neutral-point-clamped (NPC)) inverter [1, 4, 6], flying-capacitor (FC) inverter [8, 9], and cascaded inverter [10-13], as shown in Fig. 1. The NPC configuration is almost restricted to three-level inverters because of the need for balancing dc-link voltages and limited voltage rating of blocking diodes [14]. FC inverters are simple in topology and flexible to control active and reactive power. They can achieve a higher voltage level than the NPC in commercial applications. However, their drawbacks are associated with the need for large capacitor banks, additional precharging circuitry, and measures to minimize the voltage imbalance amongst the flying capacitors [15]. Cascaded multilevel inverters require individual voltage sources or bulky input transformers for real power transfer. Thereby, they are suited for distributed generation where the batteries are part of the system [13, 16-20].

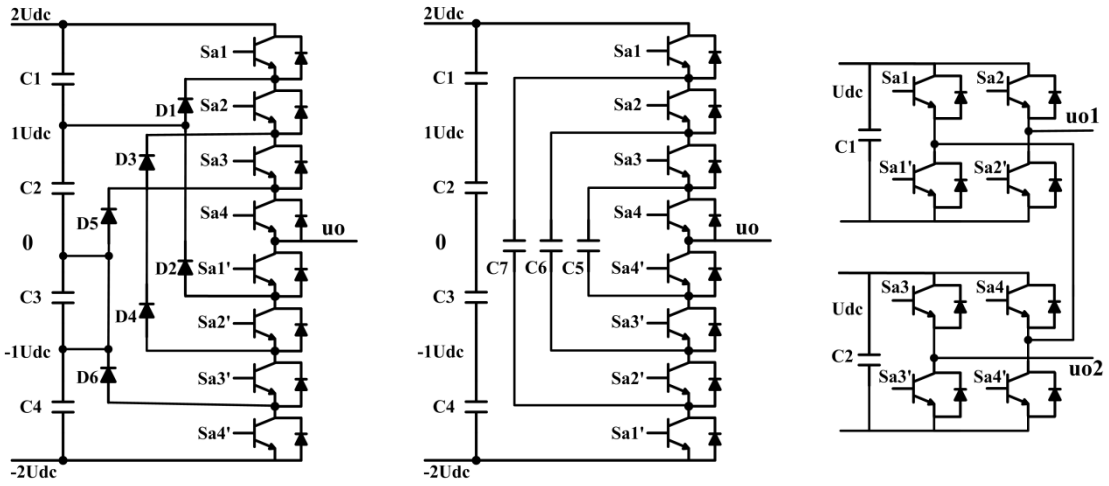


Fig.1. Three common multilevel inverter topologies. (a) NPC inverter. (b) FC inverter. (c) Cascaded inverter.

To improve the performance of multilevel inverters, hybrid-clamped multilevel topologies are proposed to combine two or more types of clamping devices [14, 21-27]. Taking the hybrid-clamped topology (Fig. 2(a)) for example [28], Sa1-Sa4 and Sa1'-Sa4' are the main switching devices to synthesize multilevel output voltages with the aid of clamping diodes D1-D6. The clamping switching devices Sc1-Sc6 and the auxiliary capacitors C5-C7 are used to maintain the four dc-link capacitor voltages in balance with a proper modulation strategy, regardless of load characteristics. In terms of modulation strategy, the phase disposition PWM (PDPWM) is commonly adopted in hybrid-clamped multilevel converters but occasionally carriers' changes are needed to cater for different hybrid-clamped topologies. Otherwise it may still suffer from unbalanced dc voltages across the dc link capacitors. Even in some modulation regions, two switching transitions will occur simultaneously at each comparison instant between the carriers and the sinusoidal reference which in practice, leads to increasing block voltages of related power switches due to their inconsistent parasitic parameters. One solution is the use of a higher and lower carrier cells alternative phase opposition PWM (HLCCAPOPWM) method [29] however it is limited to the topology shown in Fig. 2(a). In this paper, the focus is on the five-level inverter hybrid-clamped by active switches, diodes and capacitors, and a general modulation solution will be proposed to solve the voltage imbalance problem of the DC link capacitors and furthermore avoid two switches' simultaneous switching transitions and improve the inverter's performance.

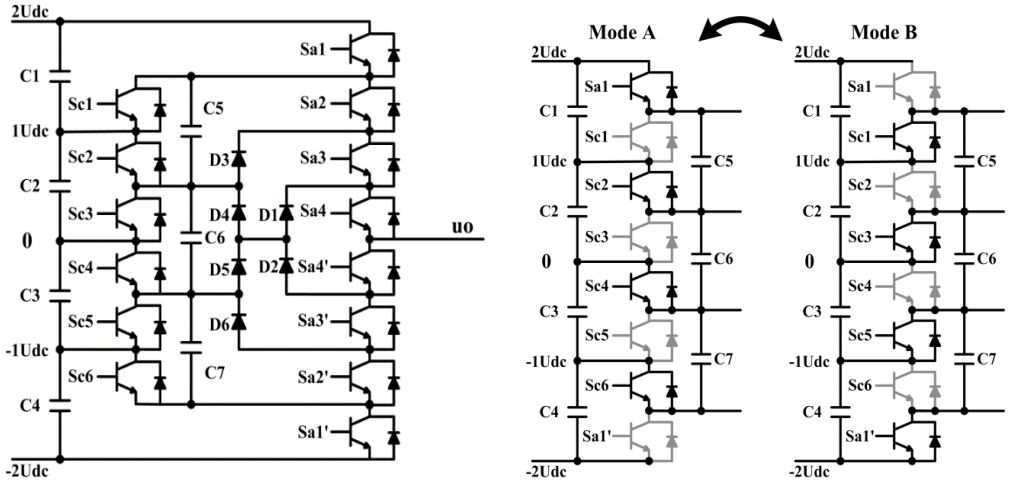
In order to achieve balanced DC link capacitor voltages for the inverter clamped by switches and auxiliary capacitors in Fig. 2(a), it needs to operate between two modes which are presented in Fig. 2(b). For instance, when Sa1 is on in mode A, capacitors C1 and C5, C2 and C6, C3 and C7 are in parallel, respectively. The two parallel capacitors will be charged and discharged to achieve: Uc1 =Uc5, Uc2 = Uc6, Uc3 = Uc7. While Sa1 is off as in mode B, capacitors C2 and C5, C3 and C6, C4 and C7 are in parallel, respectively, thus Uc2 = Uc5, Uc3 = Uc6, Uc4 = Uc7. In effect, all capacitor voltages are equalized when they operate alternatively. All possible switching states of the hybrid-clamped inverter are listed in Table I. For each switching state, the first letter and the first number denote the output level while the second letter represents the state of the clamping device. For example, P1A means that the output voltage is positive U_{dc}, and capacitors connected in mode A are operational.

TABLE I

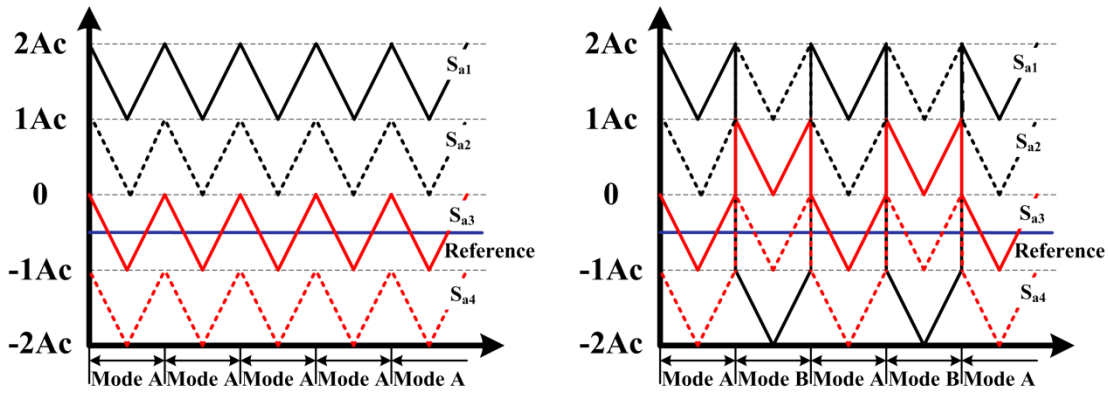
RELATIONSHIP BETWEEN OUTPUT VOLTAGE AND SWITCHING STATES

Switching State	Output voltage	Switch			
		Sa1	Sa2	Sa3	Sa4
P2A	+2Udc	1	1	1	1
P1A	+1Udc	1	0	1	1
P1B	+1Udc	0	1	1	1
O0A	0	1	0	0	1
O0B	0	0	0	1	1
N1A	-1Udc	1	0	0	0
N1B	-1Udc	0	0	0	1
N2B	-2Udc	0	0	0	0

Fig. 2(c) shows the traditional PDPWM method for general five-level topologies where Ac is the peak–peak value of the triangle carrier. However, the carrier of switch Sa1 stays at the top of four carriers all the time so that alternative operating modes cannot be realized on the topology in Fig. 2(a). As a result, a modified modulation method [28]is used to solve this problem. As shown in Fig. 2(d), in the second switching period, the order of the carriers is rearranged to have a switch over between the two modes. However, by the modified PDPWM strategy, two switches commutate simultaneously when the reference voltage is located in regions -1Ac to 2Ac. See overlapped lines in Fig. 2(d). As an example, Sa1 and Sa4 operate at the same time when carrriers' rearrange at the end of the first switching period. Furthermore, the switching times of Sa1 and Sa4 are doubled in one switching period compared to the traditional case in Fig. 2(c), while the switching losses are increased consequently. This paper proposes an optimized PDPWM strategy which can ensure that only one switch commutates at each comparison instant of carriers and the reference.



(a) (b)



(c) (d)

Fig. 2 Five-level hybrid-clamped topology and its operation principle. (a) One leg of the five-level hybrid-clamped topology. (b) Two operational modes of dc-link capacitors. (c) Carrier waveforms of the upper four main switching devices under traditional PDPWM strategy. (d) Carrier waveforms of the upper four main switching devices under Modified PDPWM strategy [28].

II. Operational Principle of Proposed Switching State Sequences

Fig. 3 presents a switching state diagram of the five-level hybrid-clamped topology. The inverter's output voltage is divided into four operational regions to generate different output voltage levels depending on the variable r (r = 1, 2, 3, 4). Within every region, the switching state is circled and arranged in sequence. Since each switching state includes all switches' transaction information, the switching state sequence means that all switches are controlled sequentially to generate the expected voltage output. Furthermore all existing switching states in the region can be arranged in different sequences to output commanded voltage in a redundant way. However all the switching state sequences have totally the same operation time of two switching periods no matter how many switching states are included in the sequences. As illustrated in Fig. 3, a series of possible switching state sequences can be obtained.

Obviously, the initial switching state should be determined first when a switching state sequence is identified, and this switching state sequence should be ended with the initial switching state as well. Second, two variables (Sp and Sd) are needed to further distinguish the different switching state sequences. Sp is the phase shift angle whilst Sd is the switching state change of the switching state sequence. Sp determines the starting position of the switching state sequence ranging between 0 to 2π, and Sd switches between 0 and 1. When Sd = 0, the initial switching state needs to move towards a low voltage level switching state in the next step. It is opposite when Sd = 1.

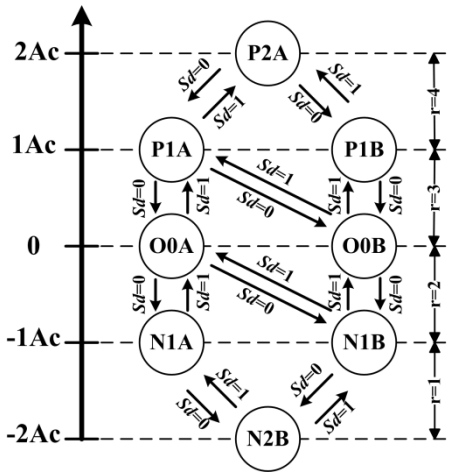


Fig. 3. Switching state diagram of the five-level hybrid-clamped topology.

A. Initial state of the switching state sequence

In each operating region, there are two voltage levels. Taking the region $r = 4$ for example (see Fig.3), three switching states circulate in the designed sequence and four possible candidates can be selected as follows,

(i) When the state P2A is selected as the initial state, the consequent switching sequence can be P2A→P1A→P2A→P1B→P2A (for $Sd = 0$). Since these three switching states only involve the top two switches Sa1 and Sa2, and the other two switches keeps turning on in the region $r = 4$, for easily calculating the operating time of each state in the next step, the relationship between the switching state sequences and carrier generation is presented in Fig. 4(a). T_c denotes the switching cycle. It could be found that the switching state switches to another at each comparison instant between the carriers and the reference. When all the carriers are beneath the reference, the related switching state is state P2A, and if only the carrier of switch Sa2 is above the reference, the state P1A works. It is similar when the state P1B is in action.

(ii) When the state P2A is selected as the initial state, the other alternative is P2A→P1B→P2A→P1A→P2A (for $Sd = 0$). Its carrier generation is shown in Fig. 4(b).

(iii) When the state P1B is selected as the initial state, the switching sequence is P1B→P2A→P1A→P2A→P1B (for $Sd = 1$). Similarly, Fig. 4(c) shows its carrier generation.

(iv) When the state P1A is selected as the initial state, the switching sequence is P1A→P2A→P1B→P2A→P1A (for *Sd* = 1). And Fig. 4(d) gives its carrier generation diagram.

(v) When the state P1B or P1A is selected as the initial state, two redundant switching state sequences can be achieved as well, that is P1B→P2A→P1B→P2A→P1A→P2A→P1B or P1A→P2A→P1A→P2A→P1B→P2A→P1A.

Obviously the top four cases provide the shortest switching state sequences only including four state transitions and should be given high priority. Since these sequences can achieve the fewest switching times. However in terms of avoiding two switches' simultaneous communication, all five kinds of switching sequences can achieve the expected good performance. Similarly for regions *r* = 2 and 3, there are four switching states within each sequence and their shortest switching state sequences includes six state transitions. Furthermore three switches are involved to generate the appointed switching states.

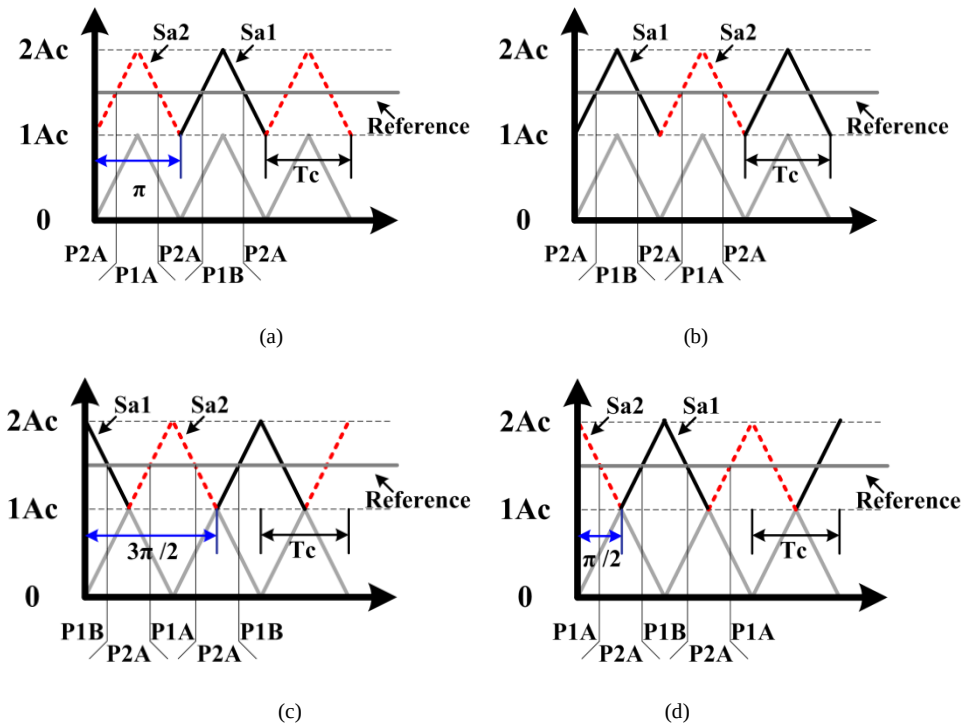


Fig. 4. Relationship between switching state sequences and carrier generation under optimized PDPWM strategy in region r=4. (a) Case (i) with *Sd*=0, *Sp*= π. (b) Case (ii) with *Sd*=0, *Sp* =0. (c) Case (iii) with *Sd*=1,*Sp*=3π/2. (d) Case (iv) with *Sd*=1, *Sp*=π/2.

B. Phase shift angle in the switching state sequence

When the initial switching state and *Sd* are determined, the switching state sequence is dictated by *Sp* which can cause horizontal shifts of the carriers virtually. Clearly, a particular triangle carrier should be taken as the phase base in order to evaluate phase shift angles of other carriers in each region. In this paper, the carrier for the switch Sa1 is assigned as the phase base in region $r = 4$, and *Sp* in this region indicates the phase shift angle between zero and the start of positive edge of the Sa1 carrier, as described in Fig. 4. The carriers of Sa2, Sa3 and Sa4 are assigned as the phase bases for regions $r = 3$, 2, and 1, respectively. As shown in Fig. 4(a), the Sa1 carrier is phase-shifted by one switching cycle T_c towards right, therefore $Sp = \pi$ can be obtained. It is identical when $Sp = 0$ and $Sp = 2\pi$ from the definition of *Sp*, which just match the fact that all switching sequences have the operational time of two switching cycles of $2T_c$. Similarly the cases of $Sp = 0$, $Sp = 3\pi/2$ and $Sp = \pi/2$ are shown in Fig. 4(b), Fig. 4(c) and Fig. 4(d) respectively.

In this paper, the modulation strategy in the appointed region is optimized by changing *Sd* and *Sp*. In addition, different *Sp* and *Sd* can also be used for different phase legs in the same regions when some specific harmonic components are required to be cancelled. Obviously, further FFT calculations need to be done for harmonic cancellation purpose. For ease of implementation, only $Sp = n\pi/2$ ($n = 0, 1, 2, 3$) are considered in this paper, and all possible shortest switching state sequences for four regions are listed in Table II. The proposed modulation strategy is advantageous in selecting switching state sequences randomly from different regions but still generates required output performance. Consequently, this strategy is more flexible and robust than the traditional PDPWM and the modified one.

TABLE II

ALL POSSIBLE SHORTEST SWITCHING STATE SEQUENCES FOR FOUR REGIONS

r	*Sd*	*Sp*	Switching state sequence
1	0	π	N1A→N2B→N1B→N2B→N1A
	0	0	N1B→N2B→N1A→N2B→N1B
	1	$\pi/2$	N2B→N1B→N2B→N1A→N2B
	1	$3\pi/2$	N2B→N1A→N2B→N1B→N2B
2	0	0	O0B→N1B→O0A→N1A→O0A→N1B→O0B
	0	$3\pi/2$	O0A→N1A→O0A→N1B→O0B→N1B→O0A
	0	$\pi/2$	O0A→N1B→O0B→N1B→O0A→N1A→O0A
	1	$\pi/2$	N1B→O0B→N1B→O0A→N1A→O0A→N1B
	1	$3\pi/2$	N1B→O0A→N1A→O0A→N1B→O0B→N1B
	1	π	N1A→O0A→N1B→O0B→N1B→O0A→N1A
3	0	0	P1B→O0B→P1A→O0A→P1A→O0B→P1B
	0	$3\pi/2$	P1A→O0A→P1A→O0B→P1B→O0B→P1A

	0	π/2	P1A→O0B→P1B→O0B→P1A→O0A→P1A
	1	π/2	O0B→P1B→O0B→P1A→O0A→P1A→O0B
	1	3π/2	O0B→P1A→O0A→P1A→O0B→P1B→O0B
	1	π	O0A→P1A→O0B→P1B→O0B→P1A→O0A
4	0	0	P2A→P1B→P2A→P1A→P2A
	0	π	P2A→P1A→P2A→P1B→P2A
	1	3π/2	P1B→P2A→P1A→P2A→P1B
	1	π/2	P1A→P2A→P1B→P2A→P1A

Fig. 5 illustrates two typical modulation methods with different *Sd* and *Sp* values in different regions and further listed in Table III in detail. Especially shown in Fig. 5(a), two redundant switching state sequences in regions *r*= 1 and 4 are applied, and the related simulation and experimental results are given subsequently which fully present the required excellent output performance.

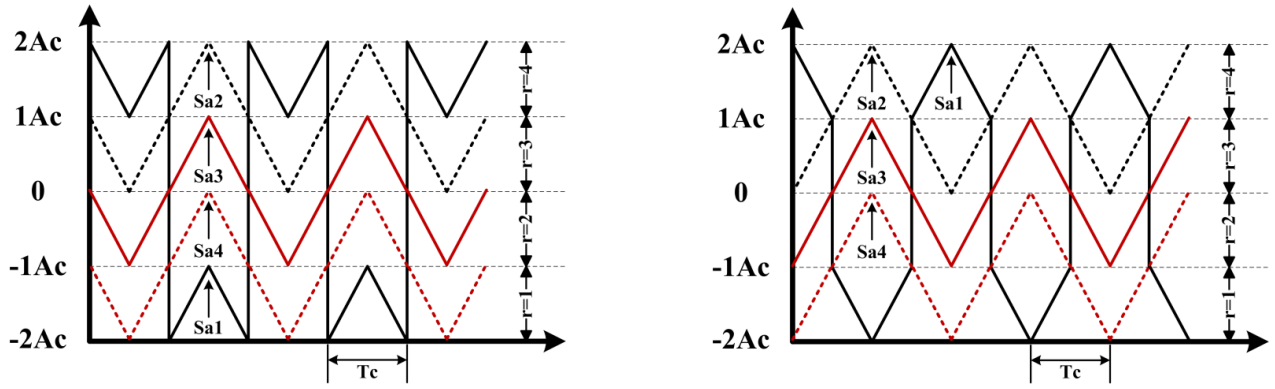


Fig. 5. Two typical modulation methods with different *Sp* and *Sd* deduced from the proposed optimized modulation strategy. (a) Carriers for Sa1-Sa4 under method 1. (b) Carriers for Sa1-Sa4 under method 2.

TABLE III

SWITCHING STATE SEQUENCES AND CONTROL VARIABLES OF TWO TYPICAL MODULATION METHODS

Modulation method	***r***	***Sd***	***Sp***	**Switching state sequence**
1 (Fig. 5(a))	1	1	π/2	N2B→N1B→N2B→N1A→N2B→N1A→N2B
	2	1	π/2	N1B→O0B→N1B→O0A→N1A→O0A→N1B
	3	1	π/2	O0B→P1B→O0B→P1A→O0A→P1A→O0B
	4	1	π/2	P1B→P2A→P1B→P2A→P1A→P2A→P1B
2 (Fig. 5(b))	1	0	0	N1B→N2B→N1A→N2B→N1B
	2	0	0	O0B→N1B→O0A→N1A→O0A→N1B→O0B
	3	0	0	P1B→O0B→P1A→O0A→P1A→O0B→P1B
	4	1	3π/2	P1B→P2A→P1A→P2A→P1B

III. Implementation of the Optimized Modulation Strategy

Fig. 6 shows the pulse waveform generation of the modulation method 1 (see Fig. 5 (a)) for switching state transitions in region $r = 3$. Three switches Sa1, Sa2 and Sa3 participate in the switching state transitions and the operating time t1-t6 of six switching states need to be calculated to generate the switching state sequence. Generally for a five-level inverter, the amplitude modulation index m_a and the frequency ratio m_f are defines as

$$m_a = \frac{A_m}{4A_c} \tag{1}$$

$$m_f = \frac{f_c}{f_m} \tag{2}$$

where A_c and A_m are the amplitude peak-peak values of the triangle carrier and the sinusoidal reference waveform, respectively. f_c is the carrier frequency, and f_m is the modulation signal frequency. When $f_c >> f_m$, the sinusoidal reference can be approximated as constant in one switching period. Therefore, considering the simple geometrical relationship, the turn-off time of the initial switching state can be obtained:

$$\frac{\mathrm{t1}}{\frac{\mathrm{T_c}}{2}} = \frac{A_c - \frac{A_m}{2}\sin\omega_m t}{A_c} \qquad \left(\omega_m = 2\pi f_m\right) \tag{3}$$

By using the same method, $t2$ can be expressed as

$$\frac{\mathrm{t2}}{\mathrm{T_c}} = \frac{\frac{A_m}{2}\sin\omega_m t}{A_c} \tag{4}$$

Owing to the geometrical symmetry, $t3 = t4 = t6 = t1$, and t5 = t2. Therefore, by substituting these two equations into (3) and (4), all time variables for one switching state sequence can be obtained, which are

$$\mathrm{t1} = \mathrm{t3} = \mathrm{t4} = \mathrm{t6} = \left(1 - 2m_a \sin\omega_m t\right)\frac{\mathrm{T_c}}{2} \tag{5}$$

and

$$\mathrm{t2} = \mathrm{t5} = 2\mathrm{T_c} m_a \sin\omega_m t \tag{6}$$

Similarly, the operating time of the switching states in other regions can be obtained. Therefore, the proposed modulation strategy is implemented based on determined *r*, *Sp*, *Sd* and operating time of the switching states. Fig. 7 shows the flowchart of switching state sequence generation. In this paper, the digital controller with the proposed modulation strategy is implemented in a Texas Instruments TMS320F2812 digital signal processor (DSP) platform with the gating signals generated from an EP1C3T144C8 field-programmable gate array (FPGA).

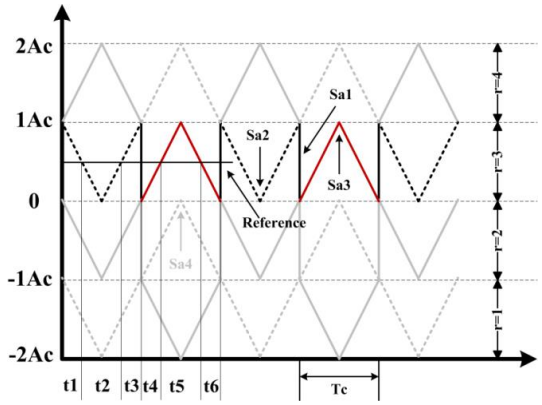


Fig. 6. Pulse waveform generation of a switching state sequence in the region *r* = 3.

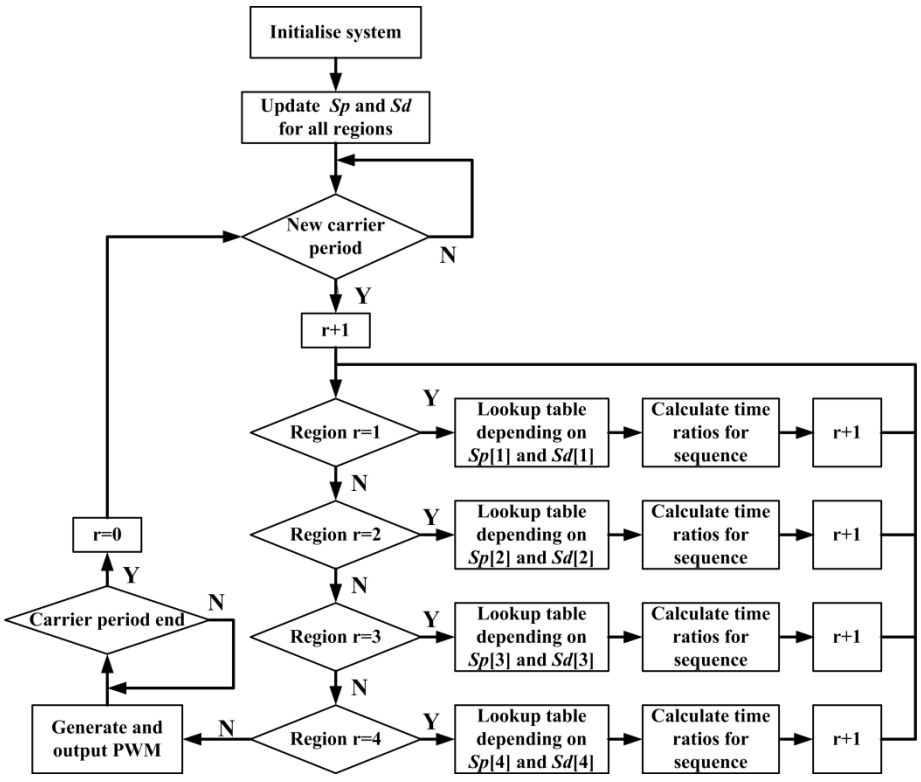


Fig. 7. Flowchart of switching state sequence generation.

IV. Simulation and Experimental Results

In order to verify the proposed modulation strategy, a 6 kW single-phase hybrid-clamped five-level inverter is developed and shown in Fig.8. Simulation work is conducted in Matlab environment. Experimentally tests are carried out on resistive load with the neutral point of the dc-link capacitors as the reference point. The parameters used for simulation and experiments are listed in Table IV.

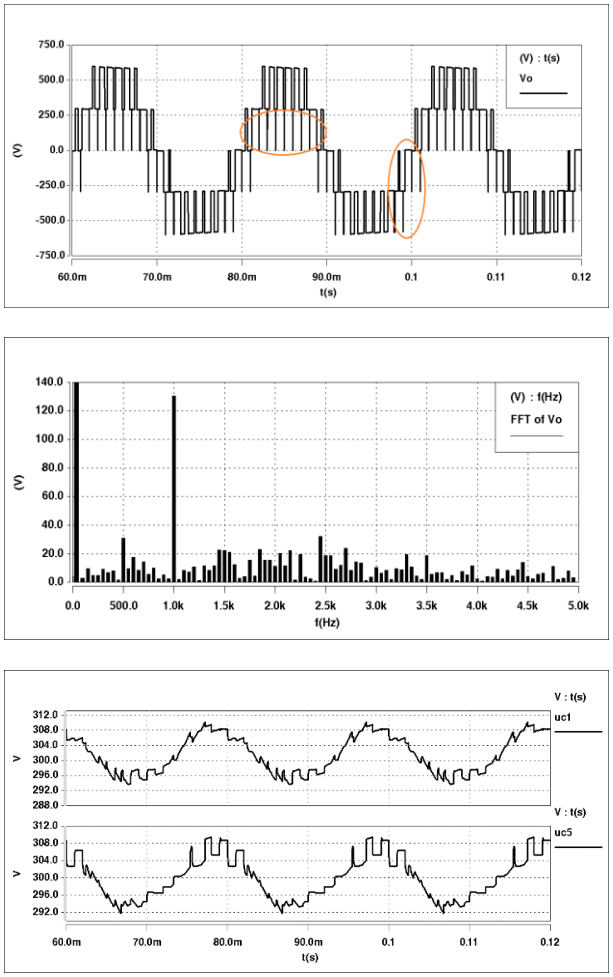
Fig. 8. Prototype of the 6 kW single-phase hybrid-clamped five-level inverter.

TABLE IV
PARAMETERS FOR SIMULATION AND EXPERIMENTS

Parameter	Value
Ac output frequency f_m	50 Hz
Carrier frequency f_c	1 kHz
Modulation index m_a	0.9
DC bus voltage Vdc	1200 V
AC output power Vac	6 kW

Fig. 9(a) shows the simulation results with the modified PDPWM method illustrated in Fig. 2(d). In the top of Fig. 9(a), the unexpected switching state transitions are highlighted, which give rise to switching times and blocking voltages of related switches. Its middle subfigure shows the fast Fourier transform **(**FFT**)** analysis of output voltage where the magnitude of the carrier fundamental

harmonic is relatively high (in exceed of 120V). Then the bottom one shows the voltage ripples of the dc-link capacitor C1 and the auxiliary capacitor C5, where the magnitudes are approximately 16V for uc1 and 18V for uc5, which means dynamic balance of capacitor voltages can be achieved.



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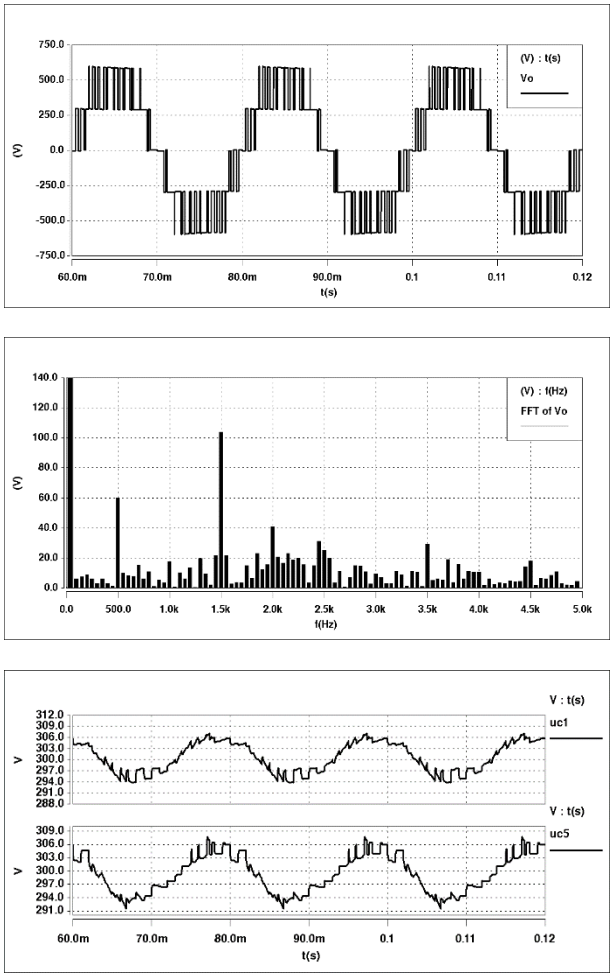

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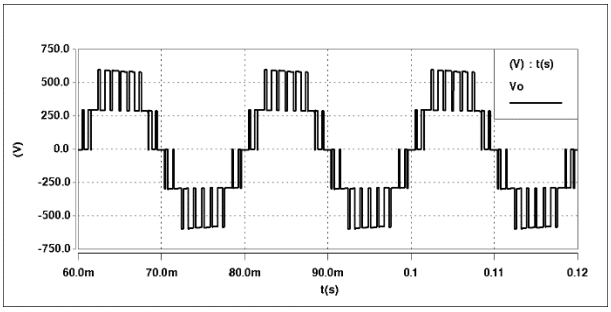
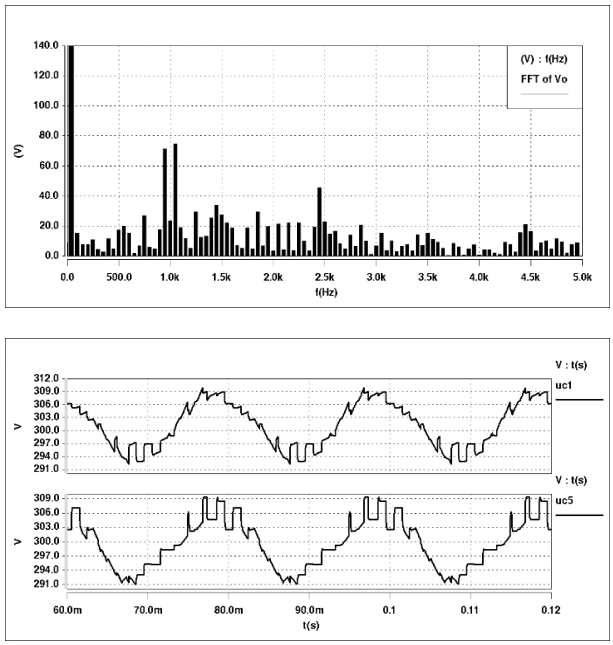




(c)

Fig. 9. Simulation results and comparisons of the modified PDPWM method, proposed method 1 and method 2. (a) Modified PDPWM method. (b) Method 1. (c) Method 2. (From top to bottom of all subfigures: Phase voltage uo, harmonic spectrum of uo and voltage ripples of C1 and C5).

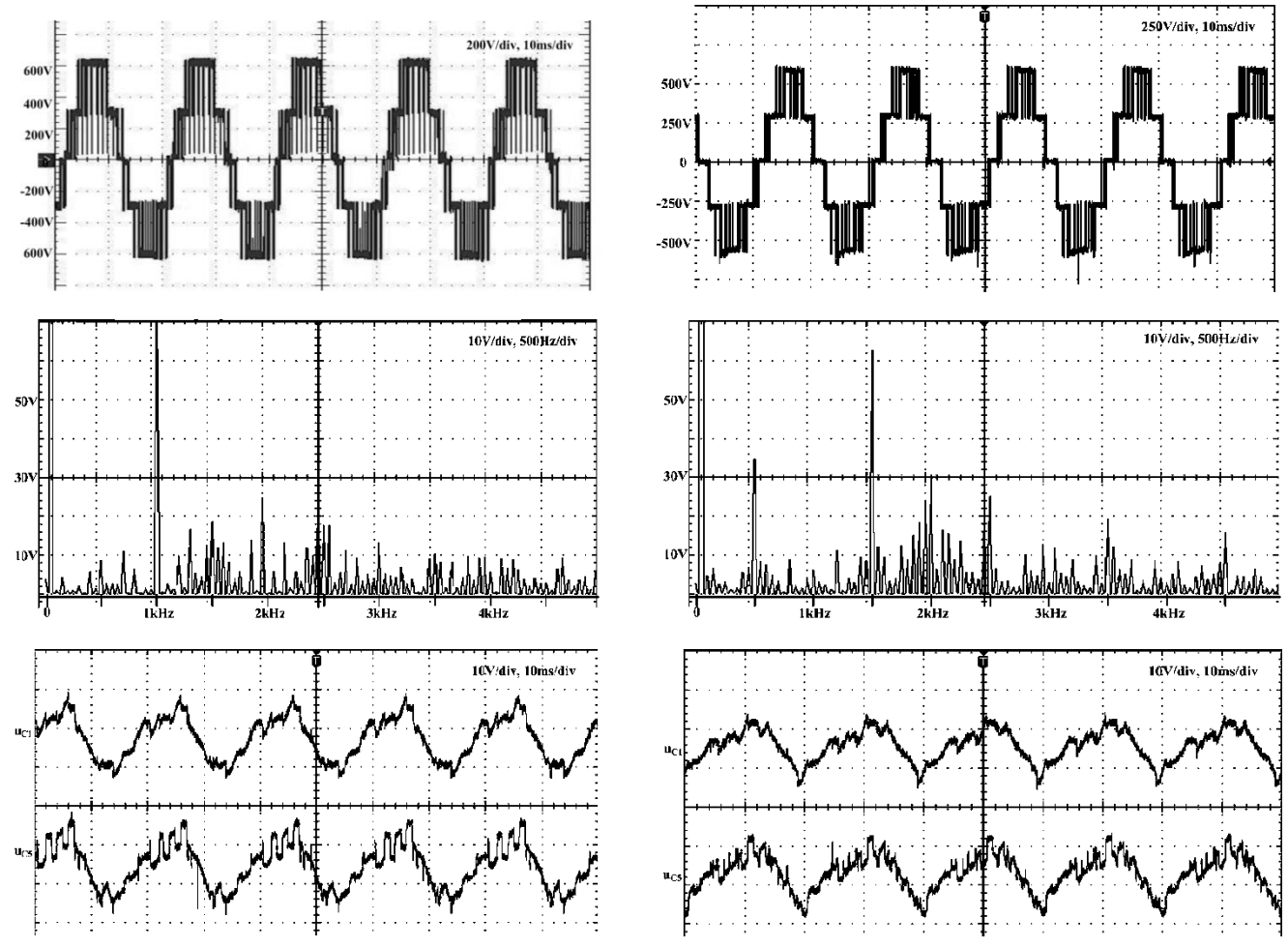
The simulated waveforms of the proposed optimized modulation strategy with different values of *Sp* and *Sd* are shown in Figs. 9 (b) and 9(c), which have ordinal correspondence with the modulation methods illustrated in Figs. 5(a) and 5(b). As shown in the top subfigures of Figs. 9(b) and 9(c), there are not any unexpected switching state transitions as in Fig. 9(a) since the proposed optimized modulation strategy can guarantee that only one switch operates at any given time. Hence, the carrier fundamental harmonic is reduced in its magnitude as well as the THD of the output voltage uo. However, the two methods with different *Sp* and *Sd* result in slightly different harmonic distributions. The significant harmonics are 1.5 kHz and 500 Hz for method 1 (The middle subfigure of Fig. 9(b)), and 1050Hz and 950Hz for method 2 (The middle subfigure of Fig. 9(c)). Furthermore, the voltage ripples of the dc-link capacitor C1 and the auxiliary capacitor C5 are slightly lower than the modified PDPWM method shown in Fig. 2(d). The THD values of the output voltage are tabulated in Table V for comparison between the modified PDPWM and the proposed optimized PDPWM. Although the total THDs for these different modulation strategies are almost the same, the low order harmonics for optimized PDPWM are much less than those for the modified PDPWM.

TABLE V

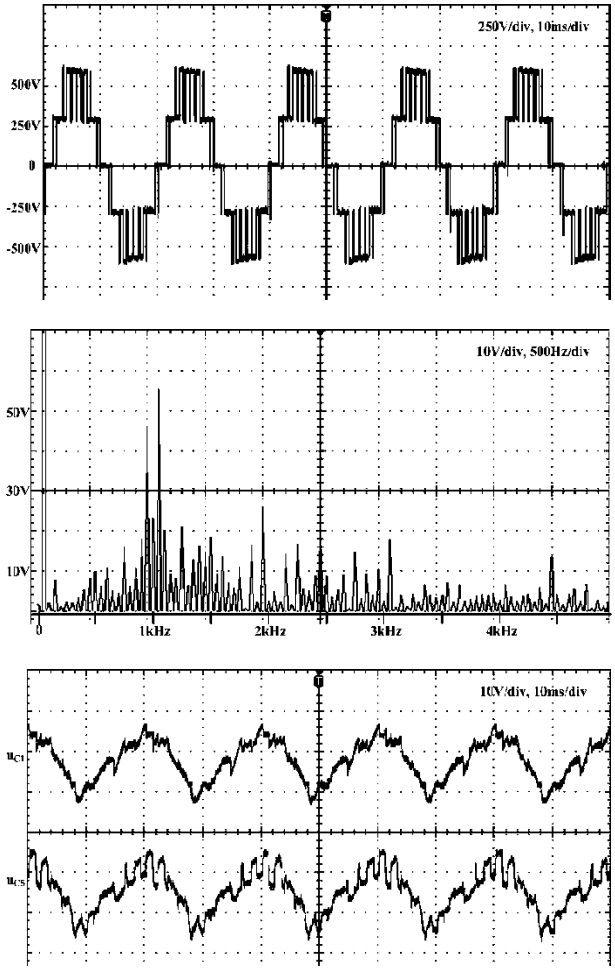
NORMALIZED MAGNITUDE OF HARMONICS FOR THREE MODULATION METHODS

Value	Modified PDPWM	Method 1	Method 2
21st THD	22.52%	10.68%	19.19%
30th THD	23.76%	20.52%	22.27%
Total THD	30.81%	30.64%	30.43%

Fig.10 shows the experimental waveforms for the modified PDPWM method and the optimized PDPWM method. As can be observed, the experimental results differ slightly from the simulation ones in Fig. 9 in terms of voltage magnitudes, but the characteristic features and trends are similar. A reasonable agreement can be found. Overall, these results confirm the effectiveness of the proposed hybrid-clamped five-level converter and its hardware development.



(a) (b)



(c)

Fig. 10. Experimental results of the modified PDPWM method, proposed method 1 and method 2. (a) Modified PDPWM method. (b) Method 1. (c) Method 2. (From top to bottom of all subfigures: Phase voltage uo, harmonic spectrum of uo and voltage ripples of C1 and C5).

V. CONCLUSIONS

This paper has presented an optimized PDPWM modulation strategy for hybrid-clamped multilevel converters. For the original PDPWM strategy, more switching actions are required for the hybrid-clamped multilevel converter in order to realize a natural balance of the dc-link capacitors at the cost of high switching losses and as well increase blocking voltages of some switches. To overcome these disadvantages, the paper has introduced two crucial control variables of switching state sequence to improve topology operation, and to ensure that only one switching transition occurs at each comparison between the carriers and the sinusoidal reference. Furthermore, by manipulating the variables *phase shift angle* and *switching state change*, a series of different modulation methods can be obtained. The

simulation and experimental results on a 6 kW prototype inverter have validated the proposed strategy and the converter design. Additionally, the proposed optimized modulation strategy can also be applied to other hybrid topologies, which are promising to improve their switching efficiency and reduce low order harmonic contents.

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