A NON-LINEAR ENCODER,

USING A BINARY COUNTER,

FOR PULSE-CODE MODULATION.

A thesis submitted for the degree of

MASTER of SCIENCE

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SUMMARY

A review of pulse-code modulation has shown that interest is again being taken in pulse-count encoders. On these and other p.c.m. systems, logarithmic companding is desirable but it is usually applied in a separate stage. This is an investigation into methods of incorporating the companding action in a pulse-count coder.

A theoretical appraisal has revealed at least five possible methods of non-linear pulse-count coding. The first may be instrumented simply only at the encoder. Three methods may not instrumented conveniently at either end. The fifth method may be applied to p.c.m. because the same type of coder is required at both ends.

The first method was checked experimentally by testing the transfer characteristic of a monostable multivibrator which had transistor resistance modulators as timing elements. A new timing circuit has been proposed which should give a symmetrical characteristic for positive and negative modulation. Experimentally, a small asymmetry was given, and it is concluded that a non-linear encoder could not be based upon a monostable multivibrator.

To test the fifth method, low frequency models were developed for the two coders. The main component stage was a novel voltage-to-frequency convertor driven by a distorted triangular sweep waveform. The junction f.e.t. has a certain advantage as a single-ended compandor and has been used in the sweep generator.

The test upon the encoder gave a symmetrical characteristic but on the overall test, errors due to asynchronism occurred. It is concluded that these errors are inherent in a system where the clock pulse frequency is smoothly varied.

Finally, an alternative encoder giving a segmented characteristic, which should be error-free, is proposed.

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LIST OF SYMBOLS

C	Capacitance - subscripts denote position in circuit. e.g. C_{ce} - capacitance between collector and emitter
df/dV	gradient of the transfer characteristic of a voltage-frequency converter
f	clock pulse frequency variable; subscripts s = send-end, r = receive-end.
f_o	constant value of clock p.r.f. which will give the maximum number of quantum levels in the full channel pulse duration
f_m	highest value of modulating signal frequency
F (and ϕ)	general modulating functions
h_{fb}	Current gain factor in common base) parameters of a
h_{fe}	" " " " " emitter) bipolar transistor
h_{oe}	Output slope conductance
i	general current variable; in particular the drain current of a f.e.t. Subscript denotes branch in which i flows
I	normalised value ($= i/I_{max}$)
I_p	f.e.t. drain current when drain and gate values are at pinch-off and zero values respectively
J,K	The inhibiting inputs of a J.K. binary stage
l	the number of quantum levels corresponding to a modulating signal sample of height U volts
L	the maximum number of levels - also the general symbol for inductance
m	number of channels (see Chapters 3 and 10) also R_2/R_1 in compound CR coupling (see Chapter 4) also τ_c/τ_e in separate-stage companding (see Appendices I and J)

LIST OF SYMBOLS Continued

n	number of binary digita pulses such that 2^n = maximum number of quantum levels
$0, 1$	The lower and upper logic levels in a binary system
Q_1, Q_2 etc.	Symbols for different transistors
r	general resistance variable: in particular the drain-source resistance of a f.e.t.
r_c	resistance of compressor element) in separate
r_e	resistance " expander ") stage companding
r_r	resistance of receive- and send-end compandors
r_s	in Method 5 coding - second subscripts 0 or 1 denote resistance at zero and maximum voltage input -(e.g. r_{ro} , r_{s1})
R_p	drain-source resistance of a f.e.t. when $i = I_p$, $v = V_p$
R_e, R_b	resistance values in emitter and base leads
R_S, R_D	" " " source and drain leads
R_L	resistance in series with collector (or drain)
σ	deviation from the ideal (see Chapter 7)
σ	r.m.s. noise deviation (see Chapter 1)
s	number of segments in a segmented companding characteristic
t	general time variable
t_n, t_{n+1}	instants just before and just after respectively the trailing edge of the clock pulse

LIST OF SYMBOLS Continued

τ	time delay in a stage
T	pulse duration variable
T_s, T_r	pulse duration at send- and receive-ends respectively
T_o	pulse duration for zero modulating signal
ΔT	time deviation from T_o
T_{min}, T_{max}	Minimum and maximum values of pulse duration
T	also temperature (see Chapter 2)
T_1, T_2	general symbols for different transistors in a circuit
U, V	Normalised output and input voltages (i.e. $V = v/V_m$)
v	general voltage variable: in particular, the drain voltage of a f.e.t.
V_m	maximum value
v_g	the gate-source voltage of a f.e.t.
v_{ce}	voltage between collector and emitter
v_{be}	" " base and emitter
V_{BES} V_{CES}	Saturation values of base and collector potentials w.r.t. the emitter respectively
V_γ	The smallest value of base-emitter voltage for which an appreciable value of current flows (i.e. the cut-in value = 0.5 v for a silicon transistor)
V_{OU}, V_{OL}	Upper and lower clamping levels of a difference amplifier characteristic

CHAPTER ONE

INTRODUCTION

CONTENTS.

1.1. Principle of Pulse - Code Modulation

1.2 Historical Review

1.2.1 The Post-War Period 1947-1957

1.2.2 The Semi-conductor Period 1962-Present

1.1 The Principle of Pulse - Code Modulation

This work is concerned with the design of a particular type of coder for pulse code modulation.

Pulse-code modulation (p.c.m.) is a system of communication where the signal is sampled by a pulse train, the height of each sample being made to generate a train of binary digit pulses of equivalent value . (fig 1.1.) This is the encoding process. The binary digit pulses (sometimes called code pulse groups) are transmitted and at the receiver the code pulse groups are decoded by a process, which is usually (though not always), the inverse of that of the encoder. A block diagram of a typical multi-channel system is shown in fig 1.2. The sampling process occurs in a channel gate and the outputs of these gates are applied to the coder. The coding process cannot convert all values of signal amplitudes, for a binary digit train of n pulses per sample can only represent up to 2^n amplitudes . Hence the amplitudes are said to be quantised and a typical value of n is seven which gives 128 levels. The quantiser is shown as a separate stage, although in some systems it is an integral part of the coding process. The term encoder is usually reserved for that stage in which the binary digit trains are produced. At the receiver, the decoder converts the incoming code pulse groups into pulses whose height (or duration,) is proportional to the amplitude of the original modulating signal. After separation into the appropriate channels, these pulses are demodulated by passing through a low pass filter.

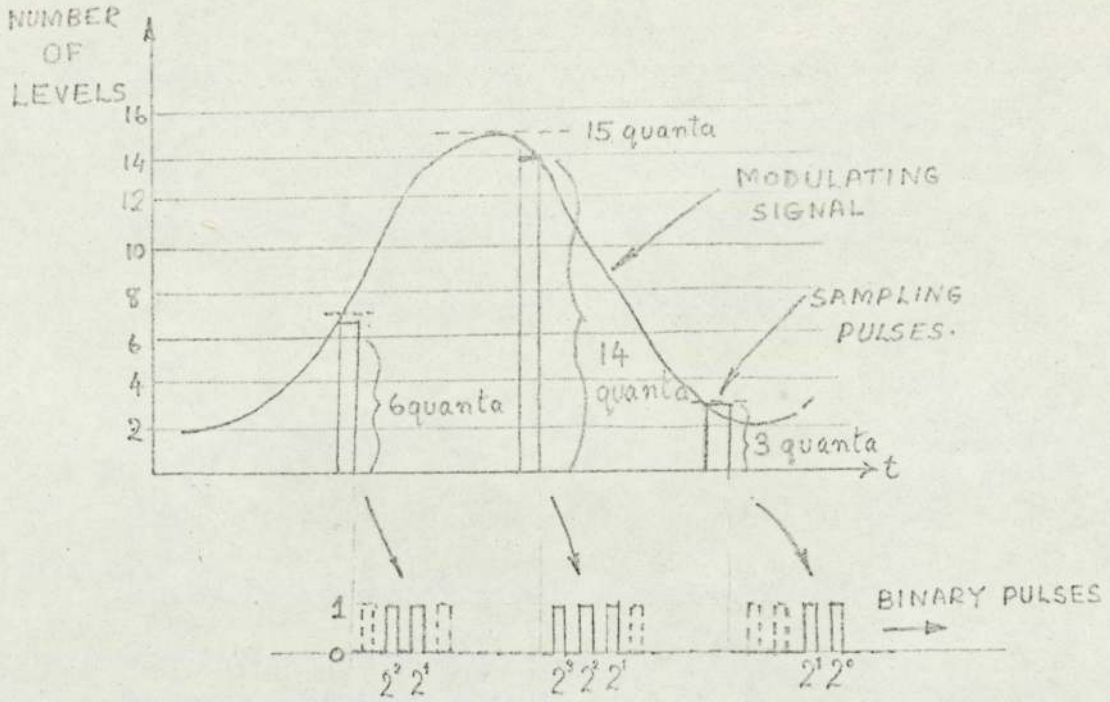


Figure 1.1 QUANTISATION IN PCM.

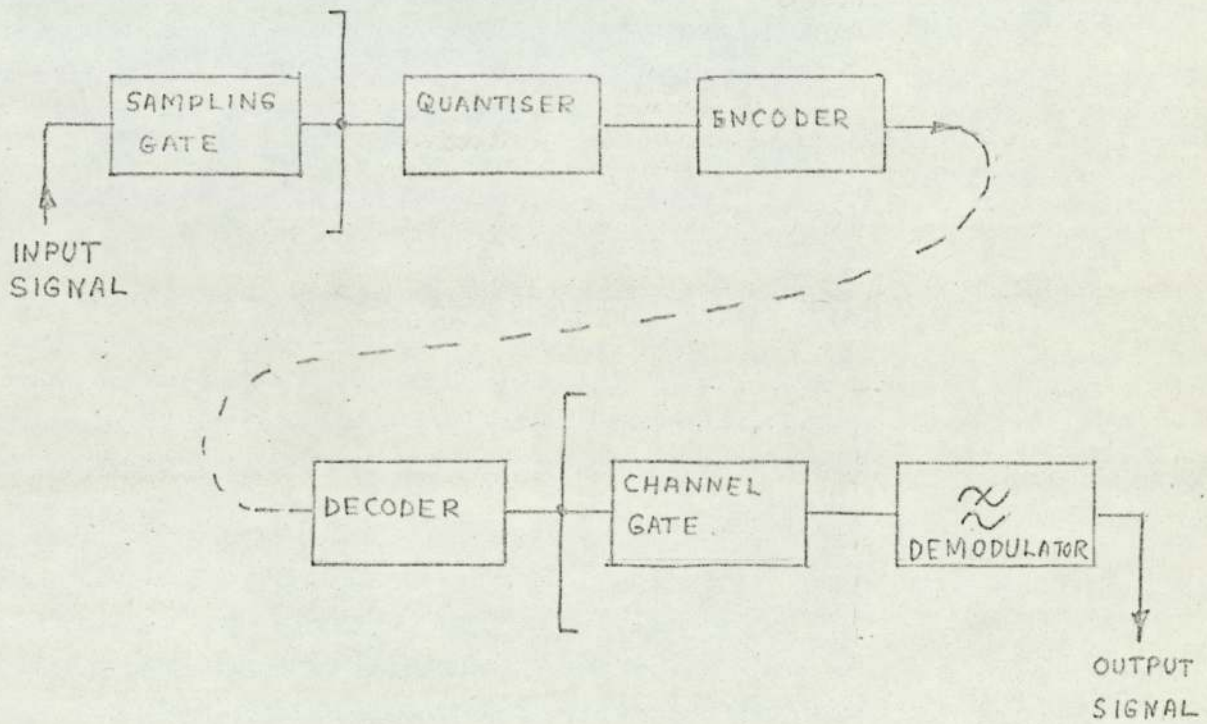


Fig. 1.2 MAIN COMPONENT STAGES OF ENCODER AND DECODER

Quantisation of amplitudes inherently introduces error [1] which gives rise to quantisation distortion. That is, at the receiver, the reconstituted signal may differ from the original signal by as much as one step. This may be seen in fig. 1.3. which shows the quantisation errors which occur when an arbitrary modulating signal is sampled by pulses whose amplitudes range over eight levels. The amount of distortion may of course be reduced if the number of levels is increased.

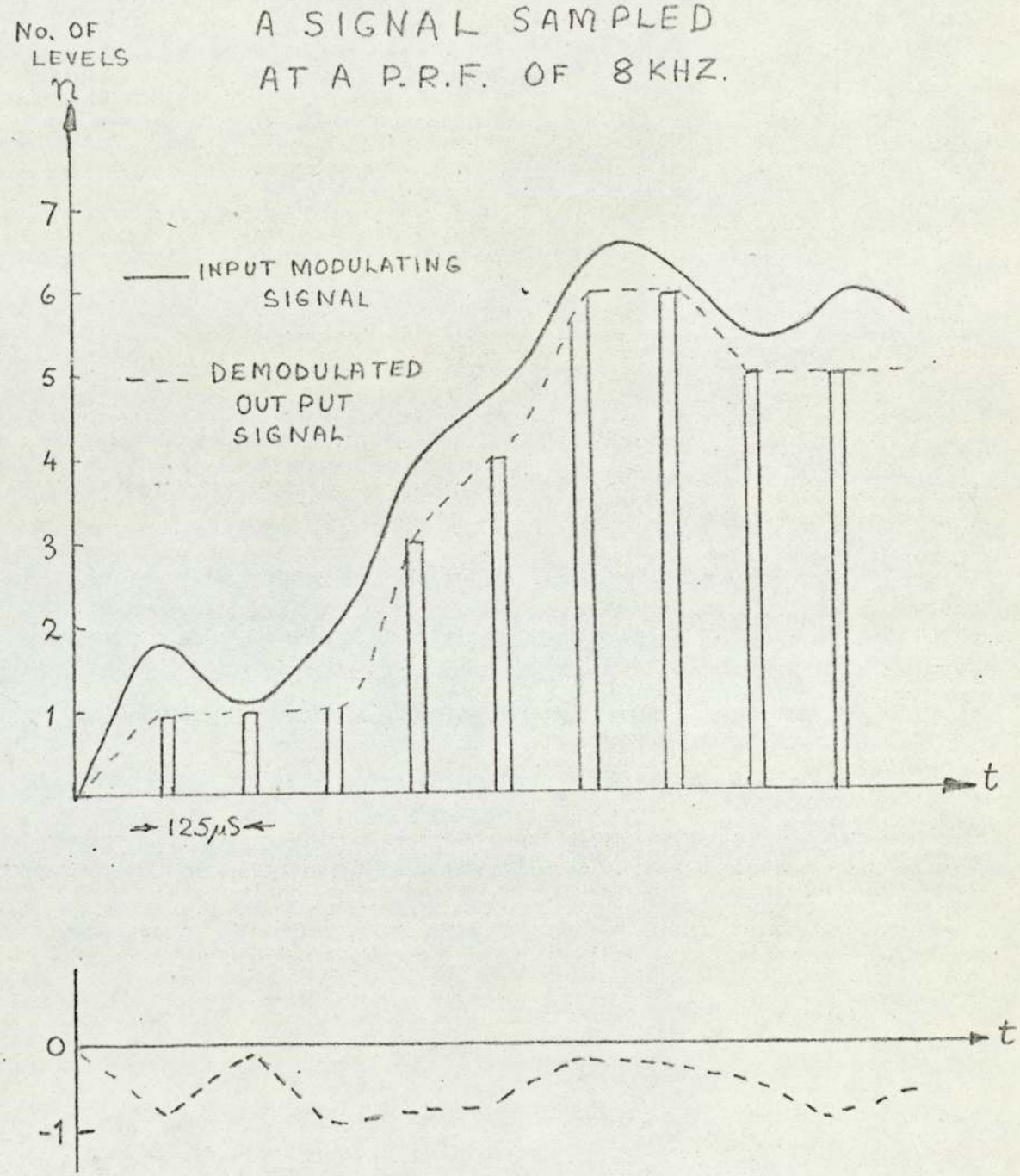
Since all values of error from zero to one step are equally likely, the result is a fluctuating error in the receiver output which manifests itself as a "hiss" noise, [2] not unlike that due to thermal agitation in a resistance. The maximum value of the signal: quantising noise ratio has been given [3] as:-

$$(10.8 + 6n) \text{ decibels} \qquad (1.1)$$

That is for n=7 the signal: noise ratio at peak signal level is nearly 53 db. At low signal levels, however, the ratio reduces and would become unacceptable. To improve the small signal performance, non- linear quantisation is carried out in which the step size reduces with the signal level. In effect the signals are compressed at the encoder. At the decoder the inverse process of expansion is required to restore the signal to become a faithful replica of the original input signal. The processes of compression and expansion are together termed companding. This work describes a study of the application of non-linear companding to a particular form of encoder i.e. one using a binary counter.

Fig. 1.3

A SIGNAL SAMPLED AT A P.R.F. OF 8 KHZ.



DIFFERENCES BETWEEN INPUT AND OUTPUT SIGNAL INDICATE DISTORTION OR NOISE

Although the coding process introduces quantisation noise, p.c.m. systems offer considerable signal: noise advantage over other pulse systems. This may be seen from the following reasoning. Noise modulates the amplitude and to a smaller extent the duration of a pulse. Hence pulse - modulation systems will only operate satisfactorily if the noise variation is a small part of the amplitude or duration of the pulse. On the other hand, in a p.c.m. system the noise will vary the amplitude and timing of the "bit" pulses, but as long as the presence or absence of a pulse can be detected, noise will not degrade the modulation. The reliability of detecting the presence or absence of a pulse, however, is a function of signal: noise ratio. If this is too low, the output of the detector will occasionally be mistaken as a pulse when there is none. If the noise is assumed to be white gaussian, it will have a normal probability density function. That is, the probability of a noise burst exceeding any value, no matter how large, is never zero. It follows that even with the largest pulse power, there will be certain error rate due to received noise. It has been shown [29] that the probability of error in the presence of white noise is given by:-

$$p = \tfrac{1}{2}\left(1 - \operatorname{erf}\frac{V_o}{2\sigma}\right) \qquad \text{(1.2)}$$

where V_o = peak signal pulse

σ = r.m.s noise amplitude

and $\operatorname{erf} x$ = the error function

$$= \frac{1}{\sqrt{2}} \int_{-x}^{+x} \exp\left(-u^2/2\right) du$$

Values of p calculated from equation (1.2) are shown in table 1.1. It may be seen that in p.c.m. transmission there is a definite S/N threshold, at about 20 db, above which the error rate is negligibly small. This figure of 20 db may be compared with the S/N ratio of 60/70 db required for high quality A.M. or P.A.M. transmission of audio signals.

Table 1.1. Relation between error - rate and signal to noise power ratio in a p.c.m. system

S/N db	PROBABILITY OF ERROR	ERROR FREQUENCY. ONE ERROR EVERY
13.3.	10^{-2}	10^{-3} seconds
17.4	10^{-4}	10^{-1} seconds
19.6	10^{-6}	10 seconds
21	10^{-8}	20 minutes
22	10^{-10}	1 day
23	10^{-12}	3 months

P.c.m. offers two advantages in multiplexing and switching.

(a) Channel Multiplexing

As with other pulse methods of modulation (p.a.m. p.l.m. etc.) pcm lends itself to multiplexing on a time basis (t.d.m.) thus many channels (24 typically) may be accomodated on one pair of wires (for each way)

The system uses semi-conductors and components which are small and relatively cheap. This may be contrasted to a frequency-division multiplex (f.d.m.) system which requires expensive channel filters [1] That is, a p.c.m. transmission system should be less expensive than a f.d.m. system.

(b) Channel Switching

P.C.M. uses digital techniques so that it may be integrated with a t.d.m. switching system. This means that once the signal is encoded, it may be routed through electronic switches until it reaches the switch serving the called subscriber, when it may be decoded. P.c.m. can also be integrated with electronic controlled space - division switching (e.g. a system using reed relays). Hence p.c.m. is compatible with both modern switching techniques.

1.2. Historical Review of the Development of P.C.M.

Although p.c.m. was specified by Reeves [4] in French and U.S. patents in 1939 and 1942 respectively, organised development did not commence until after World War II. It would appear from the literature reviewed [5-26] that such development occured in two phases i.e. the post war - experimental era (1947 - 1957) and the "semi - conductor era" (1961 - present day).

In the first period (1947-1957) the reports were of two kinds.

(a) Descriptions of the instrumentation of experimental systems, mainly in the U.S.A. using thermionic valves.

(b) Descriptions of the principles and theoretical derivation of the properties of p.c.m.

In the second period of 1960 onwards the reports were more comprehensive studies by groups of workers. The papers reviewed covered the application of p.c.m. systems to local area telephony, television and programme distribution in the U.K. and France, in addition to the U.S.A.

1.2.1. Post War Period 1947-1956

In 1947, Black and Edson [5] at Bell Telephone Laboratories and Grieg [6] at Federal Communication Laboratories, both constructed five - digit multi-channel systems, based upon the Reeves method of pulse counting. In this method, the signal is sampled by a pulse train. The height of each sample produces a proportionate number of narrow pulses. These are applied to a binary counter so that each sample produces a code group of equivalent value. The receiver also used a binary counter as a decoder, and the principle of these methods is given in more detail in section 2.2. It is interesting to note that Black [5] reports that in the sampling process "the amplitude of the pulse is logarithmically related to the signal amplitude". The type of compandor, however, is not specified, but it maybe assumed that the compression occurs in a separate stage.

Goodall [8] in the same year described a 5-digit multi-channel system using comparators and gates. In principle, each sample is converted into the corresponding code group by a series of comparisons with the weights of the five binary digits. This method is termed Feedback-Subtraction, and is described in detail in section 2.3. Once again the decoder is functionally the reverse of the encoder.

In 1948, Meacham and Peterson [9] reported a new approach to coding. The signals from six speech channels are applied to the deflection system of a specially developed cathode ray tube, which produces the corresponding 7 - digit code groups. A beam tube cannot be employed conveniently for decoding, and so a simple method based upon a C.R. circuit, and originally proposed by Shannon, [2] was used. Three years later, in 1951, Goodall [12] outlined an experimental beam coding system for the transmission of a single television channel. The sampling frequency was 10 MHZ which meant that the coding process for one character had to be accomplished in 100 ns. The earlier tube was not capable of such high speed operation, and a tube operating upon a different principle, was developed. The principles of operation of beam tube encoders and Shannon-type decoders are described in detail in section 2.4. and 2.5.

Throughout the post-war period a number of papers were written which dealt with the principles and

properties of p.c.m. Since the subject of the research reported here, is concerned with the design of coders, only a brief review of the main points of each paper will be given here.

In 1947, Clavier, Panter and Grieg [13] showed the relation between signal to quantisation noise-power ratio and the number of levels when the latter were equally spaced. Bennet [14], in a comprehensive paper, in 1948, studied the relation between quantisation distortion and step-size, by considering the frequency spectra of quantised signals. In the same year, Oliver, Pierce and Shannon [15] discuss the properties of p.c.m. and the advantages over frequency modulation. A year later (1949) Clavier, Panter and Dite [16] show that when quantisation noise is smaller than the input noise, p.c.m. can bring about considerable improvement in the signal-to-noise ratio. In 1951, Panter and Dite [17] studied the effect of logarithmic quantisation upon quantisation distortion. In 1957, Smith [18] in a detailed study of logarithmic quantisation, describes a process for choosing the number of digits (i.e. the number of levels) and the degree of companding to establish a given signal to quantisation error ratio.

1.2.2. The Semiconductor Period 1962 - Present Day

The period under review was marked by the tremendous increase in the use of transistors and, later, integrated circuits. Such devices made the

p.c.m. time division system an economic practical alternative to the analogue frequency division system. Consequently the main papers of this period were concerned with operational p.c.m. systems.

In 1962, C.G. Davis of Bell Laboratories [38] described an experimental 24-channel, 8 digit telephony system, which, as the Bell T.1. system, was the first to become operational. One year later, in France, Mornet, Chatelon and La Corre [20-22] reported upon the application of p.c.m. to an integrated telephone network. Chatelon [21] describes an encoder in which the companding is given by a digital method. The companding action is based upon the fact that a logarithmic compression characteristic may be achieved by a piecewise-linear characteristic; (this topic is treated in more detail in section 2.6.).

Cattermole, Barber, Price and Smith [23] followed in 1963, with a paper dealing with the application of p.c.m. to local area telephony. The problem of transferring binary-coded signals through transformers, is discussed, and it is concluded that a unit disparity code is more convenient than simple binary code. The encoder appears to be relatively complex, as it incorporates 36 level comparators and a matrix of 36 x 7 cores.

During the period 1967-1968 the B.B.C. Research Department published a series of reports upon an investigation of p.c.m. for high quality sound signal distribution.

Howarth and Shorter [24] gave an appraisal of the requirements for the p.c.m. distribution of music signals. The use of instantaneous companding, to improve the signal to quantisation error ratio is discussed. On the basis of Chew's results, (see below), it is concluded that such methods are unsuitable for programme distribution. Chew and Inglis [25] describe experiments to test the distortion due to companding with diodes. They found that, even though the measured value of harmonic distortion was low, the distortion was audible. This result is commented upon further. Finally in another report Chew [26] discusses the choice of coding method. He describes a 11-bit encoder using a binary counter, operating at 80 MHZ, constructed from integrated circuits. Companding was not incorporated in the coder, although provision was made for its inclusion, as a separate stage. Hence the review commenced, and finishes with references to binary counter encoders. The research described here is an investigation into the same type of encoder, but one in which non-linear companding is incorporated. Before setting out the objects of the research, the principles of the main types of encoder will be described.

CHAPTER TWO

METHODS OF CODING AND COMPANDING

CONTENTS.

2.1. Methods of Coding

2.2. Coding by Bimary Counter

2.3. Coding by Feedback-Subtraction

2.4. Coding by Beam Tube

2.5. Miscellaneous Coding Methods

2.6. Methods of Companding

2.6.1. Continuous Companding Function by Diodes

2.6.2. Segmented Companding Function by Diodes

2.7. Objects of Present Research

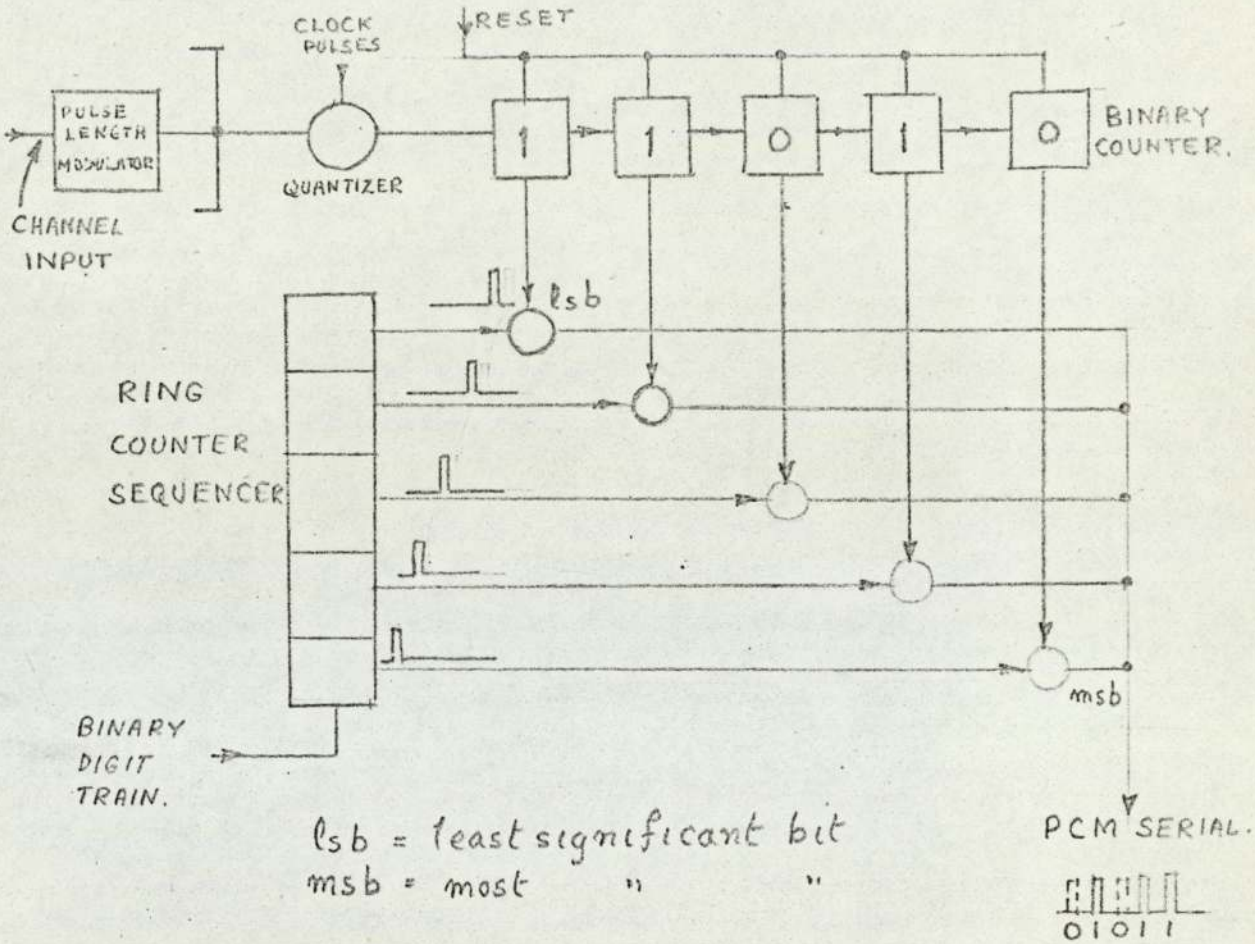
2.1. Methods of Coding

It appears from the review of the literature of the previous chapter, that there are three main coding methods, i.e. those incorporating binary counters, those using the feedback-subtraction principle, and those using beam-coding tubes. The principles involved in instrumenting the encoders and the corresponding decoders will now be described, using block diagrams in fig. 2.1 - 2.10. The first type will be described in greater detail, because the principles underlie the research being reported here.

2.2. Coding by Binary Counter

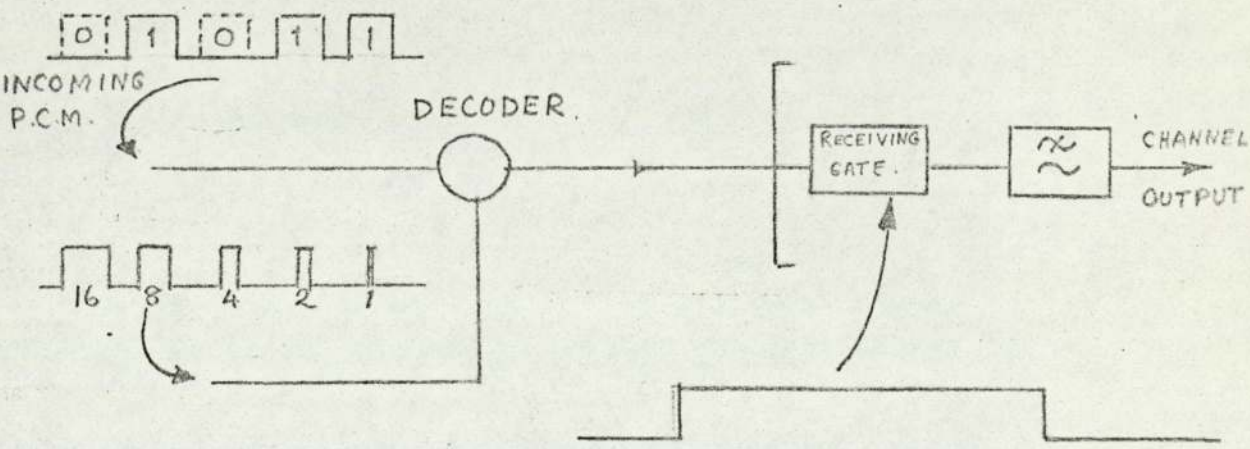
The principle of the coding methods used by Black[5], and Grieg[6] is as follows. In fig. 2.1 the signals from each channel modulate the duration of the channel pulse train (p.r.f. = 8KHZ). The length-modulated pulses from each channel feed a common quantizer. This consists of a gate which is opened by a channel pulse, to admit a pulse train of much higher p.r.f. ($\sim$ 1.6 MHZ). Hence successive "bursts", each containing up to 31 pulses (2^n -1) are applied to the coder, which is a 5-stage binary counter. The five counter outputs are gated by the outputs of a 5-stage ring counter which is synchronised at the binary digit rate (320 KHZ), so that a p.c.m. serial output is obtained. A typical code conversion is given in fig. 2.1 for the case when the instantaneous signal sample has a height in between 11 and 12 quanta. The corresponding channel pulse length, causes 11 dock pulses to be admitted through the quantizing gate. These step the counter forward from the reset

Figure 2.1 A 5-BIT BINARY COUNTER ENCODER



lsb = least significant bit
msb = most " "

Figure 2.2 BINARY COUNTER RECEIVING END.



condition to give the binary stage outputs as shown. The parallel-serial conversion gives the corresponding binary pulse code group 01011.

In both references (5) and (6) it is stated that the receiver is functionally the reverse of the transmitter, but the actual arrangement is not clearly specified. In his review Flood[7] writes "At the receiver the incoming code pulses operate a circuit which produces pulses whose lengths are proportional to the 'weight' of the digits represented by the incoming pulses." It is shown in fig. 2.2 that groups of such weighted pulses are passed to the appropriate channel gate, and demodulated by a low-pass filter. The actual decoding stage is shown as a gate, but in fact it consists of an input register whose outputs set the corresponding stages of a binary counter. These early coding systems were instrumented with thermionic valves. That is, a counter was formed from a cascade of double-triodes with diode steering, while a gate was formed from the pentode coincidence circuit.[27] The number of levels (32) was just large enough to provide the required signal: quantisation error ratio, necessary for transmissions of "toll" quality. High quality music and speech signals, however, require a peak signal to peak error ratio greater than 67db,[24] which, if the levels are equally spaced, will just be provided by a 11-bit system. A counter type coder for such a system would be difficult to instrument using thermionic valves, or indeed discrete transistors, for the following reason. The clock pulse frequency would need to be at least equal to (2 x number of

levels x highest signal frequency); that is, greater than 60 MHZ. Now in a "ripple through" binary counter (i.e. a cascade of bistable elements) a transition from logical 0 to logical 1 at the 8th stage can only occur when stages 1 to 7 have successively switched from 1 to 0. If the transition time per stage is 40 ns, the 8th stage will switch 320 ns after the input clock pulse. This time is nearly (20 x the clock recurrence period). Hence the outputs of long binary chains do not represent the exact count at high count rates.[27] With thermionic valves (and discrete transistors) the problem may only be overcome by a large increase in circuit complexity. From 1965 onwards, digital integrated circuits became available. These not only provided complete bistable elements with small transition times (typically 10 ns), but also facilitated the construction of synchronous-type counters, in which all transitions occur simultaneously.

The 11-bit coders due to Chew[24] were constructed from integrated circuits and block diagrams are shown in fig. 2.3 and 2.4. The encoder operates as follows. The input signal is sampled and compared with the voltage across a capacitor which is being charged with constant current. Just before the sample occurs the capacitor is short-circuited and the counter is reset. When the sample occurs, the short-circuit and reset conditions are removed; the capacitor voltage increases linearly, and the counter is stepped forward by the 80 MHZ clock pulses. When the capacitor voltage balances the sample, the comparator gives an output, which stops the counter. That is, like the

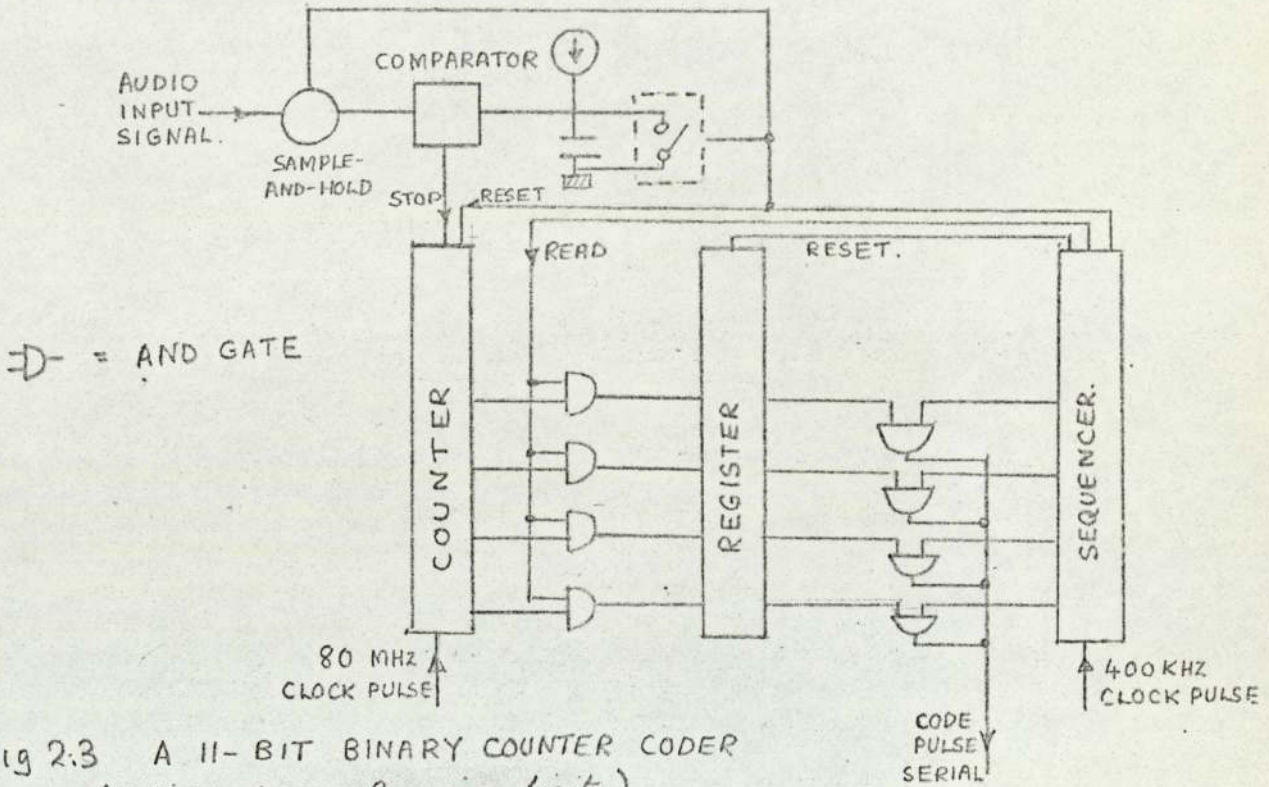


Fig 2.3 A 11-BIT BINARY COUNTER CODER
(4 bits shown for simplicity).

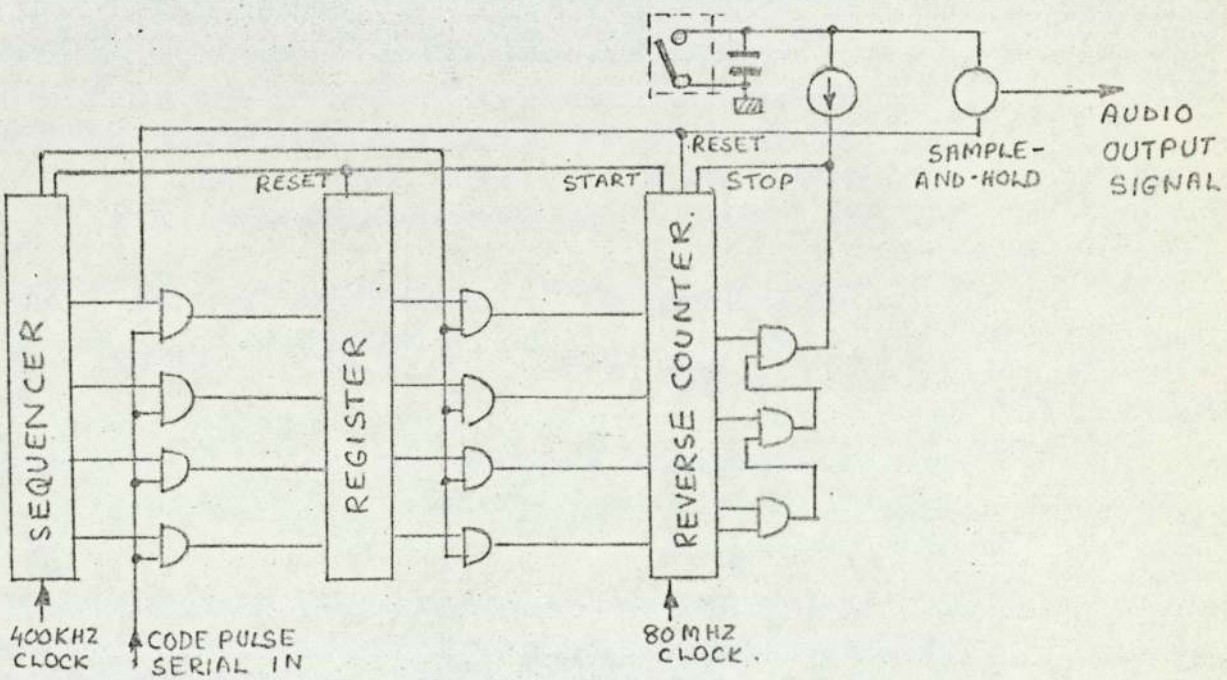


Fig 2.4 A 11-BIT BINARY COUNTER DECODER
(4 bits shown for simplicity)

earlier encoder shown in fig. 2.1, the counter stage outputs register, in binary code, the height of the sample. In this version of a counter encoder there does not appear to be a stage of pulse-length modulation. However, the ramp voltage across the capacitor produces a duration proportional to the amplitude. Note that the sampling p.r.f. was 30 KHZ, so that the time to execute the maximum count (2048), must be less than the recurrence period of 33.3 μs. In fact, with transition times per bistable of 13 ns, the maximum count time was some 26 μs. In this type of encoder the count corresponding to an instantaneous sample, occurs during the interval following that instant. The parallel-serial conversion must then occur while the next sample is being counted. Hence the need (a) to transfer a completed count to a register and, (b) to derive "reset" and "read" pulses from the sequencer.

The decoder for the 11-bit system is very nearly the encoder in reverse[24], (see fig. 2.4). The incoming p.c.m. serial undergoes serial to parallel conversion in the input register. The outputs of the latter set the corresponding stages of the reversing counter. The sequencer then gives the counter a start pulse to initiate a count-down, driven by the 80 MHZ clock pulses. A capacitor is simultaneously charged with constant current, the process being completed when the counter outputs are all at logical 0. The voltage on the capacitor is proportional to the weight of the code pulse group being decoded. A replica of the original modulating signal is obtained at the output of the low-pass filter.

2.3. Coding by Feedback-Subtraction

The principle of the Feedback-Subtraction method[8] is shown in fig. 2.5 and 2.6. The modulating signal is sampled, each sample charging up a capacitor in the STORAGE CIRCUIT, to its respective amplitude. This is compared with the first reference value, a pulse of height 16 quanta (the half maximum value). If the sample exceeds the reference, a binary pulse is gated through and amplified. This pulse is also fed back and delayed by an amount equal to the digit time interval. It then acts in the SUBTRACTION CIRCUIT to remove 16 quanta of charge from the capacitor. The remaining charge (or voltage) is compared with the second reference value of 8 quanta. Once again, if the charge exceeds the reference a second binary digit is transmitted and fed back. If, however, the capacitor charge is less than the reference, then no binary digit is transmitted. The feedback is zero, no charge is subtracted, and so the same charge is compared with the third reference value (one of 4 quanta). Hence it may be seen that a binary code pulse group is transmitted.

In the receiver (see fig. 2.6), a capacitor is charged up to the maximum level (32 quanta), and then successively reduced by the action of the incoming code group in the SUBTRACTION CIRCUIT. At the end of code group, the residual charge is measured and subracted from the initial maximum level, so that the total significance of a code group is given. Hence, the incoming p.c.m. is converted into p.a.m. samples which are demodulated by the low-pass filter.

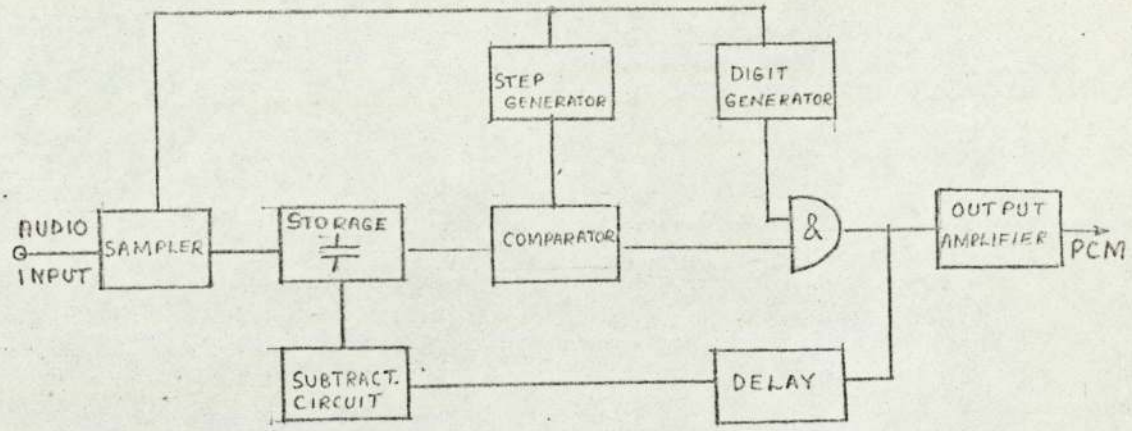


Fig. 2.5 THE ELEMENTS OF A FEEDBACK - SUBTRACTION CODER.

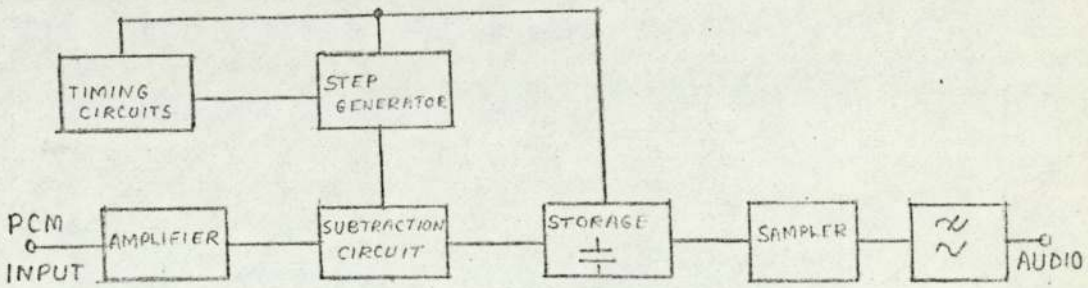


Fig 2.6 THE ELEMENTS OF A FEEDBACK SUBTRACTION DECODER

Coders of the Feedback-Subtraction proved more convenient to instrument than the counter type. Jarvis and Hutt[19] used the same principle, but with transistor current sources controlled by bistable elements, instead of a capacitor.

2.4. Coding by Beam Tubes

The beam coding system of Meacham and Peterson[9] represented a radical departure from the practice of coding with an arrangement of circuit elements. The whole coding process was accomplished in one tube. A functional diagram of the tube is shown in fig. 2.8 In it, an electron beam is arranged to scan an aperture plate in the x - direction, while the y - displacement is proportional to the amplitude of a signal sample. This arrangement may be compared with that in a cathode ray oscilloscope, in which the p.a.m. samples are displayed on a screen. In the coding tube, however, each p.a.m. sample gives rise to a corresponding train of binary digit pulses. To do this, the aperture plate contains seven columns of holes (see fig. 2.8), the first containing 2^6 holes, the second, 2^5 holes, etc. The lengths of the holes, in the y - direction, are such that when the beam scans a row of holes, it is interrupted in a binary sequence, whose weight is proportional to the y - deflection. The beam electrons which pass through a hole impinge upon the PULSE PLATE to cause a current pulse in the output circuit.

Accurate scanning of the holes in a row is difficult to

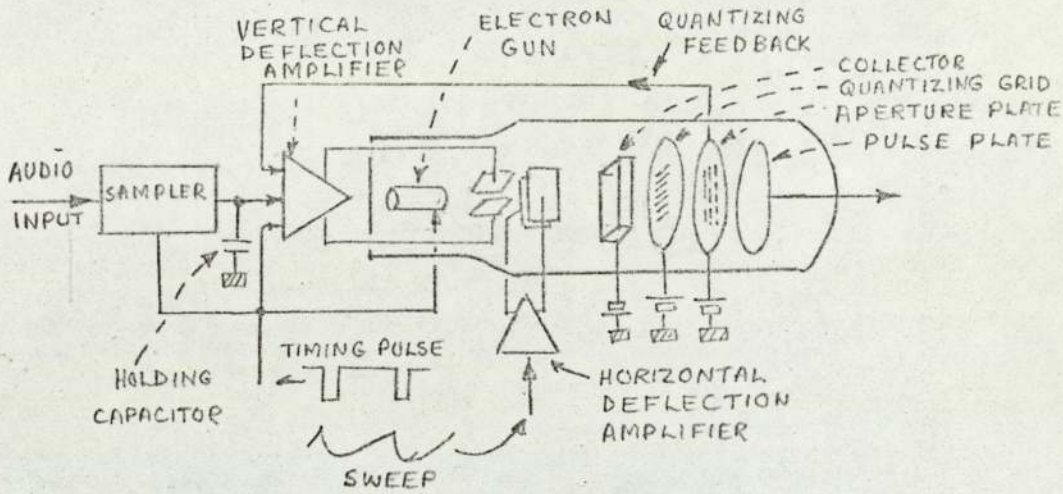


Fig. 2.7 FUNCTIONAL DIAGRAM OF CODING TUBE

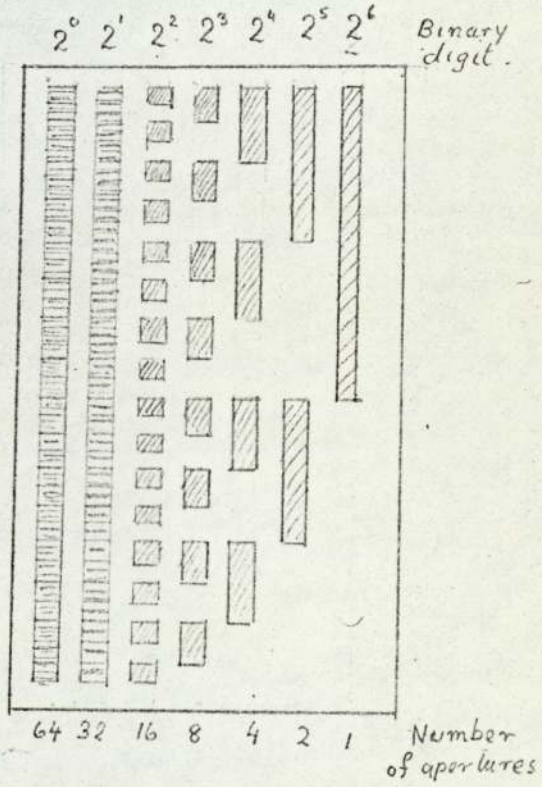


Fig 2.8 THE APERTURE PLATE.

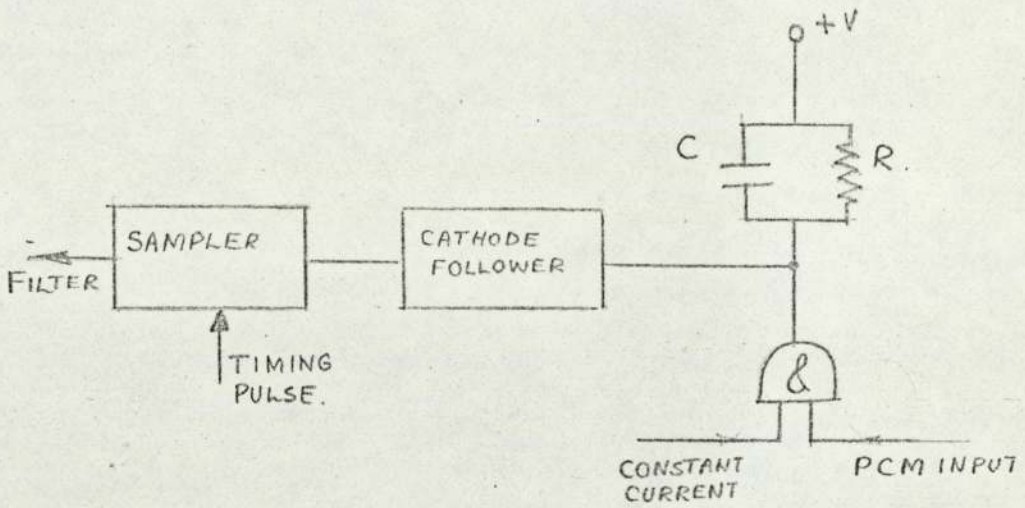
achieve without some controlling guide.[10] This is provided by the QUANTISING GRID, with its feedback connection to the y - amplifier and the COLLECTOR PLATE. The quantising mesh has 128 wires spaced so that a wire lies just below the top edge of each row defined by each of the 64 apertures and 64 spaces of the first column. The operation is as follows. When the beam is being scanned in the x - direction, the x - sweep controls a bias voltage to the y - amplifier, so that the beam tends to drift in the y - direction during the x - sweep. This movement, unless limited, would cause the beam to strike one of the wires. In such an event, secondary electrons would be emitted, and these would be captured by the collector plate. The resulting loss of current from the quantizing grid is fed back to the y - amplifier to control the quantizing bias. Hence the bias, which tends to move the beam in the y - direction, is limited to the value which sets the beam to pass just below the wire corresponding to the y - sample.

Although the idea of performing the quantization and coding operations in one envelope, offered an attractive solution to the coding problem, it does not appear to have been developed except by Goodall.[12] Three reasons are suggested. Firstly, there would not be sufficient demand for a specially developed tube, to reduce the cost of manufacture to an economic level. Secondly, with the increasing use of semiconductor devices with low voltages, in communications, it is undesirable, from an engineering

viewpoint, to incorporate high-voltage devices. Thirdly, the coding time is large, (due to the quantization-grid and feedback). Goodall[12] overcame this third objection by having a tube working on a different principle. The alignment errors were reduced by making the aperture plate produce a special code, (called "reflected" binary). This conversion to simple binary was made in the output circuit.

2.5. Miscellaneous Coding Methods

The principle of the Shannon decoder[2] is shown in fig. 2..9. The input binary digit train is reversed in time so that the least significant bit is directed to instantanteously charge a capacitor. The interval between bits is such that the charge decays exponentially by one half. In the example shown the 2^1 bit is absent so that the charge falls to one quarter of the initial value by the time of arrival of the 2^2 bit. Hence the net charge after the final interval is 13/15 of the total charge which would have been given if the 4-digit train had been complete. Hence the voltage input to the cathode follower is proportional to the total weight of the incoming code pulse group. The output of the cathode follower is applied to a sampling gate with appropriate channel pulses, so that p.a.m. samples are produced. These are demodulated with a low-pass filter to obtain a copy of the original modulating signal.



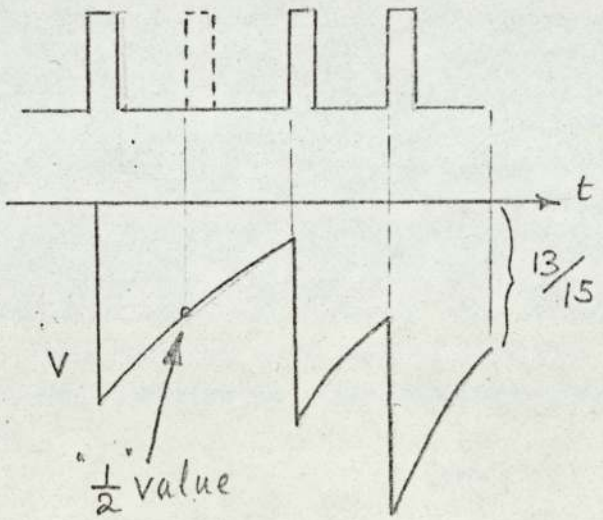
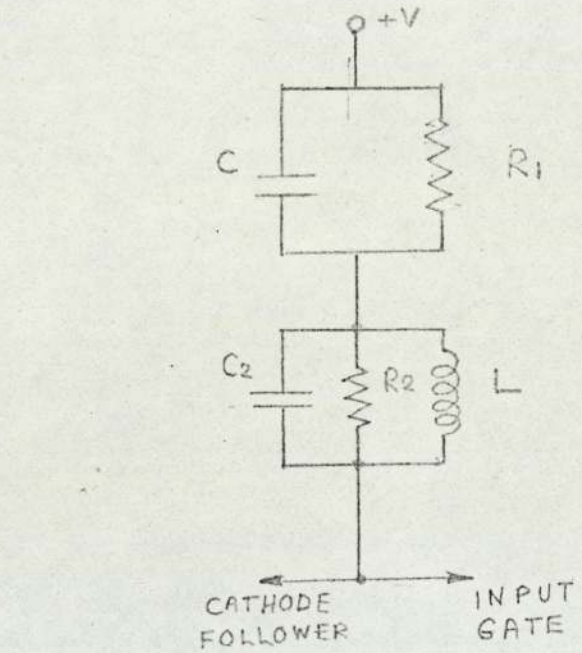


Fig 2.9 THE SHANNON DECODER WITH WAVEFORMS.

A disadvantage of the simple CR circuit is the uncertainty which occurs, because the more significant digits give contributions of charge on the steep parts of the exponential curve. The slope of the exponential curve is large for these digits and therefore precise timing of binary digit pulses is required.[11] A modification, suggested by Rack, largely overcomes this limitation. A parallel branch circuit, LC_2R_2, resonant at the 'bit' rate is connected in series with the Shannon circuit, C_1R_1 (See fig. 2.10). By properly choosing C_1, C_2, R_1 and R_2, the first (and second) derivatives of charge are made zero at successive points one pulse period apart. Hence, the charge decay curve has zero slope when the binary digit pulses occur, and timing is less critical.

These CR decoders although simple and elegant in operation, appear to have been used only for those systems, where the receiving-end cannot use the same method as the sending-end. One possible reason for this, is the need to reverse the order of code pulse group from the conventional one, of sending the most significant bit first.



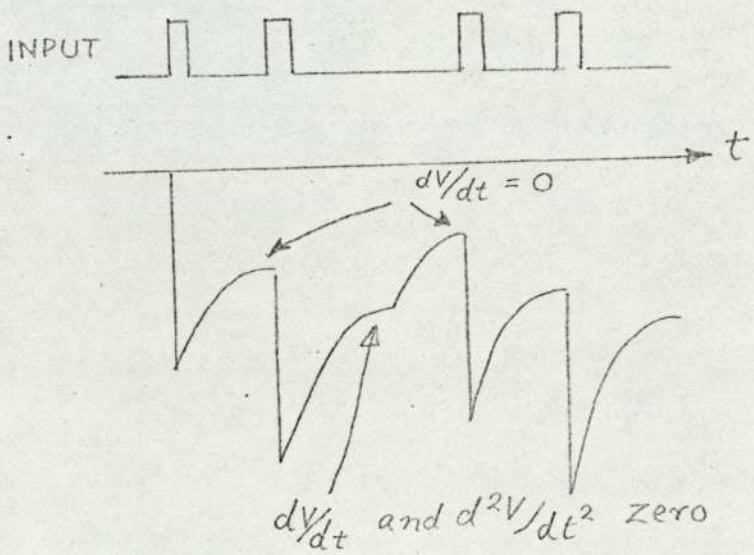


Fig 2.10 THE RACK MODIFICATION TO THE SHANNON DECODER WITH WAVEFORMS

2.6. Methods of Companding

Companders are of two main types (a) SYLLABIC and (b) INSTANTANEOUS. The former have been used[30] for many years in radio and carrier-telephony systems to maintain adequate signal/noise ratio at low signal levels, and are not relevant here. Instantaneous compressors are used in p.c.m. systems to increase the signal:quantisation error ratio at low levels.

It has been shown[17,29] that a logarithmic companding characteristic is desirable, and that if v and u are respectively the normalised input and output (compressed) amplitudes respectively, then u is given by:

$$u = \pm \frac{\log(1 \pm \mu V)}{\log(1+\mu)} \quad - - - - - - - - (2.1)$$

In this expression, μ is the compression parameter, (usually having a value between 5 and 500), and gives the degree of companding. The companding characteristic may be a continuous curve as shown in fig. 2.11, or it may be a piece-wise linear curve of two or more segments,[33] as shown in fig. 2.12.

2.6.1. Continuous Companding Function by Diodes

The p.n. junction diode has an approximate logarithmic current/voltage characteristic, and has been much used as a companding element.[19,25] The principle of the balanced diode compander is shown in fig. 2.13. Resistances R_1 and R_2 have values such that the compressor output follows the input signal current, while the expander output follows the input

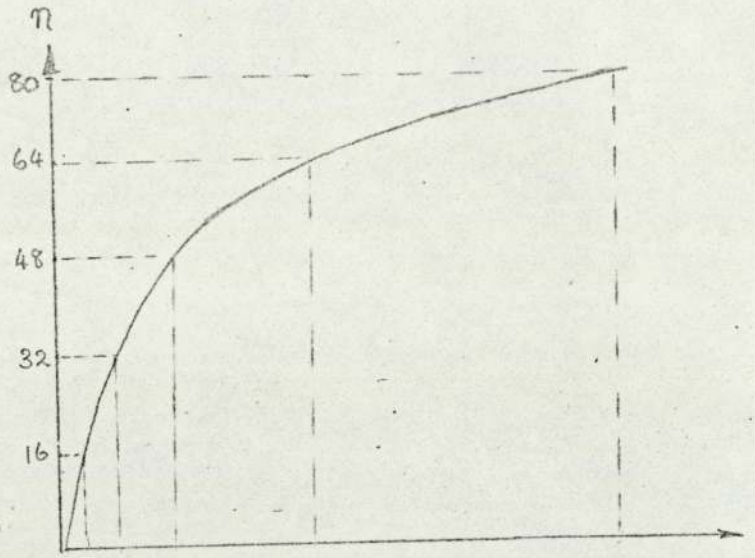


Fig. 2.11 SMOOTH COMPANDING CHARACTERISTIC

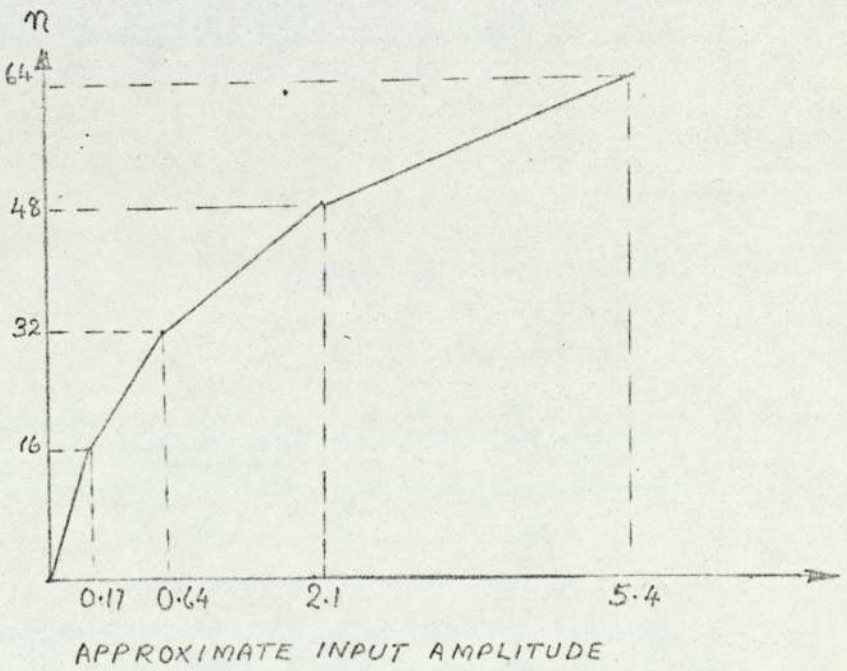
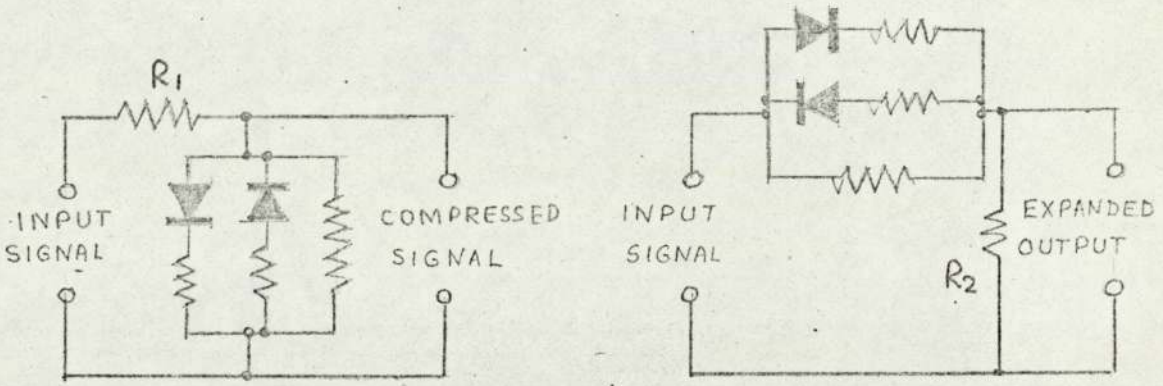


Fig. 2.12 4-SEGMENT CHARACTERISTIC.

FIGURE 2.13



THE COMPRESSOR THE EXPANDER.

BALANCED DIODE COMPANDORS WHICH GIVE SMOOTH CHARACTERISTICS

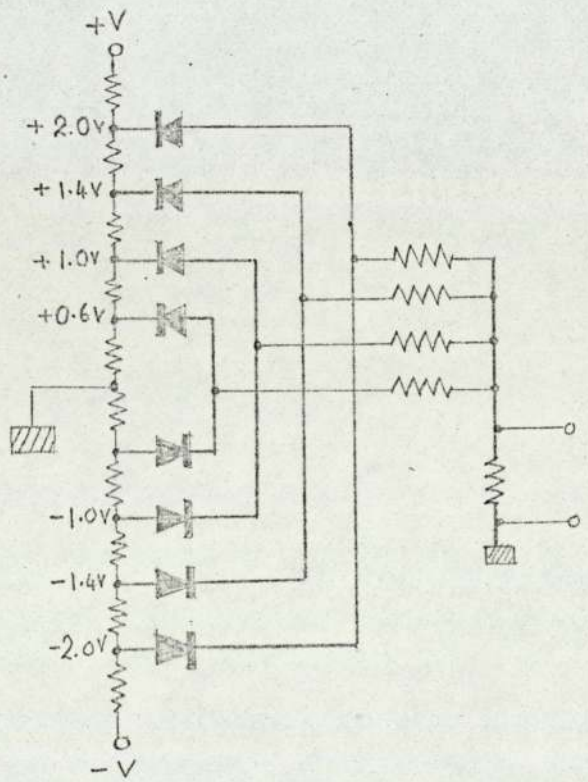


FIGURE 2.14 A DIODE COMPANDOR WHIGH GIVES A SEGMENTED CHARACTERISTIC.

signal voltage. The two circuits have inverse transfer characteristics if the diodes in the two units have identical characteristics.

There are a number of disadvantages which limit the usefulness of diodes as companding elements:-

(i) the i/v characteristic of a two-terminal device cannot be conveniently varied by external bias; therefore the compression parameter (μ) cannot be readily controlled, and elements in the compressor and expander cannot be readily matched.

(ii) the small range of junction voltages (700 mV for silicon) required to give a change of current from maximum to minimum, implies precise control of voltage at the expander.

(iii) the forward biassed junction is temperature sensitive for $\log(\propto V/T$. This suggests that temperature control is desirable[25] to maintain matching of characteristics at sender and receiver.

It is shown in chapter 7 how the use of junction field-effect transistors overcomes the most serious of these disadvantages.

2.6. Methods of Companding

2.6.2. Segmented Companding Function by Diodes

The disadvantages, given above, for the diode compander may also be overcome by the segmented compander[19,33] shown in fig. 2.14. Here there are two sets of diodes; one for each half cycle of signal. All the diodes conduct at maximum signal current, but as the signal is reduced the number of conducting diodes falls. The forward resistance of a diode is swamped by the resistance in series, giving a five-segment characteristic, which will be independent of the diode characteristics. The companding law may be controlled by the series resistances.

Hence, it may be seen that the segmented compander has the advantage of instrumental convenience.[19] There is, however, some degradation in signal:noise ratio[33], as compared with a compander giving a smooth characteristic. It would therefore appear advantageous to use a companding element with a quasi-logarithmic i/v characteristic which may be controlled precisely. It is considered that the junction f.e.t. is just such a device.

2.7. The Objects of Present Research

In the first chapter the history of p.c.m. has been reviewed primarily to show that the first encoders were of the pulse-count type. Even the idea of logarithmic compression in such an encoder is not new. The early encoder of Black and Edson[5] probably incorporated a non-linear compander, as a separate stage in the signal path. The pulse-count method could not, however, be conveniently applied to high-quality multi-channel systems, using discrete components, and subsequent development of the Feedback-Subtraction method occurred. With the advent of integrated circuits, Chew[26] has demonstrated that a 11-bit counter-type encoder may be made.

At the outset of this investigation there did not appear to be a pulse-count coder in which non-linear companding is an integral part of the coding process.* This is rather surprising, since in the basic Reeves method there is a p.l.m. stage which may be made to follow a quasi-logarithmic law. A theoretical study of this method and other related methods of companding is given in chapter 3, while the experimental investigation of the basic method (termed Method 1) is described in chapter 4. From the theoretical study one method emerged which could be more conveniently instrumented at both sending and receiving ends. A description of this coder is given in chapters 5 - 8 inclusive.

* Cattermole[33] mentions a possible coding technique where the frequency of the clock pulses is varied in discrete steps, to give a segmented companding law.

The two most important stages of the coder are a clock-sweep generator and a linear voltage-frequency converter. It was decided to use integrated circuits where possible and this led to the design of a dual monostable-astable voltage-frequency converter, which is described in chapter 6 .

During the investigation it was found that junction field-effect transistors (f.e.t.) had certain advantages over diodes, as companding elements. Hence these have been used in the clock-sweep generator; an account of this work is given in chapter 7 .

The other stages of the coder, such as the synchronous binary counter and parallel-serial converter etc. are fairly well known. It is considered, however, that some of the methods of synchronising and interconnecting these stages, are now, and this part of the work is reported in chapters 5 - 8

The results of tests carried out on the encoder and decoder are given in chapter 8 , while the work is concluded in chapter 10 .

CHAPTER THREE

AN APPRAISAL OF FIVE METHODS OF INCORPORATING COMPRESSION IN PULSE-COUNT ENCODERS

3.1. Statement of Methods

3.2. Coding by Methods (1) and (2)

3.3. Coding by Methods (3) and (4)

3.4. Coding by Method (5)

3.5. The Expansion for Decoding

3.6. Decoders for Methods (1) and (5)

3.1. Statement of Methods

It has been stated in chapter 2 that an instantaneous compressor should have a transfer characteristic [18,29] :-

$$U = \pm \frac{\text{Log } (1 \pm \mu V)}{\log (1 + \mu)}$$

In a p.c.m. system the compressed normalised voltage ($\pm$ V) is uniformly quantised in a number of levels 1 up to a maximum value L. Thus 1 is given by

$$1 = \frac{L}{2}\left[1 \pm \frac{\log (1 \pm \mu V)}{\log (1 + \mu)} \right] \quad \text{-----(3.1)}$$

Now, in a pulse-count encoder the channel pulse is usually length-modulated by the signal, and is then gated with short-duration clock pulses so that the number of the latter contained within the duration (T) of the channel pulse is the number of levels 1, as shown in (fig. 3.1.)

To incorporate the companding process in the p.l.m. stage merely requires that the channel pulse duration (T) be varied according to equation (3.1). For single-edge length-modulation the trailing edge of the channel pulse is varied by the modulating voltage, so that the duration is given by:

$$T = To \pm \Delta T$$

where $\pm \Delta T$ corresponds to positive and negative modulation. Hence for logarithmic companding in the p.l.m stage:-

$$T = To \left[1 \pm \frac{\log (1 \pm \mu V)}{\log (1 + \mu)} \right] \quad \text{-----(3.2)}$$

This expression implies that the duration T is zero when V = -1. This is clearly inconvenient in practice and so equation (3.2) is modified as follows:-

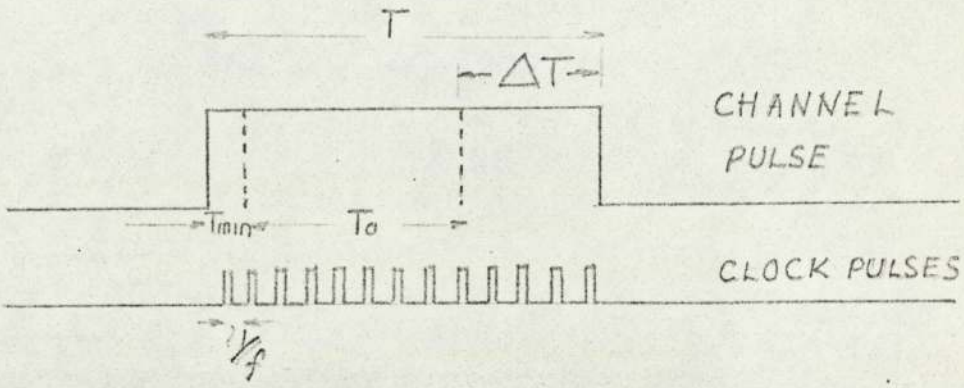


Figure (3.1) PRINCIPLE OF PULSE-COUNT METHOD

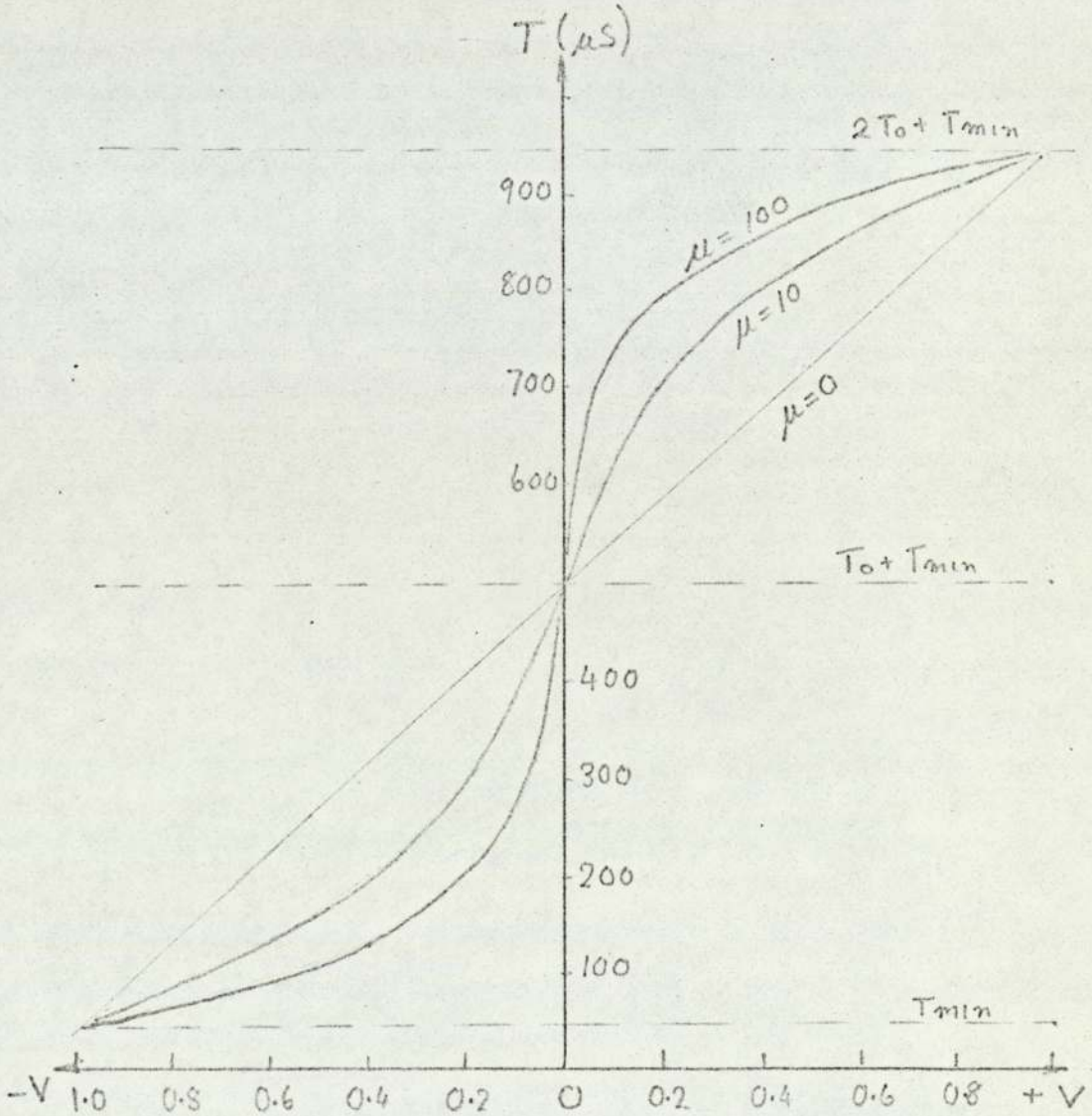


Figure (3.2) VARIATION OF CHANNEL PULSE DURATION(T) WITH MODULATING SIGNAL (V)--- METHOD 1

$$T = T\,min + To\left[1 \pm \frac{\log(1 \pm \mu V)}{\log(1+\mu)}\right] \qquad (3.3)$$

The variation of T with V is shown in fig 3.2 If now the clock p.r.f.(f) is constant at fo, then the number of levels corresponding to an input V is given by:-

$$1 = fo\,(Tmin + T) = fo\left\{T\,min + To\left[1 \pm \frac{\log(1 \pm \mu v)}{\log(1+\mu)}\right]\right\} \qquad (3.4)$$

Now, equation (3.4) has been derived for the method in which T alone is modulated. Examination of equation 3.4 shows that the same companding law would be given if T was held constant, and the clock p.r.f. (f) was modulated. Also two further methods may be possible if the signal modulates both T and f, one linearly, and the other in a way to be determined. It may be noted that these additional methods have become possible because the channel modulating and companding functions have been separated. In fact the principle of four methods may be defined as follows. The waveforms of channel and clock pulses during a modulating signal interval, for the four methods are shown in fig. 3.3

Method (1) A pulse-length modulator where the duration of the channel pulse is a particular logarithmic function of the modulating signal amplitude. The length-modulated pulses are then gated by very short duration pulses of constant p.r.f. so that the number of pulses contained within the duration of a given channel pulse is proportional to the logarithmic function of the modulating voltage.

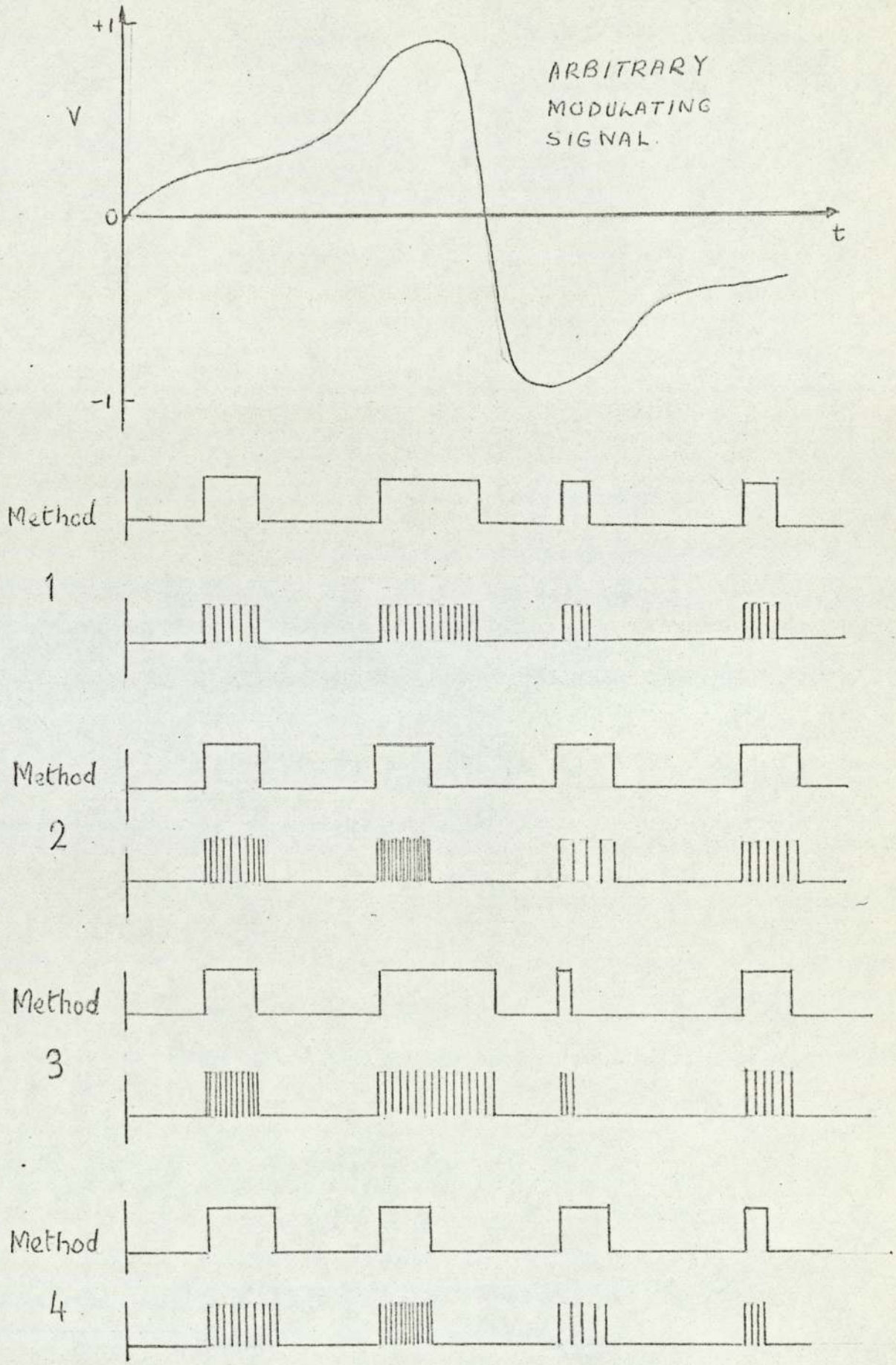


Figure (3.3) CHANNEL AND CLOCK PULSES FOR FOUR CODING METHODS

Method (2) The channel pulses are of constant duration and are gated by short duration pulses, whose p.r.f. is the particular logarithmic function of the modulating signal amplitude. The number of gate pulses contained within the duration of a channel pulse is the same as for Method (1)

Method (3) A pulse duration modulator where the duration of the channel pulse is a linear function of the modulating signal. The length-modulated pulses are gated by very short duration pulses whose p.r.f. is a non-linear function of the modulating signal. The number of gate pulses contained within the duration of the channel pulse is the same as Method (1)

Method (4) The duration of the channel pulse is a non-linear function, while the clock p.r.f. is a linear function of the modulating signal. The number of clock pulses is again the same as for Method (1) A positive increase in modulating signal causes the duration (τ) to decrease non-linearly, and the clock p.r.f. to increase linearly. Once again the number of clock pulses for one channel pulse is the same as for Method (1). A fifth method may now be defined if the compression is applied by a sweep voltage.

Method (5) The signal linearly modulates the length of the channel pulse, while the clock p.r.f. is swept (ina manner to be determined) during the channel pulse duration. The waveforms of the channel, clock and clock sweep pulses are shown in fig. 3.4.

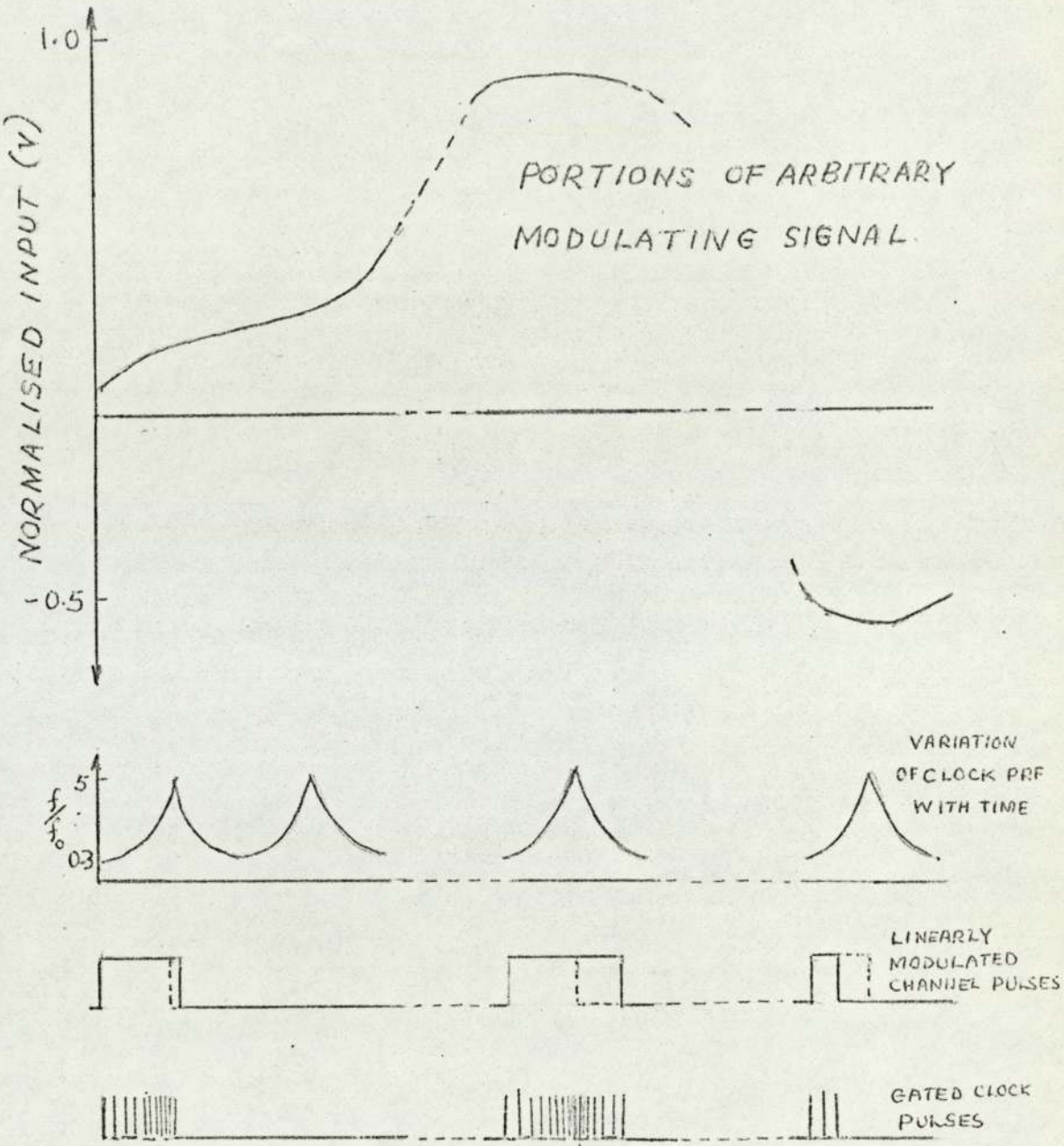


Figure (3.4) CHANNEL, SWEEP AND CLOCK PULSE WAVEFORMS FOR METHOD 5.

Each of the five methods will now be studied in order to:

(a) show how the channel pulse duration, clock p.r.f. and modulating signal are related;

(b) review possible systems for instrumenting each encoder;

The principles of expander action in the corresponding decoders are discussed, together with the principles of instrumentation of two of the decoders. Finally, it is concluded that one method is inherently more convenient to instrument in both the encoder and decoder.

3.2. Coding by Methods (1) and (2)

This first method is basic, and the principle has already been given in the introduction to the five methods stated in section (3.1). The channel pulse duration T is given by equations (3.2) and (3.3) while the clock p.r.f. has a constant value (f_0). The variation of T with modulating signal (v) is shown in figure 3.2. It may be noted that the number $(1 \pm \mu V)$ is always positive, for the (-) sign occurs with negative values of v.

A block diagram showing the components required to instrument this method is given in fig. 3.5(a). The stages of divider, sequencer, gate, binary counter and output register are common to all the coding systems described in this chapter, and their functions are outlined first of all.

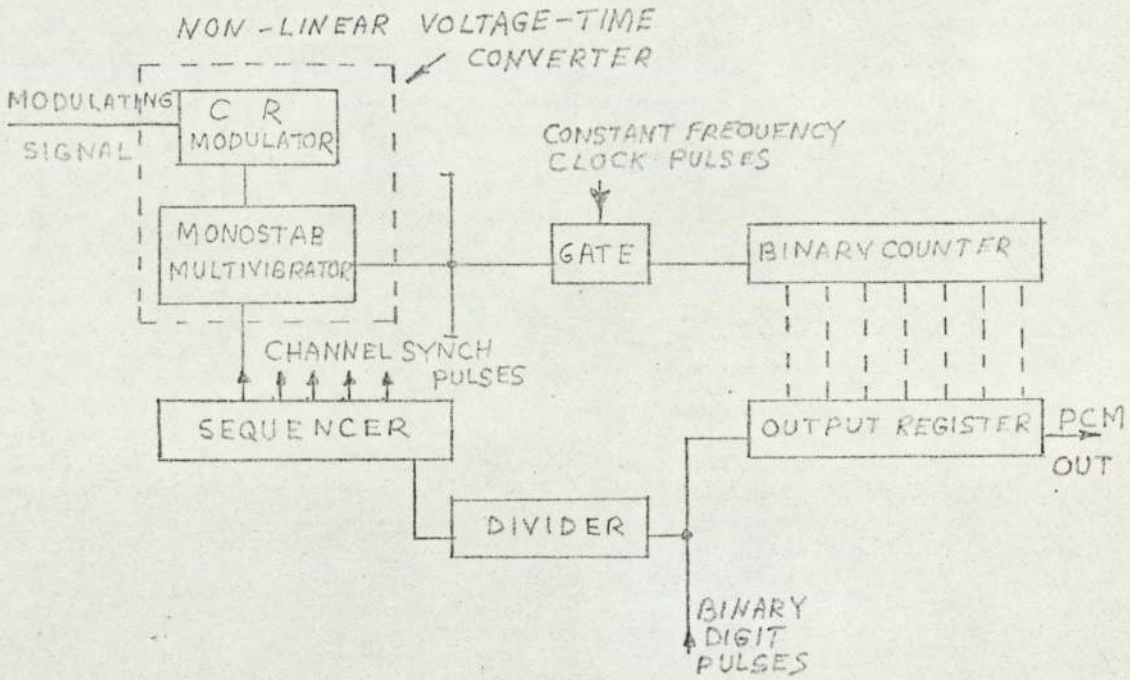


Figure 3.5(a) ENCODER FOR METHOD 1

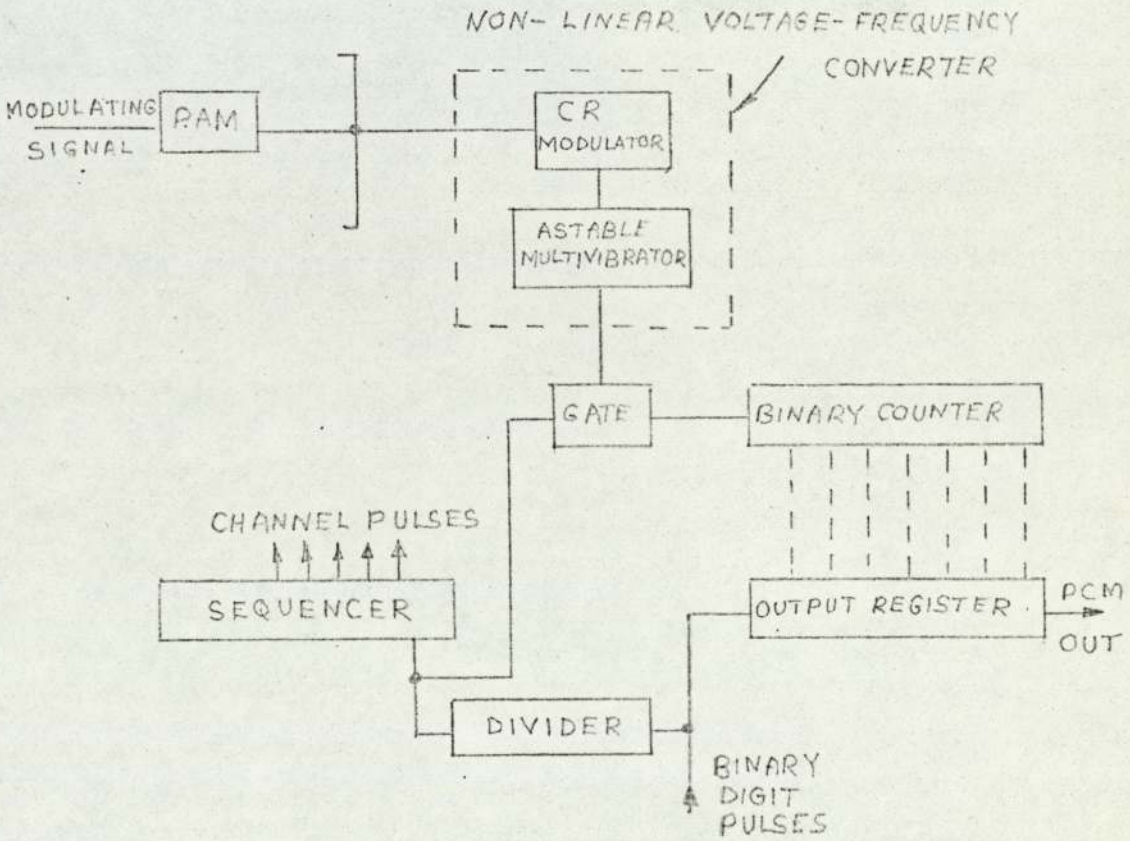


Figure 3.5(b) ENCODER FOR METHOD 2

The Divider

The binary digit train should be synchronised with the channel pulse train. Hence a 'bit' train of frequency f_b at the input to a divider, formed by a cascade of n bistables, is used to give a synchronising pulse of period $2^n/fb$ to the sequencer.

The Sequencer

The pulse train of frequency $f_b 2^{-n}$ is applied to the channel sequencer, which may be formed by a ring counter of m bistables. Each of the bistables gives a channel synchronising pulse of duration $2^n/f_b$, and repetition frequency $f_b 2^{-n}/m$, i.e. there are m pulses in a frame.

The Gate

The channel pulse which may be length-modulated (as in Methods (1), (3), (4) and (5), is used to gate a number of high frequency clock pulses, which may be frequency-modulated (as in Methods (2), (3), (4) and (5)).

The Binary Counter

The gated clock pulses are applied to a binary counter, so that the bistable outputs register the number of clock pulses in binary code.

The Output Register

The counter stage outputs are transferred to the corresponding stages of the output register, at the end of a channel synchronising pulse, to enable the binary code to be given out in serial form.

The main component of the system for Method (1) is the voltage-time converter where the duration T is varied by the modulating signal (v) in accord with eqn. 3.3. This length-modulation may be realised with a monostable multivibrator which has 3 - terminal active devices for the elements of the timing circuit. The input modulating signal samples vary the resistances of the devices, and hence vary the period T.

An experimental investigation into the feasibility of these ideas is described in Chapter 4 and it will be seen that a major difficulty arises in that the transfer characteristics for positive and negative modulation are not identical.

A further disadvantage of the first method brought out in section 3.6, is that the instrumentation of the corresponding decoder is extremely complex.

The secondmethod is very similar to the first. The channel pulse duration, however, has a constant value To, while the signal modulates the clock p.r.f.(f). The relation between f and v may be obtained from equation (3.4) which applies to all of the methods (1-5). For constant To,

$$f = f_{min} + f_o \left[1 \pm \frac{\log(1 \pm \mu V)}{\log(1+\mu)} \right] \text{ ---- } (3.5)$$

The variation of f with v is similar to the variation of T for method 1 shown in fig (3.4) The range of values of f for positive, zero and negative modulation have been

calculated from equation (3.5.) for a high-quality telephony system. These are shown in Table 3.1, and it may be noted that f must vary over a 10:1 range for negative and positive modulation. This is a wide range for a voltage frequency converter to operate precisely in accord with some particular law. In addition, the similarity to Method (1) suggests that similar disadvantage will apply. The instrumentation of an encoder for Method 2 is shown in fig.3.5(b)

It may be noted that there are two distinguishing features in the block diagrams for the first two methods.

(a) In the first method the channel pulse is length modulated in a non-linear voltage-to-time converter, while in the second method the clock p.r.f. is modulated in a non-linear voltage-to-frequency converter.

(b) Multiplexing in Method (1) is achieved in the p.l.m. stage, while in Method 2 a separate p.a.m. stage of channel gating is required.

3.3 Coding by Methods 3 and 4

In the third method, the signal modulates both the channel pulse duration T, and the clock p.r.f.(f). On the one hand, T varies linearly with v, so that the channel pulse length is given by:

$$T_2 = T_{min} + T_0 (1 + V) \quad \text{-----} \quad (3.6)$$

Table 3.1.

Variation of Clock Frequency for Method 2

	HIGH QUALITY SOUND SYSTEM
Highest Modulation Frequency (fm)	15 KHz
Channel p.r.f. (2fm)	30 KHz
Channel recurrence period $\frac{1}{2fm}$	33 μs
No. of channels	2
Unmodulated channel duration	8 μs
No. of levels for each half cycle	256
Unmodulated clock p.r.f.	6.4 MHz
Minimum clock p.r.f.	32 MHz
Maximum clock p.r.f.	64 MHz

On the other hand, f varies so that the logarithmic companding law is given, To show the relation between f and v, consider the number of levels given by the number of clock pulses within a duration T. This is given by:-

$$l = \int_0^{(2T_o + T_{min})} f\,dT \qquad \text{---------(3.7)}$$

The modulating signal period, however, is much greater than the channel pulse duration T, so that to a first approximation f does not vary during the duration T. Hence, the integral may be omitted and the clock p.r.f. is given by combining equation (3.4) and (3.6) to give :-

$$f = \frac{f_o}{T_{min} + T_o(1+V)} \left\{ T_{min} + T_o \left[1 \pm \frac{\log(1 \pm \mu V)}{\log(1+\mu)} \right] \right\} \quad \text{...(3.8)}$$

The variation of f with v, for various values of μ, given by equation (3.8) is shown in fig 3.6. It may be noted that f = fo at values of v equal to zero, and $\pm$ 1. At intermediate values of v, the clock p.r.f. increases by 20% for positive modulation and decreases by 40% for negative modulation. To gain more symmetry between the curves for positive and negative modulation, the minimum value of T may be increased.

The instrumentation of a system obeying the principles of Method (3) may appear complicated, at first sight. The variation of clock p.r.f. with modulating signal v is not unlike the I/V characteristic of a device, which can exhibit both positive and negative resistance. If such a device precedes a linear voltage-frequency converter, the output voltage may be made to have a frequency which is the required function of the input voltage.

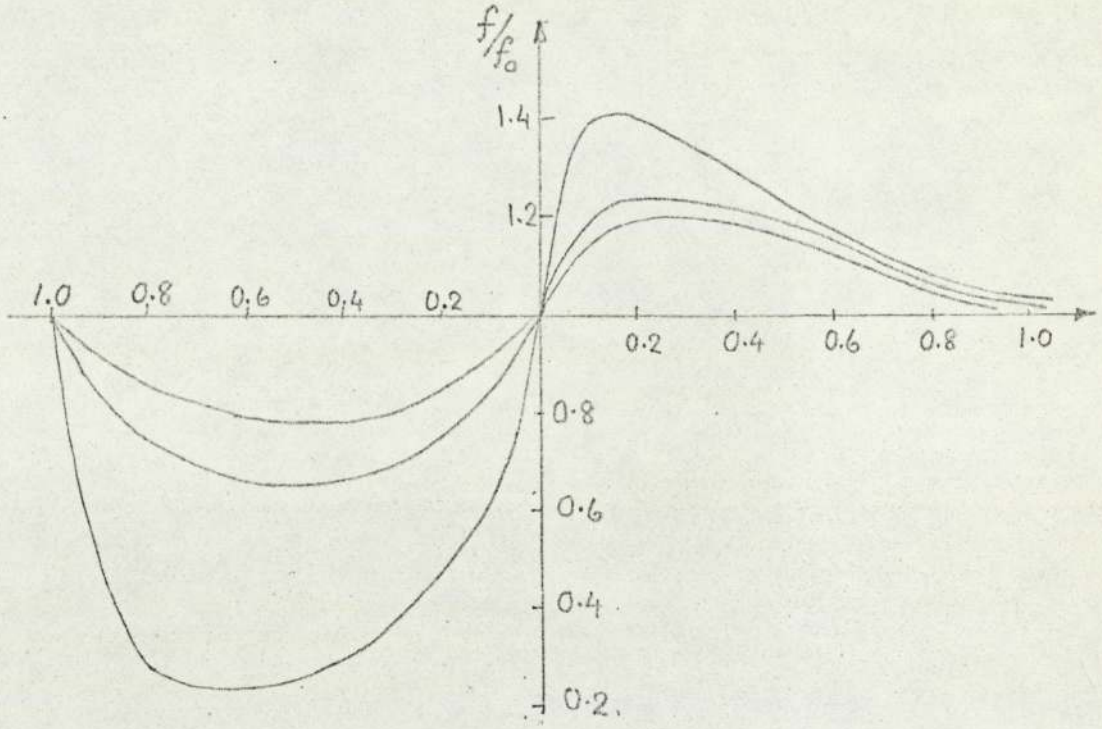


Fig 3.6 VARIATION OF CLOCK FREQUENCY (f) WITH MODULATING SIGNAL FOR METHOD 3

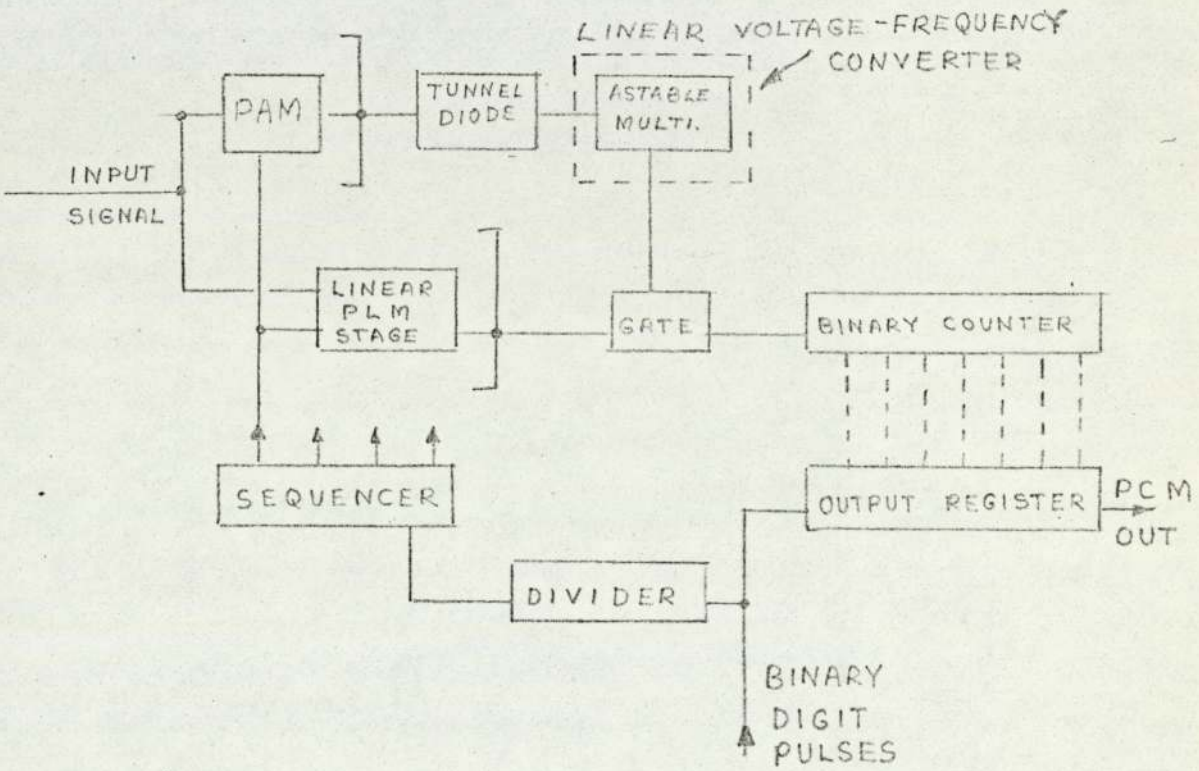


Fig. 3.7 ENCODER FOR METHOD 3

Such devices as tunnel diodes have negative resistance characteristics, and while no particular diode may have an I/V characteristic which will permit the clock p.r.f. to obey equation (3.8) exactly, it may suffice to use the same type of diode in the encoder and decoder in the same mode of operation. A block diagram of an encoder working on these lines is shown in figure 3.7, while typical waveforms are shown in fig. 3.3. It can be seen that the instrumentation of this encoder is considerably more difficult than the two encoders described previously, for two reasons.

Firstly, a device with an I/V characteristic exhibiting negative resistance is required to be driven from a source of low resistance, so that the resulting current follows the variation required for the clock p.r.f, which is shown in fig 3.5. It is considered that such operation may well be unstable.

Secondly, the signals from different channels have to be multiplexed in both the p.a.m. and p.l.m. stages. It is thought that this double process will produce timing errors and false counts.

The fourth method is very similar to the third method, but the T and f functions are interchanged. Hence, similar principles may be applied to the instrumentation; that is a linear voltage-time converter maybe preceded by a device with a "negative resistance" I/V characteristic.

Obviously, this method will be no less complicated than the third method and hence no block diagram is shown.

3.4. Coding by Method 5.

In the previous four methods, the logarithmic companding is obtained by applying the modulating signal to a device which controls the channel pulse duration (T) and/or the clock p.r.f. (f).

In Methods (3) and (4), one parameter (T or f) is subjected to linear modulation, and the departure from linearity (to obtain the companding law) is arranged by causing the modulating signal to vary the other parameter (f or T)

In the fifth method, the channel duration is subjected to linear modulation, but the clock pulse train is given by an independent variable-frequency generator. To obtain the required departure from linearity, the clock p.r.f. must be varied so that, during a given channel pulse, the number of clock pulses corresponds to the level of the modulating signal. Hence the clock p.r.f must depend upon the channel pulse duration (and modulating signal). At this point, it may well appear that Methods (5) and (3) are effectively the same, for in both the channel pulse duration is given by equation(3.6), re-written below:-

$$T = T_{min} + T_o (1 + V) \quad \text{---------- (3.6)}$$

In the fifth method, however, the clock p.r.f. is swept within the duration of the channel pulse, according to a certain law. To show this law, the integral form for the number of levels given in equation (3.7) is recalled:-

$$l = \int_{0}^{(2T_o + T_{min})} f\,dT \qquad \text{- - - - - - -} \quad (3.7)$$

If T is given by equation (3.6), then dT = To dV. Now the number of levels or clock pulses contained within a given channel pulse duration is the same for all pulse-count methods, and is given in equation (3.4). Hence it follows that:

$$T_o \int f\,dV = f_o \left\{ T_{min} + T_o \left[1 \pm \frac{\log(1 \pm \mu V)}{\log(1+\mu)} \right] \right\} \qquad \text{- - - - -} \quad (3.9)$$

Differentiating (3.9) w.r.t. V gives the following expression for the clock p.r.f.:-

$$f = \pm \frac{\mu f_o}{\log(1+\mu)} \left\{ \frac{1}{1 \pm \mu V} \right\} \qquad \text{- - - - - - -} \quad (3.10)$$

Although equation (3.10) shows the clock p.r.f. as a function of signal input V, it is from (3.6) an implied function of duration (T). This time-dependence may be seen, when V is replaced by $\left[\frac{T - T_{min}}{T_o} - 1 \right]$ in equation (3.10). i.e $f = \frac{\mu f_o}{\log(1+\mu)} \left\{ \frac{T_o}{T_o \pm \mu [T - T_{min} - T_o]} \right\}$ - - - (3.10a)

The variation of f in the channel pulse duration is shown in figure (3.8), for various values of μ, while the variation throughout a typical modulation period is shown in figure (3.4). It may be noted from fig (3.8) that the clock p.r.f. varies rapidly with time at values near to To, especially when there is a moderate degree of companding. Also, the clock p.r.f. variation is symmetrical for both positive and negative modulation.

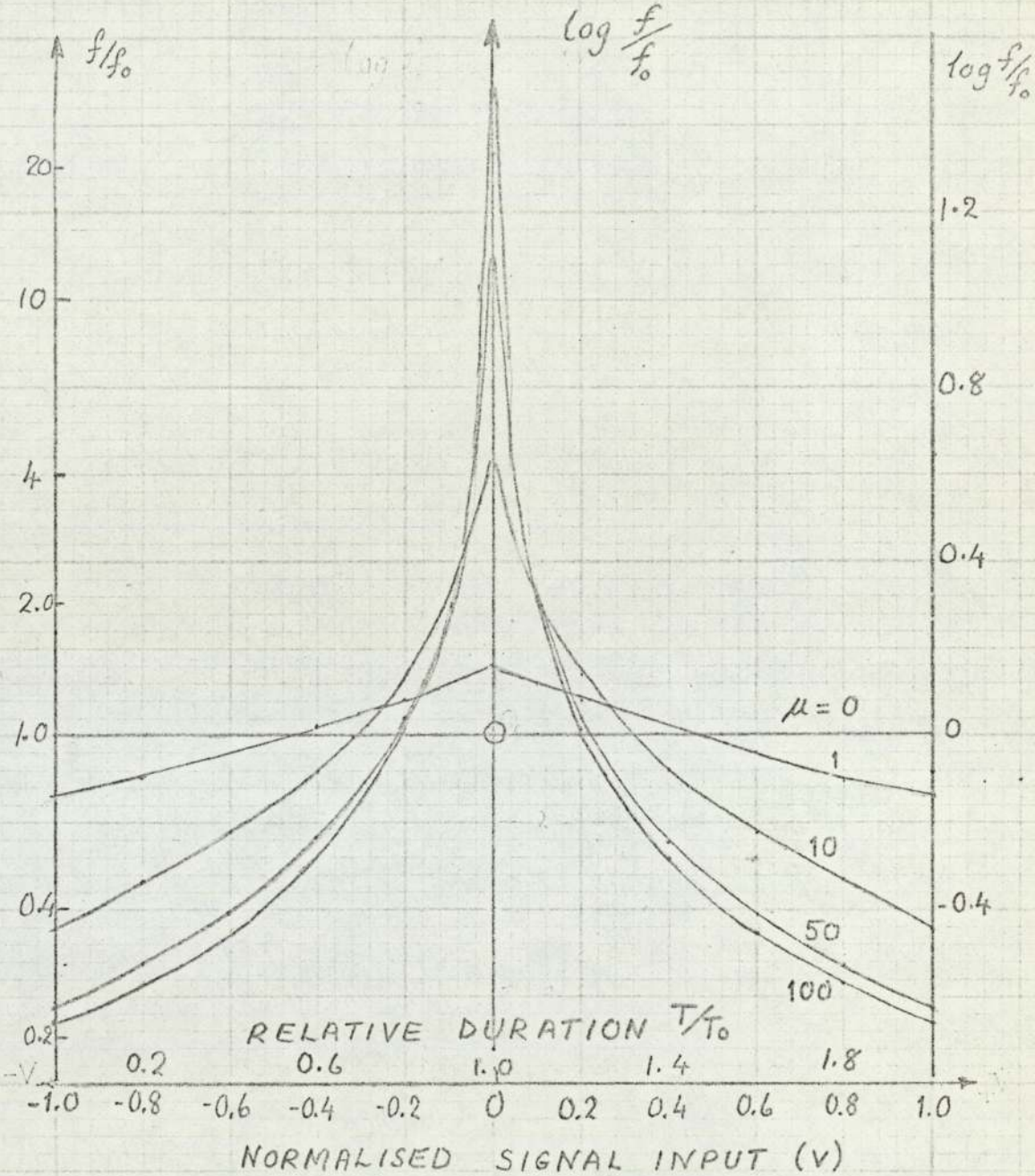


Fig. 3.8 VARIATION OF CLOCK FREQUENCY IN THE CHANNEL DURATION.---METHOD 5.

When the variation throughout a modulation period is considered (figure 3.4), the following features are seen:-

(i) the clock p.r.f. reaches maxima at instants where the trailing edge of the unmodulated pulse would occur;

(ii) the sweep period is twice the duration of the unmodulated pulse (2 To);

(iii) the variation resembles the output of a full-wave diode rectifier, with clamping (or compression) of the peak value.

There are two ways of instrumenting this encoder, as shown in figure 3.9. In both, the signal linearly modulates the channel pulse duration in a monostable multivibrator.

On the left-hand-side of figure (3.9), a sawtooth waveform is applied to a logarithmic compressor, whose output feeds a differentiator. The output of the latter feeds a linear voltage-to-frequency (v-f) converter to control the clock frequency.

Alternatively, a triangular waveform is compressed (not logarithmically) and is applied to a linear v-f converter to vary the clock frequency.

In both schemes, (as for the previous four methods), the gated clock pulses are applied to a binary counter and then to a shift register for parallel-to-serial conversion.

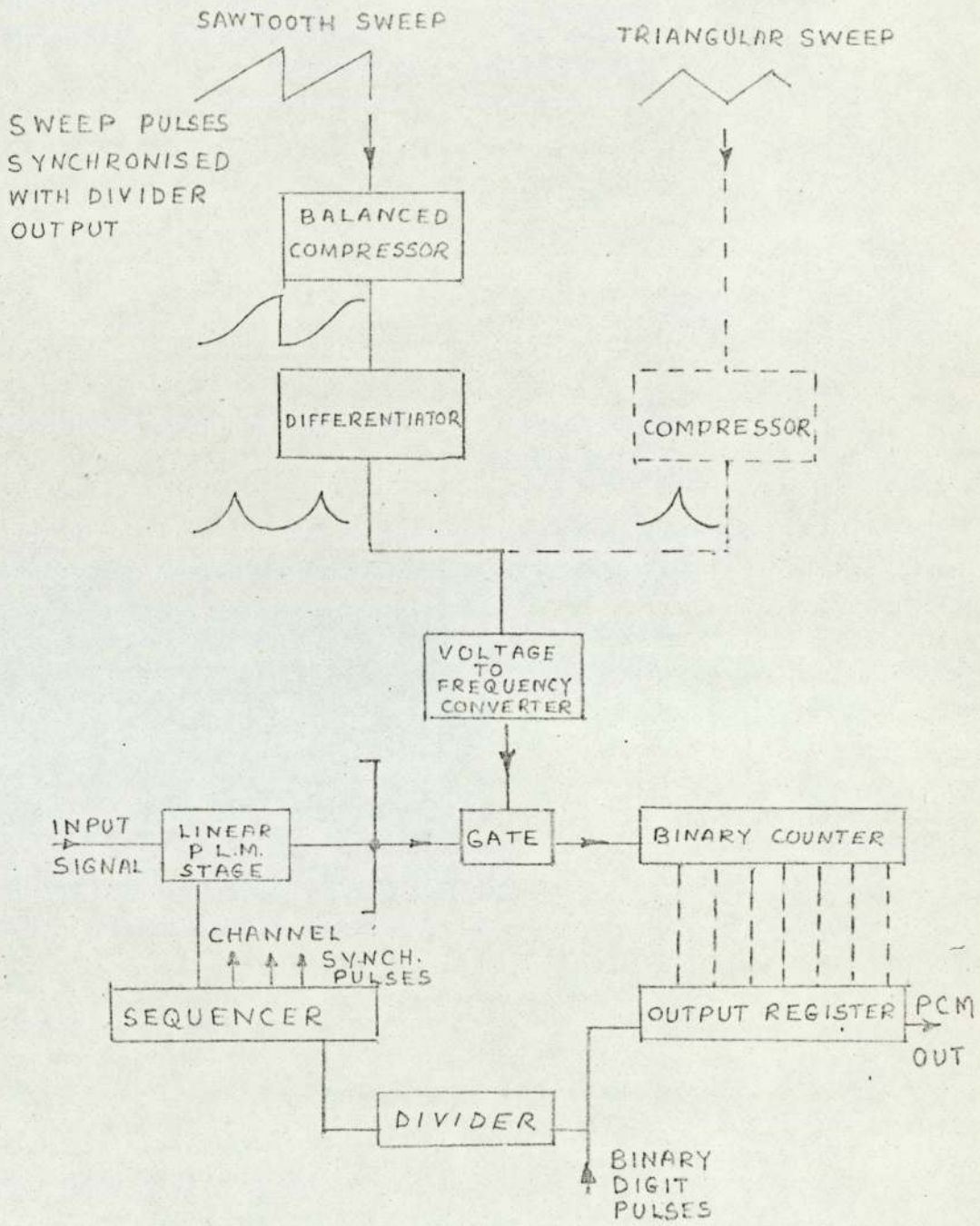


Fig. 3.9 ENCODER FOR METHOD 5

The Expansion for Decoding

In general, the encoder and decoder may operate on different principles, eg. a beam tube-type encoder was complemented with a Shannon-type decoder [2]. As pulse-count encoding is the subject of this particular work, it is convenient to specify a counter-type decoder, like the one proposed by Chew [26]. If compression in the encoder is obtained in a separate stage, it is necessary only to have the same type of companding elements in a separate expansion stage in the decoder. The inverse characteristics for such compandors may be achieved by voltage - and current driving the two sets of companding elements respectively, as shown in fig (2.13).

When the companding action is incorporated in the coding process, there may be more restrictions upon decoder design, depending on the extent to which the modulating and compression functions have been separated in the encoder. The form in which the expansion must be made in the five methods proposed, is now considered.

The theoretical relation between the transmitted level number (l) and the normalised modulating signal (V) is given in equation (3.1) and is repeated here for convenience:

$$l = \frac{L}{2}\left[1 \pm \frac{\log(1 \pm \mu V)}{\log(1+\mu)}\right] \quad ----- \quad (3.1)$$

Decoders for all of the methods stated should have transfer characteristics which are the inverse of equation (3.1). That is if l is the weight of a received code pulse group, and v' is the output of a low-pass filter, then

l and v' are related, as follows:

$$v' \ (= V) \quad = \pm \frac{1}{\mu}\left[(1+\mu)^{\pm\left(\frac{2l}{L}-1\right)} - 1\right] \qquad \text{---- (3.11)}$$

If the expansion is not incorporated in the process of decoding, but takes place in a separate stage following the decoder, the expander itself must have a transfer characteristic given by equation (3.11), the normalised input voltage being $^{2l}/_{L}$.

If the expansion is incorporated as in Methods (1) and (2), the elements of timing circuits in the decoder should be varied by the level number (l), so that equation (3.11) holds.

The problem of determining the form of expansion for methods (3-5) will now be considered. Consider firstly Method (5). Here the signal modulates the channel pulse duration linearly, and the companding is applied by a swept variation of clock p.r.f. The period of the sweep is the full channel pulse duration, while the variation of frequency (f) with T is given by equations (3.10) and(3.6) A given signal sample will then generate a channel pulse of duration (T), while the sweep generator produces a train of pulses. The corresponding level number (l), given by fdT, is counted to produce a code-pulse group whose weight is given by equations (3.4) and(3.9). At the receiver the code pulse group may be set into a counter. To make the demodulated output proportional to the input signal sample, an expansion correction must be made. This may be achieved by a sweep generator which drives the receiver counter at an

instantaneous frequency (fe). This can be made to generate a pulse of length T which must equal that in the encoder. Clearly, this may only be done if the encoder and decoder sweep generators are identical. This rather surprising result implies that the decoder for Method (5) may be conveniently instrumented using the same design principles given for the encoder, in section (3.4)

The same result, however, is not true for those methods where the signal modulates both f and T. Consider now Method (3); the compression is given by making the clock p.r.f. a function (ϕ) of the modulating signal (v), while the channel pulse duration $T \propto V$.
The transmitted level number (l) corresponding to a signal sample (v) is then given by :-

$$l = fT = T\phi(V) \quad \text{-------} \quad (3.12)$$

At the receiver, a code pulse group of weight (l) is set into a binary-counter. To make the required expansion, the pulses which drive the counter should be controlled by the modulating signal, which, obviously, is not present. If the weight (l) is used to control the clock p.r.f. (fe), then $fe = \phi e(l)$ where ϕe is an unknown function. Hence, a pulse is produced having a duration given by:

$$T_e = \frac{l}{\phi_e(l)} \quad \text{- - - - - -} \quad (3.13)$$

If the expansion is to be correct, $T = Te$, and

$$\phi(v) = \phi_e(l) \quad \text{- - - - -} \quad (3.14)$$

The implication of equation (3.14) is seen if the logarithmic companding function given in equation (3.1) is written $l = F(v)$, and $v = F^{-1}(l)$.

Equation 3.14 then becomes -

$$\phi_e(l) = \phi[F^{-1}(l)] \quad \text{(3.15)}$$

Hence to give the required expansion, the level number (l) must be decoded, applied to a device having the inverse characteristic $F^{-1}(l)$ and then to a device having the transfer function ϕ. The clock pulses are then generated to drive the counter and to generate a pulse of length (T).

As a decoding method, this is impractical for two reasons. Firstly, the decoding is carried out twice: the step of obtaining the inverse characteristic ($F^{-1}(l)$) implies decoding. Secondly, it will be difficult to find a device for which $V = F^{-1}(l)$, for the encoder to this method does not have a stage which gives $l = F(V)$ explicitly.

The instrumentation principles of the decoders are now considered in the next section.

3.6 Decoders for Methods (1) to (5)

In Method (1) compression is obtained by the way in which the modulating signal varies the resistive elements of a timing circuit, which control the channel pulse duration. To obtain the inverse process in the decoder, the incoming binary digit train should be converted into an identical train of length-modulated pulses.

This pulse train should then be applied to an integrator, the output of which should be a faithful copy of the original modulating signal.

There are at least three requirements for such an integrator and these are as follows:-

(a) It must have the same type of active resistance elements as the encoder timing circuit.

(b) The resistances of the active elements should be controlled by the output voltage.

(c) It must distinguish between pulses subject to positive and negative modulation respectively.

A possible decoding system is illustrated in figures (3.10) and(3.11). The incoming p.c.m. train is set into the reversing counter. The constant-frequency clock pulses, with a start pulse from the bistable element, drive the counter to zero. The 0 levels from the counter stages are gated, to give a signal which causes a transition in the bistable. Hence the output of the bistable is the channel pulse and it will have the same compressed duration as the corresponding encoder channel pulse. To separate positive - and negative - modulation pulses, the p.l.m. train is gated by a train of pulses, having the unmodulated pulse duration (To). The action of the negators may be seen from the pulse waveforms, shown in fig (3.11) to result in negative length and positive length-

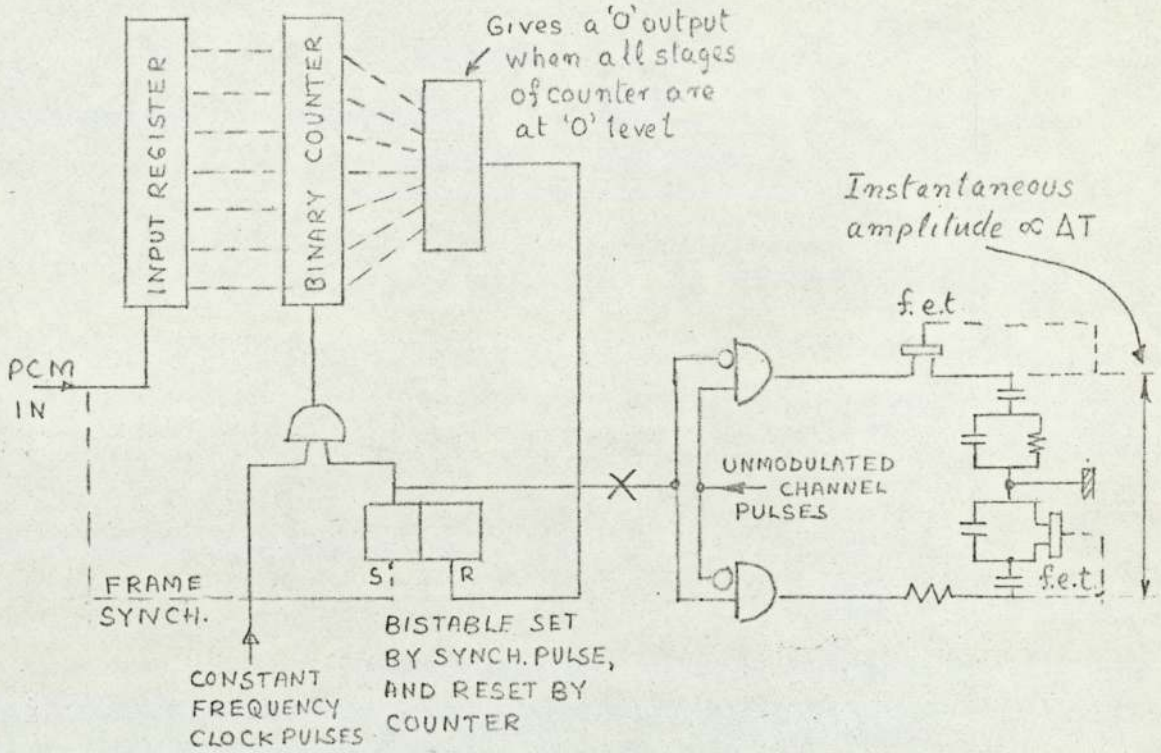


Fig. 3.10 DECODER FOR METHOD 1

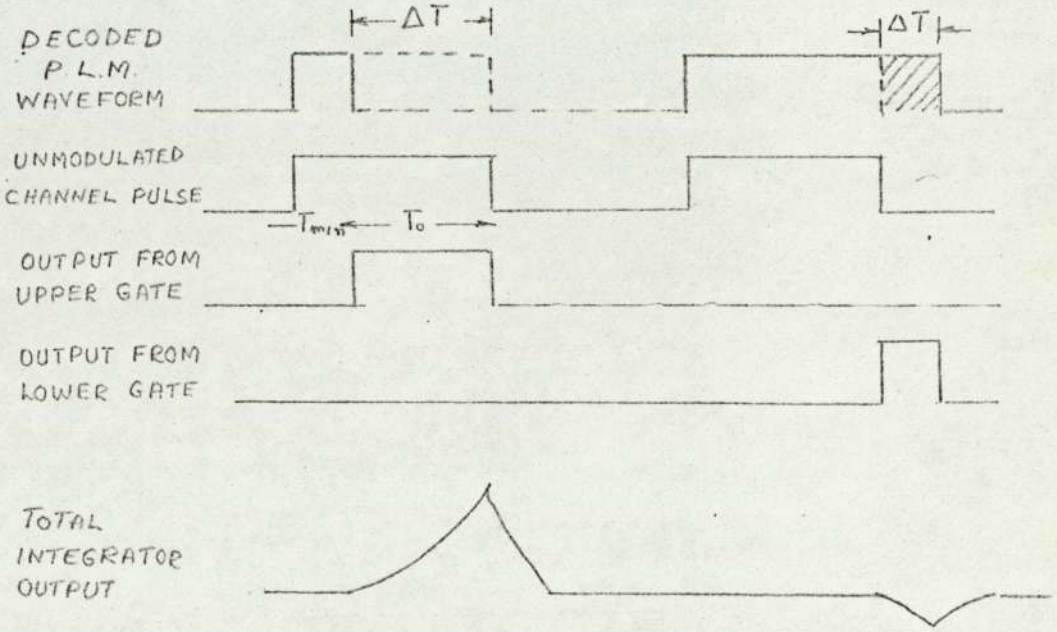


Fig. 3.11 WAVEFORMS FOR THE DECODER OF METHOD 1

modulated pulses being directed to the upper and lower integrators respectively. The integrators contain active elements similar to those in the timing circuit of the encoder p.l.m. stage. The active elements are controlled by the output voltage of the integrator, so that the correct expansion is given. The outputs of the two integrators are combined and demodulated by a low-pass filter, to give a copy of the original modulating signal.

This is a possible decoding system for Method (1). It has been described in detail in order to show the difficulties in instrumentation when the companding action is incorporated in the coding process. In Method (1) the difficulty arises in distinguishing between positive and negative length-modulated pulses. Moreover, it is doubtful whether the expansion can match exactly the encoder compression. In the simple encoder developed in Chapter 4, a saturation-mode monostable multi-vibrator was used in which the timing capacitance tends to discharge towards the reverse polarity, as a result of a switching action. In the integrators proposed for the decoder, there is no such switching and the timing capacitance tends to discharge towards zero. Finally, it may be noted that decoding for only one channel is shown. Channel separation, however, can be made at the point X in fig 3.10, and reference to fig 3.12 (i.e. Method 5) will show how each channel may be gated by a pulse train from the sequencer.

If the decoder for Method (1) appears difficult to design, that for Method (2) appears impossible.

In this method, the clock p.r.f. must be varied in a particular manner. It is difficult to see how the weight of binary digits, which are set into the receiving counter, may be used to control the timing elements of the clock pulse generator, and hence control the frequency.

With reference to Methods (3) and (4), it has already been pointed out in section (3.5) that decoder instrumentation is impracticable. Hence of methods (1) to (4) it only appears feasible to instrument a decoder for Method (1)

On the other hand a decoder obeying the principle of Method (5) is just as convenient to instrument as the encoder. This may be seen from the block diagram in figure (3.12). The clock pulses, which drive the counter, maybe obtained in two ways, as in the encoder, but one only is illustrated. As in the decoder for Method 1 , there are the input register, binary counter with decoding gate and the bistable element in which the channel pulse is formed. In addition, a channel sequencer is shown and this provides the pulse trains which enable the channel gates to give channel separation. For each channel a low-pass filter demodulates the length-modulated pulses.

Hence, coding by Method(5) appears to offer a considerable advantage over the other methods in that the encoder and decoder may be similarly instrumented. The original aim of incorporating the companding action in the coding process is fulfilled.

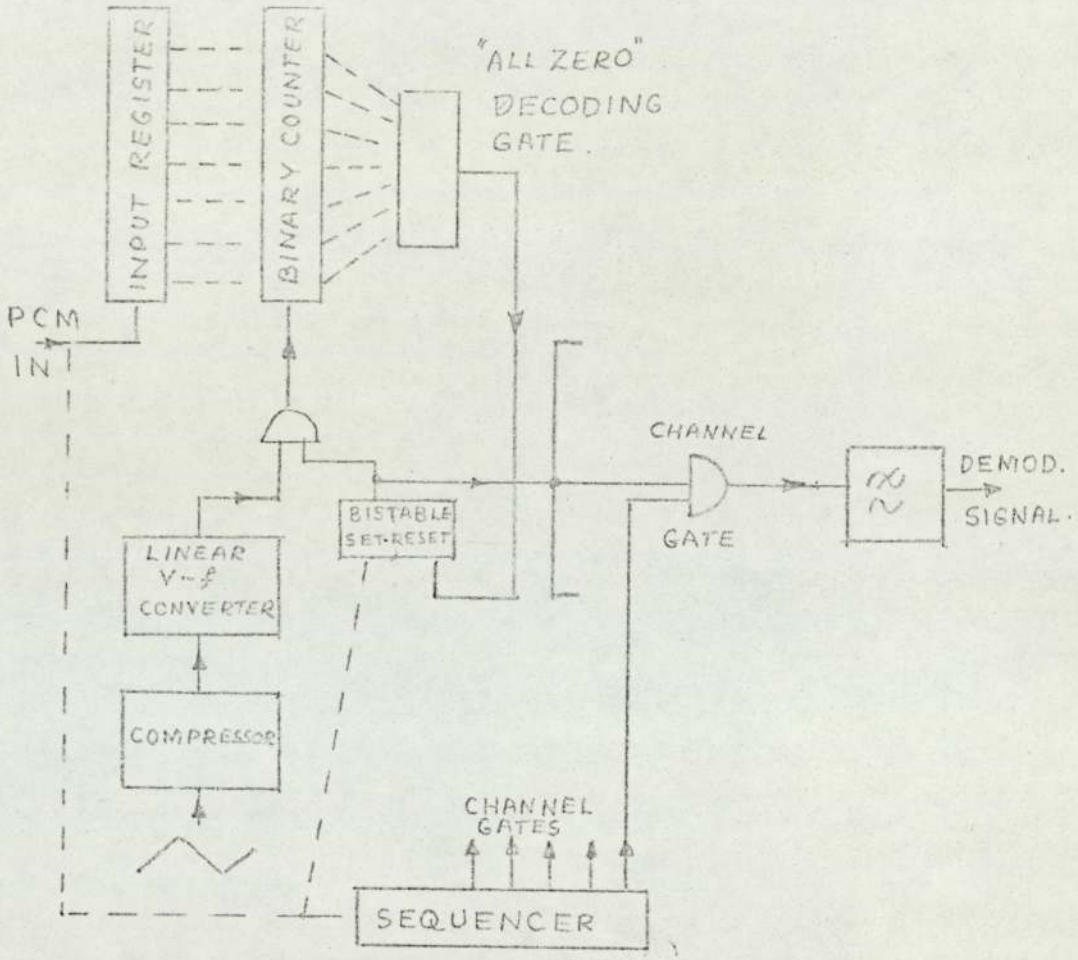


Fig. 3 12 DECODER FOR METHOD 5

To simplify the instrumentation problem, however, it appears necessary to separate the signal modulation and companding functions in the way outlined. A detailed design for this coder is given in chapters 5 to 8.

In the next chapter, an account is given of the experimental work to test the feasibility of coding by Method (1)

CHAPTER 4

INITIAL EXPERIMENTS TO TEST THE FEASIBILITY OF ENCODING BY METHOD 1.

4.0. Statement of Work to be Done to Test Method 1

4.1. Methods of Measurement

- 4.1.1. A Low Frequency Model
- 4.1.2. A D.C. Method of Measurement
- 4.1.3. A.C. Methods of Measurement

4.2 Monostable Multivibrator with Modulated Timing Resistance.

- 4.2.1. A Single Bipolar Transistor Resistance Modulator
- 4.2.2. A Double Transistor Resistance Modulator

4.3. Monostable Multivibrator with Compound C.R. Coupling.

4.4. A F.E.T. as a Resistance Modulator

- 4.4.1. Features of a Junction F.E.T.
- 4.4.2. F.E.T. Resistance Modulator

4.5. Conclusions from the Tests on Method I.

4.0 Statement of Work to be done to Test Method (1)

This is an account of the initial experimental work which was carried out to test the feasibility of Method (1) encoder. A block diagram of the system has been given in fig 3.5. The principle is recalled as follows. The signal to be encoded, modulates the duration of the channel pulse according to the logarithimic law given in equation (2.1). The pulse duration is then measured by counting the number of constant frequency clock pulses which are gated by the channel pulse. Successive counts are converted into binary code pulse groups.

Clearly, the main difference between Method (1) and traditional pulse-count methods is in the design of the p.l.m. stage. Hence, any initial experiments to test the feasibility of the method need only be concerned with the non-linear p.l.m. stage.

The p.l.m. stage proposed is based upon the collector coupled monostable multivibrator circuit shown in fig. 4.1. In this circuit the pulse length is given by $0.7\ C\ R_B$ (31) where CR_B is the discharge time constant. It is considered that the pulse length may be varied logarithmically when one (or both), of the timing components is (are) replaced by three-terminal active devices which are operated non-linearly. In the following sections (4.2 and 4.4), bipolar and field effect transistors are considered as a replacement for R_B, and to modify the value of C.

4.1. Methods of Measurement

To simplify the measurement of small pulse durations, it was decided to use a low frequency model for the p.l.m. stage. A description of this and the methods of measurement are now given.

4.1.1. A Low Frequency Model

In a typical p.c.m. system, 24 channels may be accomodated in the channel pulse interval. That is, in a telephony system, where the channel pulse repetition frequency is 8 KHZ, the maximum channel pulse length is 125/24 μS i.e. approximately 5μS

The unmodulated pulse duration in a p.l.m. system would then be 2.5μS. This would be used to gate about 128 clock pulses, which would each have a pulse length 2500/256 $\simeq$ 10 nS.. These small duration values are difficult to measure accurately, and so it was decided to scale down frequencies by a factor of 50, or thereabouts, by making measurements on a low-frequency model.

The parameters of a suitable model may be chosen as follows:-

Highest modulating frequency (arbitrary)	100 HZ
Channel prf	200 HZ
Channel recurrence period 1/200	5 mS
Number of channels (arbitrary)	5

Duration per channel 5/5---------- 1 ms
Unmodulated pulse duration----------500 uS
Guard bands between channels (arbitrary)------200 uS
Change in duration on largest signal--------- 400uS
Duration on maximum negative modulation------ 100uS
Duration on maximum positive modulation------ 900uS
Number binary digits in a pulse group(arbitrary) 8
Number of quantum levels 256
Period of clock pulse 800/256---------- 3.1μS

It will be noted that some of the parameters are labelled as arbitrary, and an attempt is now made to justify their choice. The overall choice is dictated by the smallest duration of pulse, which may be conveniently measured. It is considered that a change of pulse duration of 1-2μS could be readily determined, and a clock pulse period of some 3μS was chosen. The number of quantum levels (2^8) chosen, is typical for a commercial telephony system. There appeared little point in scaling down here, since a small number of levels would give a large step size which would tend to mask any coding errors which might occur. It may now be seen that the choice of the maximum channel pulse duration followed from the clock pulse period and the number of quantum levels. The channel p.r.f. and the highest modulation frequency are then determined by the channel pulse and the number of channels. A choice of five for the latter was influenced by two considerations. Firstly, larger number of channels would make the channel p.r.f.

inconveniently small. Secondly, in these initial experiments, the duration of the channel pulse is the sampling period, and this would be too large if the number of channels < 5.

The validity of any test results from the model may be questioned at this stage. It is considered, however, that if the types of device used in the model, behave similarly at the higher operational frequencies, the results are valid.

The models to be described in sections 4.3 and 4.4 were made up from discrete components rather than integrated circuits, because they allowed greater freedom in the choice of working voltages.

A major component of the model p.l.m. stage will be the transistor which forms a variable timing resistance. The modulating signal which is applied to control this resistance may therefore be either a direct - or an alternating - voltage. That is, the method of measurement may be termed d.c. or a.c.

4.1.2 A D.C. Method of Measurement

If the d.c. input to the variable timing element(s) is varied in steps, the resulting variations in pulse duration may be measured by using the calibrated time base controls of an oscilloscope (CRO). To display a pulse waveform on a C.R.O. screen, the internal timebase needs to be synchronised by the pulse-train. If the leading edge of the pulse is made to synchronise

the time base, then as the timing resistance is varied in steps, the duration of the pulse may be seen to increase in steps. It is considered that these durations may be measured to an accuracy of ±1% with the better type of C.R.O. Greater accuracy may be obtained with a universal-type counter, having 1μs clock pulses for time measurement.

4.2.2. A.C. Methods of Measurement

An ac method of measurement may be convenient for some coding methods. Indeed, if the performance of a complete system, including encoder and decoder is to be tested, then an ac method is desirable, mainly because of the presence of coupling capacitors at the modulating signal input to the encoder.

In general, there are two types of a.c. methods.

(a) the OBJECTIVE method and (b) the SUBJECTIVE method In both of these methods, a.c. signals are applied to the input to the encoder and the corresponding a.c. signals at the decoder output are examined.

In an objective method a variable frequency sinusoidal generator is applied to the encoder input and the decoder output is examined with a waveform analyser (or frequency selective voltmeter), to measure the harmonic and attenuation distortion.

With the subjective method speech and / or music signals are applied to the encoder input

A group of observers listen alternatively to the decoder output and encoder input signals and a statistical assessment is made of the observers' aural appreciation of harmonic, attenuation and error distortions.

For both of these methods, however, it is necessary to devise a method to determine whether poor performance occurs at the encoder or at the decoder. That is, if such methods are to be used then it is necessary to design an a.c. method of testing the encoder and decoder separately. Consideration was given to an a.c. method, and a major difficulty arose. For when an a.c. signal modulates the duration of a pulse, (the signal and pulse are derived from independent sources), a steady single line trace cannot be observed on a C.R.O. screen. The problems involved with a.c. testing, and how they may be overcome, are considered in Appendix A. It is clear, however, that a d.c. method of measurement is simpler, and so this is the method adopted.

4.2. A Monostable Multivibrator with Variable Timing Resistance

The p.l.m. stage is shown in fig. 4.1. The d.c. signal which controls the timing component(s), may be varied over the range - V to + V, so that the discharge time constant varies from $(CR_B)_{min}$ to $(CR_B)_{max.}$ The transfer characteristic required is shown in fig. 4.2., and clearly a balanced resistance modulator will be required. Hence, the feasibility tests were conducted in four phases as follows:

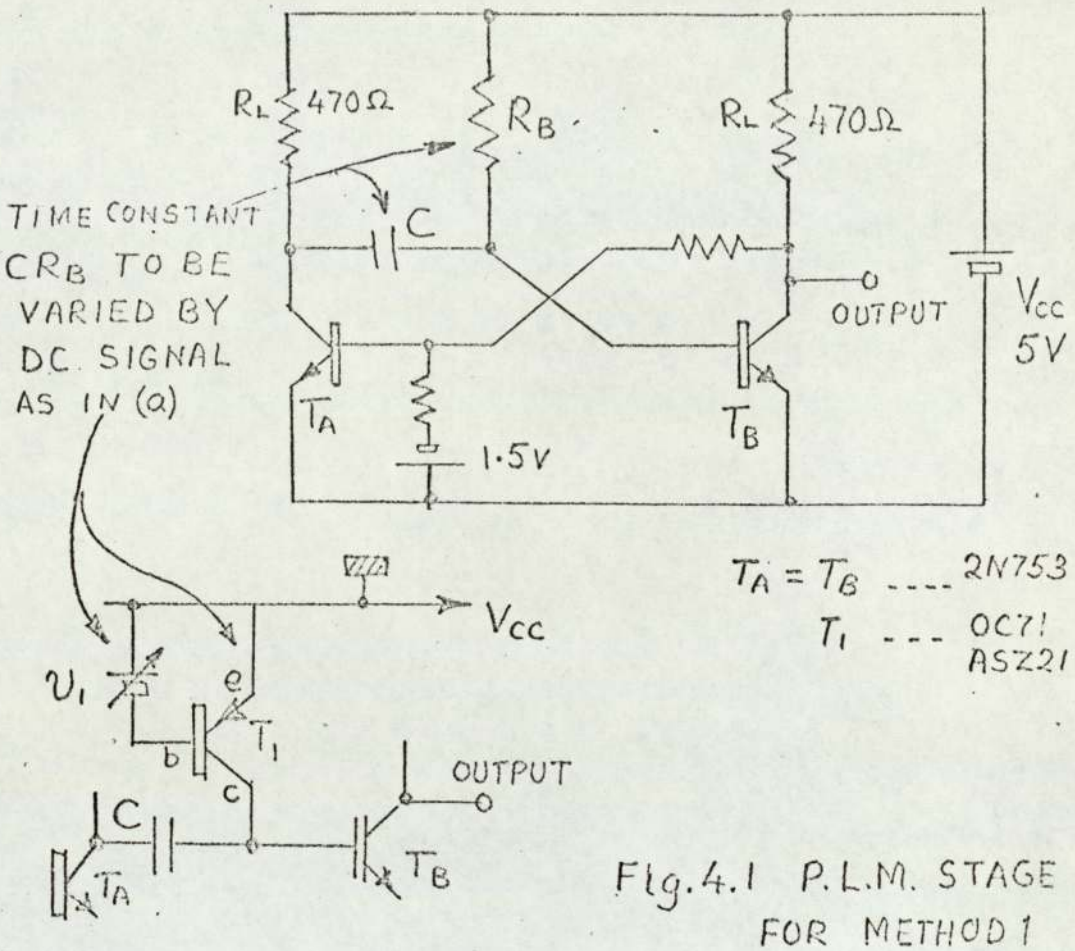


Fig. 4.1 P.L.M. STAGE FOR METHOD 1

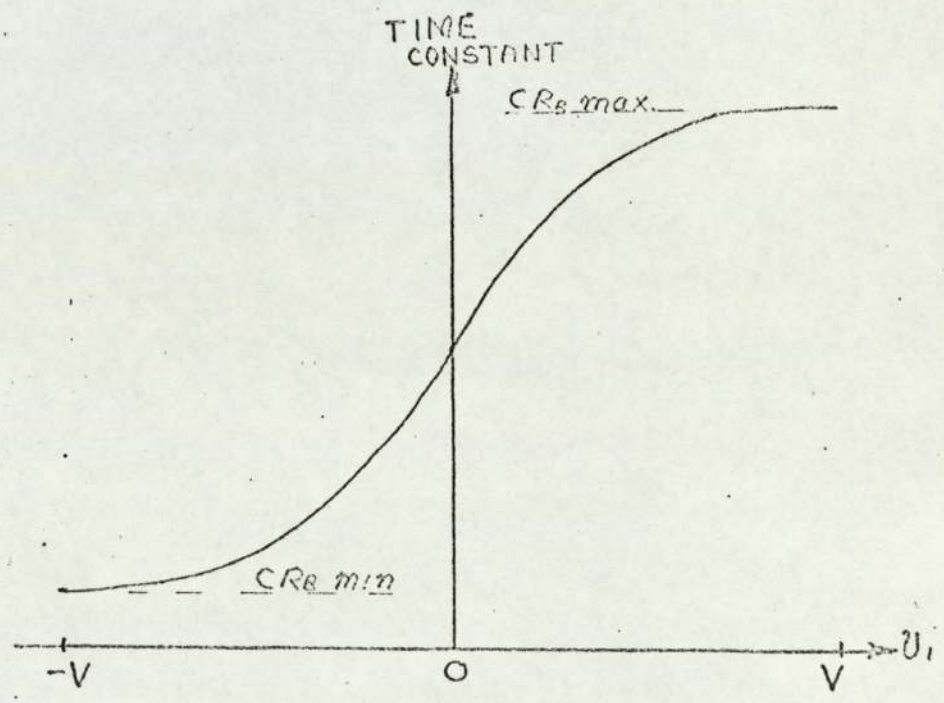


Fig. 4 2 CHARACTERISTIC REQUIRED

(a) A single bipolar transistor for resistance modulation on negative signals only

(b) A double bipolar transistor conductance modulator

(c) Transistors modulating both R_B and C.

(d) A single f.e.t. modulator.

4.2.1. A single bipolar transistor with negative modulation

The p.l.m. stage is given by the collector-coupled monostable multivibrator in fig. 4.1. in which the normal timing resistance R_B is given by a p.n.p. transistor T_1. The resistance between collector and emitter is controlled by a negative-going voltage V_1, which represents the modulating signal. An increase in V_1 increases the collector current, which causes the capacitor C to discharge in a shorter time. The discharge time is also the pulse duration and this may be shown to be a logarithmic function of V_1, as follows:-

Consider firstly, the operation of a monostable multivibrator. The output pulse commences when T_A is switched to conduction, C is charged to the supply voltage Vcc, and a nearly constant discharge current flows through T_1, tending to charge C to the opposite polarity. The output pulse is completed when the capacitor p.d. reaches zero approximately. Hence, T_1 collector - emitter p.d. (V_{ce}) varies between $2V_{cc}$ and V_{cc} and has a collector current which varies only upon the base input voltage V_1. That is, during the

discharge, the collector current is constant if V_1 is constant. (In the a.c. method of measurement described in Appendix A, V_1 is only approximately constant, since the discharge time is 10% of the period of the modulating signal; this is a source of error in that method of measurement). The approximate relation between i_c and v_{ce} may now be obtained[31, 36] as follows:-

$$i_c = (1 + h_{fe})\, i_{cbo} + h_{fe}\, i_b$$

$$= (1 + h_{fe})\, i_{cbo} + h_{fe}\, i_{cbo}\left[\exp.\left(\frac{V_1}{V_t}\right) - 1\right] \quad \text{----(4.1)}$$

$$\simeq h_{fe} \exp.\left(\frac{V_1}{V_t}\right) \quad \text{----------(4.2)}$$

h_{fe} = large signal current gain of T_1 (or T_2)

i_{cbo} = collector-base reverse leakage current

v_t = voltage equivalent of temperature

= 26 mV at 300K

$$\therefore R_B = \frac{v_{ce}}{i_c} = \frac{V_{cc}}{h_{fe}\, i_{cbo}} \cdot \exp.\left(\frac{-V_1}{V_t}\right) \quad \text{------(4.3)}$$

The duration T of the ouput pulse $\propto CR_B$

$$\therefore T \propto \exp.(-V_1)$$

This variation, shown in fig 4.3. has approximately the correct shape for negative going signals. It may be seen however, that the pulse duration increases to a maximum value for values of V_1 near to zero. This is because the collector leakage current (i_{ceo}) of T1 limited the value of R_B to about 100 KΩ.

It may be noted here that if the resistance modulator were current driven at the base, the collector current would be proportional to the driving voltage

i.e $$i_c = h_{fe}\left[V_1/R + i_{cbo}\right] \quad \text{-------(4.4)}$$

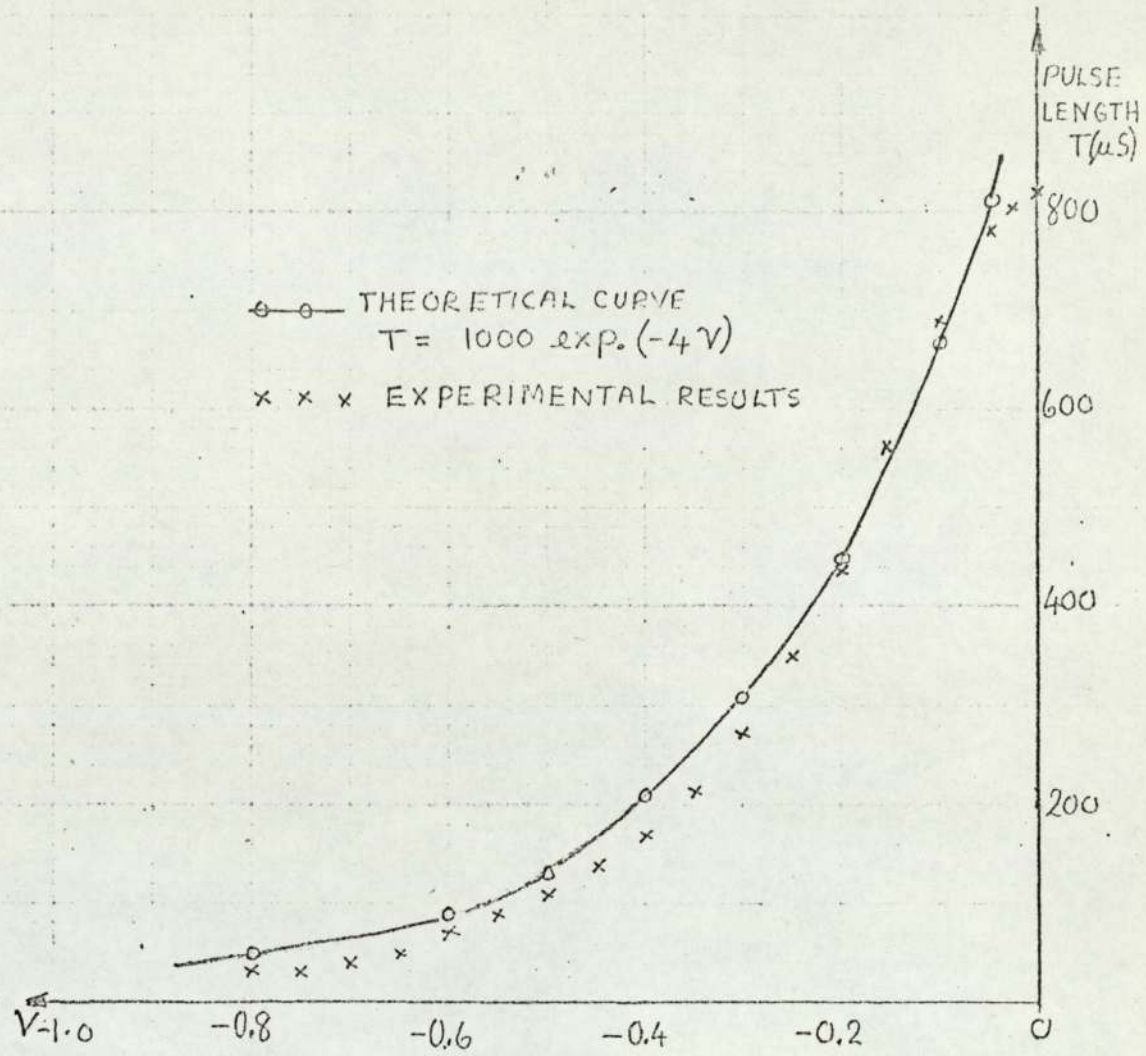


Fig. 4.3 SINGLE TRANSISTOR MODULATOR. (OC71)

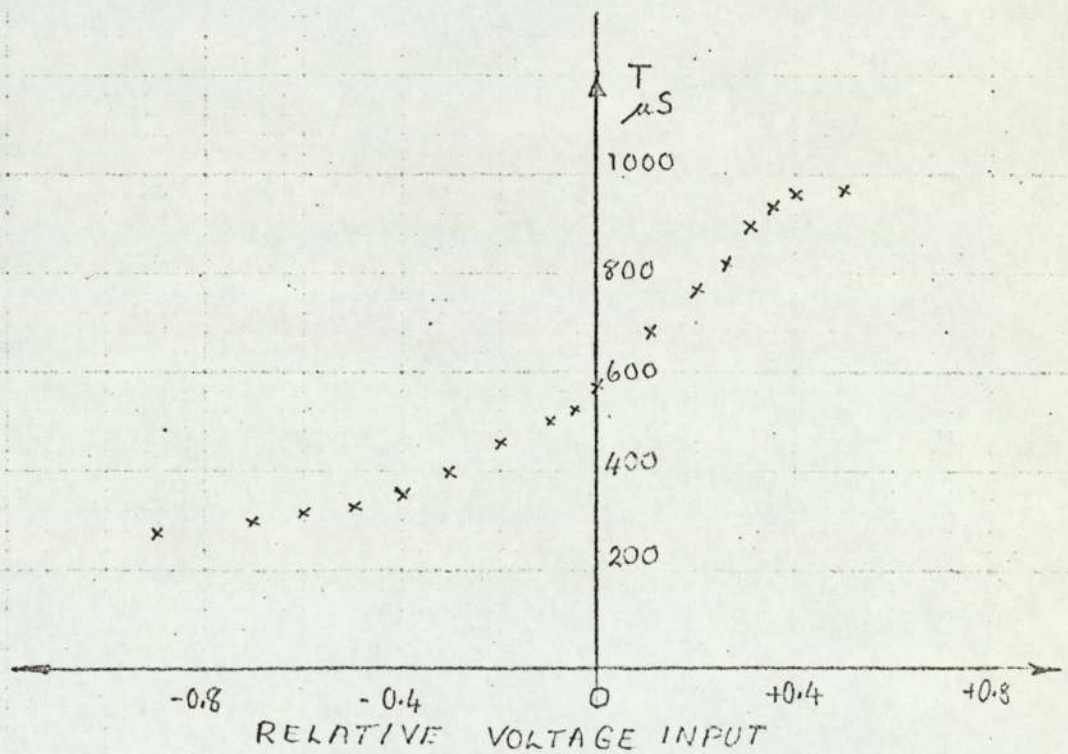


Fig. 4.4. SINGLE TRANSISTOR MODULATOR (AZ21)

Hence the resistance Rb is given by.

$$R_B = \frac{V_{cc}}{i_c} = \frac{V_{cc}}{h_{fe}\, V_i/R \left(1 + \frac{i_{cbo}}{i_c}\right)}$$

Where the base driving current is V_i/R. That is, the resistance (and pulse duration) are nearly inversely proportional to the input voltage. (The principle of current - driving a resistance modulator is also the basis of Biddlecomb's voltage - frequency converter, which is fully treated in Chapter 6. In that case $V_i \propto f$ which corresponds to the result above, $V_i \propto 1/T$). This may also be considered as a suitable companding characteristic. It has the added advantage that it will be more easily reproducible, as it is independent of the base-emitter characteristic, which is subject to "spreads".

The fact that the resistance tended to a limiting value at both high and low values of V_i suggested that one transistor may give the correct resistance modulation on both positive and negative modulation. In effect, the transistor would be biassed at the value which gave a pulse having half the maximum duration. A germanium p.n.p. transistor having a low leakage current (AZ21) was tested as a resistance modulator. The companding characteristic is shown in fig 4.4. It may be seen that the compression for positive and negative modulation is not symmetrical. It is considered that this feature is undesirable in a commercial system. If asymmetry were allowed, it would mean that positive and negative modulation signals would have to be distinguished

throughout the system, so that the correct inverse expansion may be given at the decoder.

4.2.2. A Double Transistor Conductance Modulator

A companding characteristic with symmetrical compression may be achieved if two transistors are connected in parallel and the following conditions hold.

(1) Two silicon transistors with small but finite leakage

(2) One base-emitter junction slightly forward biassed.

The other base - emitter junction biased.

(3) Both Transistors to be current-fed.

(4) The heavily biassed transistor to have a a collector resistor to ensure saturation.

The predicted variations of the two component conductances and their resultant are shown in fig 4.5. The double modulator was connected as shown in fig 4.6, and the companding characteristic is shown in fig 4.7.

It may be seen from figs.4.6 and 4.7 that the double modulator when current fed, should give a symmetrical characteristic, but there tends to be marked asymmetry in practice. The main reason for this is that compressions for positive and negative signals arise from different effects. For positive-going signals are limited by leakage current or shunt conductance, while negative signals are limited by saturation. It also appears doubtful whether limiting by leakage current or saturation is even approximately logarithmic.

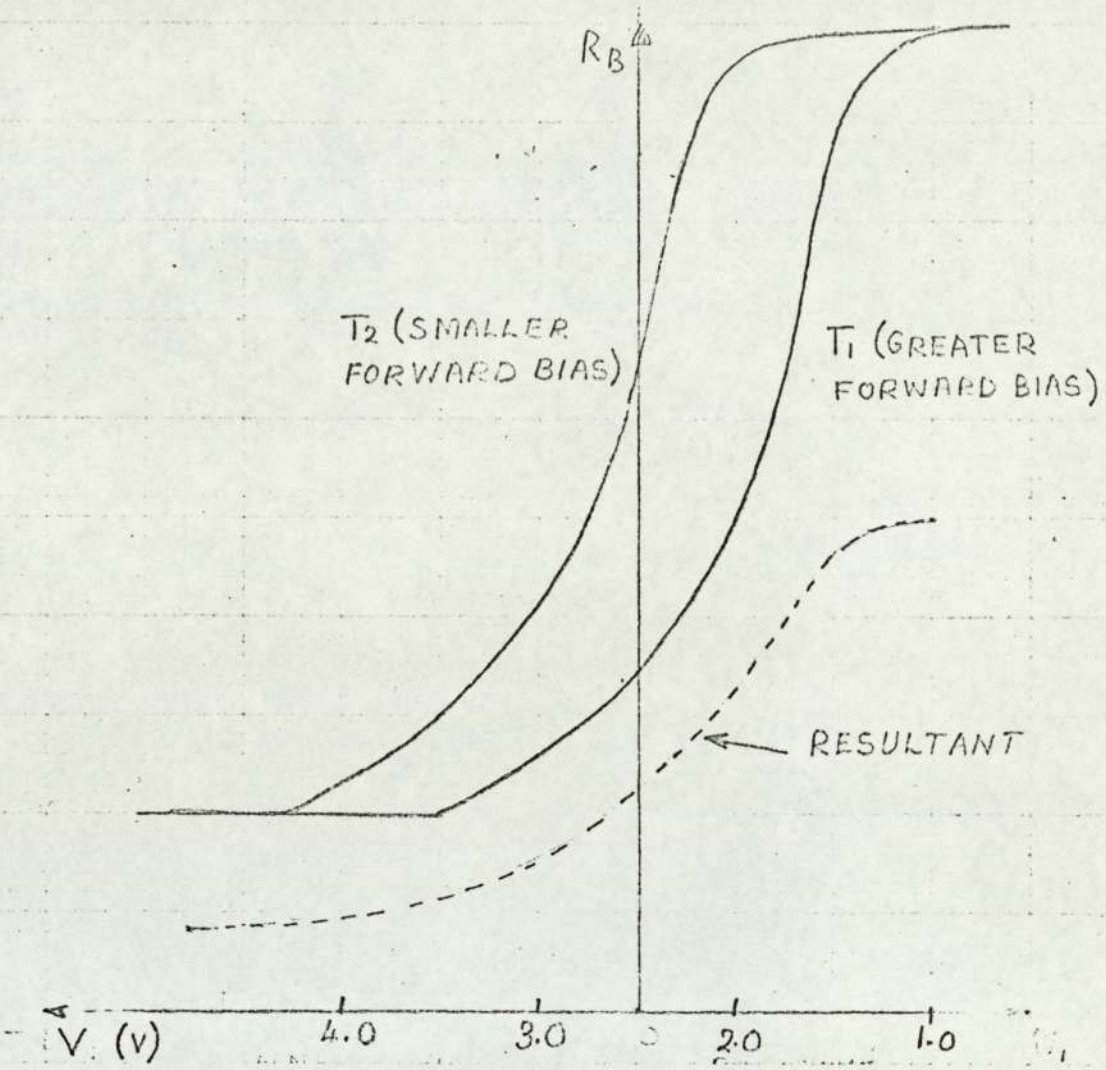


FIG. 4.5 PREDICTED CHARACTERISTIC FOR BALANCED RESISTANCE MODULATOR

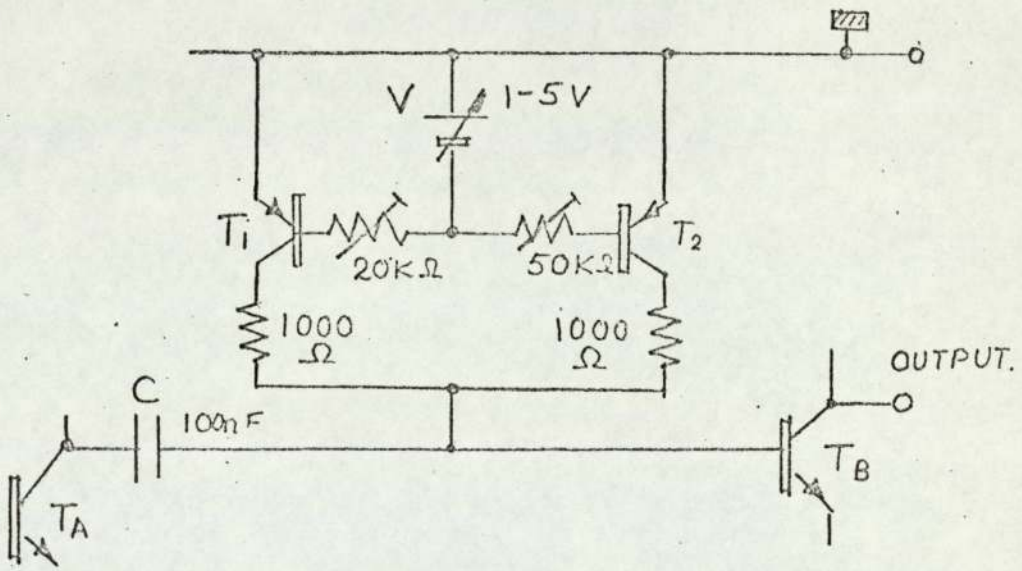


FIG 4.6 THE BALANCED RESISTANCE MODULATOR

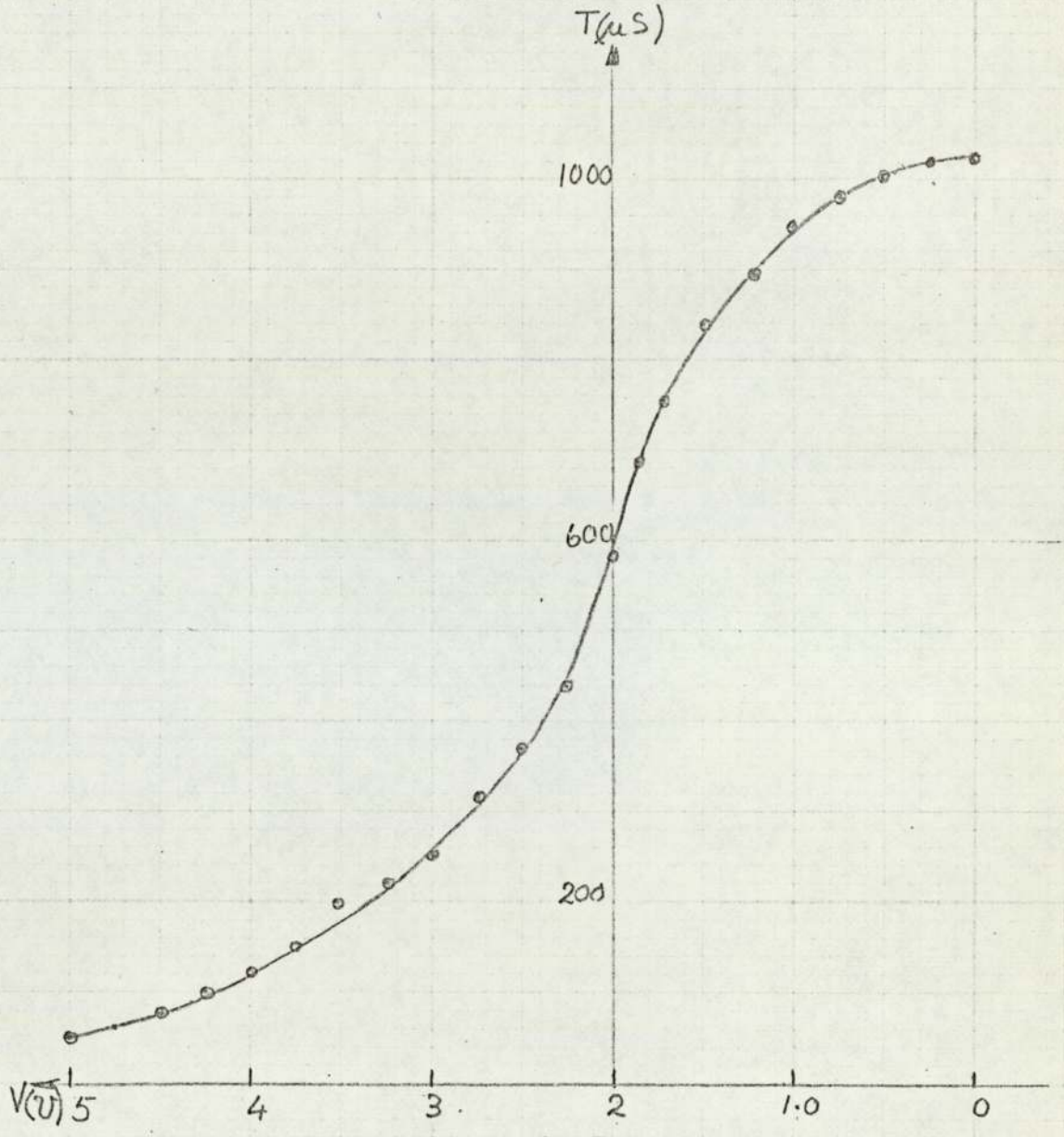


FIG. 4.7 EXPERIMENTAL CHARACTERISTIC FOR "BALANCED" RESISTANCE MODULATOR.

4.3. A Monostable Multivibrator with Compound C.R. Coupling

The resistance modulators, considered so far, have replaced the resistance Rb. The pulse duration may, however, be varied by the capacitance C, and consideration is now given to the modulation of C by a transistor.

The use of transistors as reactance modulators, which may vary the tuning capacitance of a high frequency oscillator, is well known. (3) The variations of capacitance given are small and providing the oscillator signal excursions are not too large, the a.c. output conductance of the transistor is small.

In a multivibrator, however, the capacitor p.d. decreases to zero, and if replacement by a transistor were attempted its conductance would be too large to hold the charge for the required time.

It was decided therefore to connect a transistor across the coupling capacitor (C_2) and to have a second larger capacitor (C_1) in series to block the direct current. The timing circuit, which resulted, is shown in fig 4.8, and R_2 is the resistance which will be modulated. In effect, conductance, rather than capacitance, is to be modulated.

At first sight, it may appear that an increase in R_2 will cause an increase in discharge time. A closer inspection of the timing circuit shows that in the stable state, the capacitors C_1 and C_2 are ultimately charged to Vcc and zero

respectively: (the charge on C_2 has leaked through R_2)
During the quasi-stable state C_1 tends to discharge to the opposite polarity, (as in normal multivibrator action), while C_2 tends to charge. The total capacitor voltage V_{BE} will decrease to zero when $V_{C2} = V_{C1}$. A large value of R2 permits C_2 to gain a high voltage and hence the quase-stable state is terminated in a shorter time.

A more rigorous analysis is given in Appendix C , where it is shown that the differential equation governing discharge [40] is given by:-

$$\left\{ p^2 + \left[\left(\frac{1}{C_1} + \frac{1}{C_2} \right) \frac{1}{R_1} + \frac{1}{C_2 R_2} \right] p + \frac{1}{C_1 C_2 R_1 R_2} \right\} i = 0 \quad \ldots\ldots (4.6)$$

where p denotes the operator $\partial/\partial t$ and i is the discharge current at time t.

Itis further shown that equation (4.6) has a solution:

$$i = \left[\frac{2}{m(\alpha_1 - \alpha_2)} \cdot \exp.(-\alpha_2 t) + \left(2 - \frac{1}{m(\alpha_1 - \alpha_2)} \exp.(-\alpha_1 t) \right) \right] \quad \ldots\ldots (4.7)$$

where $\alpha_1 = \frac{1}{C_2 R_1} \left(\frac{1}{n} + \frac{1}{m} + 1 \right)$, $\alpha_2 = \frac{1}{C_2 R_1 (m + n + mn)}$

$m = R_2/R_1$ and $n = C_1/C_2$.

The roots α_1^{-1} and α_2^{-1} are the two time constants of the discharge current components. The smaller of the two, α_1 , indicates a relatively large component which decays rapidly through three parallel resistances R_1, $n R_1$ and R_2 . The exponent α_2 indicates a smaller component of current due to C_1 discharging into three resistances in series i.e. R_1, R_2 and R_2/n

The quantity of interest is v_{BE} and in particular, the time taken for v_{BE} to decrease to zero. Clearly, the time T for v_{BE} to fall to zero is given by the solution of the equation:-

$$V_{cc} - iR_1 = 0 \quad \text{------(4.8)}$$

when substitution for i is made from equation (4.7). This solution, however, can not be obtained by simple algebra, because of the presence of two exponential terms, of comparable magnitude in equation (4.7). Hence solutions by numerical methods were obtained. That is, values of m ranging from 0.1 to 10 were inserted inturn into equation (4.7), for various values of n in the range 1 - 25, and the corresponding values of t which made equation (4.8) zero, were computed. The tables of results are given in Appendix C , and the values of relative pulse duration are shown graphically in figs. 4.9 and 4.10.

It is pointed out that R_1 and R_2 have been considered as passive elements, and have not yet been replaced by active elements. The curves in fig. 4.9, show the theoretical variation of relative pulse duration T/T_o with $m \left(= R_2/R_1\right)$. In general, there is an approximate logarithmic "roll - off" for large values of m, and the values of T/T_o do tend to asymptote for large and small values of m.

It was observed in section 4.3.1 that if a transistor resistance modulator were current-fed the resistance between

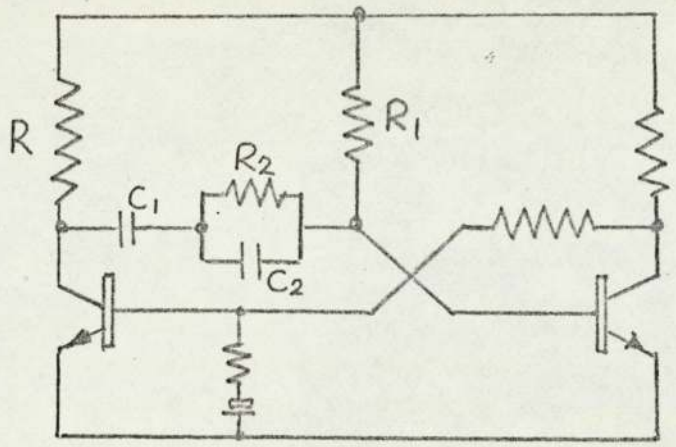
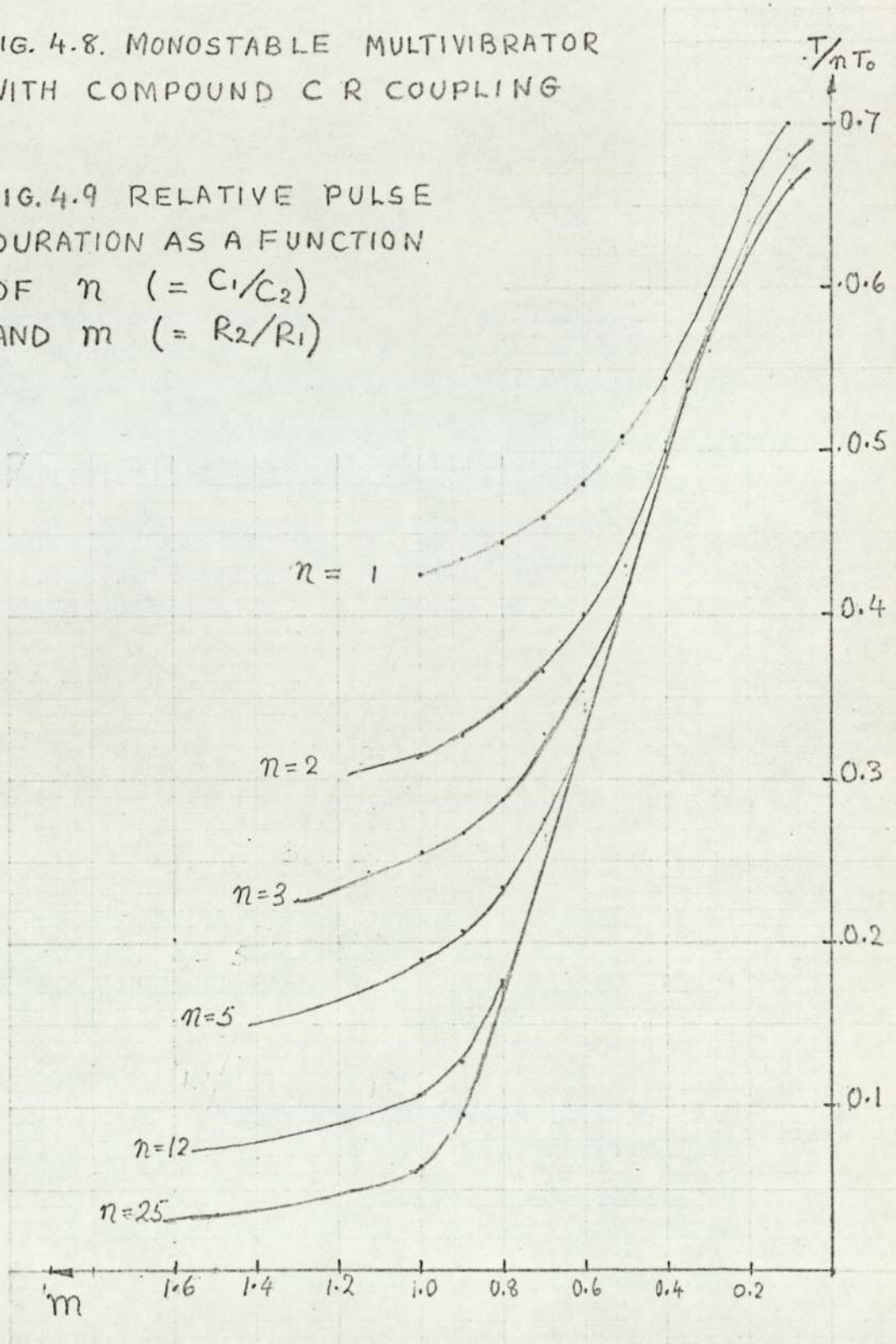


FIG. 4.8. MONOSTABLE MULTIVIBRATOR WITH COMPOUND C R COUPLING

FIG. 4.9 RELATIVE PULSE DURATION AS A FUNCTION OF n ($= C_1/C_2$) AND m ($= R_2/R_1$)



collector and emitter would be inversely proportional to the input voltage. That is, if R_2 were replaced by a current-fed bipolar transistor it should give a companding characteristic like that shown in fig 4.9. but with the abscissa $1/m$ ($=R_1/R_2$). Hence, the variation of relative pulse duration T/T_0 with $1/m$ is shown in fig 4.10. for one value of n . It will be seen that the origin has been chosen at $m=0.5$ in order to predict the characteristic, which will be obtained, when R_1 and R_2 are replaced by resistance modulators. In such a case, one polarity of input voltage would effect high values of R_1 and a constant value of R_2 , while the other polarity would give high values of R_2 for a constant R_1 . It can be seen that the predicted companding characteristic shows only a small asymmetry.

An attempt was made to confirm the above result. The timing circuit shown in fig. 4.11 was tested. The experimental characteristic is shown in fig. 4.12. The overall shape is correct but the asymmetry is greater than that predicted. It is considered that the asymmetry arises from the use of a p.n.p. - n.p.n. pair. While the use of a complementary pair is not strictly necessary, a difficulty occurs in correctly setting the bias points of the two transistors.

4.4. The F.E.T. as a Conductance Modulator

The bipolar transistor only has so far been considered as a resistance modulator. The unipolar, or field-effect, transistor (f.e.t.), which is perhaps a more logical choice for a voltage-controlled conductance, is now considered.

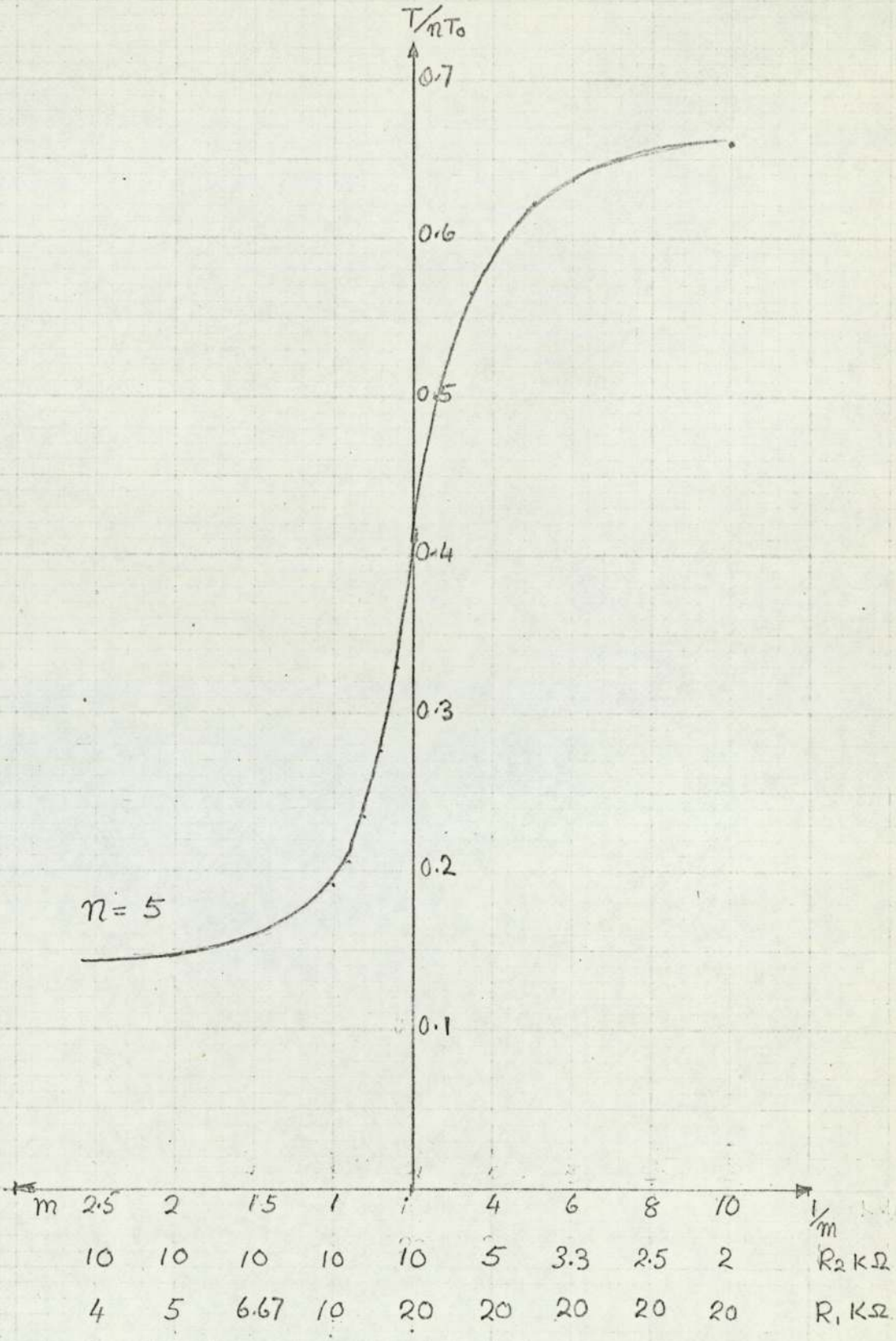
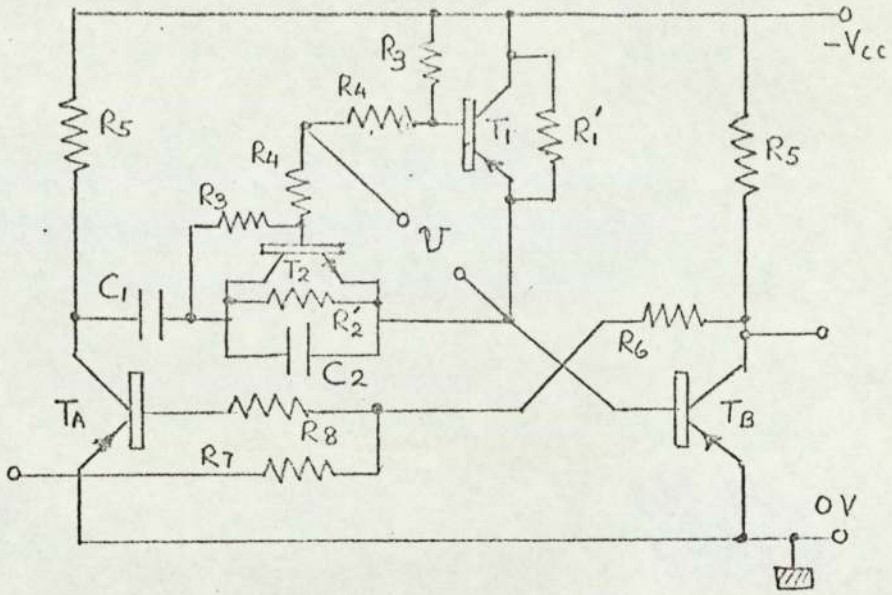


FIG. 4.10. PREDICTED CHARACTERISTIC WHEN RESISTORS R_2 AND R_1 ARE REPLACED BY CURRENT FED TRANSISTORS.



COMPONENT	VALUE /TYPE
C_1	150 nF
C_2	33 nF
R_1'	22 KΩ
R_2'	11 KΩ
R_3	1·5 MΩ
R_4	100 KΩ
R_5	470 Ω
R_6	3·3 KΩ
R_7	4·7 KΩ
R_8	6.2 KΩ
T_1	BCY 71 pnp
T_2	BC 108 npn
T_A	2N 2904 pnp.

FIG. 4.11. A P.L.M. STAGE IN WHICH BOTH C AND R TIMING COMPONENTS ARE TRANSISTOR CONTROLLED

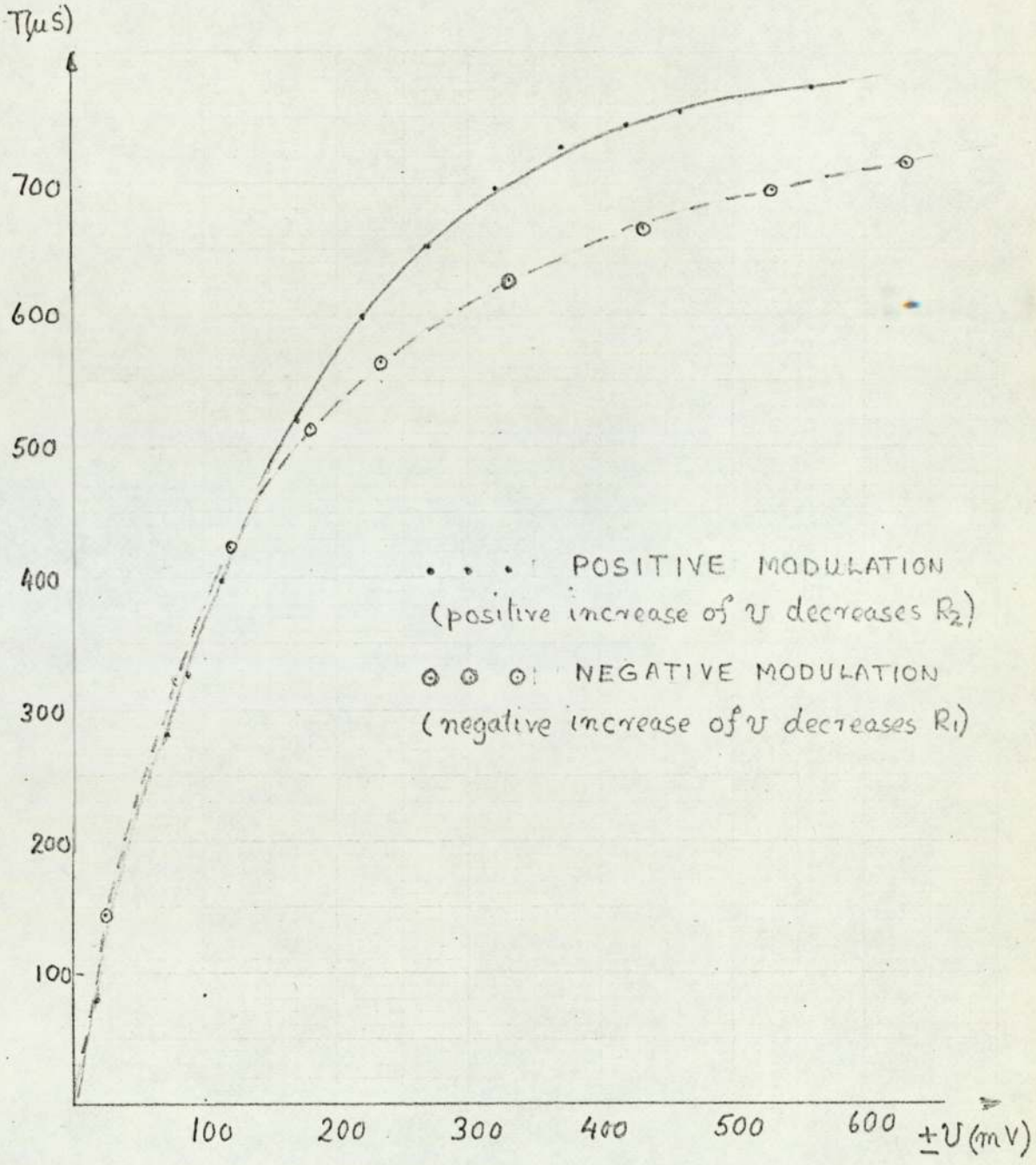


FIG. 4.12. EXPERIMENTAL CHARACTERISTIC WHEN RESISTORS R1 AND R2 ARE REPLACED BY CURRENT-FED TRANSISTORS

The f.e.t was predicted by Shockley [41] in 1952, and the analysis of experimental units was reported in 1955. The manufacture of the device, however, awaited the development of silicon fabrication techniques, so that they did not become available until the early 1960's.[41] Initially, the f.e.t. received prominence as a simple low-noise pre-amplifier at low and high frequencies. The planar epitaxial bipolar transistor could provide higher power gains at higher frequencies and the latter appeared to be preferred after about 1963. The f.e.t. has the merits of low noise, high input impedance and zero off-set voltages [31]. Hence, the device currently has had only limited applications as a high input impedance amplifier, and as a chopper-type amplifier [31]. There are two main types, namely, the junction and insulated-gate f.e.t.s. The latter have a near infinite input impedance and have recently been fabricated into integrated circuits. [37] The junction f.e.t. is a more robust device which is more convenient for experimental use.

4.4.1. Features of a Junction F.E.T.

The junction f.e.t. consists usually of a lightly doped silicon channel, as shown in fig 4.13. whose ends are called the source (S) and the drain (D). The channel is surrounded for a large part of its length by more heavily doped material, called the gate (G), of the opposite kind to the channel. That is, a n-type channel will have a p-type gate. There is a depletion region surrounding the channel and this region will be widened if the gate-channel p-n regions are reverse biassed. This

will occur, when the p-type gate is made negative w.r.t. the source, and it maybe seen that the channel is therefore restricted. In the n-type channel shown in fig 4.13 a current will flow from drain to source, when the drain is made positive w.r.t. the source. Current will of course flow from S to D if the polarity is reversed and this is one of the main operational difference between f.e.t's. and thermionic pentodes.

If, in fig 4.14 the gate bias (v_g) is increased the channel resistance is increased and the drain current (i) is decreased. When v_g = PINCH-OFF value (V_p), the drain current is decreased to zero, and this gives one definition of the pinch-off effect. The drain-source p.d. (v) also affects the depletion region, (A full description of this effect is given in Appendix D when an expression for the resistance of an f.e.t. channel is derived), and pinch-off may also be defined as the smallest value of v at which the saturation current (I_o) flows. These definitions are illustrated in fig. 4.15 which shows the variations of drain current with v and v_g

4.4.2 F.E.T. as a Resistance Modulator

When the application of the f.e.t. as a resistance modulator, to replace R_B, is considered, the drain voltage (v) varies over the constant current portion of the drain characteristic (i.e. to RHS of the line $v = V_p$). Hence the current may be considered to depend only upon v_g. An equation for the transfer characteristic,

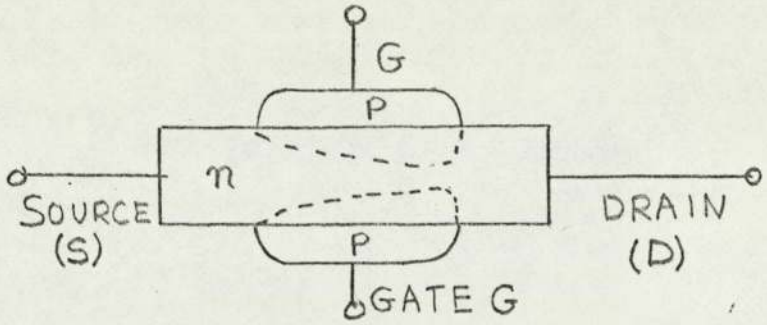


FIG. 4.13 A JUNCTION F.E.T.

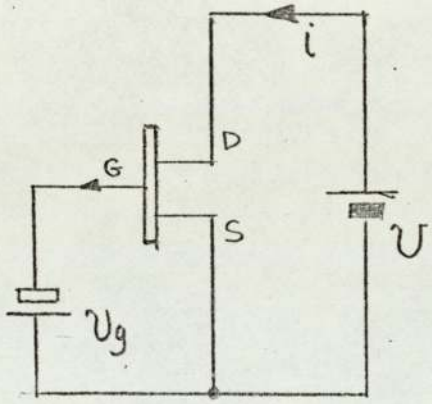


FIG 4.14 SYMBOL AND MODE OF OPERATION

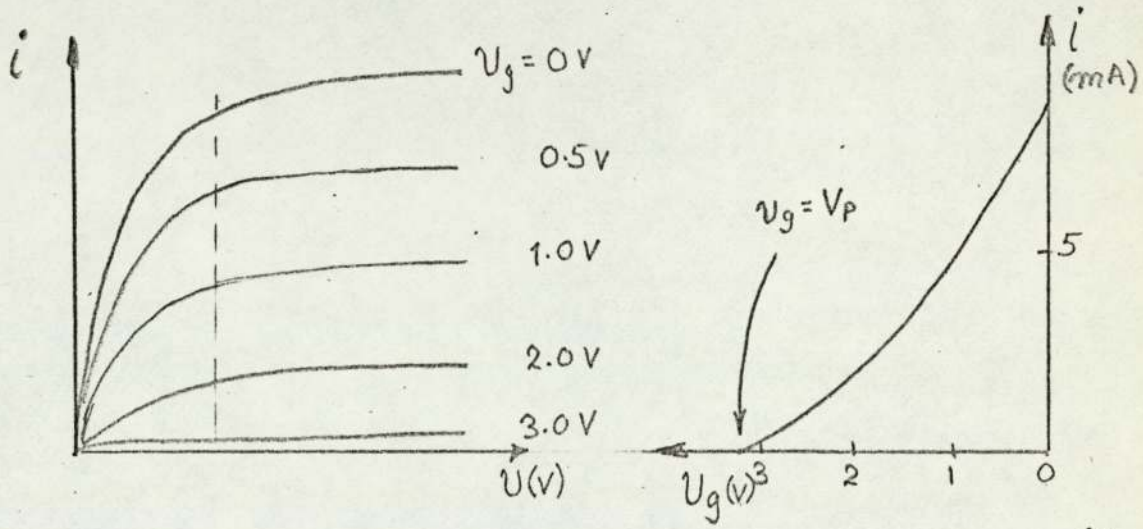


FIG. 4.15 TYPICAL VARIATION OF DRAIN CURRENT(i) WITH DRAIN VOLTAGE(U) AND GATE VOLTAGE (U_g)

when $U > V_p$ has been given [4.2] as:

$$i = I_p\left(1 - v_g/V_p\right)^2 \qquad (4.9)$$

The resistance of the channel (r) is then given by:

$$r = \frac{V_{cc}}{I_p\left(1 - v_g/V_p\right)^2} \qquad (4.10)$$

where Vcc is the d.c. supply voltage.

In the required companding characteristic shown in fig 3.2, the duration T, which is proportional to R_B should asymptote either to some high, or to some low value of T. As equation (4.10) stands large values of v_g will cause the resistance to asymptote the wrong way. Hence, to replace R_B, the f.e.t. should be biassed to pinch off and positive - going modulating signal should then drive the f.e.t. into conduction and lower resistance.

An approximate relation may be derived by adjusting the origin of the transfer characteristic to $v_g = V_p$. The drain current, as a function of input voltage (v_i) is then given by:-

$$i = I_p\left(v_i/V_p\right)^2 \qquad (4.11)$$

$$\text{and } r = \frac{V_p^2}{I_p} \cdot \frac{V_{cc}}{v_i^2} \qquad (4.12)$$

The predicted companding characteristic from equation (4.12) is shown in fig 4.16

To obtain experimental confirmation, a n-channel f.e.t. was connected as shown in fig. 4.17. The input

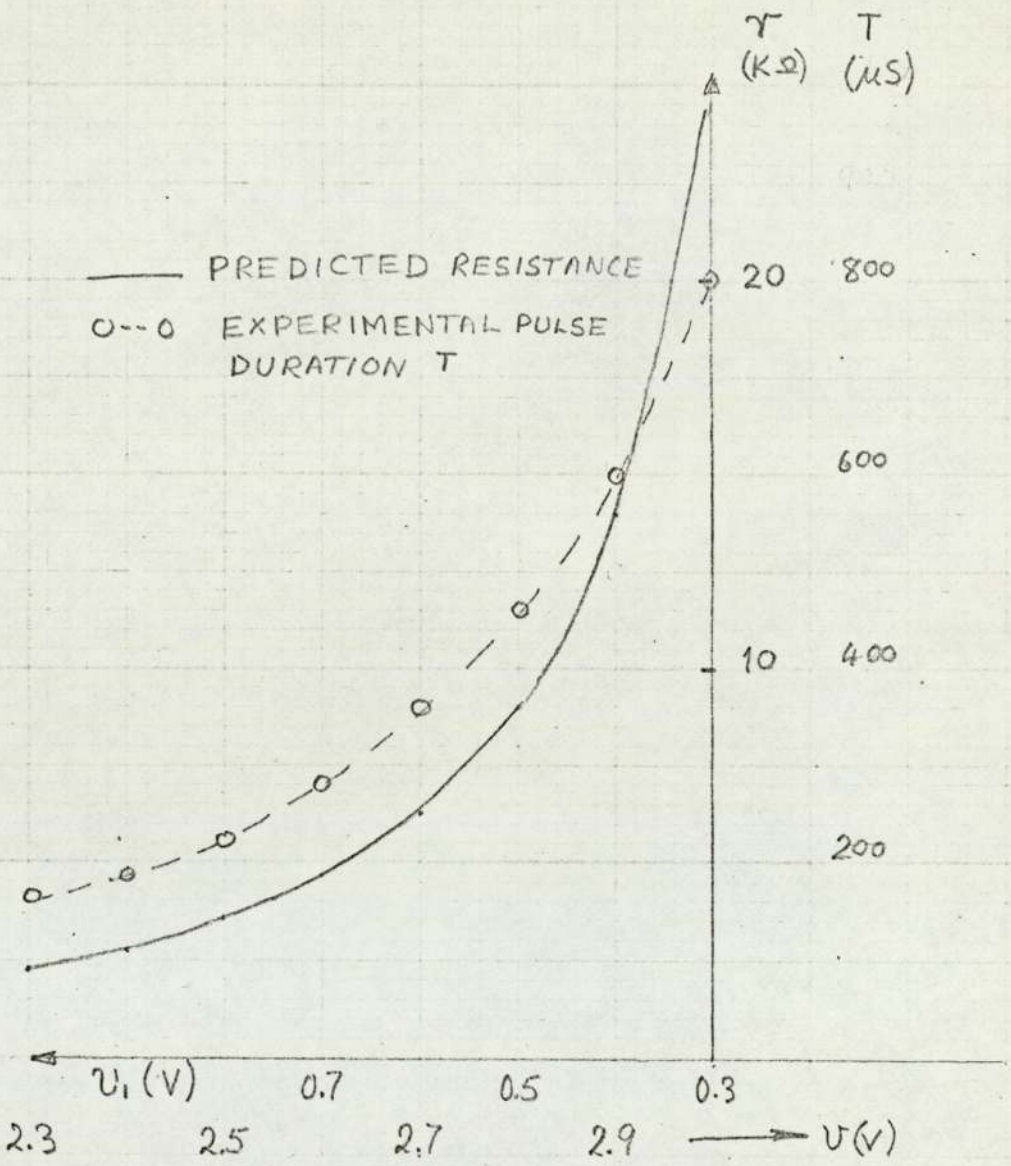
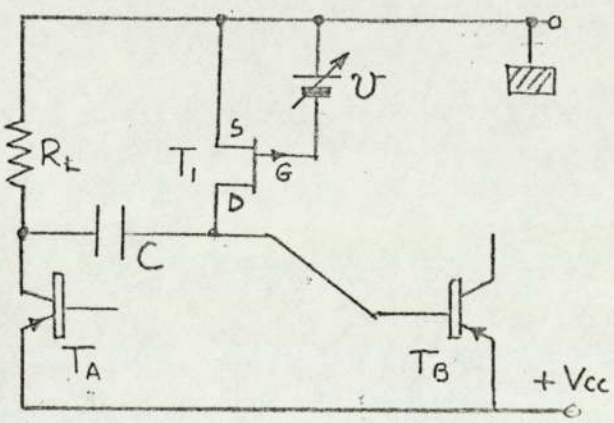


FIG 4.16. COMPANDING CHARACTERISTIC WHEN R_B IS REPLACED BY FET.



COMPONENT	VALUE/TYPE
T_A, T_B	2N2904A Si pnp
T_1	BFW10 n-channel
C	50nF
R_L	470Ω

FIG. 4.17. TIMING CIRCUIT WHEN R_B REPLACED BY A JUNCTION F.E.T.

voltage (V_1) was varied from zero to 3v for which the resistance changed from 20KΩ to 400Ω . The corresponding relative pulse durations are shown in fig 4.16.

The following observations maybe made on fig. 416

(1) The f.e.t's used, (Mullard B.F.W.10 and Motorola MPF 102), appear to have a transfer characteristic approximately given by:-

$$i = I_p\left(1 - V_g/V_p\right)^{1.5} \qquad (4.13)$$

rather than that given by equation (4.10)

(2) A high value of compression parameter (μ) is possible with a f.e.t.

It should be noted that no attempt has been made to obtain a balanced companding action from f.e.t.s. It is considered that the problems involved will be similar to those with bipolar transistors.

4.5. Conclusions from the Tests on Method 1.

The principle of coding by the first method has been investigated experimentally to test its feasibility. The p.l.m. stage, which is peculiar to the method, has been constructed from a simple monostable multivibrator, in which the timing elements are transistors connected as resistance modulators.

The principle of the method consisted in determining the transfer characteristic of the p.l.m. stage. That is a variable direct - voltage / current was applied to the base (gate) of the resistance modulator, and the corresponding duration of the output pulse was determined.

To simplify the measurement of pulse-duration, the tests were conducted with pulses which had a duration some 50 times larger than those which obtain in practice. The tests were carried out in four phases.

Firstly a single p.n.p. bipolar transistor replaced the base feed resistor (R_B) and a negative - going input voltage (V_i) was applied between base and emitter. It was predicted from simple theory that the transfer characteristic should be a curve for which the pulse duration (T) is proportional to exp. ($-V_i$). The experimental characteristic was of approximately this form.

The second and third phases were attempts to obtain transfer characteristics which were symmetrical for positive and negative modulation. In the second phase, a resistance modulator consisting of two transistors replaced R_B. The bases were current-fed to obtain $T \propto 1/V_i$. In the event, there was slight but unacceptable asymmetry. This was because the non-linearising of the transfer characteristics on positive and negative modulation were due to different effects.

In the third phase, the timing circuit was modified to include a capacitor C_2 shunted by a second bipolar transistor (R_2). It was shown that a symmetrical transfer characteristic is theoretically possible, but difficult to obtain precisely in practice.

The fourth and final phase was an investigation of the field-effect transistor as an alternative to the bipolar transistor. Although the operating principles are somewhat different, the companding characteristic obtained is similar to that obtained in the first phase described above.

Hence, it has been shown that it is possible to design a p.l.m. stage which will permit coding by the first method. It has also been demonstrated that considerable difficulties can occur in obtaining a transfer characteristic which is symmetrical on positive and negative modulation. These difficulties stem from the inability to devise a monostable multivibrator which gives a symmetrical characteristic. The problem may be likened to that of designing a single-ended class A stage, to have a large amount of odd harmonic distortion, but using a device with a parabolic transfer characteristic. It is, therefore, concluded that a multivibrator p.l.m. stage using ordinary transistors as timing elements to provide logarithmic companding, does not provide a practicable coding method.

CHAPTER 5

DEVELOPMENT OF A MODEL FOR THE METHOD 5 ENCODER

5.0. The Encoder in Outline

5.1. Use of Integrated Circuits

5.1.1. The T.T.L. NAND Logic Circuit

5.1.2. The J.K. Master-Slave Bistable

5.2. The Divider

5.3. The Sequencer

5.4. Channel Pulse Generation

5.4.1. A Monostable Multivibrator P.L.M. Stage

5.4.2. A Ramp and Comparator P.L.M. Stage

5.5. The Binary Counter

5.6. The Parallel - Serial Converter

5.7. The Decoder

5.8. Clock Pulse Sweep Generation (Introduction)

5.0. The Encoder in Outline

It was shown in Chapter 3 that the fifth method proposed for pulse-count coding, had a definite advantage over the other four methods. Namely, the encoder and decoder required identical methods of clock pulse generation, so that the two coders could be similarly instrumented. Consideration is now given to the designs of models for this coding method. Once again, to simplify the problems of accurate measurement of pulse duration, a low-frequency model is planned, but with some parameters different from those given for Method 1 in Chapter 4. The relevant parameters for the Method 5 encoder are as follows:-

Clock p.r.f. at instant of zero modulation - - - 450 KHZ
Number of binary digits - - - - - - - - - - - 7
Number of quantum levels 2^7 - - - - - - - - - 128
Number of channels - - - - - - - - - - - - - - 5
Channel pulse duration (including guardbands) - - 1.00 ms

It will be shown in the following sections that the above values were dictated both by the availability and limitations of the chosen devices.

Block diagrams have already been given for the encoder and decoder in figs. 3.9 and 3.12 respectively. The principle of the method is recalled as follows. The channel pulses are derived from the binary digit pulse train via the DIVIDER and SEQUENCER. The channel pulse length is linearly modulated by the signal in the P.L.M. stage. The variable-length pulses then GATE the swept-

frequency clock pulses, which may be generated in two ways. In both types of CLOCK PULSE GENERATOR the frequency is proportional to

$$\frac{d[\log(1+\mu V)]}{dv}$$

where log $(1 + \mu V)$ is the companding function given in equation (2.1). The gated high frequency pulses are applied to the BINARY COUNTER, whose stage outputs then represent the weights of the binary equivalent of the logarithmically compressed signal. These are applied to a PARALLEL-SERIAL CONVERTER, and converted into a train of code pulse-groups.

Certain stages of the coder are common to all methods of pulse-count coding, and because their principles are well established,[28,31] they are considered in this chapter. In particular, designs are given for the divider, the sequencer, the p.l.m. stage, the gates, the binary counter and parallel-to-serial converter. The two types of clock pulse generation each contain two main stages, namely a LINEAR VOLTAGE-FREQUENCY CONVERTER and a SWEEP GENERATOR. Since the development and application of these stages are original to this work, a brief introduction only is given in this chapter. More detailed descriptions of the two stages are given in Chapters 6 and 7.

5.1. Use of Integrated Circuits

It was decided to use integrated circuits where possible, and to simplify design and construction, one type of base, the dual-in-line, was adopted. On the

grounds of economy, circuits from the medium speed Transistor - Transistor - Logic (T.T.L.) family were selected. The latter choice set a limit to the minimum pulse duration of about 100 ns, but this was negligible in the low-frequency model on which measurements were made. The basic digital I.C. is the NAND logic gate, for it is not only fundamental to all the gates in the model but also to the J-K bistable circuit used in the counter, register etc. and to the monostable circuit used in the p.l.m. stage. Hence, the description of the instrumentation commences with these basic logic circuits.

5.1.1. The T.T.L. NAND Logic Circuit

The T.T.L. arrangement is particularly suited to integrated circuit techniques for it can give the greatest number of logic gates for a given size of silicon chip. This arises because T.T.L. makes more use of p.n. junctions than other components. This is in contrast to Transistor-Resistor Logic (T.R.L.), which tends to use a larger number of resistances. Furthermore, in the manufacture of an I.C., it is possible to fabricate the multi-emitter transistor which enables the convenient formation of the T.T.L. NAND gate.

The circuit of a typical NAND gate is shown in fig. 5.1. It may be noted the n.p.n. formations shown, make positive logic preferable and this appears to be a fairly uniform convention. Another fairly common standard in T.T.L. logic is the requirement for a

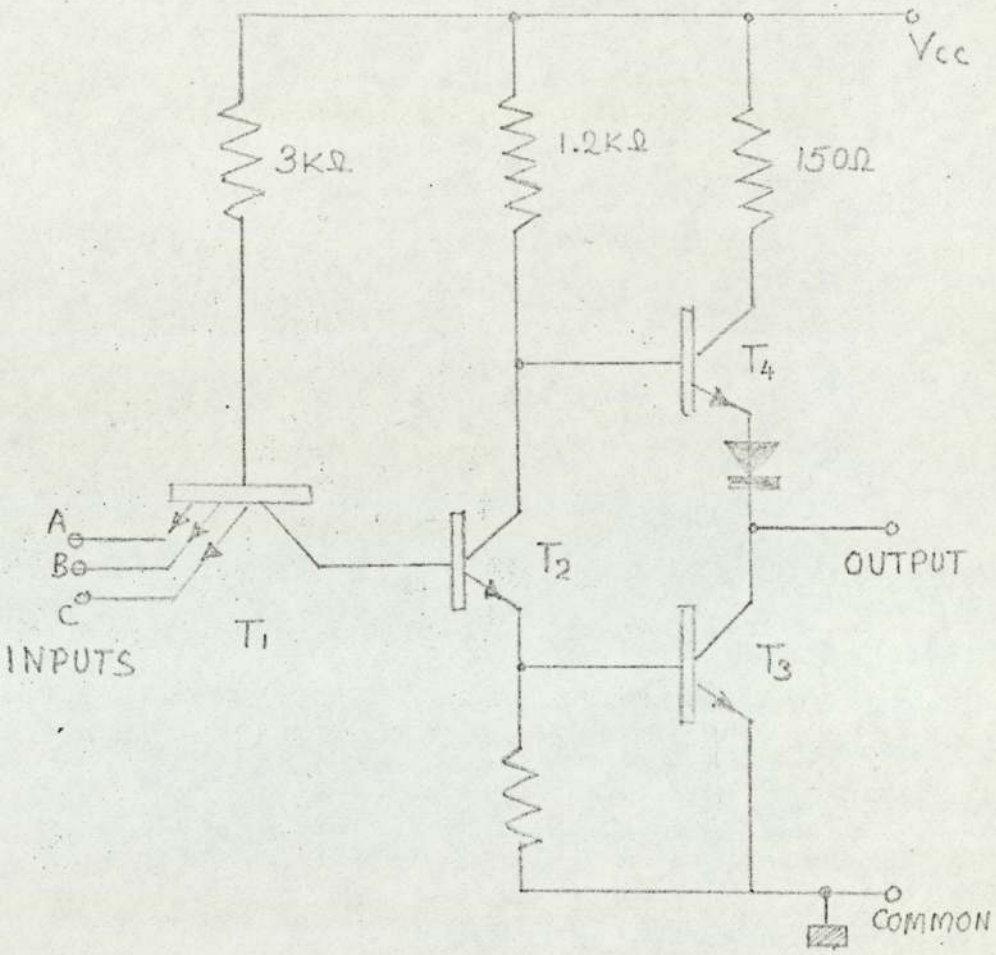


Fig. 5.1 AN INTEGRATED CIRCUIT WHICH GIVES THE NAND FUNCTION.

single 5V d.c. supply.

The operation of the NAND circuit is as follows. When the inputs A, B or C are at a logical '1' level (or unused), the circuit is in the normal state with T_1, T_4 non-conducting and T_2, T_3 conducting, giving a logical 0 level at the output. When one of the inputs A-C is grounded, T_1 conducts which makes in turn, T_2 non-conducting, which gives logical 1 at the output. Hence, the presence of one or more 0 level inputs will give a 1 level output, which is an expression of the NAND function. It may be noted that the T.T.L. NAND gate cannot distinguish between an unused input and a 1 level. This is an advantage when interconnecting gates, for it obviates the connection of those inputs which are not required.

The applications of the NAND gate to the encoder are straight forward as indicated in fig. 3.9. In the first case, when a clock pulse occurs within the duration of the channel pulse, it should be transmitted to the binary counter. That is, the outputs of the p.l.m. stage and the v-f converter form the inputs A, B to an AND gate, which may be given by two NAND gates in tandem. Another application is described in the parallel-to-serial conversion stage.

5.1.2. The J.K. Master-Slave Bistable

The bistable multivibrator may be considered as two NAND gates cross-connected. This circuit may be made

into a divide-by-two, or binary stage (or "toggle") by arranging a CR diode circuit at the trigger input as shown in fig. 5.2. The input pulses are steered first to one side and then to the other. The development of I.C.s has shown that the master-slave circuit may be realised conveniently, and this permits a toggle-action without external components.

A master-slave circuit is shown in fig.5.2 as two sets of cross-connected NAND gates. The J.K. master-slave bistable is a particular type in which the normal (Q) and complementary ($\overline{Q}$) outputs are connected to the K and J inputs respectively, to permit toggle action. The operation of the circuit, when a clock pulse waveform is applied, follows a four-point sequence, as shown in fig. 5.2. and as follows:-

(1) gates 3 and 4 close, isolating slave from master,

(2) gates 7 and 8 open, connecting master to inputs,

(3) gates 7 and 8 close, isolating master from inputs,

(4) gates 3 and 4 open, connecting master to slave.

Hence, the leading edge of the clock pulse may only cause a transition in the master section at point (2), while it is isolated from the slave. Whether a transition actually occurs, depends upon the logic levels at the J and K inputs.

At the trailing edge, the master section is isolated from the inputs, and at point (4) the logic levels, which have been determined by the J-K inputs, are transferred from the slave to the master. The follow-

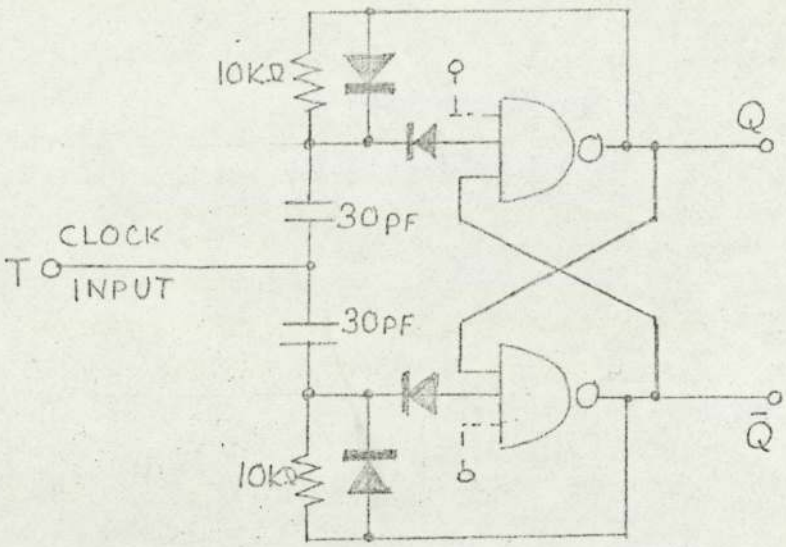
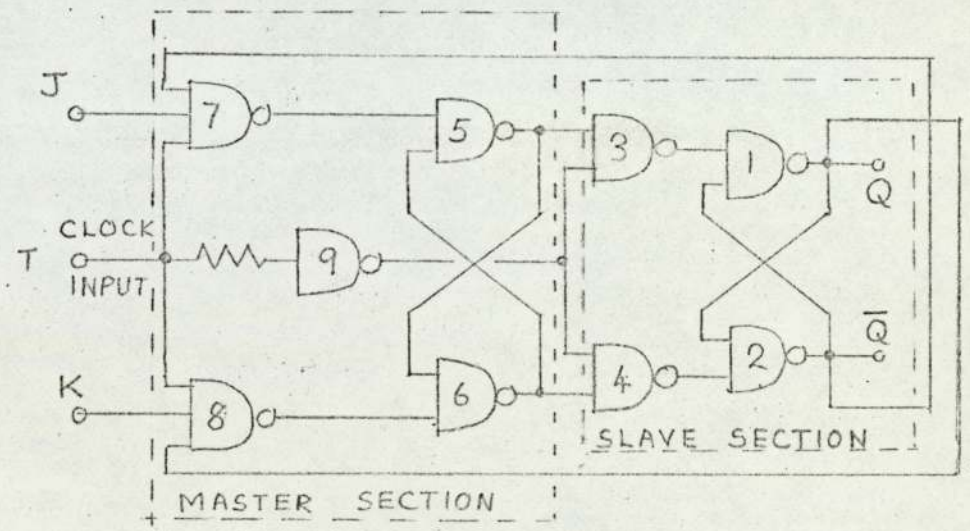
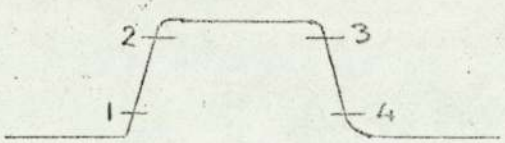


FIG. 5.2(a) A BISTABLE MADE WITH I.C. NAND GATES AND MADE TO "TOGGLE" WITH EXTERNAL COMPONENTS





1 GATES 3 & 4 CLOSE — SLAVE ISOLATED FROM MASTER
2 GATES 7 & 8 OPEN — MASTER CONNECTED TO INPUTS
3 GATES 7 & 8 CLOSE — MASTER ISOLATED FROM INPUTS
4 GATES 3 & 4 OPEN — MASTER CONNECTED TO SLAVE

FIG. 5.2(b) A J.K. MASTER-SLAVE BISTABLE WITH A TOGGLE ACTION ACCORDING TO THE 4-POINT SEQUENCE SHOWN.

ing characteristics of J-K master-slave bistables may, therefore, be noted:-

(a) Transitions in the output are observed on the trailing edge of the clock pulse.

(b) A single logic 0 level at any K input, can prevent a transition from 1 to 0 at Q.

(c) A single logic 0 level at any J input can prevent a transition from 1 to 0 at $\bar{Q}$.

(d) The control of the J and K inputs may be over-ridden by the application of 0 levels at the set and clear terminals. That is, a 0 at SET forces a 1 at Q (and a 0 at $\bar{Q}$) and a 0 at CLR forces a a 1 at $\bar{Q}$ (and a 0 at Q).

The following truth table may now be drawn.

Table 5.1. TRUTH TABLE FOR J.K. BISTABLE

Inputs at tn		Output at t_{n+1}
J	K	Q
0	0	same as Q at t_n
0	1	0
1	0	1
1	1	same as Q at t_n

In table 5.1. t_n and t_{n+1} denote the instants just before and just after the trailing edge of the clock pulse.

The J-K flip flop is desirable in a synchronous binary

counter and a sequencer and has been so applied. To simplify construction, it has also been used in the divider, parallel to serial converters and the start-stop bistable of the decoder. These applications are described in the following sections.

5.2. The Divider

In a pulse-count coder the clock pulses are counted during one channel pulse duration, and converted into a binary digit train during the next channel pulse. In order to observe a code pulse group upon an oscilloscope, however, the bit pulse period should be related to the full channel pulse duration. This is achieved conveniently by applying the binary digit train to a divide-by-eight scaler followed by the sequencer shown in fig. 5.5.

The divider, shown in fig. 5.3., consists of a cascade of three J-K bistables, in which the normal outputs (Q) of the first and second stages are connected respectively to the clock inputs of the second and third stages. This is the "ripple-through" connection, so called because the transitions occur sequentially from stage to stage. This gives a disadvantage as the transition at the Nth stage suffers a time delay w.r.t. the input pulse of $n\tau$, where τ is the propagation delay per stage. With the I.C's used the propagation delay is only 20 ns per stage so that the pulse at the third stage is only delayed by some 60 ns. It is considered that this small delay will not prevent synchronism.

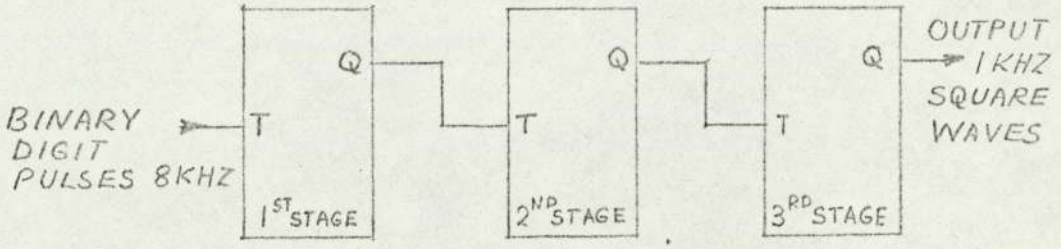


FIG. 5.3. THE DIVIDER USING J.K. BISTABLES IN "RIPPLE THROUGH" MODE.

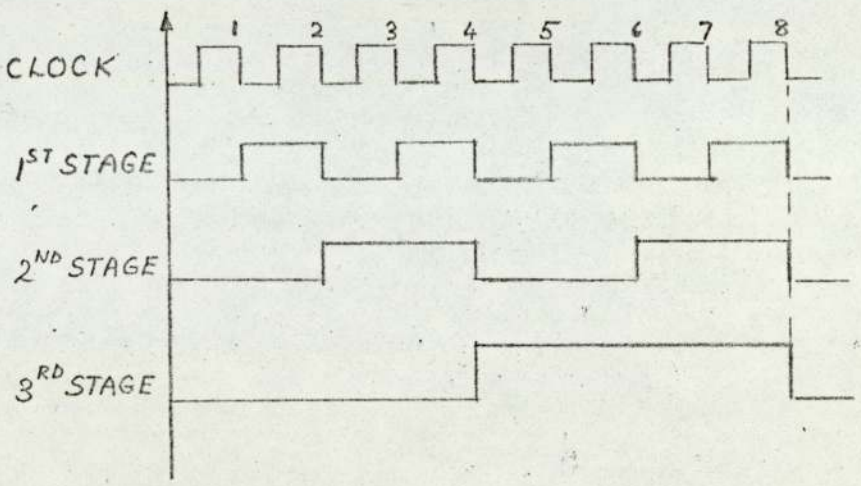


FIG. 5.4. WAVEFORMS IN DIVIDER (ALSO IN BINARY COUNTER.)

The pulse-waveforms are shown in fig. 5.4. It may be noted that transitions at each stage output only occur when the input pulse goes from logic level 1 to logic level 0. This characteristic of the master-slave flip flop[28] has been noted in section 5.1.2. and arises from the transfer of logic levels from master to slave sections on the negative edges of the clock pulse. The J and K inputs are left unconnected in a "ripple-through" counter, but in T.T.L. logic an unused input constitutes a 1 level. Hence each complete clock pulse causes one output transition, and the final stage produces one complete pulse for every eight binary digit pulses.

5.3. The Sequencer

The divider output, consisting of 1KHZ square pulses, is applied to the sequencer which generates five channel synchronising pulse trains. The channel synchronising pulse is 1.00 ms long while the recurrence period is 5 ms, as shown in fig. 5.5.

These pulse trains are generated in a five stage ring counter formed with five J-K bistables[28] as shown in fig.5.5

The normal (Q) and complementary ($\bar{Q}$) outputs are connected respectively to the succeeding J and K inputs as in a shift register. The final outputs, however, are not returned to the initial J and K inputs, as is usual in ring counters. Instead, as shown in fig. 5.5., the J and K inputs of FFA are inhibited by the $\bar{Q}$ outputs of FFB, FFC and FFD. If any of these are at logic 0, Q_A cannot go to

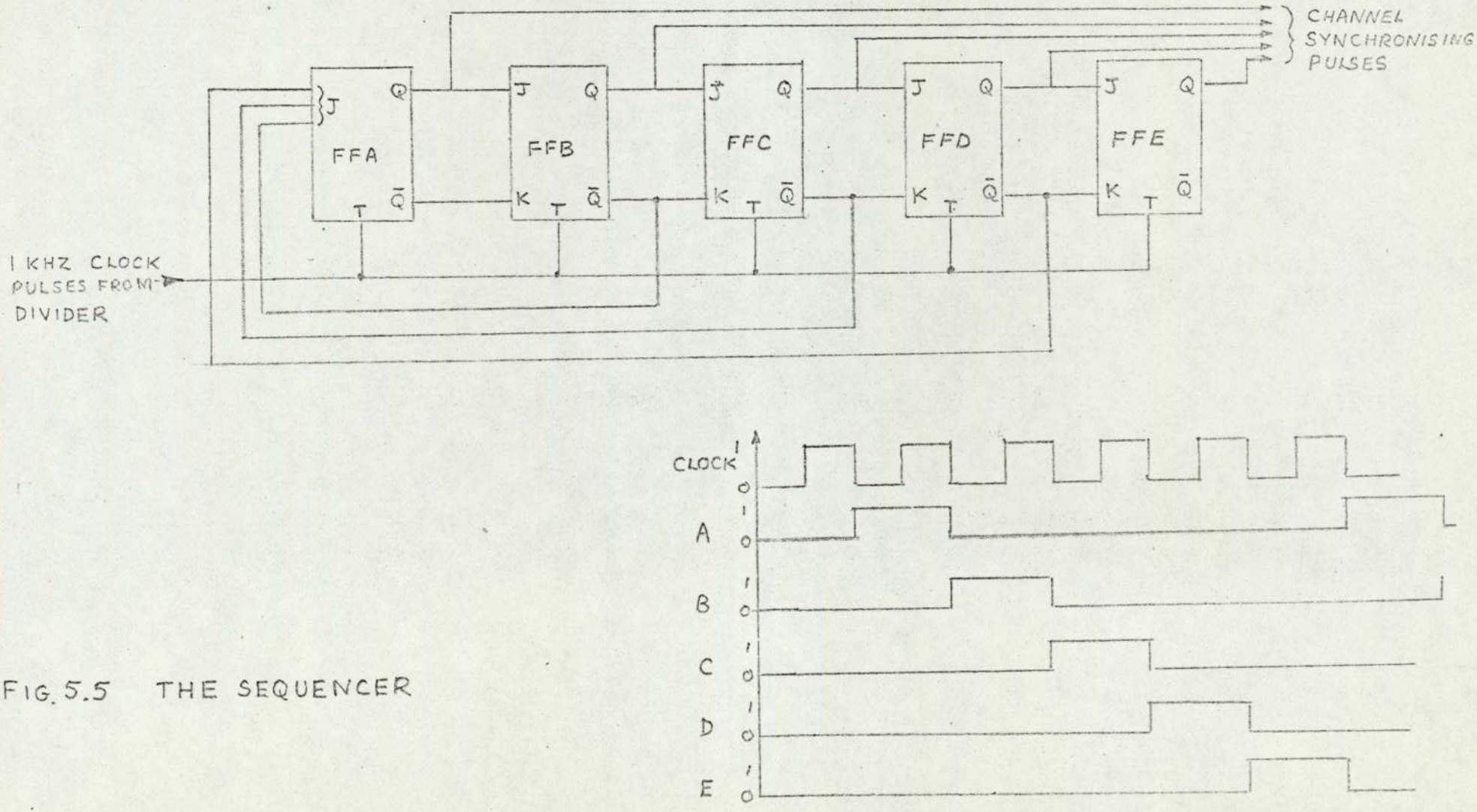


FIG. 5.5 THE SEQUENCER

logic 1 level. Hence, when the normal outputs Q_B and Q_C have been at 0 level for one clock pulse period, a pulse will be generated at Q_A.

This method of connecting the J and K inputs has the advantage that the final output Q_D is not loaded by feedback. Hence, the full output is available not only to trigger the p.l.m. stage but also to provide the clear pulse for the seven stage binary counter, which forms a considerable logic load.

It may be noted, however, that a limitation arises from the use of J-K bistables, in that the number of J-K inputs is usually limited to three. This number, (the FAN-IN), may be increased by the use of external gates. This procedure, however, was decided against, because of the additional complexity in wiring. Hence the number of channels in the model is limited to five.

5.4. Channel Pulse Generation

The outputs of the sequencer consist of the channel marker pulses which may be used to synchronise the length modulated pulses. In the experimental encoder one channel only is to be instrumented, but two different types of p.l.m. stage are considered as follows:-

(a) a monostable multivibrator;

and (b) a ramp-and-comparator.

5.4.1. A Monostable Multivibrator P.L.M. Stage

The design of a linear p.l.m. stage using discrete transistors in an emitter-coupled monostable multi-

vibrator is well established[31]. There seemed little point, however, in designing such a stage, which would inevitably have some non-linearity which may mask the errors, due to non-linearity in the novel part of the coding process. To make use of integrated circuits therefore, it was decided to simulate the p.l.m. stage by a single I.C. monostable multivibrator. The duration of the channel pulse could be varied linearly over several decades with an external decade capacitor, and measured by a digital universal counter. In this way the duration of a given channel pulse could be accurately measured and any coding errors which occur would not be due to non-linearity in the p.l.m. stage.

A diagram of the monostable used is shown in fig. 5.6. With a timing resistance (R_T) of 10 KΩ, the pulse duration could be varied linearly with timing capacitance (C_t) over the respective ranges 1 μS to 1 mS, and 150 pF to 150 nF.

During tests upon the experimental encoder in which the monostable was used to produce length-modulated pulses, a variation was occasionally observed in the number of clock pulses gated by a given channel pulse. In order to eliminate timing jitter in the p.l.m. stage, an alternative circuit consisting of a comparitor with a ramp input, was tried.

5.4.2. A Ramp and Comparator P.L.M. Stage

Although the use of a linear I.C. operational amplifier

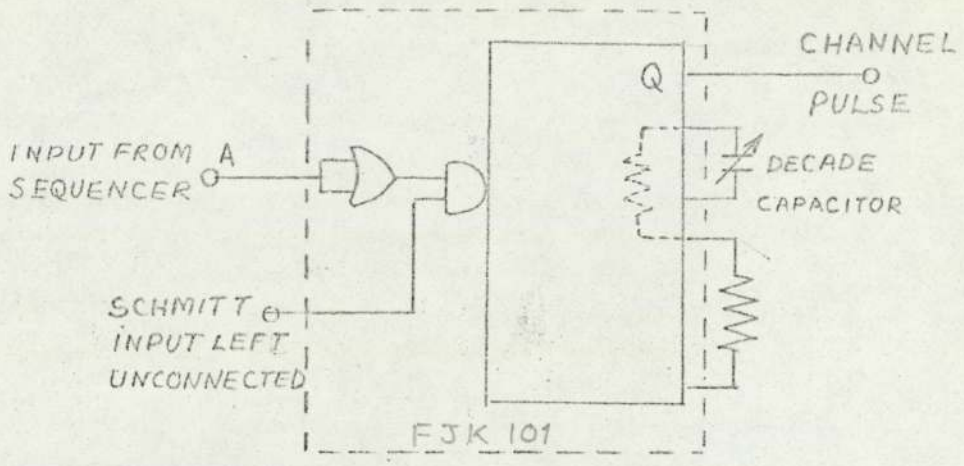


FIG. 5.6 AN I.C. MONOSTABLE FOR THE CHANNEL PULSE GENERATOR.

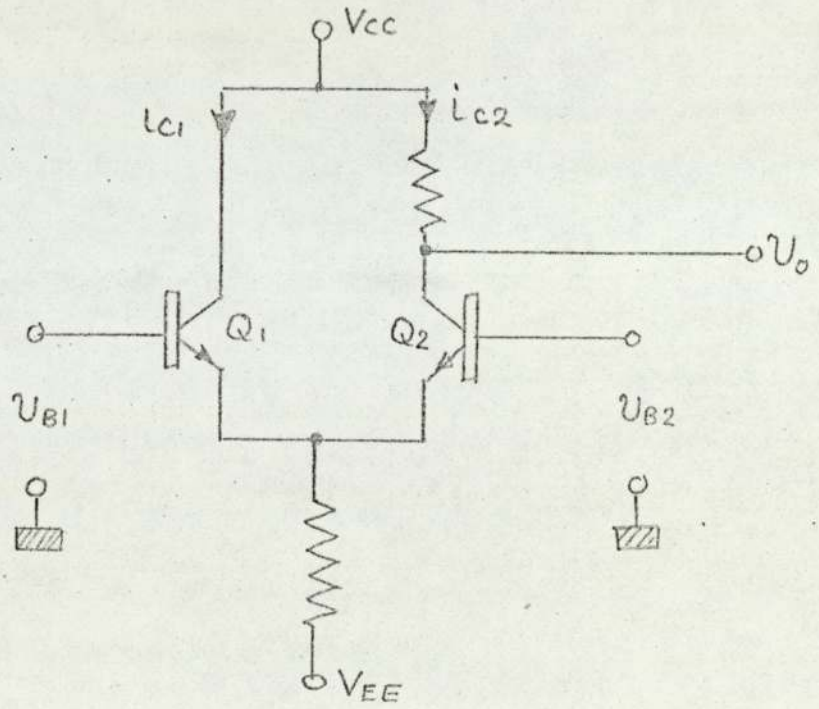


FIG. 5.7 THE TRANSISTOR COMPARATOR.

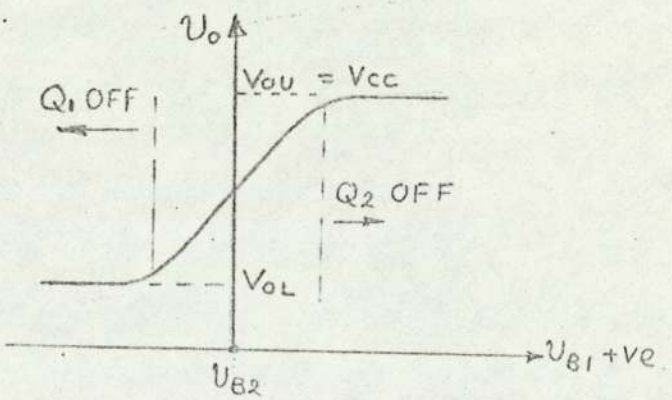


FIG 5.8 TRANSFER CHARACTERISTIC FOR THE TRANSISTOR COMPARATOR.

(O.A) as a comparator is relatively new,[28] the idea of using it with a ramp input for analogue to digital conversion is becoming well used.[28,31] A common form of I.C. comparator is based upon the emitter-coupled clipper[31] shown in fig. 5.7. The principle may be explained as follows.

Consider that the applied voltage v_{B1} drives transistor Q1 into cut off. Transistor Q2 will conduct only if the voltage v_{B2} drives it into the active region. The output voltage (v_o) will have the steady value (V_{OL}) as shown in fig. 5.8. If now v_{B1} is increased positively, Q1 conducts, raising the emitter potential, and therefore decreasing the base-emitter voltage of Q2. The current i_{C_2} falls and v_o increases to the saturation level (V_{CC}), as Q2 is cut off. Hence, the transfer characteristic of the emitter coupled clipper takes the form shown in fig. 5.8.

To show how this circuit functions as a comparator, consider in fig. 5.8. a reference voltage (v_{B1}) to be at the value when Q1 is conducting. Let an input voltage (v_{B2}) be increased by Δv, so that i_{C2} increases and i_{C1} decreases. Clearly, if Δv is large enough, the output voltage undergoes a transition from V_{OL} to V_{OU}. That is, the property of a comparator is that the output voltage changes state when the input voltage (v_{B2}) reaches a certain value. If the comparator were preceded by a high gain differential amplifier, the output transition could be made to occur when input and reference voltages differ by a few

millivolts. The high gain of a balanced differential transistor pair can be further enhanced by reducing the gain to common-mode signals,[31] and this is achieved by a constant current supply to the common emitter. The complete high gain comparator is shown in fig. 5.9.

If now the reference voltage, applied to the non-inverting input (+), is a positive-going linear ramp, while a signal voltage is applied to the inverting input (-), then when the ramp is zero, the output is at V_{OL}. As the reference rises to within a few millivolts of theinput signal, the output abruptly increases to V_{OU}. If the signal input is increased, the referance has to increase to a higher value and the transition to V_{OU} is delayed. Hence, the step voltage is linearly modulated in time, and if a sawtooth reference is applied, the resulting pulses are length-modulated. The linear I.C. used, (710 OPA), is a high gain operational amplifier ($A_V = 50 \times 10^3$) and was specially designed to have low thermal drifts. A feedback resistor R was connected to provide hysteresis. This is required because the high gain makes the comparator sensitive to noise.[28] The feedback increases the threshold level by about 20mV, but since the input signals are greater than this, the error due to hysteresis should not be large.

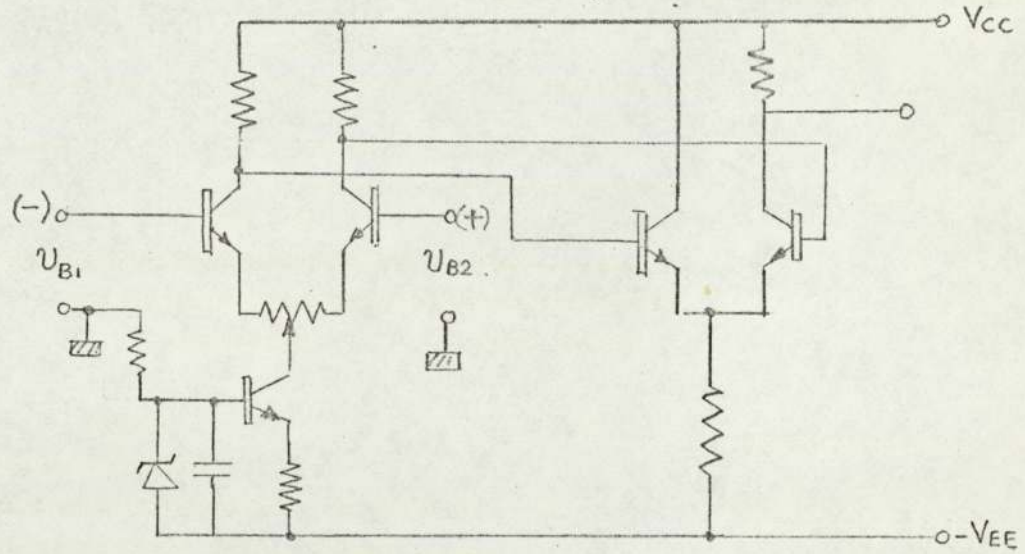
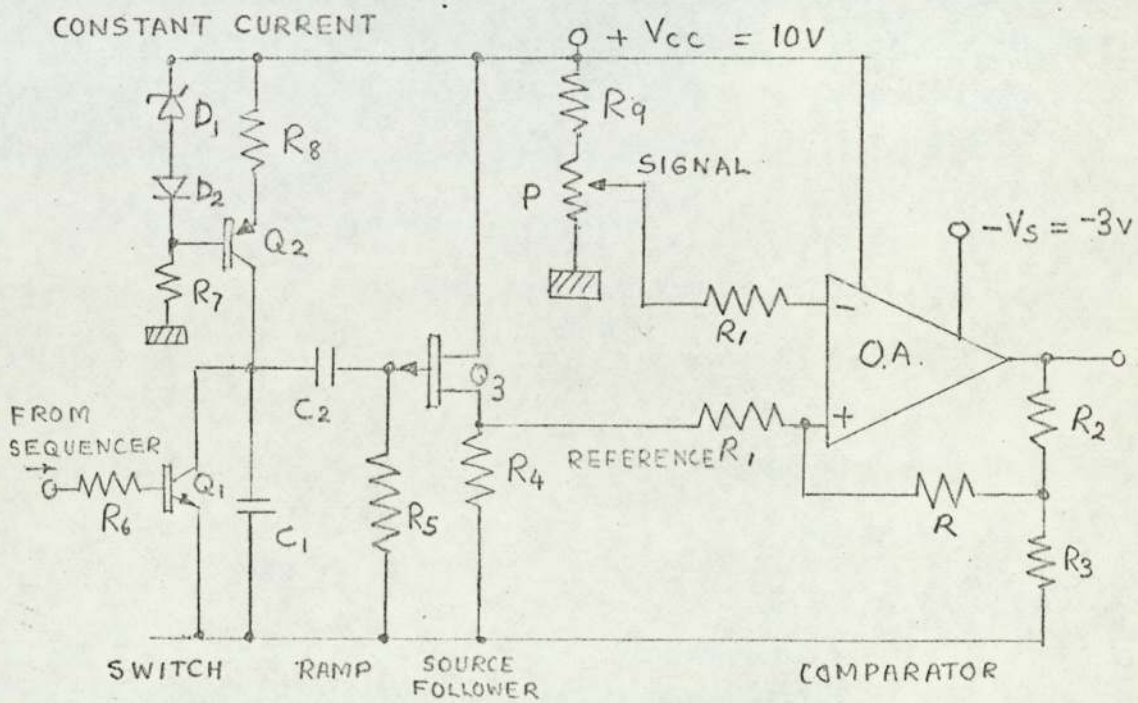


FIG. 5.9 A DIFFERENTIAL COMPARATOR.



COMPONENT	R_1, R_9, R_2, R	R_3	R_4	R_5	R_6, R_7	R_8	P	C_1	C_2
VALUE	100KΩ	200Ω	1KΩ	3MΩ	5KΩ	47KΩ	4.7KΩ	5nF	100nF

COMPONENT	D_2	D_1	Q_1	Q_2	Q_3	O.A
TYPE	2N4285 (e-b diode)	2.2V Si Zener	2N4286	2N2904	BFW10	710 OPA.

FIG. 5.10 A RAMP AND COMPARATOR P.L.M. STAGE

A diagram of the circuit used is shown in fig. 5.10. The complementary output of the sequencer ($\bar{Q}$) is applied to a transistor switch so that the capacitor (C) charges during the channel pulse duration. A linear ramp is obtained by constant current charging[31], by transistor Q2. To avoid shunting C, and increasing non-linearity, a junction f.e.t. is connected as a source-follower. The sawtooth output voltage of the latter is applied to the non-inverting input (+) of the i.C. comparator. The signal input voltage is simulated by a potential divider, so that when the input voltage was changed from 50 mV to 200 mV, the duration of the high output state (i.e. when $V_o = V_{OU} = V_{cc}$) varied from 800 μs to 200 μs.

It must be admitted that the comparator p.l.m. stage differs in two respects from the monostable stage

(a) the leading edge (rather than the trailing edge) is varied;

(b) the variation in pulse duration is smaller.

Nevertheless, both stages were tried, but as far as timing jitter was concerned, both appeared to give the same result. The monostable stage, however, is provided by a simple digital circuit (fig.5) and hence this was incorporated in the experimental model.

5.5. The Binary Counter

A binary counter could have been constructed from a cascade of bistable elements in a "ripple through" connection, i.e. the output Qr is connected to input Tr+1. Such counters are unable to register correct counts at high pulse frequencies, because of the propagation delays in each stage.(31) Since the input pulses to the experimental encoder may have frequencies up to 10^6 HZ, it was considered advisable to connect the bistables to form a synchronous counter. It is convenient to do this with digital I.C's because of the special property of the J-K flip-flop. It has been stated in section 5.1.2. that the J-K terminals can be used to inhibit a transition in a bistable.

To explain the synchronous connection, consider the pulse waveforms of the outputs of a binary counter shown in fig. 5.4. The τ th stage in a n-stage counter undergoes a transition when all the preceding stages go from logic level 1 to logic level 0. This means that the τ th stage must be inhibited by having at least one pair of J-K terminals at logic level 0, right up to the $[2^{(\tau-1)}-1]$ th clock pulse. This condition is given by connecting the normal output Qr to the $(J\text{-}K)_{r+1}$, $(J\text{-}K)_{r+2}$ .... $(J\text{-}K)_n$ terminals.

When the binary counter was designed, there was not a master-slave J-K bistable available which had more than three J-K inputs. Neither were there available any 5 or 6 -input AND gates to expand the input capability of a bistable. Hence, it was decided to construct the counter

in two synchronous parts which were ripple connected as shown in fig. 5.11. That is, in the experimental encoder the swept frequency clock pulses are fed to the clock inputs of the first four stages, while the normal output Q_4 is fed to the remaining clock inputs.

The counter has to be cleared once a count has been transferred to the output register. In the experimental encoder the sequencer output Q is connected to the clear pulse line.

5.6. Parallel to Serial Converter

At the end of a given channel pulse, the number of swept frequency clock pulses contained within that pulse is registered on the counter outputs as a series of logic levels. To arrange for a train of binary digit pulses, the series of logic levels must be set into the corresponding stages of a register. The appropriate code pulse group will then be generated when the register is pulsed at the binary digit rate.

The counter outputs must only be connected to the set input at the end of a count and so controlling gates are interposed between the counter outputs and register. These gates are enabled (opened) by the register set pulse which is derived from the gated clock pulses.

The system for parallel-to-serial conversion is shown in fig. 5.11. The shift register is made up of I.C. J-K bistables with the same type of inter-stage coupling as the sequencer.

BINARY STAGES FJJ 111A
NAND GATES FJH 131

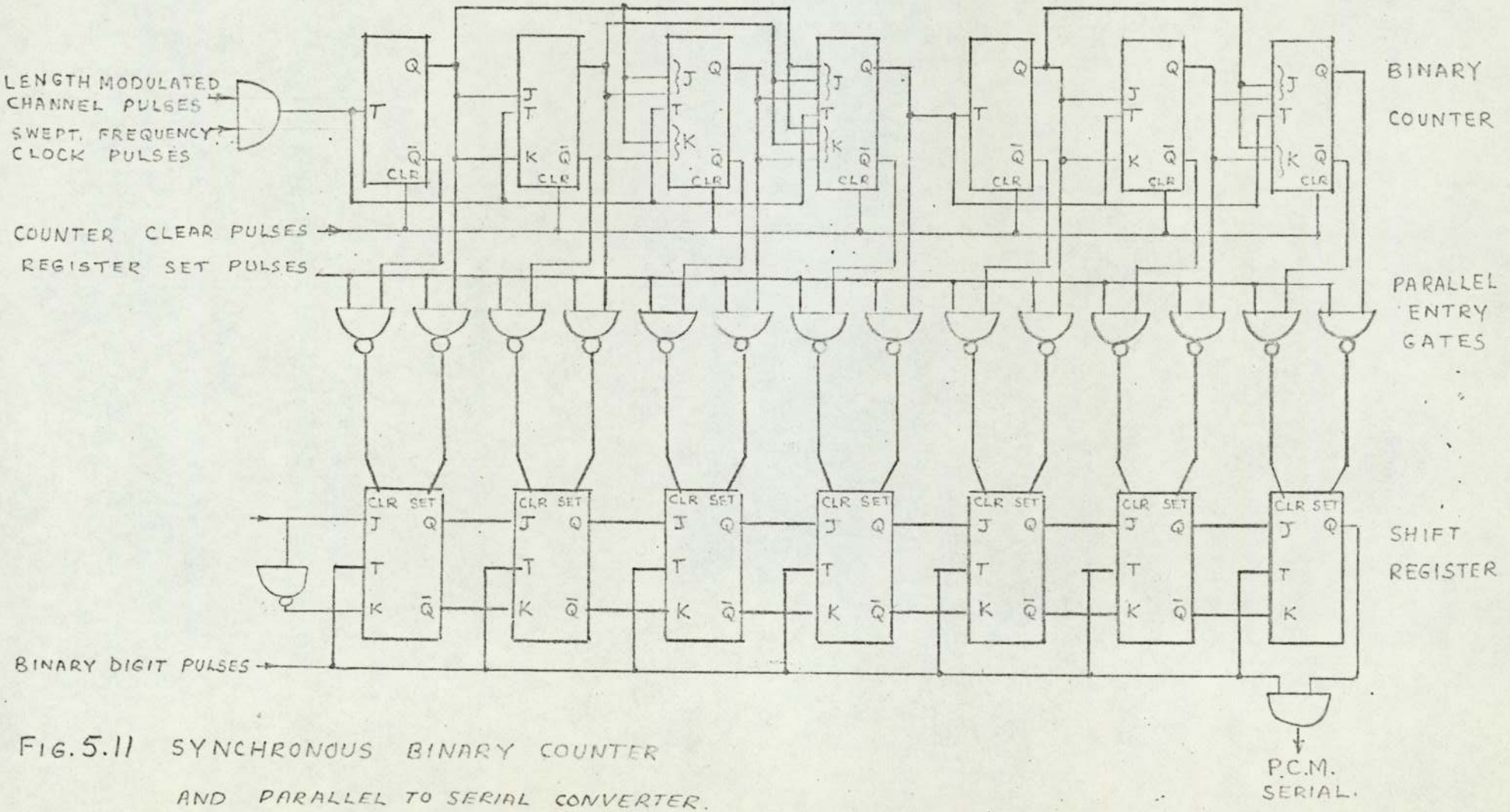


FIG. 5.11 SYNCHRONOUS BINARY COUNTER AND PARALLEL TO SERIAL CONVERTER.

The bistables are of the master-slave type having a pre-set input which, like the clear input, overrides the J, K or clock input. To ensure that when, on the register, a normal output (Q) is set at logic 1 level, the alternative output ($\bar{Q}$r) is at logic 0 level, both the normal and alternative outputs of the counter are gated. Hence there are 14 two-input NAND gates controlled by the register set pulse, for parallel entry to the register. If a logic 1 level is present at a counter output Q (then $\bar{Q}$ = 0), the next register set pulse will cause logic a 0 level to the set input, thus forcing a 1 level at the register output Q. The 0 level on $\bar{Q}$ above causes a 1 level at the clear input so that register output $\bar{Q}$ will complement the normal output.

To ensure that only a binary digit code pulse group is generated, the final output of the shift register is gated by the binary digit pulse which has itself been gated by the sequencer alternative output ($\bar{Q}$).

The pulse waveforms at various stages in the encoder are shown in fig. 8.2.

5.7. The Decoder

The components of the decoder are shown in fig. 3.12. Many of them, for example the register and binary counter etc. are common to both ends of the system. There are two important differences; firstly, of operation; secondly, the p.l.m. stage of the encoder is completely different in function from the start-stop bistable in the decoder.

The difference in operation, of course, arises because the decoder is, functionally, the reverse of the encoder. In the decoder the incoming code-pulse group is fed into a shift register which is like the output register of the encoder described in section 5.5.
The register outputs are transferred via gates to the pre-set terminals of the binary counter, as in the encoder, except in reverse. The binary counter is driven under a swept frequency clock-source which is gated by a channel synchronising pulse. This leads to the second important difference between the encoder and decoder.

The binary counter may be made to count up or down from the pre-set code, and the latter alternative was chosen. At the start of a count-down, a bistable is set. When the count reaches zero, a NAND gate whose inputs are connected to the complementary ($\bar{Q}$) outputs of the counter, will give a logic 0 output. This is applied to the reset terminal of the bistable. That is, the interval for which the bistable has been set is the count-down time which should correspond to the length-modulated pulse of the encoder. Therefore, the start-stop bistable corresponds to the p.l.m. stage.

It will be recalled from section 5.4.1. that the modulated signal in the encoder was simulated by variation of the timing capacitor of the p.l.m. stage in order to ensure that any coding errors were not due to non-linearity in that stage. For similar reasons, it was decided to measure the "set-time" of the start-stop bistable and use that as the decoder output. Hence, in the testing of the overall system

the corresponding pulse durations at encoder and decoder could be measured and compared.

The components of the experimental decoder are given, in detail, in fig. 8.1 . The following points are worthy of note:

(a) The reverse-counting operation of the binary counter is ensured by connecting the complementary outputs ($\bar{Q}$) to the succeeding J-K inputs.

(b) The synchronising pulse-trains e.g. register clear pulses, and counter write-in pulses are obtained from the encoder. (The topic of synchronisation in the model is treated in Chapter 8).

5.8. Clock Pulse Sweep Generation (Introduction)

It has been shown in Chapter 3 that for a compression parameter (μ) value of 15, the clock p.r.f. must be swept over the range $0.33f_o$ to $5f_o$. Assuming a maximum value of 450 KHZ, given in section 5.0, the clock p.r.f. is to be varied from 30 KHZ to 450 KHZ.

The clock pulses, however, are to be swept so that the frequency varies non-linearly with time, as shown in figs. 3.4 and 3.8. Therefore, the clock pulse generation is in two stages:

(a) a linear voltage-to-frequency converter and

(b) a non-linear sweep generator which provides a voltage waveform whose time dependence is the same as that required for the clock p.r.f.

The first stage (a) is developed in chapter 6, while the second stage (b) is covered in chapter 7.

CHAPTER 6

THE VOLTAGE-TO-FREQUENCY CONVERTER

6.1. Introduction

6.2. The Biddlecombe V-f Converter

6.3. Factors Affecting Non-Linearity, Upper and Lower Frequency Limits

- 6.3.1. A simplified Circuit
- 6.3.2. Effect of Output Resistance upon Linearity
- 6.3.3. Effect of Shunt Capacitance upon Linearity
- 6.3.4. Effect of Temperature upon Linearity
- 6.3.5. The Upper Frequency Limit
- 6.3.6. The Lower Frequency Limit

6.4. A Dual Monostable-Astable V-f Converter

6.5. Conclusion

6.1. Introduction

A linear voltage-to-frequency converter is a circuit for which the frequency of the output voltage is directly proportional to an input voltage. The output is to be applied to a counter so that a pulse - , rather than a sinusoidal - , generator is required. There are, at least, two methods of voltage-to-frequency conversion. Firstly, a fixed duration pulse may be conveniently generated, and then by integrator/comparator technique the interval between the pulses may be varied.[28] Secondly, the frequency of an astable multivibrator may be swept by varying the resistive elements of the timing circuit.[31] Since a relatively large range of frequency variation (15:1) is required, and because, in the latter method, the frequency would be varied directly, it was considered to be the simpler and more convenient method. Hence, a v-f converter based on this method is described.

It has been stated by Biddlecombe[32] that a linear v-f relation, extending over 4 decades may be given by an astable multivibrator formed with discrete semiconductors. Since it was hoped to use integrated circuits, it was considered necessary to understand how the v-f relation is achieved, and the limitations of the method. Consequently, the development of the v-f converter occurred in three phases.

(i) Study of the Biddlecombe circuit and derivation of the linear v-f relation.

(ii) Simplification of the original circuit to obtain an understanding of the factors influencing non-linearity and the upper and lower frequency limits.

(iii) Application of the technique to an IC astable multivibrator.

6.2. The Biddlecombe v-f Converter

The circuit proposed by Biddlecombe is shown in fig. 6.1. It consists of an emitter-coupled astable multivibrator with the base currents controlled by transistors T_3 , T_4. The use of active elements to control the timing resistance of a monostable multivibrator has been investigated in Chapter 4, but there the emphasis was upon utilising the non-linear variation of resistance. Now, transistors T_3 and T_4 are there to preserve constant base current during a quasi-stable state.

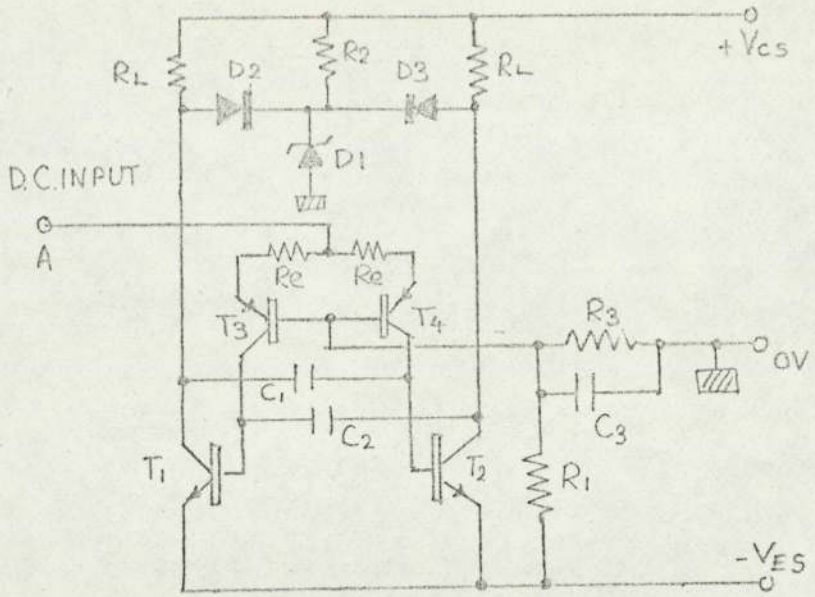
In a simple astable multivibrator at the start of a quasi-stable state, the charged timing capacitor on one side is applied between base and emitter of T_1 to drive that transistor into cut-off; (see fig. 6.2.). Thereafter, the capacitor voltage (Vc) decreases exponentially from -Vcc towards +Vcc, according to the relation.

$$v_c = V_{cc}\left[1 - 2\exp.\left(-t/CR\right)\right] \qquad \text{------(6.1)}$$

The discharge is terminated when $v_c \simeq$ zero, i.e. when $T = CR \log_e 2$. During the time T the discharge current is decreasing exponentially. If, however, constant current is maintained, a charge of Q coulombs is transferred in a time T, so that $Q = IT$, where I is the constant current. The initial voltage is Vcc, so that $Q = CV_{cc}$.

Hence $T = \dfrac{C V_{cc}}{I}$ and since frequency $(f) = \dfrac{1}{2T}$,

then $f = \dfrac{I}{2C V_{cc}}$



COMPONENT	VALUE	COMPONENT	TYPE	SUPPLY	VALUE
R_1, R_2, R_3	470 Ω	D_1	Zener 5·6 V	V_{CS}	10 V
R_e, R_L	1000 Ω	D_1, D_2	OA81	V_{ES}	3 V
C_1, C_2	470 pF	T_2 T_3	BCY 71	DC INPUT	0 – 7 V
C_3	4·7 μF	T_1 T_2	2N3053		

Fig. 6.1 ASTABLE MULTIVIBRATOR WITH CONSTANT BASE CURRENTS FOR LINEAR VOLTAGE – FREQUENCY CONVERSION. (circuit proposed by Biddlecombe)

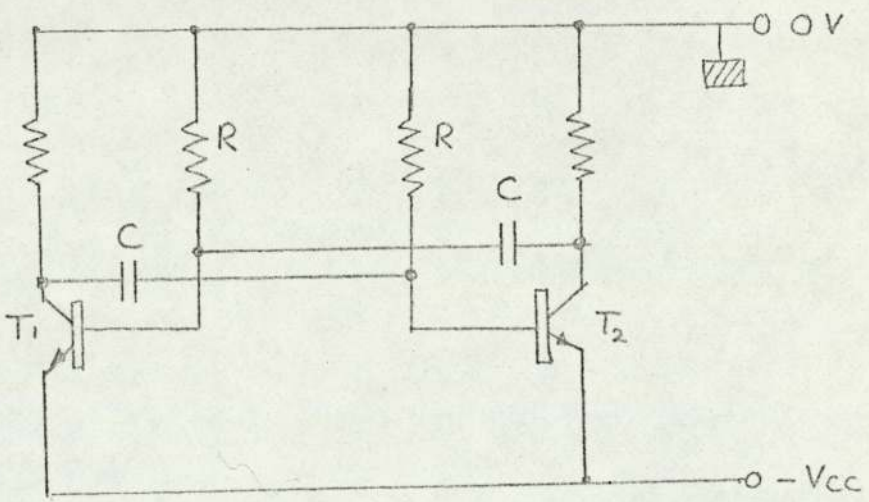


Fig. 6.2 ASTABLE MULTIVIBRATOR — SIMPLE CIRCUIT.

Now, from the original circuit in fig. 6.1. it may be seen that the constant current transistors are, in effect, emitter followers. That is ,

$$I = \frac{V_e}{R_e} \simeq \frac{V_{in}}{R_e}$$

$$\therefore \quad f = \frac{V_{in}}{2C R_e V_{cc}} \quad ----- (6.2)$$

Hence, because the current is maintained constant, the frequency (f) is directly proportional to an input voltage (V) The waveforms of the collector and base voltages (see fig. 6.4) are similar to those of the simple astable multivibrator except that the base voltage is a linear ramp.
The other components of the original circuit are there to improve the performance. For instance, the avalanche diode D1, ordinary diodes D_2, D_3 and resistor R_2, are arranged to clamp the collector voltage at a much lower value than the supply (Vcc), so that the rise-time of the output pulse is reduced. This rise-time is also the charging time for the capacitors C_1, C_2, so that the upper frequency limit is increased. The decoupling components R_1, R_3, C_3 and C_4 are ostensibly for level-changing, and permit a positive-going voltage to be applied at point A.
It will be shown in section 6.4. when the IC astable multivibrator is described, that the base-feed resistor R_3 has a significant effect upon the linearity of the v-f converter.

The circuit described in reference (32) had a maximum frequency of 7KHZ. To test its performance over a 500 KHZ range the circuit of fig.6.1 was constructed with the component values shown. The resulting frequency/input voltage response is shown in fig. 6.3. It may be seen that frequency is proportional to voltage over the range 40-480 KHZ. There is, however, a departure from linearity at high frequencies with df/dv increasing with increase of frequency.

To gain an understanding of the factors which affect non-linearity and which determine the upper and lower limits of frequency, the simplified circuit, described in the next section, was constructed.

6.3. Factors Affecting Non-Linearity and Frequency Limits.

6.3.1. A Simplified Circuit

A simplified version of the original circuit is shown in fig. 6.5. There are two main differences. Firstly, the collector clamping components are omitted, so that C_1 and C_2 charge to Vcc. Secondly, T_3 and T_4 are shown as emitter-followers, with the input voltage applied between the common bases and the +Vcc terminal. When the output frequency/input voltage response was checked, the range of operation was found to be limited to 70-108 KHZ. In addition, there was pronounced non-linearity at high frequencies with the value of df/d_V increasing with f (or V). It appeared that there were three possible reasons for the non-linearity at high frequencies which are as follows.

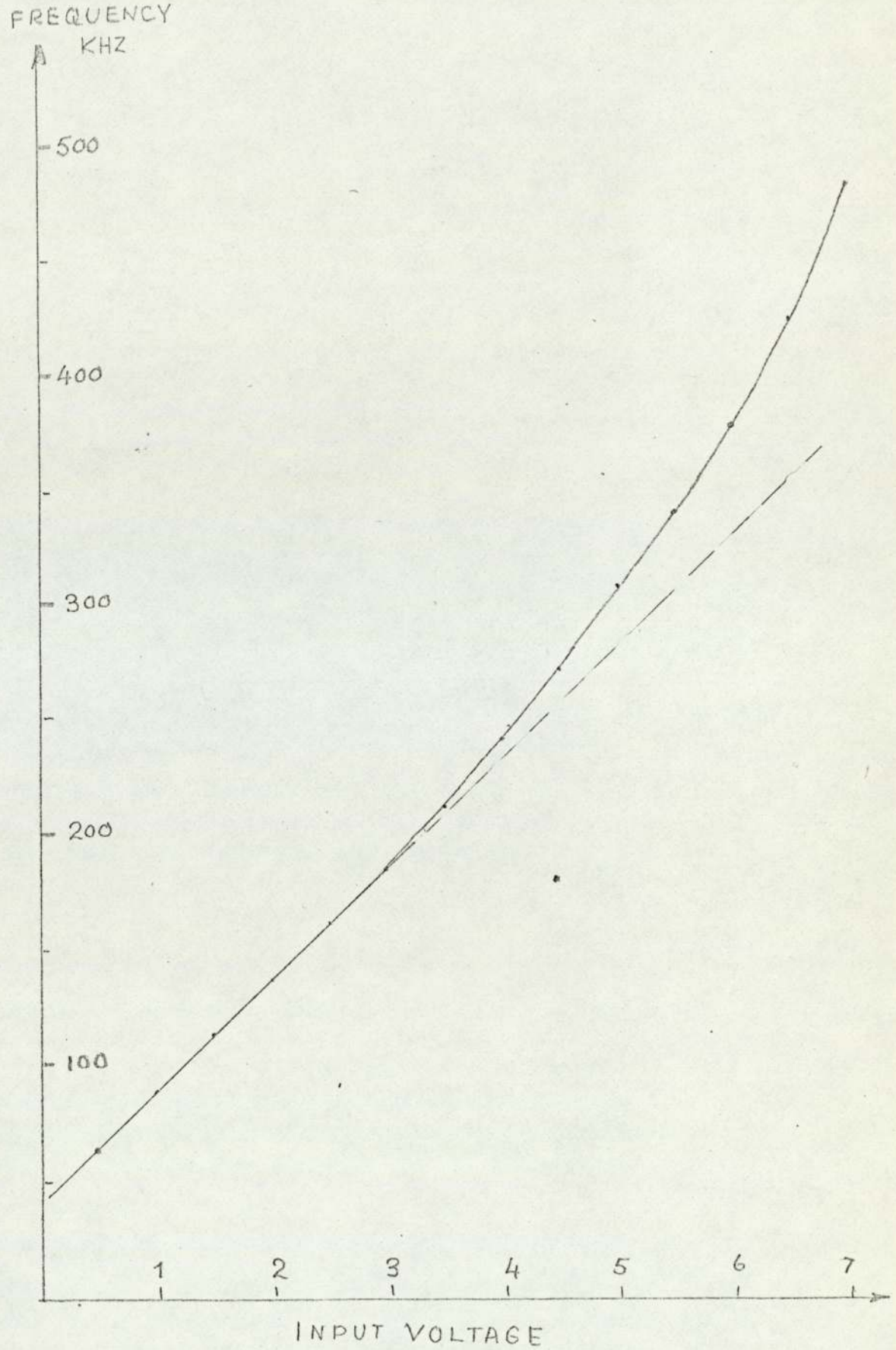


FIG. 6.3 VOLTAGE-FREQUENCY RESPONSE FOR THE BIDDLECOMBE CIRCUIT

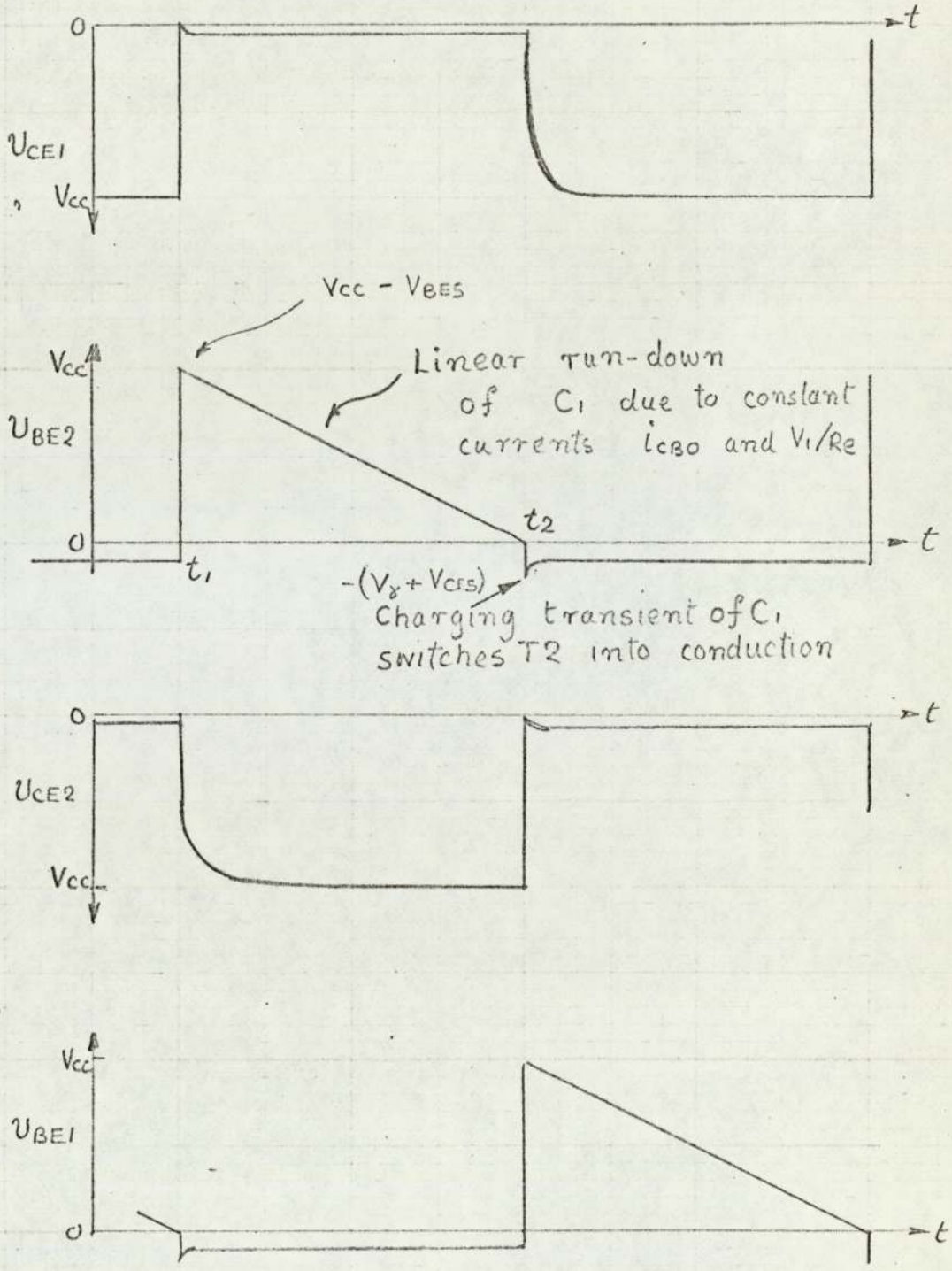


Fig. 6.4 WAVE-FORMS IN V-f CONVERTER

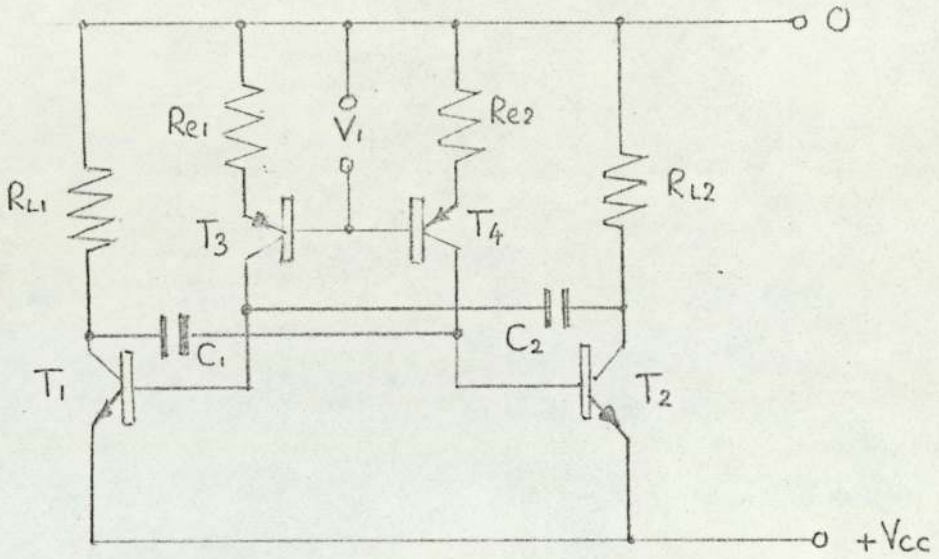


FIGURE 6.5 V-f CONVERTER — SIMPLIFIED CIRCUIT

COMPONENT	VALUE	COMPONENT	TYPE	SUPPLY	VALUE.
R_{e1}, R_{e2}	1000 Ω	T_1, T_2	2N3053	V_{cc}	5V
C_1, C_2	470pF	T_3, T_4	BCY 71	V_1	0.8-3V
R_{L1}, R_{L2}	470Ω				

(i) The output resistance (h_{oe}^{-1}) of a "constant current" transistor (T_3 or T_4), decreases with increasing base current and input voltage.

(ii) The shunt capacitance across a "constant current" transistor (C_{ce}), causes the base current to increase at high frequencies.

(iii) Increase of input voltage brings increase of temperature, which modifies the junction voltages and capacitor discharge currents upon which the frequency depends.

These three reasons (i - iii) above are now examined to test their validity.

6.3.2. Effect of Output Resistance upon Linearity

It is well known that the output resistance of a bipolar transistor decreases with increasing base current.[31,34] That is, as the input sweep voltage increases, the output resistance decreases, and hence the collector current tends to increase. The tendency to increase, however, is offset because emitter-follower operation makes the transconductance ($\partial i_e / \partial V_1$) independent of transistor parameters (see Appendix E). It is therefore considered that the limitation at high frequencies due to output resistance variation is negligible.

6.3.3. Effect of Shunt Capacitance upon Linearity

The shunt capacitance of a "constant current" transistor would cause increased currents at the higher frequencies. The capacitances involved however, (~ 20 pF) give much higher impedances than the resistances Re and h_{oe}^{-1}.

Hence, too, the limitation due to shunt capacitance is discounted.

6.3.4. Effect of Increase of Temperature upon Linearity

Biddlecombe reported[32] that increase of temperature during operation only produced a non-linearity of about 1%. It has been stated elsewhere[31], however, that the duration of quasi-stable states in transistor multivibrators are not particularly stable with temperature. Whether the non-linearity at high frequencies is a function of temperature, depends upon the extent to which the input voltage V_1 can influence temperature. Before discussing the significance of the effect, the temperature dependence of the switching transistors of the V-f converter is considered.

P.n. junctions are subject to two temperature effects, in that the junction voltage under forward bias and the reverse leakage current both vary with temperature. In a bipolar transistor the forward base-emitter voltage decreases linearly by approximately 2 mv. K^{-1}. This is substantially true for both the saturation value (V_{BES}) and the "cut-in" value (V_γ) . On the other hand, the saturation value of collector-emitter voltage (V_{CES}) increases slightly with temperature, the rate of increase varying widely with current, in the range 0.2 - 1 mV K^{-1}. This variability in (V_{CES}), and its weak temperature dependence, arise because V_{CES} is the difference between two junction voltages, both of which tend to decrease with temperature increase.

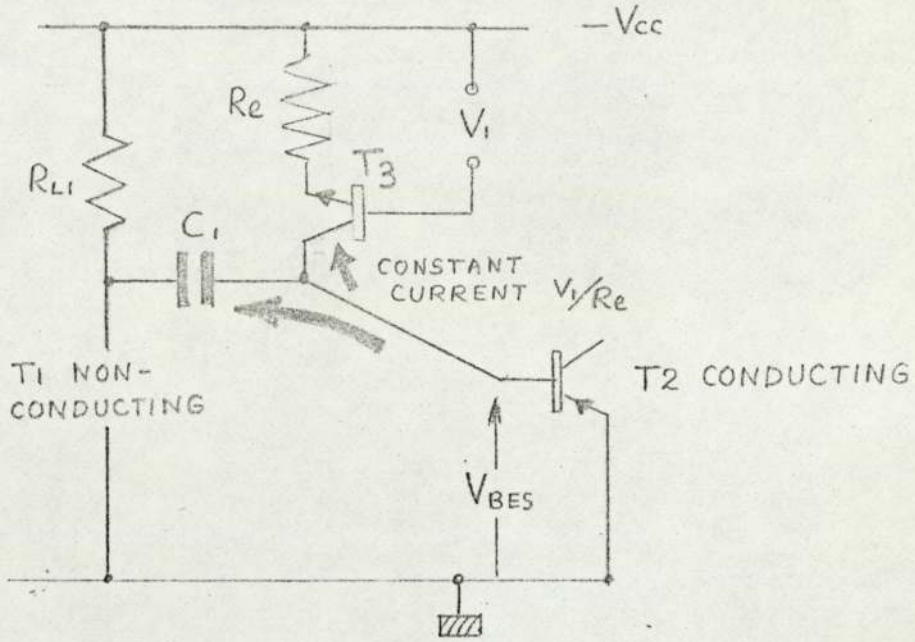
The reverse bias leakage current (I_{CBO}) increases logarithmically with increase of temperature. That is, the current doubles for a temperature increase of 10K. The possible temperature dependence of the switching transistors may now be seen with reference to figs. 6.4 and 6.6. Consider instant at which T_1 conducts. C_1 is charged to $v_c = V_{cc} - V_{BES}$, and is about to be discharged by a constant current $h_{FB} V_1/R_e \simeq V_1/R_e$ The base-emitter junction of T_2 is reverse-biassed by the capacitor voltage, and hence a current, I_{CBO} flows into the n-type base. Hence, I_{CBO} is helping to discharge the capacitor C_1 and so an increase in I_{CBO} would reduce the duration of the quasi-stable state. To analyse this dependence, Kirchoffs Current Law is applied:-

$$i_c = C\, dv_c/dt = I_{CBO} + V_1/R_e$$

Now, I_{CBO} is theoretically independent of reverse bias voltage. In practice, however, it increases with reverse voltage because it has a substantial surface leakage component, which is not temperature dependent. Therefore, assuming I_{CBO} is constant, it can be shown (see Appendix F) that the base-emitter applied voltage decreases linearly to the cut-in value ($-V_\gamma$) in a time T given by:

$$T = \frac{(V_{cc} - V_{BES} - V_{CES} + V_\gamma)\, C\, R_e}{I_{CBO}\, R_e + V_1} \qquad ---(6.3)$$

TIME $t < t_1$



TIME $t_1 < t < t_2$.

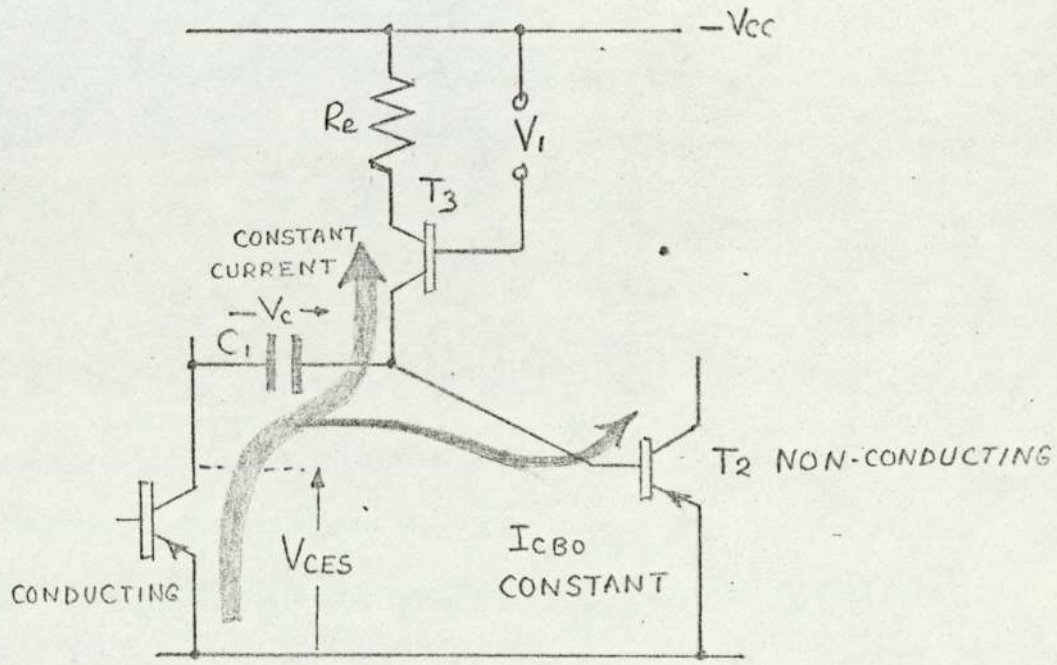


Fig. 6.6 EFFECT OF JUNCTION VOLTAGES AND REVERSE SATURATION CURRENT

The corresponding frequency $f = \frac{1}{2T}$ is then given by:

$$f = \frac{1}{2C_1R_e}\left[\frac{V_1 + I_{CBO}R_e}{V_{CC} + V_\gamma - V_{BES} - V_{CES}}\right] \quad \text{------(6.4)}$$

Hence as temperature increases, and I_{CBO} increases, the frequency f increases. Millman and Taub have given[31] an example where, if I_{CBO} is 3 nA at 25K, it will be 100 μA at 175K, giving a 12% decrease in duration T. Considering equation (6.4) it may be seen that the effect of the temperature dependence of junction voltages is very small, for ΔV_{BES} and ΔV_γ tend to cancel and ΔV_{CES} is small. In an example given,[31] ΔV_{CES} is +1 mV.K^{-1} giving a 6% decrease in duration T for a temperature increase from 25K to 175K. It is considered, however, that this case is not typical, and that the temperature dependence of I_{CBO}, only, is significant.

The question which arises now is whether an increase in input voltage V_1 can cause the junction temperatures of the switching transistors to increase. These operate between cut off and saturation with a mean collector current which is independent of V_1. The collector dissipation (P) will be $\frac{V_{CC}V_{CES}}{2R_L}$ watts.

With Vcc = 5V, V_{CES} = 200 mV, and R_L = 250 Ω, P = 2mW. This small power is hardly likely to cause a large increase in temperature. The input voltage V_1, however, ranges from 800 mV to 4 V giving a maximum current of 4mA in the base of switching transistor. With a saturation base-emitter voltage of 750mV, an additional

3mW are dissipated at maximum input V_1. The total dissipation 5mW is still small, but it is suggested that the increase with V_1 is significant. Moreover, the increase in temperature for appreciable non-linearity need not be as great as indicated in the example above. The values of I_{CBO} which obtain in practice maybe much greater than 3nA at 25K. Millman and Taub,[31] in discussing the spread of reverse leakage values refer to the data sheet for a silicon transistor whose minimum and maximum I_{CBO} values are respectively 200pA and 300nA at room temperature. Hence, it is concluded that an increase in V_1 can produce increase in temperature, and that this is the main factor determining the non-linearity at high frequencies. It is suggested that this effect was not apparent to Biddlecombe for two reasons:-

(i) The small base currents of his circuit limited operation to low frequencies (f_{max} = 7 KHZ), and very small base powers of 300 μW.

(ii) A base feed resistor could, as shown later, correct to some extent any non-linearity.

It must be emphasised here that any non-linearity due to temperature dependence will only be apparent on slow variations of input voltage. The input voltage to the v-f converter in the experimental model will have a sweep period of $\sim$ 1 ms. This is considerably shorter than the thermal time constant of even the smallest transistor. Hence it is considered that non-linearity due to temperature increase with input voltage will be negligible.

There may, however, be long term variations in frequency due to variations in ambient temperatures, which would cause counting errors. These should be very small if the switching transistors have small reverse leakage currents. Since the use of T.T.L. integrated circuits is envisaged, it is considered that this condition will obtain.

It has been stated that the upper and lower frequency limits are 108 KHZ and 70 KHZ respectively. The factors which determine these limits are now considered.

6.3.5. The Upper Frequency Limit.

The upper frequency limit appears to be due to the rise-time of the collector pulse becoming a significant proportion of the pulse duration. Under such conditions the timing capacitors do not receive their full charge, and hence the initial height of the base ramp is reduced. In the Biddlecombe circuit the rise-time is reduced, because the capacitor, in charging towards the supply voltage, is clamped by diode D1. An alternative method of reducing the collector pulse-rise time is to separate the charging and collector load resistances (28,31) by diodes. This method is particularly suited to the fabrication techniques of I.C's. Since the use of an I.C. astable multivibrator was envisaged, it was decided to check that the alternative method was effective. Hence the simplified circuit was modified as shown in fig. 6.7. The diodes D1 and D2 isolate the charging resistors R_{C1} and R_{C2} from the collectors of T1 and T2 respectively. Both bipolar and field-effect transistors

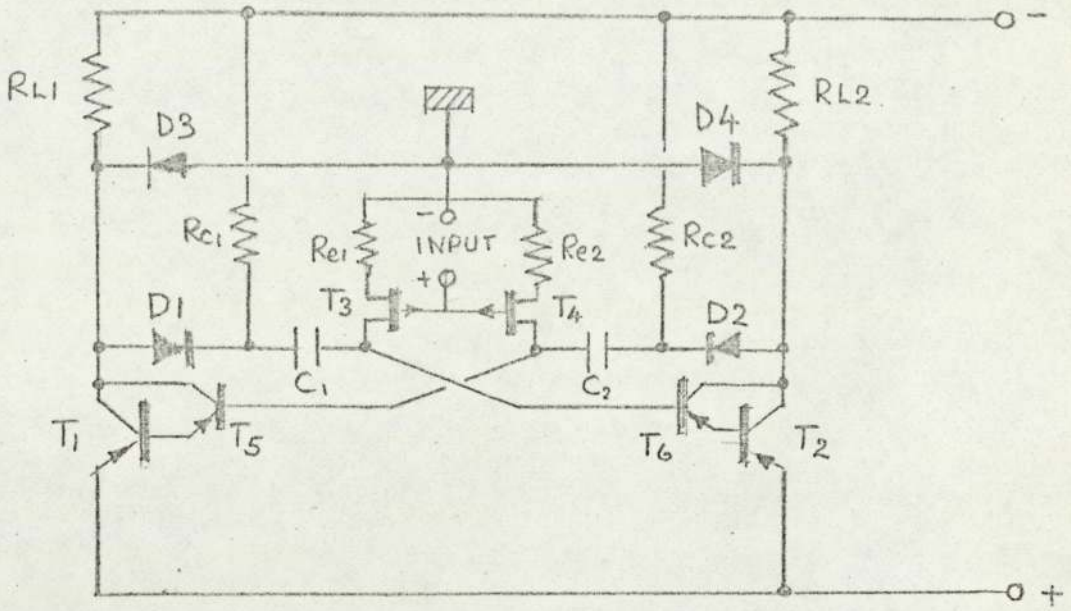


Fig 6.7 ASTABLE MULTIVIBRATOR VOLTAGE-FREQUENCY CONVERTER — MODIFIED CIRCUIT.

COMPONENT	VALUE	COMPONENT	TYPE	SUPPLY	VALUE
R_{L1}, R_{L2}	220 Ω	T_1, T_2	2N2904	V_{CC}	10V
R_{c1}, R_{c2}	470 Ω	T_3, T_4	(1) BFW10 (2) BC108	INPUT	0·8-8V
R_{e1}, R_{e2}	1000 Ω	T_5, T_6	2N4285		
C_1, C_2	470 PF	D_1, D_2, D_3, D_4	OA86		

were tried as constant current elements and the upper frequency limits exceeded 500 and 600 KHZ respectively.

6.3.6. The Lower Frequency Limit

The limitation at low frequencies may be explained as follows. At small input voltages, the base currents for T1 and T2 may not be large enough to maintain saturation. The effect of this may be explained with the aid of figs. 6.6 and 6.8. A transition to an OFF state for T2 (say) is initiated by a charging current transient through C_1, which drives T2 into saturation. At low input voltages, however, when the transient has decayed, the steady current through T3 would not be large enough to maintain saturation in T2. Hence, the pulse-form would show sag as in fig. 6.8. This effect was confirmed when the pulse wave-forms at low input voltages were monitored. When the sag reached nearly 80% or thereabouts, the pulse-form collapsed.

To reduce the low frequency limit, therefore, it must be arranged that the transistors go into saturation on the smallest currents. That is, the switching transistors must have large current gain factors. To test that high current gain is the determining factor, the circuit of fig. 6.7 was operated with (a) single and (b) double-transistor switching. It was found that in the latter case the low frequency limit was 3KHZ.

Hence, it is considered that the transistor element of a T.T.L. integrated circuit would provide the current gain required for a lower limit of 30-40 KHZ.

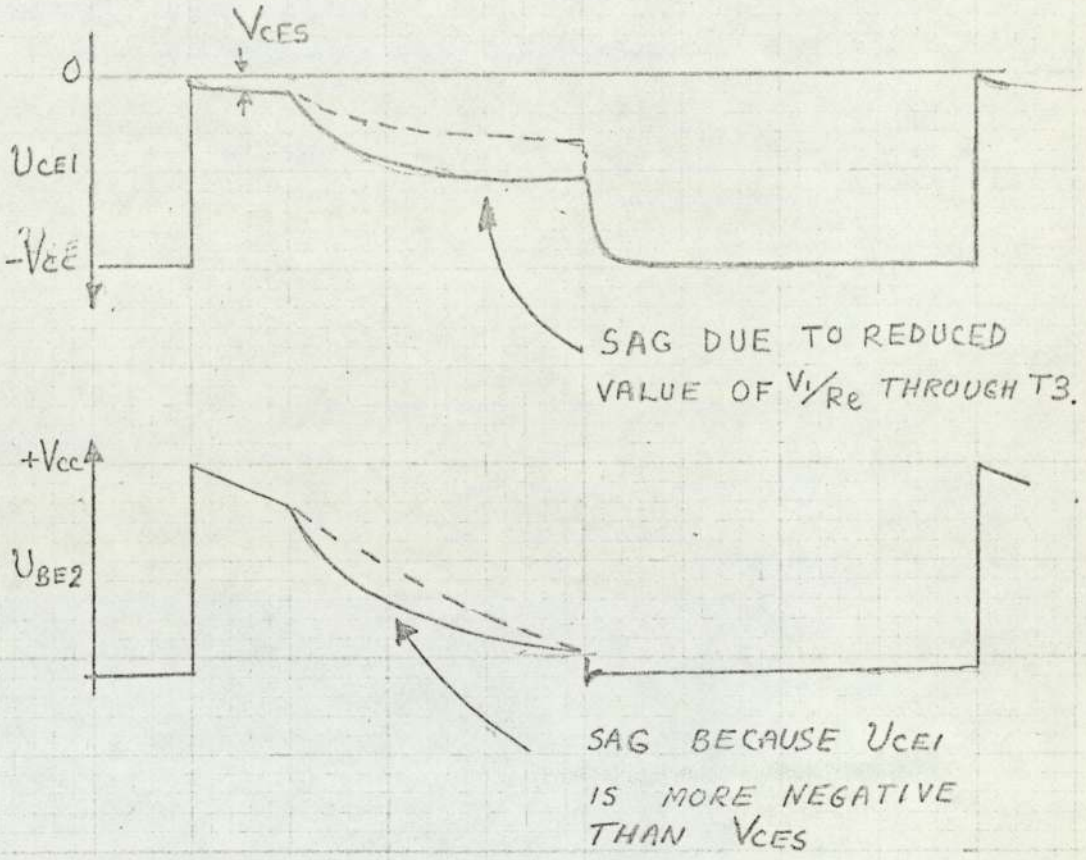


FIGURE 6.8 WAVE-FORMS AT LOW FREQUENCY LIMIT.

Hence those factors affecting non-linearity, upper and lower frequency limits of the V-f converter have been considered with the aid of simplified circuits using discrete components. It is thought that in each of the three cases an integrated circuit construction will give an improved performance. An integrated circuit V-f converter is considered in the next section.

6.4. Dual Monostable Astable V-f Converter

Apparently astable multivibrators are not manufactured in one IC package.[28] One may, however, be made up from (a) connections of NAND gates as in fig. 6.9, or (b) from two monostable circuits[28] as in fig. 6.10.

The circuit configuration given under (a) will operate at frequencies up to 1MHZ, with a frequency (f) given by:-[28]

$$f = \frac{1}{2C(R+R_1)}$$

The frequency range obtainted by varying $(R + R_1)$, however, was not large, and hence circuit (b) was adopted. The latter is termed the dual mono-astable, and since the duration (T) of a quasi-stable state of one monostable is $T = CR \log_e 2$, then the frequency (f) is given by:-

$$f = \frac{1}{2CR \log_e 2} \qquad \text{-----(6.5)}$$

Since most T.T.L. integrated circuits appear to be designed for positive logic, the constant current elements had to be p.n.p. bipolar transistors, or p-channel f.e.t.s. The supply voltage to digital T.T.L. ICs is normally only 5V, however, and so p.n.p. bipolar transistors type 2N2904 were

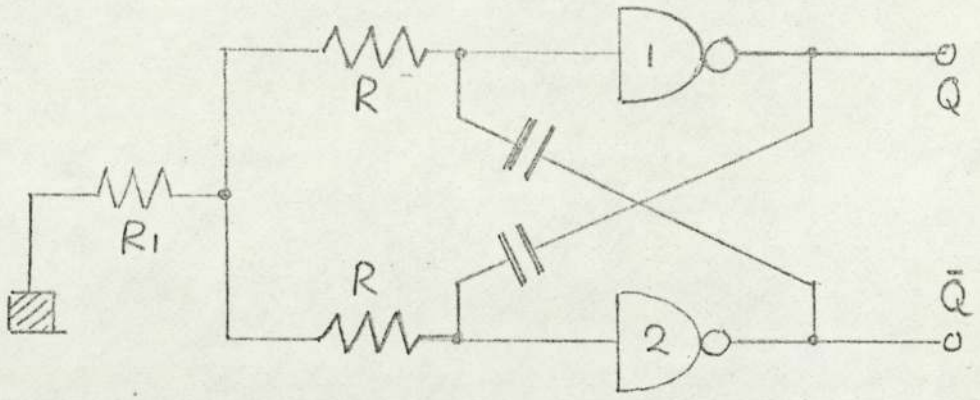


FIGURE 6.9 ASTABLE MULTIVIBRATOR FROM NAND GATES

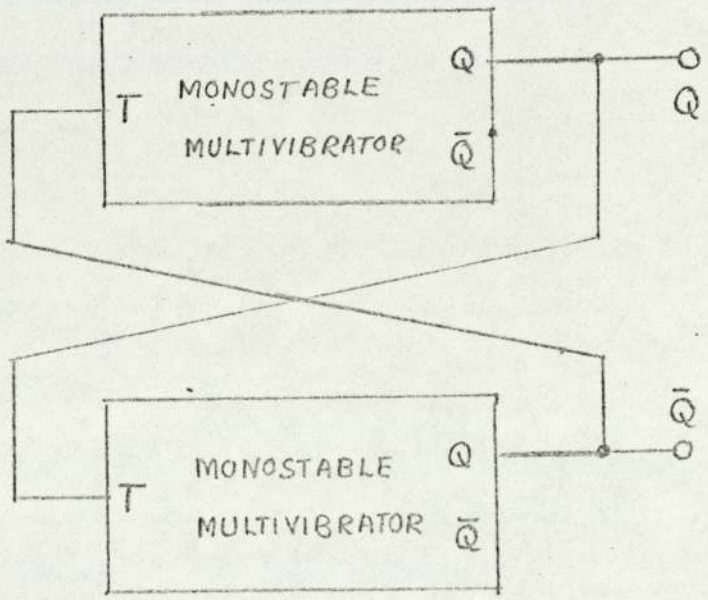


FIGURE 6.10 DUAL MONOSTABLE-ASTABLE. PRINCIPLE OF THE CONNECTION.

selected. The complete circuit is shown in fig. 6.11. Monostables type SN74121A (Texas Inst.) were selected (an identical specification is given for type FJK101 (Mullard)). [35,37] The emitter loads Rel and Re2 and base feed resistor Rb were variable.

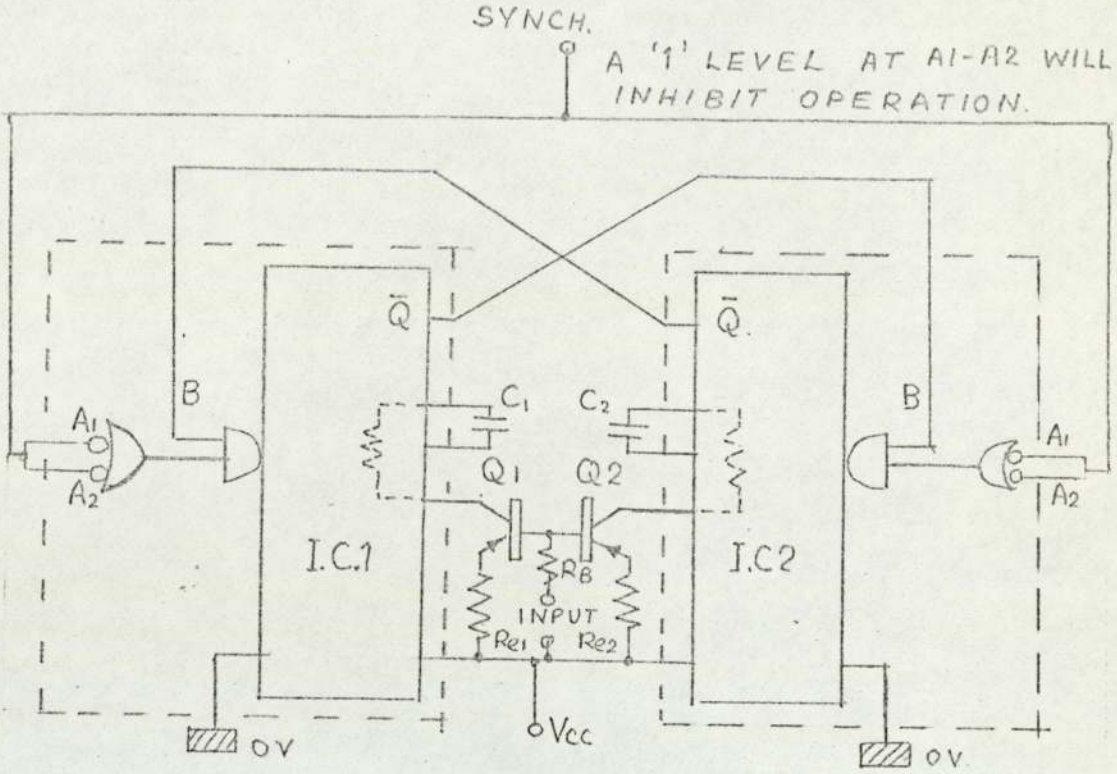
The frequency/input voltage response obtained, is shown in fig. 6.12. The frequency range extends from 25 to 500 KHZ with a maximum non-linearity of 5%, which showed the same trends as before. A variation of Re showed that a value of 1K Ω gave the required frequency range for the value of timing capacitance used (470 pF).

There followed next a series of tests to determine the most convenient way of connecting the input voltage V_1. Firstly, the input voltage was applied so that it caused a decrease in operating frequency. The idea here was to test whether non-linearity could be associated with low frequencies rather than high frequencies. Two connections were tried (a) and (b) shown in fig. 6.13.

In (a) the input voltage was applied between the common terminal (i.e.ground) and the base input resistor R_b, so that it subtracted from the forward bias at the base-emitter junctions of T_3, T_4.

In (b) the input was applied as in (a) but with reversed polarity so that it increased the forward bias at the emitter-base junction.

The frequency/input voltage curves are shown in fig. 6.14. The results for (a) show the frequency decreasing as the input voltage is increased, as might be expected. It may be noted, however, that the non-linearity still tends to be larger at



COMPONENT	VALUE	COMPONENT	TYPE	SUPPLY	VALUE
R_B	750Ω	Q_1 Q_2	BCY	V_{cc}	5V
R_{e1}, R_{e2}	1000Ω	IC.1, IC.2.	FJK.101	INPUT	0.7-3.0V
C_1, C_2	470pF				

Fig. 6.11 THE DUAL MONOSTABLE-ASTABLE MULTIVIBRATOR CONNECTED AS A LINEAR V-f CONVERTER.

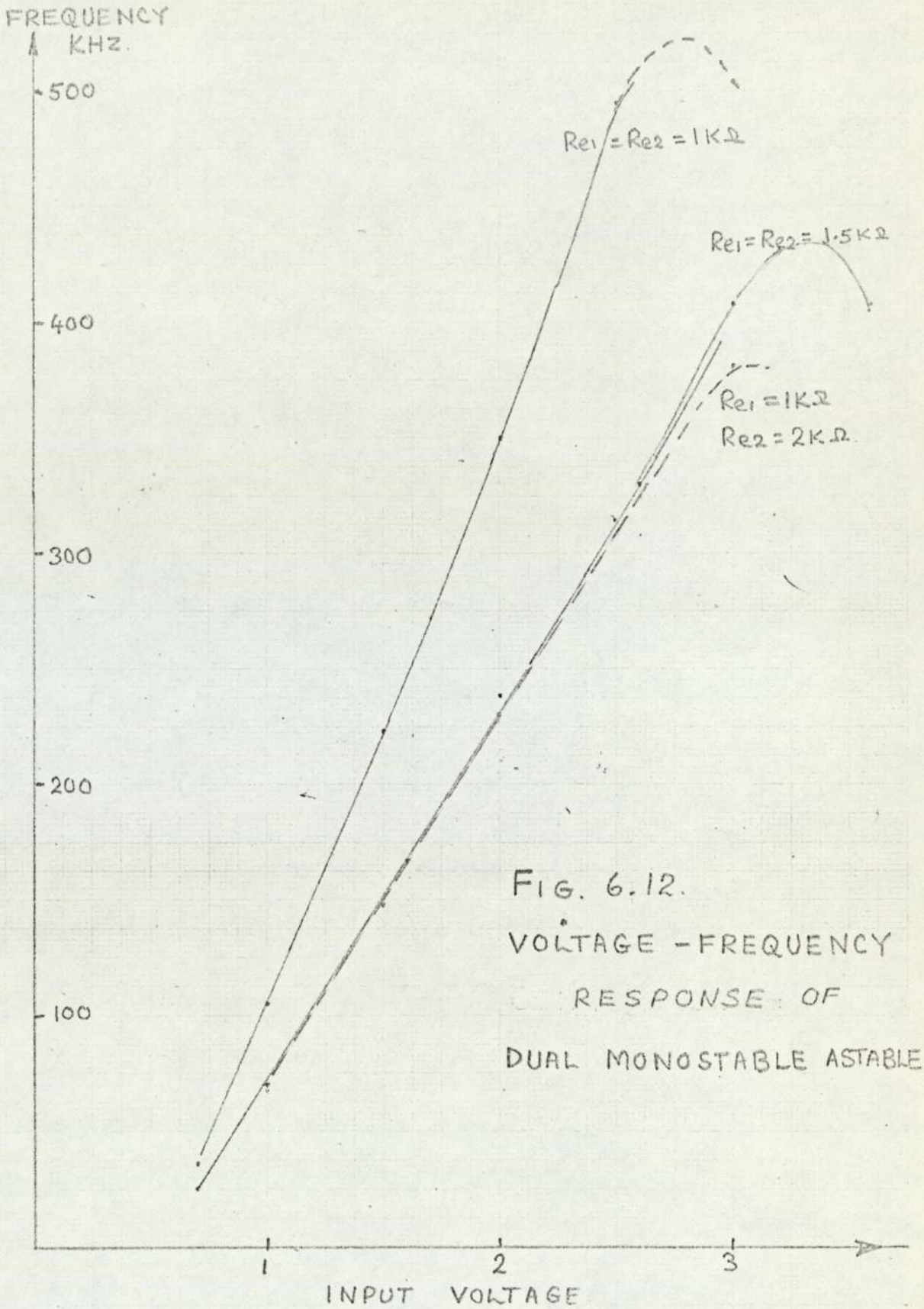


FIG. 6.12.
VOLTAGE - FREQUENCY
RESPONSE OF
DUAL MONOSTABLE ASTABLE.

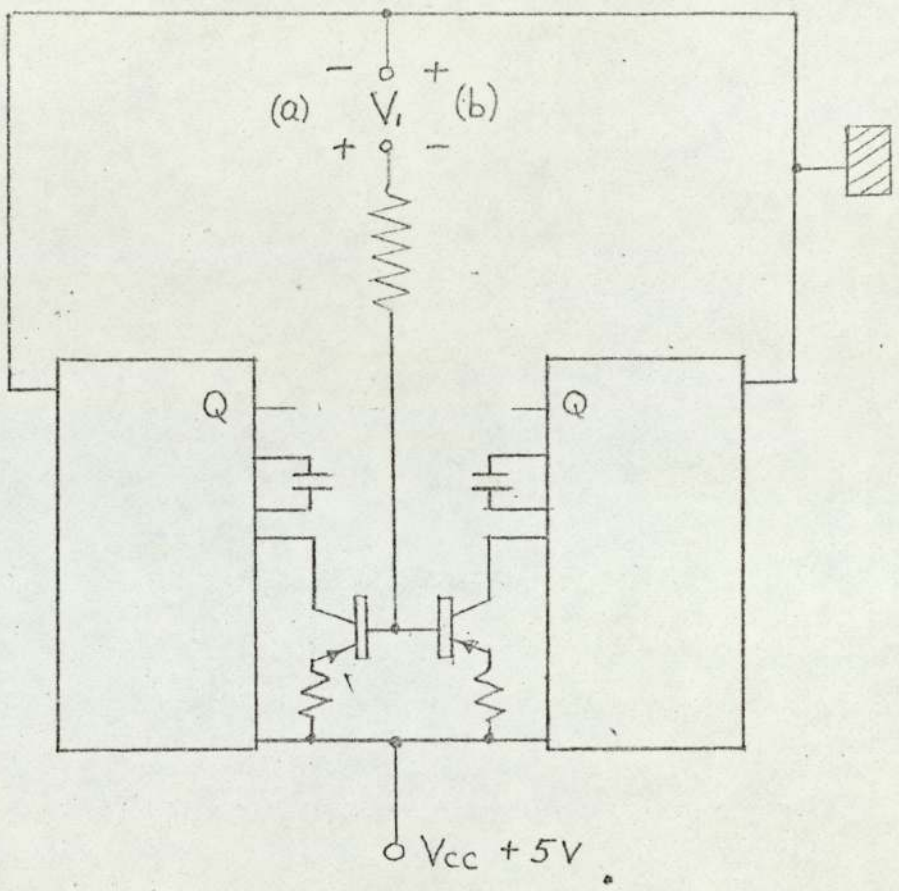
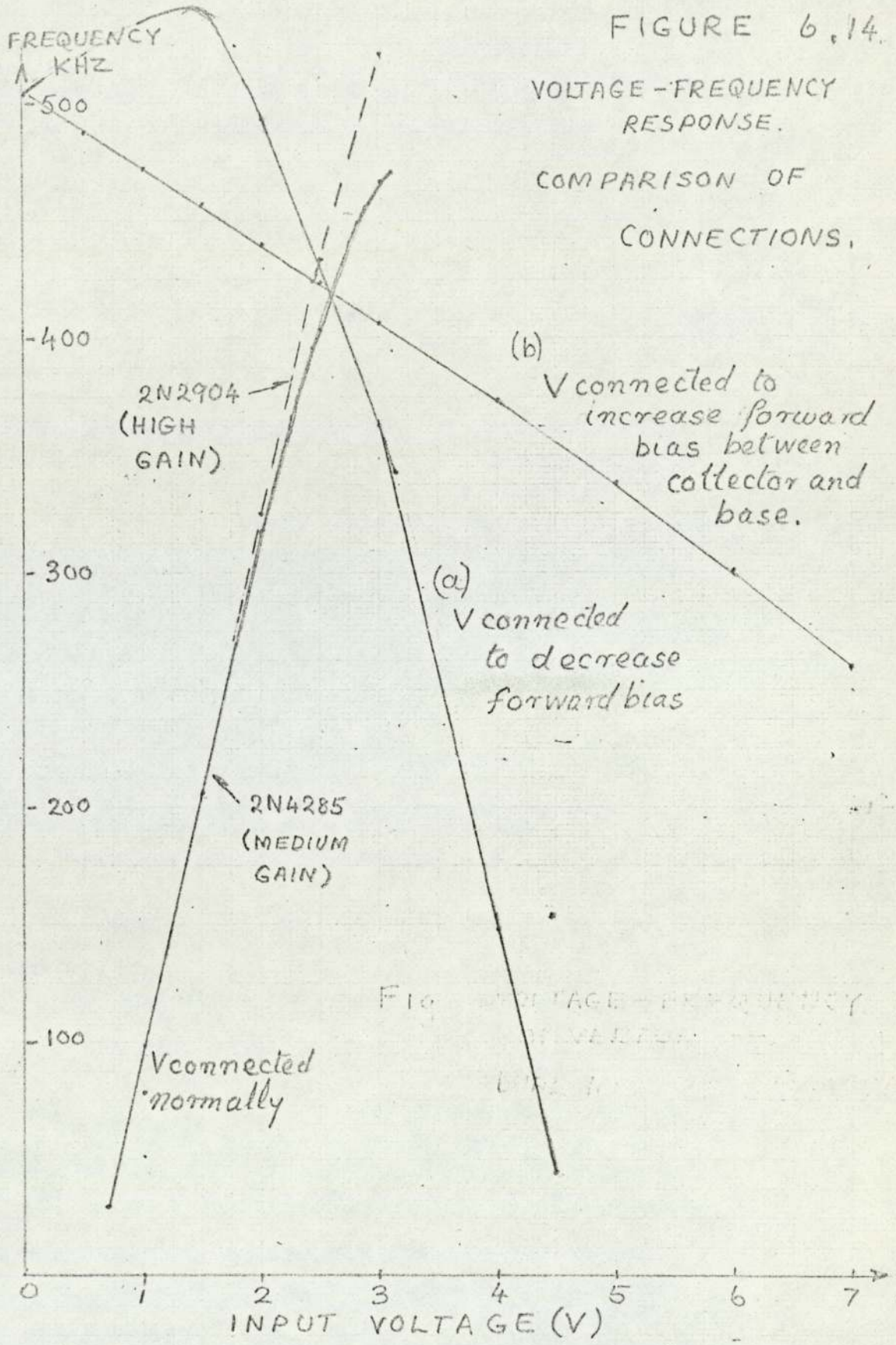


FIGURE 6.13: ALTERNATIVE METHODS OF APPLYING THE INPUT VOLTAGE (V_i)

FIGURE 6.14.

VOLTAGE-FREQUENCY RESPONSE.

COMPARISON OF CONNECTIONS.



high frequencies. In effect, the curve shows the same variation as those for the normal input connection, but with the input voltage reversed. The results for (b) show the frequency decreasing more or less linearly with increase in put voltage. The range of frequencies (500-200 KHZ) however, is too small to show whether non-linearity occurs at low frequencies. It did appear however, that non-linearity is always associated with high forward bias at the base-emitter junctions of the constant current transistors, and therefore with high frequency operation.

During this test it was noted how the presence of R_b could affect the non-linearity. In fact if the curves in fig. 6.12 and the "normal connection" curves in fig. 6.14 are compared it will be seen that in the latter the value of df/dv decreases with input V, instead of increasing: this is the effect of R_b.

To show the effect of R_b upon the non-linearity, the frequency/input voltage responses were determined when R_b had various values between zero and 5KΩ, and these results are shown in fig. 6.15. The non-linearity could be varied from +5% (when R_b = zero) to -20% (when R_b = 5KΩ), with a minimum when R_b = 750Ω. This was considered to be a surprising result and it was thought at first that the same result would be given when each base was fed through its own resistor. Hence, resistors R_{b1} and R_{b2} were incorporated, and it was then found that the non-linearity could not be minimised even when $R_{b1} = R_{b2} = 1500\Omega$. Hence, only when the two bases were fed from a common resistance of 750Ω, was the non-linearity reduced to zero.

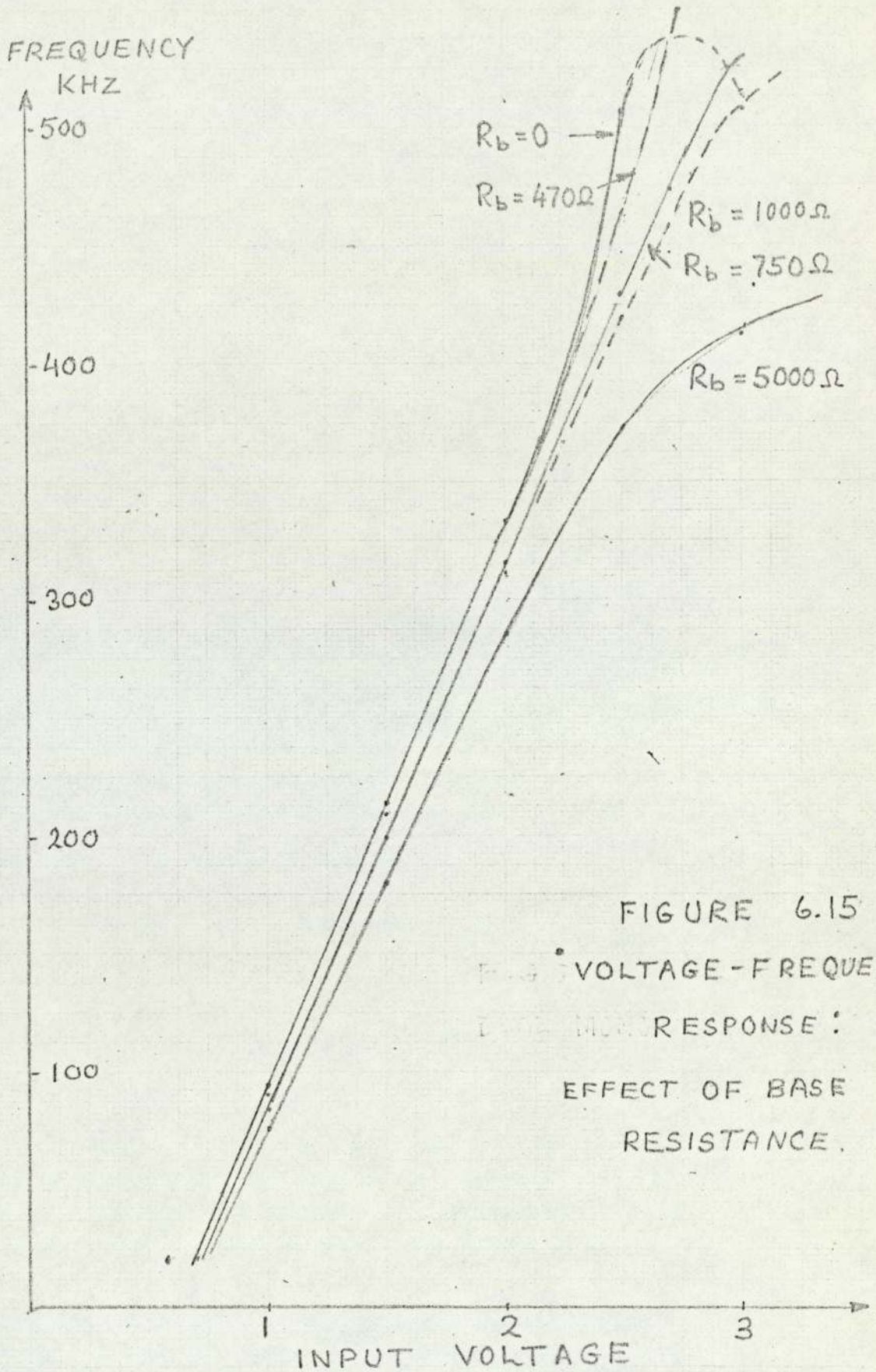


FIGURE 6.15

VOLTAGE-FREQUENCY RESPONSE: EFFECT OF BASE RESISTANCE.

The only inference which may be made is that interaction was occurring between the two constant-current transistors. That is, a large base current on one side reduced the input to both sides. To explain this, the operation of the circuit is examined in detail as follows.

Consider the simplified circuit shown in fig.6.16 and the pulse waveforms in fig. 6.4 at the instant t_1 at which transistor T_2 goes into cut-off, and transistor T_1 goes into saturation. A current I_3 flows in constant current transistor T_3, tending to discharge C_1 and to recharge it with opposite polarity. That is, the operation of T_3 is at point P on the output characteristic, shown in fig.6.17. The current I_3 should remain nearly constant, moving from P-Q as the linear run-down of C_1 occurs. Also, at time t_1, as T_2 goes into cut-off, a pulse of charging current into capacitor C_2 raises the potential of T_4 collector to +Vcc volts, i.e. the collector-base junction of T_4 is FORWARD-BIASSED by the input voltage. Hence a current flows into the collector and out of the base and is limited only by R_L, the forward biassed junction, and R_b. Therefore at instant t_1, T_4 does not operate as an emitter-follower and so two relatively large current components flow out of T_4 base. This process occurs for a relatively short time (i.e. the charging time constant) and hence has no significant effect at small inputs and low frequencies. At larger values of input voltage, the current (which is discharging a capacitor) is larger and the times of discharge are smaller, and of the same order as the charging time constant. Hence, the increased base current on the charging side has a more significant

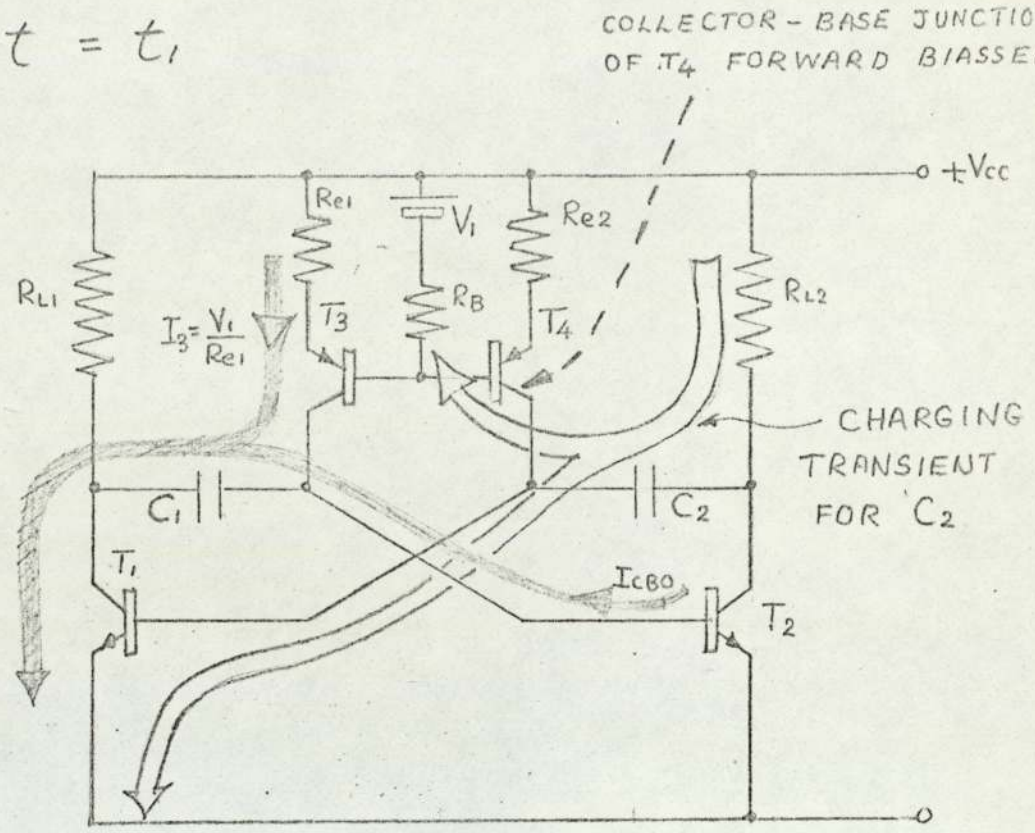


FIGURE 6.16 V-f CONVERTER — CURRENTS AT THE ONSET OF A TRANSITION.

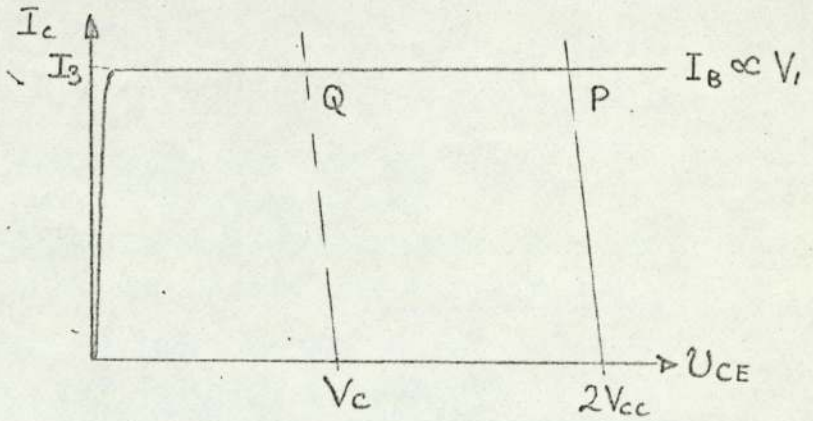


FIGURE 6.17 OUTPUT CHARACTERISTIC OF A "CONSTANT CURRENT" TRANSISTOR

effect at larger inputs and higher frequencies. The effect will be that the average base input current throughout the duration of a pulse will be larger than that which would be required by two emitter followers fed in parallel. Therefore, the input voltage to that emitter-follower which is discharging a capacitor tends to be smaller, by the amount which is developed across R_b.

The above description of the operation explains how the non-linearity may be controlled by the value of R_b.

6.5. Conclusion for a Linear V-f Converter

A linear V-f converter based upon an astable multivibrator has been designed. An integrated circuit construction has been developed, which uses two cross-connected T.T.L. monostable packages. The timing components are two capacitors whose discharge currents are maintained proportional to an input voltage by two discrete transistors.

The performance is such that an input voltage range from 0.8V to 2.8V results in a linear variation of frequency from 25KHZ to 480KHZ. The linearity may be controlled by a single resistance in the common input to the bases of the discrete transistors.

The dual monostable is to be applied to the production of variable frequency clock pulses with a sweep input voltage. To prevent limitation of the clock p.r.f. by the action of the V-f converter a maximum operating frequency of 450KHZ is selected. The corresponding minimum frequency will therefore be 450/15 = 30KHZ.

The positions of the V-f converter are shown in figs. 3.9 and 3.12, while the method of connection is shown in fig.6.11.

CHAPTER 7

CLOCK PULSE SWEEP GENERATION

7.0. Introduction

7.1. Triangular Sweep Method

7.1.1. Integrator

7.1.2. A Single-Ended Compandor

7.2. The Differentiated Sweep Method

7.2.1. A Ramp Generator

7.2.2. Balanced F.E.T. Compandors

7.2.3. An O.A. Differentiator

7.3. The Junction F.E.T. as a Compandor

7.3.1. Similarity to the Required Characteristic

7.3.2. Companding Errors in a Method 5 Encoder

7.4 Conclusion to Chapter 7

7.0. Introduction

The input to the linear V-f converter described in Chapter 6 is provided by a sweep generator. The sweep generation may follow one of the two forms indicated in fig. 3.9. That is:-

(A) a triangular waveform may be applied to a compandor whose output is applied to the V-f converter:

or (B) a sawtooth waveform is applied to a compandor whose output is differentiated and then applied to the V-f converter.

The input waveform generation (i.e. sawtooth or triangular) is considered as a stage in each chain, because it has to be synchronised with the channel pulse. It may be seen, however, that the first form (A) is simpler in two respects. Firstly, it contains only two stages, and secondly, as will be shown, a single-ended compandor rather than a balanced compandor is required.

In order to determine whether the required companding characteristics are realisable, it is necessary to consider the logarithmic companding function, given in equation (2.1.), and shown graphically in fig. 2.11, in more detail. The compression parameter μ is a figure which gives the amount of compression. If the transfer characteristic of fig. 2.11 were linear with a gradient equal to the initial slope, the range of output voltage would be much greater. In other words, the compression is the ratio of the linear: compressed ranges. From equation (2.1) the gradient is:-

$$\frac{dV_2}{dV_1} = \frac{\mu}{\log(1+\mu)} \cdot \frac{1}{1+\mu V_1} \qquad \text{---------} (7.1)$$

(It may be recalled that equation (7.1) is also the maximum relative clock pulse frequency (f/f_o) for the Method 5 encoder.)

Hence from equation (7.1) the initial gradient is:-

$$\left.\frac{dV_2}{dV_1}\right|_{V_1=0} = \frac{\mu}{\log(1+\mu)} \qquad (7.2)$$

The ratio:-

$$\frac{\text{linear range}}{\text{compressed range}} = \frac{\mu}{\log(1+\mu)} \qquad \text{---------} (7.3)$$

This is the amount of compression for a given value of μ.

Now the final gradient (i.e. when $v_1 = 1$) is:-

$$\left.\frac{dV_2}{dV_1}\right|_{V_1=1} = \mu/(1+\mu)\log(1+\mu) \qquad \text{---------} (7.4)$$

That is, to realise equation (2.1) a compandor should have a non-linear transfer characteristic whose initial and final gradients are given by equations (7.2) and (7.4) where μ is in the range (5 - 500).

The two methods of generating a clock pulse sweep require different compandor characteristics. In the differentiated sweep method (B) a sawtooth waveform is to be compressed, and then differentiated, so that a compandor having the logarithmic transfer function, (like equation 2.1), is required. Since, within the duration of the sawtooth, negative and positive length-modulations occur, a balanced compressor is required. In the triangular sweep method (A), on the other hand, the compandor must provide the

waveform which is the time-differential of the logarithmic companding function. By differentiating equation (7.1), it may be seen that the initial slope of the required characteristic is given by:-

$$\left.\frac{d^2 V_2}{d V_1^2}\right|_{V_1=0} = \frac{-\mu^2}{\log(1+\mu)} \qquad (7.5)$$

while the final slope is given by:-

$$\left.\frac{d^2 V_2}{d V_1^2}\right|_{V_1=1} = \frac{-\mu^2}{(1+\mu)^2 \log(1+\mu)} \qquad (7.6)$$

Hence a type A compandor should have a non-linear transfer characteristic of initial and final gradients given by equations (7.5) and (7.6).

It may be noted that these gradients are of opposite sign to those of compandor type B, and that the initial gradient is much greater. This may appear to be a surprising result for it implies that compandor A should have a greater action than that of compandor B. Although both A and B are to be applied to Method 5, B is also the basis of the separate-stage compandor. Moreover, one of the features of Method 5 is that, because the companding action is incorporated in the encoder, such action need not be as great as that required in conventional coding, using a separate stage compandor.

This may be seen from the following reasoning. The number of quantised levels (l) in a Method 5 encoder is given by equation (3.7) repeated below:-

$$l = \int f \, dT \qquad (3.7)$$

That is, if a triangular waveform (as in compandor B), with linear sides were applied to the v-f converter, it would

give a linear variation of clock pulse frequency, which would give companding action. Therefore, a companding element, which non-linearises the characteristic, is only adding to the compression which is already there. Hence, it is true to say that a non-linear companding element inserted in a type A compandor is applying a smaller action than a separate-stage compandor, for the same value of μ. It must, however, be admitted that the initial slope of the transfer characteristic of type A may be much larger than that of type B (without the differentiator). Such a large gradient however, must necessarily exist over a smaller range of inputs.

A possible major advantage of the type A compandor is that it need only be single-ended. This follows from the fact that a type A compandor provides a sweep waveform which is the time differential of the balanced logarithmic transfer characteristic of equation (2.1). Both negative and positive excursions of the latter give positive differentials. This may be seen from equations (2.1) and (3.10) which give the derivation of clock pulse frequency.

Although the transfer functions required of type A and type B compandors are different, they are sufficiently similar to the characteristics of either p.n. diodes or junction f.e.ts for either to be used as companding elements. The disadvantages of p.n. diodes have been listed in section 2.3, the most important being the difficulty in controlling the characteristics of sending and receiving diodes, so that they are exactly matched. It has been suggested[39] that

although the junction f.e.t. has the same disadvantages, these may be overcome simply because the f.e.t. characteristic may be controlled by gate bias. Hence, the use of the junction f.e.t. is considered as a companding element in the development of both types of sweep generation (A and B) given in the following sections.

7.1. Triangular Sweep Method (A)

This consists of a triangular waveform generator, synchronised with the channel pulse and is followed by a compandor. The output of the divider described in section 5.2 has a half-period equal to the duration (T_0) of the unmodulated channel pulse. Hence it was considered that the triangular waveform should be generated from it by integration.

7.1.1. The Integrator

The design of I.C. operational amplifier integrators is well established[28, 35] and a typical arrangement is shown in fig. 7.1. The feedback capacitance, C connected between the output and input terminals, causes a large input capacitance (1 + A)C where A is the open-loop voltage gain. The input time constant is much larger than the period of the input square wave and hence linear charge and discharge occurs, resulting in a triangular waveform.

With the O.A. used (Motorola type 1712CP) the purity of waveform was found to be critically dependent upon the supply voltages, and some departure from the

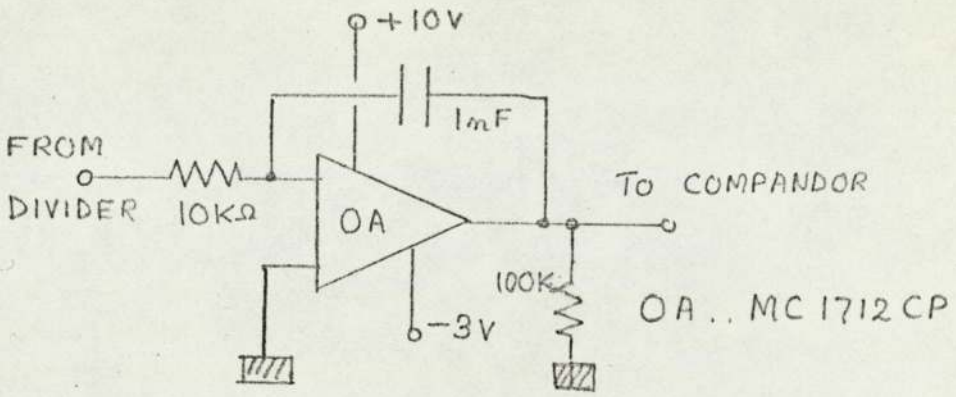


FIG. 7.1 AN OA INTEGRATOR.

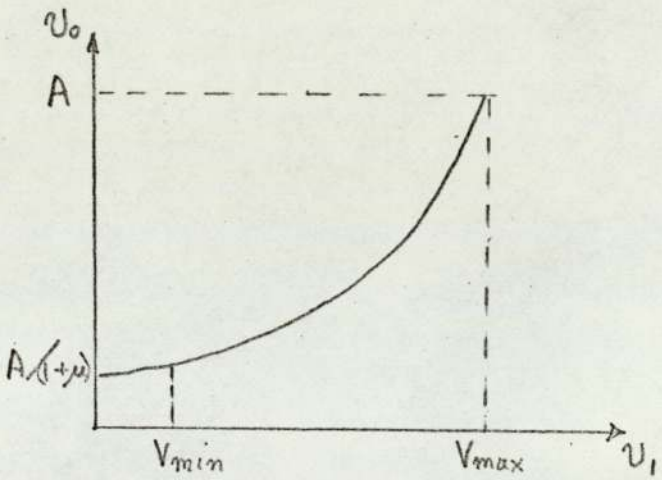


FIG 7.2(a) TRANSFER CHARACTERISTIC REQUIRED FOR SWEEP GENERATOR

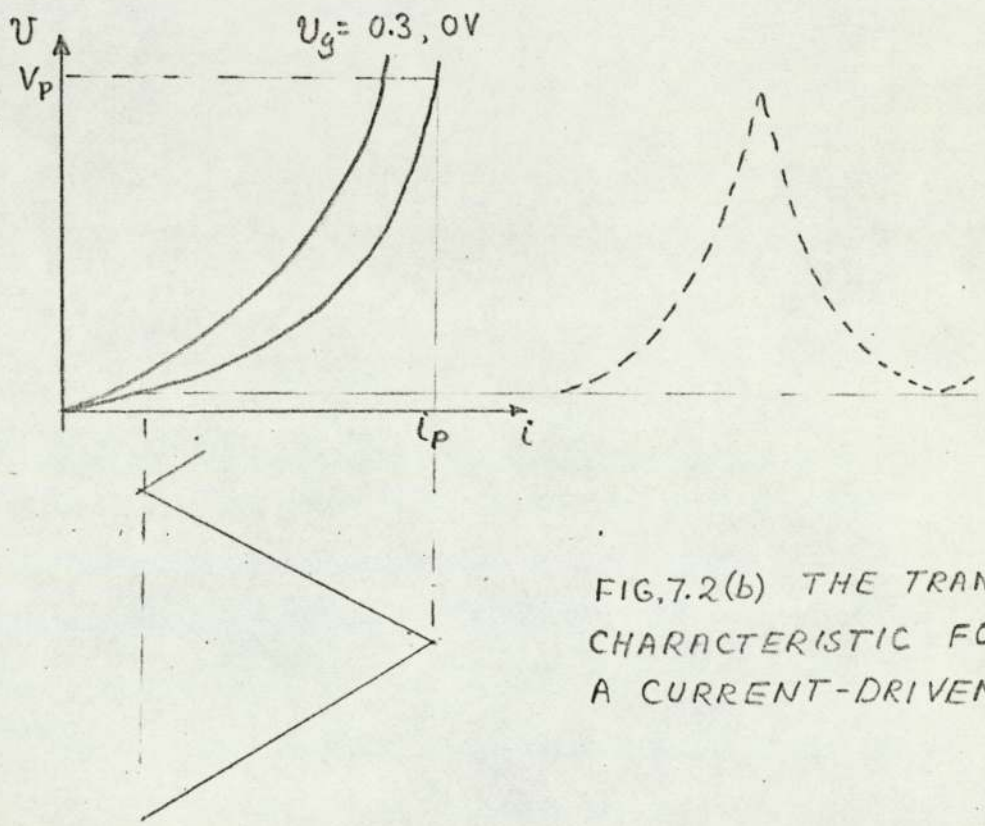


FIG. 7.2(b) THE TRANSFER CHARACTERISTIC FOR A CURRENT-DRIVEN FET.

recommended values[35] was necessary.

It is usually necessary in O.A. integrators to have some adjustment in the feedback circuit[25] in order to balance offset voltages and to ensure that the d.c. output voltage corresponds to the integral of the input voltage. Fortunately the d.c. value of the integral is not required for the output is to be capacitor coupled to the compandor.

7.1.2. The Single Ended Compandor

The sweep waveform at the input to the v-f converter should, by equation (3.10) have a voltage variation given by:

$$v_o = \frac{A}{1 + \mu \left| v/V_m \right|} \qquad \text{------} \quad (7.7)$$

where A is a constant and $\left| v/V_m \right|$ is the magnitude of the normalised input voltage. These equations (3.10 and 7.7) have been derived from the logarithmic compression curve, for which the abscissa is the signal voltage. In a p.l.m. system v/V_m corresponds to the quantity $\Delta T/T_o$, indicated in fig. 3.1, where

$$\frac{v}{V_m} = \frac{\Delta T}{T_o} = \left[\frac{T - T_{min}}{T_o} - 1 \right]$$

When a sweep generator is followed by a linear v-f converter, it is convenient to change the variable so that the time and voltage are reckoned from the sweep commencement. Hence if V_{min} and V_{max} are the minimum and maximum levels of the input sweep waveform the normalised quantity v/V_m is given by:

$$\frac{v}{V_m} = \left[1 - \frac{v_1 - V_{min}}{V_{max.}}\right]$$

Where v_1 is the instantaneous value of the triangular sweep input voltage.

The output voltage of the sweep generator given by equation (7.7) may now be written as:-

$$v_o = \frac{A/(1+\mu)}{1 - \frac{\mu}{1+\mu}\left(\frac{v_1 - V_{min.}}{V_{max.}}\right)} \quad ----(7.8)$$

The variation of v_o with v_1 given by equation (7.8) is shown in fig. 7.2.

In general, semiconductor junction devices such as p.n. diodes and f.e.t.s may be operated to exhibit the variation shown in fig. 7.2 approximately. The junction f.e.t., which has already been considered in Chapter 4 as a variable timing resistance, is particularly suitable for providing the companding function of equation (7.8.).

This may be shown by comparing the graph of equation (7.8) with the idealised drain characteristic (i/v curve) also shown in fig. 7.2. It may be seen that the compression parameters may be increased by increasing the gate bias voltage. If a f.e.t. were current-driven by a triangular waveform which had the maximum and minimum values given in equation (7.8), the waveform in fig. 7.2 would result. The similarity to the sweep waveform required, and shown in fig. 3.8, may be noted. This similarity is considered further in section 7.3.

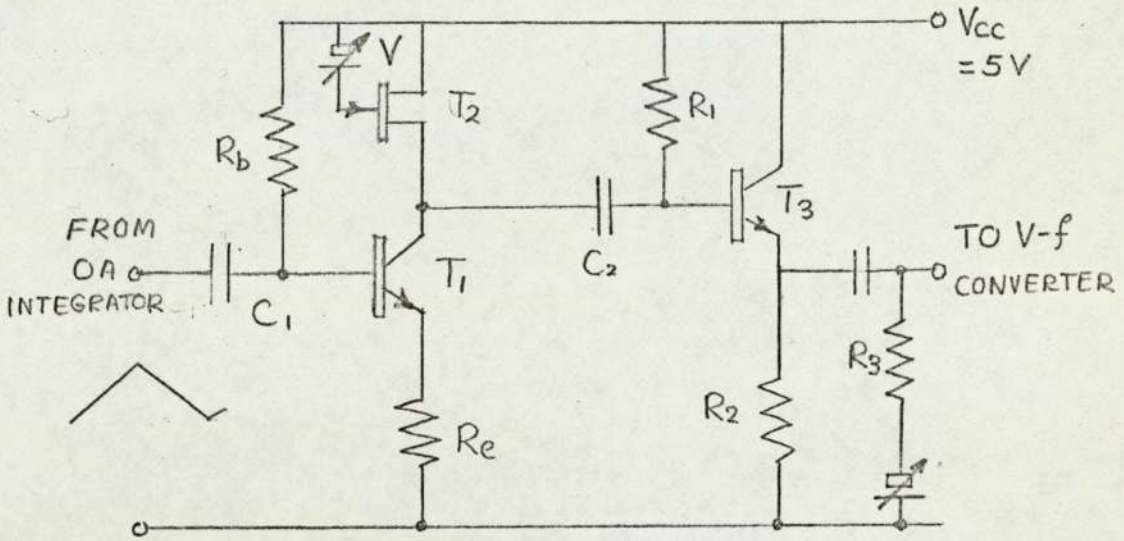
The principle of current-driving diodes has been shown in fig. 2.13. The circuit arrangement for the f.e.t. compandor is similar, and is shown in fig. 7.3. The drain current is maintained proportional to the triangular sweep voltage input by the action of bipolar transistor T_1 and its emitter resistor R_e. The output voltage is coupled via the emitter follower T_3 to the v-f converter. It is to be noted that there are two polarity reversals in the sweep generation, firstly at the integrator and secondly at the compandor. Since the input to the v-f converter should be positive-going for low clock frequencies (i.e. corresponding to large modulation depths) the input square wave to the integrator should be taken from the complementary (Q) output of the divider. The input and output waveforms are shown in the oscillograms of fig. 8.4

7.2. The Differentiated Sweep Method

There are three stages in this method - (i) a ramp generator, (ii) a balanced compandor and (iii) an OA differentiator.

7.2.1. Ramp Generator

The sawtooth generator stage is shown in fig. 5.10 The output of the sequencer is applied to a transistor switch Q_1 so that it is non-conducting during the channel pulse duration. The capacitor (C_1) between collector and emitter of Q_1, may then charge with



COMPONENT	VALUE
R_e , R_1	470 Ω
R_b , R_2	200 KΩ
R_3	100 KΩ
C_1 , C_2 , C_3	100 nF
T_1 T_3	BC108
T_2	2N5461

FIG. 7.3 THE SINGLE-ENDED CURRENT-DRIVEN F.E.T. COMPANDOR

constant current from Q_2. The operation of this constant current circuit follows the same principles as those in the v-f converter, except that the base-emitter voltage is fixed by an avalanche diode (D_1).[81] To avoid loading the ramp charging capacitor, n-channel f.e.t. Q_3 is used as a phase-splitter, the outputs of which are connected to the balanced compandor.

7.2.2. Balanced F.E.T. Compandors

The compandor for the differentiated sweep method should provide an output voltage (U) given by:-

$$U = \frac{\log(1 \pm \mu V)}{\log(1+\mu)} \qquad \text{----------(7.9)}$$

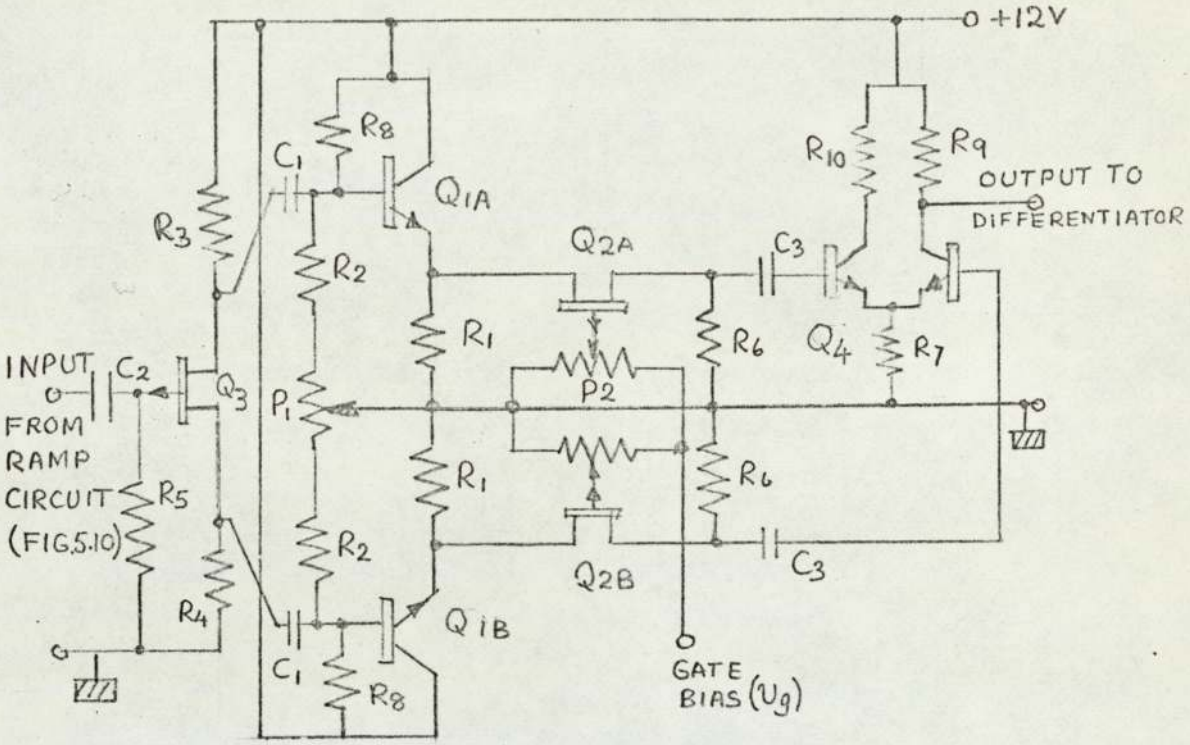
where V is the input voltage (i.e. the linear ramp) and + and - signs correspond to positive and negative values of modulation.

The compression given by equation (7.9) should be symmetrical for positive and negative values of U, and therefore, a balanced compandor circuit is required. While a balanced circuit can be made up with two diodes, as shown in fig. 2.13, the design problem with f.e.t.s is more complicated. The main complication is that a f.e.t. will conduct when the drain is positive or negative with respect to the source. Three attempts were made to overcome this problem as follows. Firstly, a p.n. diode was connected in series with each of two f.e.t.s so that they conducted on alternate half-cycles. The voltages across a p.n. diode and a

f.e.t. were of the same order. Hence it was considered that any "spreads" among diodes (and f.e.t.s) would not only give asymmetrical modulation, but would also complicate the matching of sending and receiving compandors.

Secondly, the push-pull emitter-follower circuit with a f.e.t. in each emitter lead, and shown in fig. 7.4, was tried. While this circuit could be operated to give a symmetrical compression characteristic, there was considerable "cross-over" distortion. This distortion arises from the nature of the v/i characteristic of a forward-biassed p.n. junction, and is illustrated in fig. 7.5. The distortion is reduced by adjusting the bias values of base current, but the minimum value was considered to be unacceptably large. It was considered, however, that the "spreads" in transistor values would not be a serious limitation as in the first attempt. For on the one hand, the effect of "spreads" among the bipolar elements would be negligible because of the emitter-follower connection. On the other hand, any spread in f.e.t. values may be compensated for, by adjustment of gate-source voltage. This latter point suggests that the f.e.t. has a considerable advantage over the p.n. diode as a compandor, in that errors arising from the matching of elements may be controlled. A full consideration of such errors is given in section 7.3. and Appendix. I.

A third attempt to overcome the basic limitation of the f.e.t. (i.e. its bi-directional property), was to



COMPONENT	R_1	R_2	R_3, R_4	R_5	R_6
VALUE	100Ω	33KΩ	1KΩ	3MΩ	4.7Ω
COMPONENT	R_7	R_8	R_9, R_{10}	C_1, C_2	C_3
VALUE	3KΩ	470KΩ	750Ω	100mF	1μF
COMPONENT	P_1, P_2	Q_1	Q_2, Q_3	Q_4	
VALUE/TYPE	5KΩ	BC108	BFW.10	2N3053	

FIG. 7.4. BALANCED F.E.T. COMPANDORS — PUSH-PULL EMITTER FOLLOWER CIRCUIT

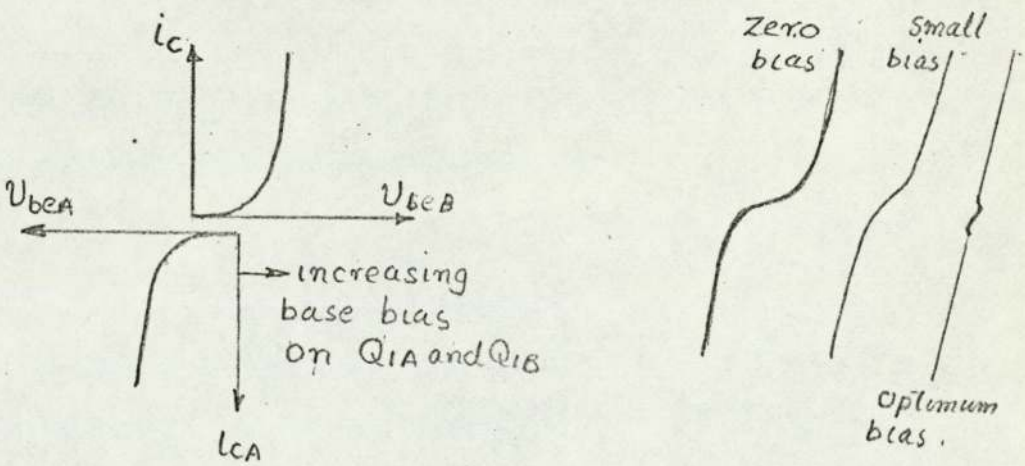
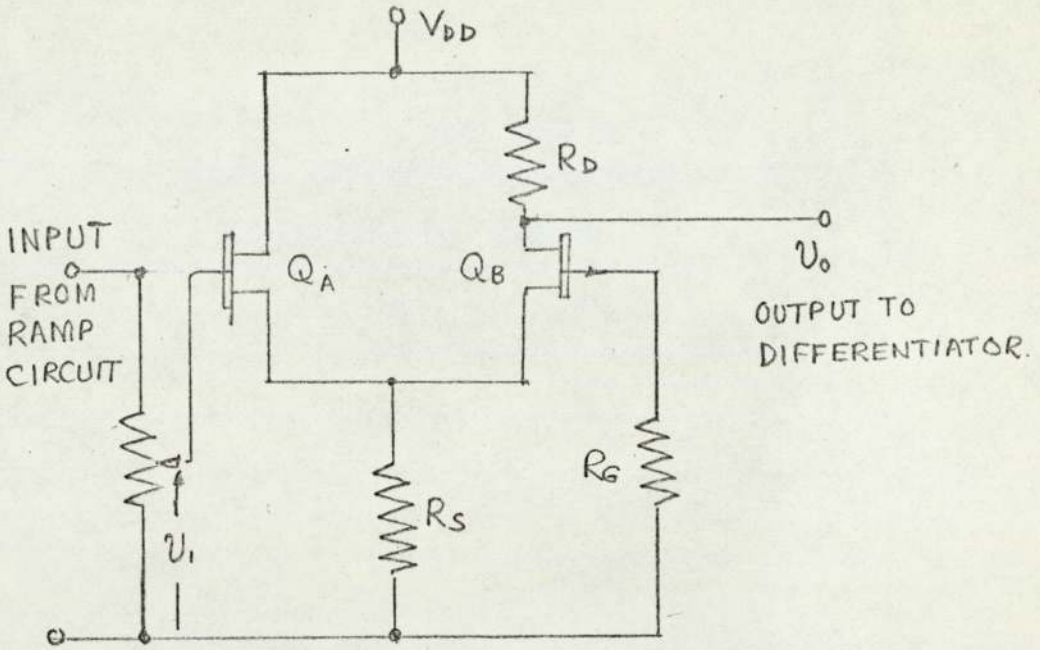


FIG. 7.5 CROSS-OVER DISTORTION IN PUSH-PULL EMITTER FOLLOWER CIRCUIT (FIG. 7.4)

use two f.e.t.s in a circuit which is similar to the emitter-coupled clipper. (The latter formed the basis of the differential comparator which is treated in section 5.4.). This balanced compandor is shown in fig. 7.6 and operates as follows. Both elements are self-biassed by the common source resistor R_s, so that they operate with gate-source voltages near to the pinch-off value (V_p). To a first approximation, the f.e.t.s are operated at constant drain voltage, so that any companding action is now due to the curvature of the transfer characteristic (i / v_g curve). The difference-connection ensures that positive and negative excursions are compressed symmetrically. The symmetry may be explained from figs. 7.6 and 7.7 by noting that the output voltage is proportional to the drain current i_2, which is a function of the gate-source p.d v_{g2}, which, in turn, is given by the p.d. $(i_1+i_2)R_S$. If the input voltage makes G_1 more negative, and reduces i_1, (i_1+i_2) tends to decrease thus making G_2 less negative and increasing i_2. This increase continues until i_1 is cut-off, when $v_{g1} = (v_1 - i_2 R_S) = V_P$, and i_2 is clamped at the upper level.

If, on the other hand, the input voltage makes G_1 more positive, i_1 is increased, (i_1+i_2) tends to be increased, making G_2 more negative, until $v_{g2} = i_1 R_S$ i.e $v_{g2} = V_P$, and i_2 = zero at the lower clamping level. The amplitude limits may be calculated, as shown in



COMPONENT	R_S	R_D	P_1, R_G	Q_A Q_B
VALUE/TYPE	15KΩ	3.9KΩ	10KΩ	MC

FIG.7.6 BALANCED FET COMPANDORS — DIFFERENTIAL SOURCE COUPLED CLIPPER

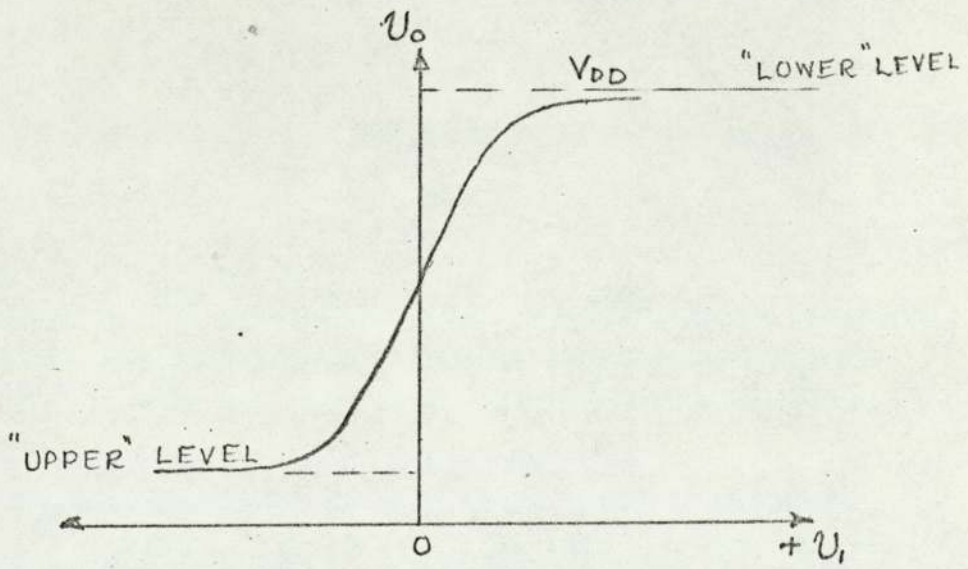


FIG. 7.7 TRANSFER CHARACTERISTIC FOR THE DIFFERENTIAL SOURCE-COUPLED CLIPPER.

Appendix 6 and with the values given in fig. 7.6, have a separation of only 0.5 V. There is, however, a serious disadvantage in that the characteristic is not even approximately logarithmic. An empirical equation has already been given[42] for the transfer characteristic at constant drain voltage in equation (4.9). This is now written as:-

$$\frac{i_{1(2)}}{I_p} = \left[1 - \frac{v_{g1(2)}}{V_p}\right]^n$$

where n has the value 2. The transistors tested* all appeared to have n = 1.5, so that the characteristic had a small curvature at finite values of current. Furthermore, the pinch-off condition is abrupt, the drain current ceasing, and giving a clamping level rather than a logarithmic "roll-off". Hence it must be concluded that a balanced logarithmic compandor cannot be conveniently constructed with junction f.e.t.s. The output of the balanced-compandor, however, requires a differentiation, and to complete the investigation of this method of sweep generation, the differentiation is described in the next section.

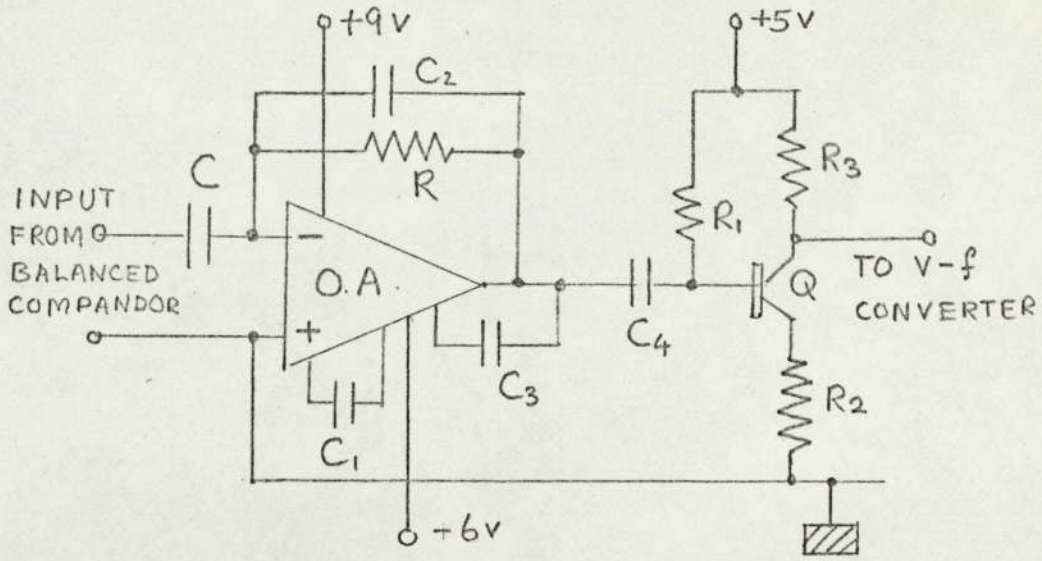
* Mullard BFW 10, Motorola. MPF102, 2N5461, MMF5.

7.2.3. The Differentiator

The principles of the O.A. differentiator, like those of the integrator are fairly well established, and the circuit shown in fig. 7.8(a) was adopted. It was found, however, that a linear I.C. of high gain, because of its higher sensitivity, gave a more noise-free waveform, than one of medium gain. It was also found that an active differentiator was susceptible to high frequency oscillation, presumably because of the relatively large phase shifts at high frequency. These however were reduced to an acceptable minimum by the decoupling capacitances shown in fig. 7.8

The principle of operation is as follows. The feedback resistance R causes a very low resistance R/(1+A) to be placed across the amplifier input terminals. Hence, a small input voltage proportional to the current in the input coupling capacitor and therefore to the time differential of the input voltage is amplified.

The action of the differentiator upon a linear sawtooth was tested and the resulting waveforms are shown in fig. 7.8(b) It was observed that any non-linearity in the input ramp gave rise to a distinguishing feature in the waveform of the differential. In fact the performance of the push-pull emitter-follower compandor was checked in this way; small "cross-over" distortions caused relatively large double-humps as shown in fig. 7.8. On the other hand, the difference compandor described in section 7.2.2. gave a waveform which when differentiated had no double humps.



COMPONENT	R_1	R_2	R_3	R	C
VALUE	120KΩ	820Ω	82Ω	1MΩ	1nF
COMPONENT	C_1	C_2, C_3	C_4	Q	OA.
VALUE/TYPE	47pF	22pF	100nF	2N3053	709 OPA.

FIG. 7.8(a) THE DIFFERENTIATOR.

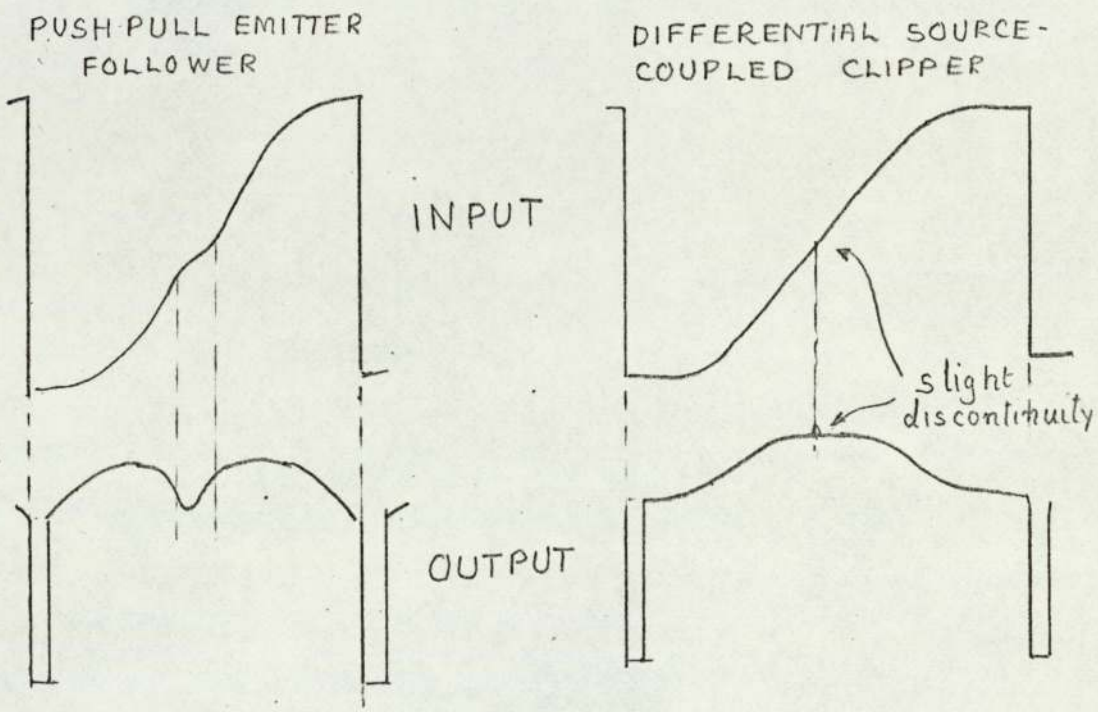


FIG 7.8(b) WAVEFORMS AT DIFFERENTIATOR.

7.3. The Junction F.E.T. as a Compandor

The junction F.E.T. has been considered as (a) a single-ended compandor with a triangular sweep, and (b) a balanced compandor with a sawtooth sweep. It has been shown that the bi-directional property of the f.e.t. limits its usefulness as a balanced current - or voltage-driven compandor. The difference connection, although giving a symmetrical waveform, gives a characteristic which is far from logarithmic. It is of interest now to consider the single-f.e.t. compandor in more detail for two reasons. Firstly, to show how closely the required characteristic can be provided, and secondly, what errors are likely to arise in the matching of sending and receiving elements.

7.3.1. Similarity to the Required Characteristic

It has been shown in section 7.1 that to give the logarithmic companding characteristic of equation (2.1), the input to the linear v-f converter should have a voltage (v_o) given by equation (7.8), and repeated below:

$$v_o = \frac{A/(1+\mu)}{1 - \frac{\mu}{1+\mu}\left[\frac{v_1 - V_{min}}{V_{max}}\right]} \qquad ----(7.8)$$

The voltage (v_o) should then be the output voltage of the single-ended compandor, for which v_1 is the input voltage, varying between limits V_{min} and V_{max}. The variation given by equation (7.8) has been compared in fig. 7.2 with that given by a f.e.t. when current driven.

To investigate the similarity in more detail, the actual compression which is given by a f.e.t. should be determined. Since the logarithmic compression curve is obtained by the integration of equation (7.8), the compression curve for a f.e.t. may be obtained by integrating the equation of the f.e.t. characteristic shown in fig. 7.2.

Hence, an expression is required for the drain voltage in terms of the drain current; the variation of $\int v\,di$ could then be compared with the logarithmic companding characteristic of equation (2.1). Two equations were obtained for the f.e.t. drain characteristic for zero gate-source bias. The first, attributed to Shockley[34] is written:-

$$\frac{i}{I_P} = \frac{3v}{V_P} - 2\left(\frac{v}{V_P}\right)^{1.5} \quad \text{------} \quad (7.11)$$

where i and I_p are the drain currents given by drain voltages v and V_p respectively, the suffix p denoting pinch-off values. Equation (7.11) was supposedly derived by considering a two-dimensional geometry of a f.e.t. It is however, unsuitable for the present purpose, because the integral $\int \frac{v}{V_P}\, d(i/I_p)$ cannot be easily evaluated. Hence, a second equation was derived from an inspection of equation (7.11) and the typical characteristic shown in fig. 7.2. This may be written:-

$$\frac{v}{V_P} = 0.33\left\{ i/I_P + (i/I_P)^2 + (i/I_P)^3 \right\} \quad \text{--} \quad (7.12)$$

Equation 7.8, 7.11 and 7.12 are shown graphically in fig. 7.9.

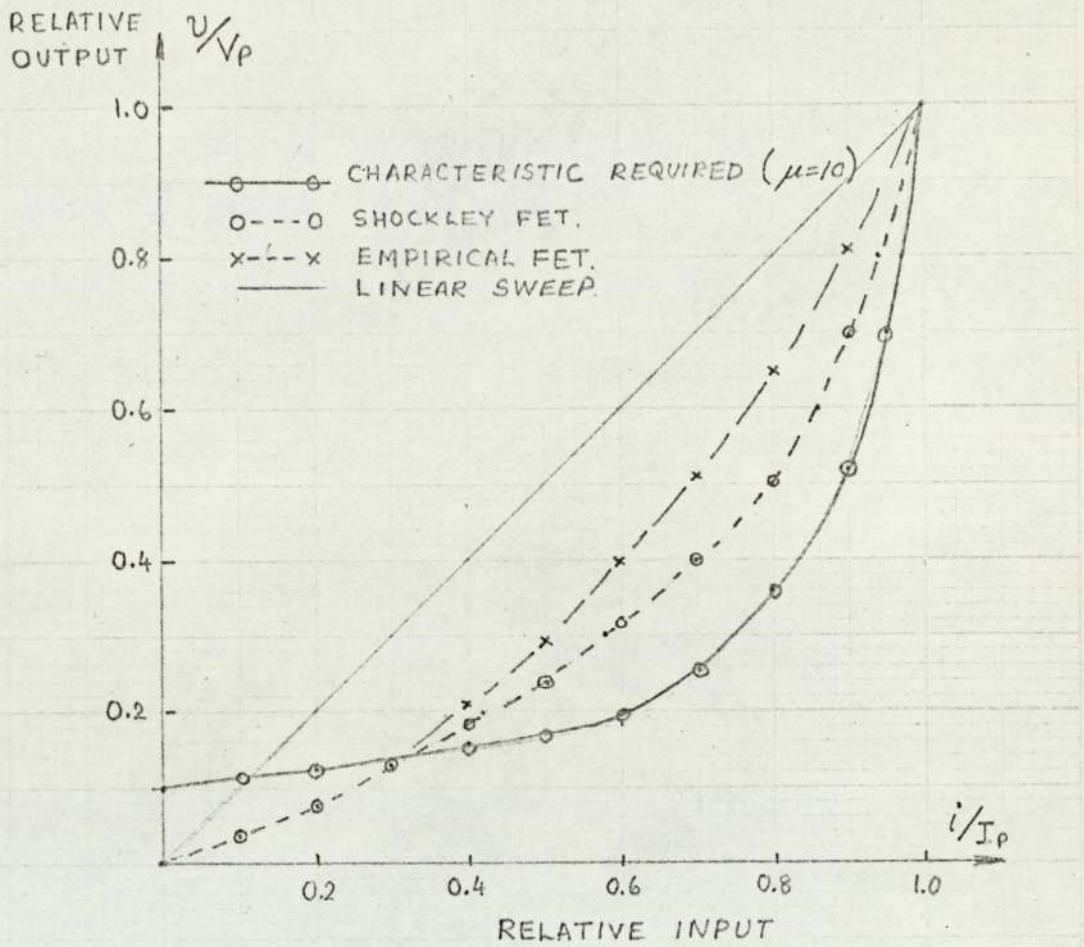


FIG. 7.9. SWEEP GENERATOR CHARACTERISTICS.

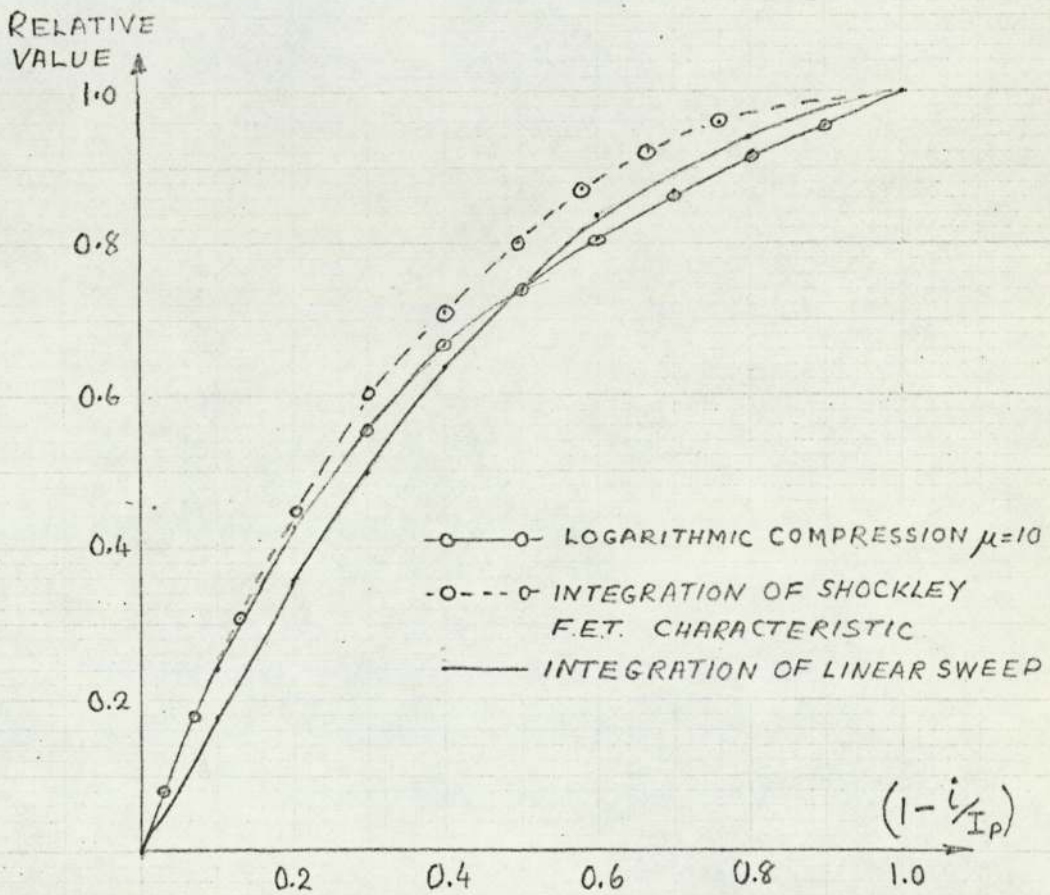


FIG. 7.10 PREDICTED COMPANDING CHARACTERISTIC.

There are two main differences between the required characteristic and the f.e.t. curves. Firstly, the characteristic for logarithmic companding requires a minimum output of 0.1, when the input current is zero. This difference may be minimised by R.C. coupling between compandor and v-f converter and the addition of a d.c. bias. Secondly, the slopes at sweep inputs corresponding to small modulating signals for the Shockley and required characteristics are very similar, while that for equation (7.12) is too small. It must be admitted that the Shockley equation more nearly represents a junction f.e.t. than equation (7.12) and clearly some method is required to evaluate $\int \frac{v}{V_p} d\left(\frac{i}{I_p}\right)$ for the function given in equation (7.11). A semi-graphical method is given in Appendix H , and the results are shown graphically in fig. 7.10 together with the logarithmic companding characteristic of equation (2.1). It may be seen from fig. 7.10 that when the relative sweep input voltage to the f.e.t. compandor is < 0.4 , the integrated Shockley characteristic is in close agreement with the logarithmic characteristic for $\mu = 10$.

It is to be noted that the comparison has only been made with a curve for a low value of compression parameter ($\mu = 10$). This restriction was necessary to simplify the integration of the function in equation (7.11). As is stated in section 7.1.2., however, larger compressions may be obtained with gate bias.

It has been stated in section 7.0 that some companding action will be given when the triangular waveform is applied direct to the v-f converter (i.e. without any non-linear companding element). The integral of the linear fall and rise portions will be a parabolic curve having an equation:-

$$v_o = 2v_i - v_i^2$$

where v_o and v_i are the normalised output and input voltages of the equivalent compressor. This function may be compared with the other compression functions in fig. 7.10 to show the inherent companding action of Method 5.

7.3.2. Companding Errors in a Method 5 Encoder

It has been found that the single-ended junction f.e.t. compandor, with a triangular waveform input can provide the required sweep waveform. It now remains to determine what errors are likely, due to the differences of the characteristics of sending and receiving compandors. A treatment of the errors which will arise in the separate-stage compandor based upon reference (39) is given in Appendix J. It is shown there are two types of residual error arising from:

(a) the inability to voltage-and current-drive the sending and receiving elements:

(b) the ratio of the resistances of compressor and expander does not remain constant for all values of modulating signal.

It is a feature of Method 5, however, that the compandors at sender and receiver are both driven from the same type of waveform. In this work, a single-ended junction f.e.t. compandor is current-driven at both sender and receiver. It is to be expected, therefore, that errors will only arise from the difference in resistances of sending and receiving elements. In the following treatment an attempt is made to show the significance of such errors.

It has been shown that the number of levels l transmitted by a pulse of length T is given by:

$$l = \int f_s \, dT$$

where f_s is the encoder clock p.r.f.

The number of levels contained within an element dT is therefore given by :-

$$dl = f_s \, dT$$

At the decoder, the number l is set into a binary counter which is driven by a clock pulse source of variable frequency (f_r) where $f_r = f_s$ approximately. The time (dT) taken to count an incremental number of clock pulses (dl) is given by:-

$$dT = \frac{1}{f_r} dl$$

Hence, the decoder counter will re-set to zero in a time T_r given by:-

$$T_r = \int_0^{T_s} f_s / f_r \cdot dT \qquad \text{------(7.14)}$$

When $f_s = f_r$, $T_r = T_s$ and error-free transmission occurs.

In the experimental model for Method 5, f_s and f_r are given by similar voltage-frequency converters so that $f_s = K_s V_s$ and $f_r = K_r V_r$ where K_s and K_r are approximately equal constants.

The voltages V_s and V_r are the respective outputs from the two compandors, which are current-driven as shown in fig. 7.3 through bipolar transistors, having emitter resistors R_e.

Hence voltages V_s and V_r are given by:-

$$V_s = V_1 \frac{r_s}{R_e} \quad , \quad V_r = V_1 \frac{r_r}{R_e}$$

and clock pulse frequencies are given by:-

$$f_s = K_s V_1 \frac{r_s}{R_e} \quad , \quad f_r = K_r V_1 \frac{r_r}{R_e}$$

By substituting in equation (7.14), the decoded pulse (T_r) is given by:-

$$T_r = \frac{K_s}{K_r} \int_0^{T_s} \frac{r_s}{r_r} \, dT \qquad \text{------ (7.15)}$$

The companding error may be defined[39] as the fractional variation of the ratio V_2/V_1 where V_2 and V_1 are the signal output of the decoder and signal input to the encoder respectively. In the coding method under consideration:

$$\frac{V_2}{V_1} = \frac{T_r}{T_s}$$

That is, if T_{ro}/T_{so} is the ratio of the pulse lengths at very small signal levels, then the companding error is given by:-

$$\mathcal{E} = \left[\frac{T_r}{T_s} \cdot \frac{T_{so}}{T_{ro}} - 1 \right] = \left[\left\{ \frac{K_s}{K_r} \int_0^{T_s} \frac{r_s}{r_r} \cdot dT \right\} \frac{dT_s}{dT_r} - 1 \right] \qquad \text{...(7.16)}$$

The value of $T_{s0}/T_{T0} = dT_s/dT_T = 1$

so that the error ε may be determined when the integral in equation (7.15) is evaluated.

The evaluation of $\int \frac{\tau_s}{\tau_T} \, dT.$

is complicated for two reasons. Firstly, τ_s and τ_T although obeying the same general function of drain voltage, have differences whose variation with drain and gate voltages is unknown. Secondly, because the duration T is proportional to clock sweep voltage, integration w.r.t. drain current, rather than drain voltage, is required.

That is, the ratio τ_s/τ_T will show a variation with current, and this is a major source of error in both the separate-stage compandor and in the method under consideration. It has been shown[39] for the former that minimum error need not necessarily occur when τ_s/τ_T is unity. This rather remarkable feature is considered in Appendix J , as it is relevant to the present investigation.

The dependence of drain resistance (r) upon drain voltage may be obtained from the Shockley equation (7.11). This latter equation is given in full as:-

$$i/I_p = 3V/V_p - 2\left(V/V_p + V_g/V_p\right)^{3/2} + 2\left(V_g/V_p\right)^{3/2} \quad \text{--(7.16)}$$

The drain conductance $(1/r)$ relative to the value $1/R_p$ given when $V = V_p$ is then as follows:-

$$R_p/r = 3 - 2\sqrt{V/V_p}\left[\left(1 + V_g/V\right)^{3/2} - \left(V_g/V\right)^{3/2}\right] \quad \text{--(7.17)}$$

It may be noted that neither of equations (7.16) and (7.17) contains information about differences in f.e.t. resistances r_s and r_τ. Only if the derivation of equation (7.16) were known, could the actual dependence of r_s and r_τ upon U and U_g be obtained. To reveal the nature of this dependence, another equation for $R_p/_T$ is derived in Appendix D. This is given below:-

$$R_{p/_T} = 3\left[1 - 0.425\sqrt{U/V_p + U_g/V_p}\right]^2 \quad \ldots(7.18)$$

Equations (7.17) and (7.18) appear somewhat different but in fact, they are similar functions of $(U + U_g)$ as may be seen from fig. 7.11. It is suggested that the similarity of two differently derived equations is a confirmation of their validity. Furthermore, any information to be obtained from equation (7.18) may be applied to equation (7.17). The following conclusions may therefore be made to Appendix D and a comparison of equations (7.17) and (7.18).

(1) The conductance of a f.e.t. channel is a function of $\sqrt{U + U_g}$

(2) A difference in conductance between two f.e.t.s. of the same type is a difference in the surd and may therefore be represented by an expression of the form $\sqrt{U(1+\sigma) + U_g}$ where $\sigma < 1$.

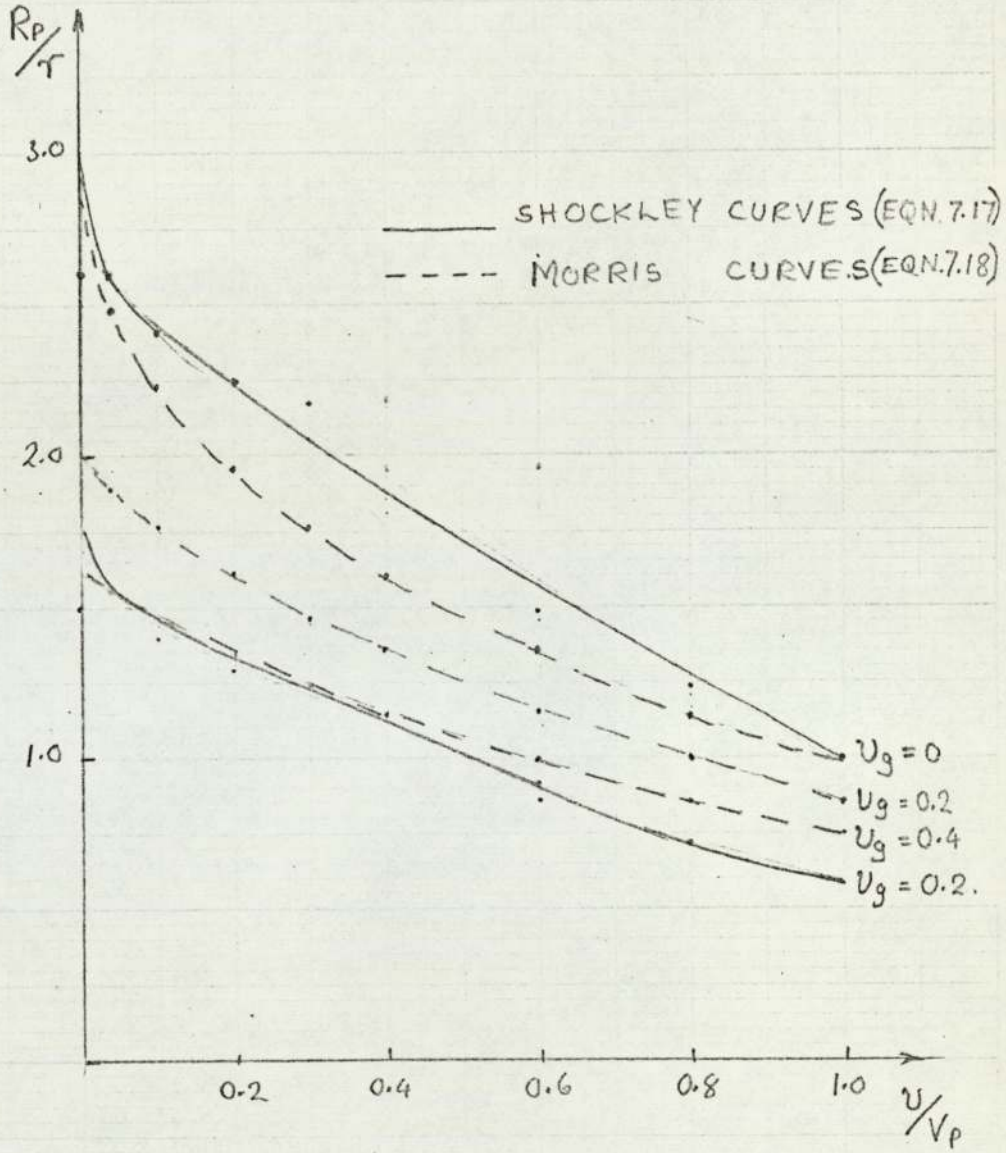


FIG. 7.11. THEORETICAL VARIATION OF THE CONDUCTANCE OF A JUNCTION FET.

(3) The Shockley equation for drain current appears to have been derived from an integration* of a conductance w.r.t. drain voltage as follows:-

$$3\int_0^{V}\left(V/V_P + V_g/V_P\right)^{1/2} d\left(V/V_P\right) = 2\left(V/V_P + V_g/V_P\right)^{3/2} - 2\left(V_g/V_P\right)^{3/2} \quad \text{------(7.19)}$$

(4) A difference in conductance between two f.e.t.s may be represented in equation (7.17) as follows:-

$$R_P/r = 3 - 2\sqrt{V/V_P}\,(1+\sigma)^{3/2}\left[\left(1 + V_g/V\right)^{3/2} - \left(V_g/V\right)^{3/2}\right] \quad \text{....(7.20)}$$

(5) Equation (7.18) implies that the conductance at $V = 0$ is independent of V_g while equation (7.19) suggests that

$$R_P/r_o = 3\left[1 - 0.425\sqrt{V_g/V_P}\right]^2 \quad \text{----(7.21)}$$

This latter result is in agreement with the experimental results in Appendix I

It is shown in Appendix I that the ratio r_s/r_r may be made very nearly independent of V (and i) by adjustment of V_g. This result has been shown experimentally[39] and confirmed theoretically in Appendix J for a special case. That is, one f.e.t., having a resistance r_s, (or r_c), a zero value of V_g and a term $(1+\sigma)^{3/2}$ as in equation (7.20), and the other, having a resistance r_r, or r_c which obeys the "Shockley" equation (7.20) exactly. It must be admitted that, although equation (7.20) suffers from the limitation given under (5) above, it did tend to give a clearer confirmation of the experimental result that matching of two f.e.t.s could be

*That the Shockley equation is an integration is confirmed by Walker[41] who states that the equation is only valid when $V > V_P$.

achieved by gate bias adjustment. Hence equation (7.20) was adopted for integration and the ratio r_s/r_r was written as follows:-

$$\frac{r_s}{r_r} = \frac{1-0.66\sqrt{V/V_p}\left[\left(1+V_g/V\right)^{3/2}-\left(V_g/V\right)^{3/2}\right]}{1-0.66\sqrt{V/V_p}\left[1+\sigma\right]^{3/2}} \qquad ----(7.21)$$

The interpretation of equation (7.21) is that:

(1) the receiving-end f.e.t. is ideal, obeying the "Shockley" equation (7.17) by a resistance r_r when the effective gate-source p.d. is $(V + V_g)$

(2) the sending-end f.e.t. has a resistance r_s which tends to be larger than in the ideal case because the effective gate-source p.d. is larger by the factor $(1 + \sigma)$

(3) the ratio tends to become independent of drain voltage V at some value of gate-bias V_g at the receiver.

The integral of equation (7.21) has been evaluated in Appendix K, between the limits $i/I_o = 0$ and $i/I_o = 1$ for the special case of both f.e.t.s having zero gate-bias. The consequent solution of equation (7.16) is the maximum companding error which will arise when no attempt is made to compensate by gate bias. This error has been estimated as 0.637σ, which should be compared with the theoretical error of 1.98σ, developed in Appendix J for the separate stage compandor.

7.4. Conclusion to Chapter 7

An investigation has been made of two types (A and B) of sweep generator. Type B had three stages, including a balanced compandor, while Type A had two stages. The junction f.e.t. has a certain advantage as a single-ended compandor, but is not easily applied as a balanced compandor. Hence generator type A, the stages of which are shown in figs. 7.1 and 7.3, was adopted for the model.

A study has been made of the f.e.t. as a compandor. Firstly, the i/v characteristic has been compared with the logarithmic compression characteristic. To do this, two equations were considered; one due to Shockley, and a much simpler one derived empirically. It has been shown that the required characteristic may be realised approximately.

Secondly, an assessment of the likely companding errors has been made. It has been shown in reference (39) (Append. I-J), that the major error in separate-stage companding is that due to the variation in the ratio of the resistances of compressor and expander with modulating signal. These variations arise from differences between two f.e.t.s of the same type. Furthermore, it has been shown that the variation of this ratio determines the error in Method 5 coding. To estimate the likely error, it was necessary to account for the spread in characteristics. Hence an equation was derived (Appendix D) which suggested that differences were due to the differences in p.d. across the depletion region. This analysis enabled the Shockley-derived equation to be modified. It was then shown (Append. J-K) that the maximum error in Method 5 may be one-third of that in separate-stage companding.

CHAPTER EIGHT

THE TESTING OF THE MODEL CODERS

8.1 Introduction to this Chapter

8.2. Synchronisation

8.2.1. The Reset (Clear Pulses)

8.2.2. The Encoder Register Write-in Pulse

8.2.3. The Decoder Counter Write-in Pulse

8.2.4. Stabilisation of the Swept Frequency Clock Pulses

8.3. Tests upon the Encoder

8.3.1. Tests for Correct Operation

8.3.2. Testing the Transfer Characteristic

8.3.3. Discussion of Transfer Characteristics

8.4. The Encoder and Decoder in Tandem

8.4.1. The Overall Tests

8.4.2. Discussion of Results of Overall Tests

8.5 Asynchronism in the coding model

8.1. Introduction to this Chapter

The stages of the Method 5 coders have been considered in chapters 5, 6 and 7. This chapter is devoted to showing how these stages are connected, and to the testing of the encoder and decoder models.

8.2. Synchronisation

Block diagrams have already been given in chapter 3 to illustrate the principles involved. The aim of this work, however, is to demonstrate how non-linear companding may be incorporated in the coder. It is not necessary, therefore, to instrument the complete systems shown in figs. 3.9 and 3.12. Also, in practice, the synchronising pulse trains, at the decoder, are extracted from the received pulse train. For convenience, in the experimental decoder and encoder, the same synchronising pulse trains are used.

The main components of both models are shown in fig. 8.1. It will be seen that the encoder and decoder are on the L.H.S. and R.H.S. respectively, and that both have full- and dashed-line connections. The full-line connections show that the 8 KHZ binary digit pulses synchronise the 1 KHZ divider output pulses which, in turn, synchronise the stages in two paths in both coders. These are called the principal connections because they show how the stages are generally connected. The dashed lines indicate the additional synchronisations which are required for stable operation.

In a pulse-count method, the length-modulated channel pulses of the first channel gate clock pulses, which are counted in that channel pulse duration. The parallel-to-serial conversion

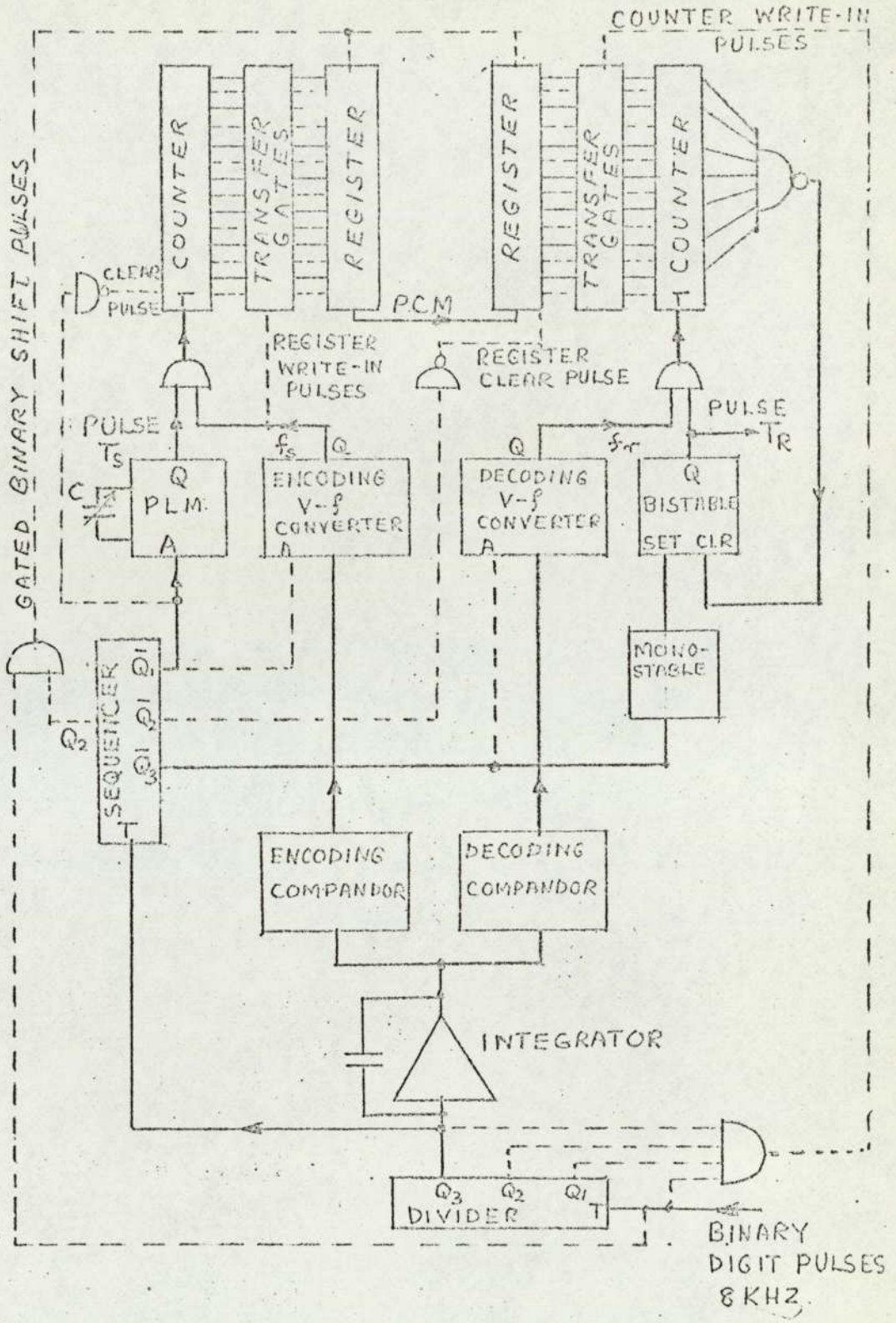


FIG. 8.1 THE ENCODER AND DECODER CONNECTED FOR TEST.

(Full lines indicate principal connections; dashed lines are subsidiary connections for synchronisation)

occurs during the second channel pulse. Since the decoder and encoder are in close proximity, the serial-to-parallel conversion and the setting of the binary counter also occur during the second channel pulse. The subsequent operation of the counter then takes place in the third channel pulse duration. This sequence is illustrated in the pulse waveform diagrams of fig.8.2.

To obtain this sequence in the coders, not only are synchronising connections from the sequencer required, but also connections, which give re-set pulses for the counter and register, in the encoder and decoder respectively. Also the transfer gates between counter and register in both coders require pulsing. In addition, to obtain stable operation with a triangular sweep, the v-f converters require additional synchronisation. These three connections are now explained in detail.

8.2.1. The Reset (Clear) Pulses

To permit sampling at frame intervals and multi-channel operation, the encoder counter required clearing when a completed count has been transferred to the output register. Ideally, the reset pulse should have small duration, with an edge coinciding with the trailing edge of the channel synchronising pulse. In the experimental model, only one channel is instrumented, and it is therefore convenient to have the counter operative only during the first channel synchronising pulse. Hence, the counter re-set pulse may be obtained from the normal output Q_1 of the sequencer. The clearing of seven bistables, however, presents a considerable logic load and so the complementary output Q_1 is taken

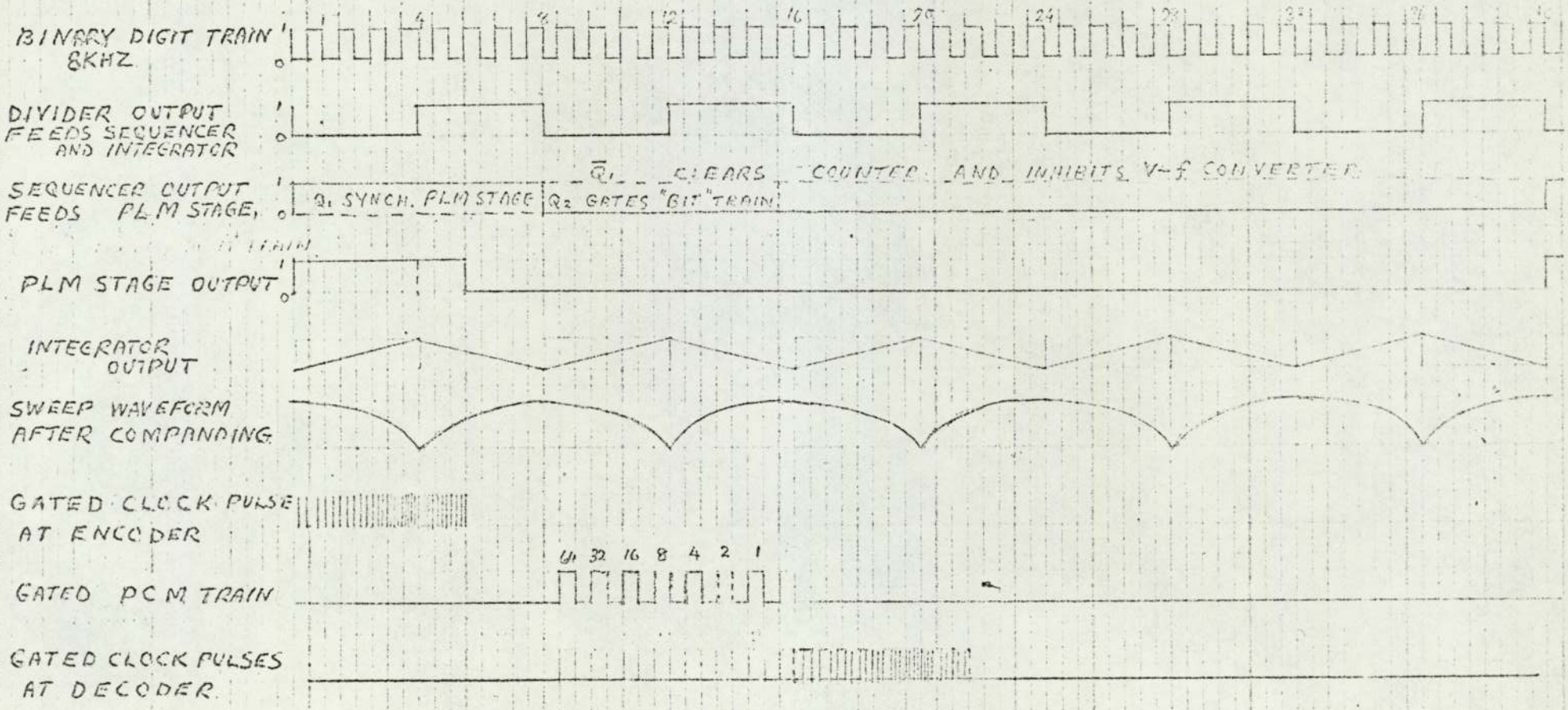


FIG. 8.2 WAVE FORMS IN THE METHOD 5 CODING MODEL.

via an inverting NAND gate to give the counter clear function. The input register of the decoder requires to be cleared for corresponding reasons at the end of the second channel pulse. Hence, the sequencer output Q_2 is taken via an inverting gate to give the register clear pulse.

8.2.2. The Encoder Register Write-in Pulse

At the end of a length-modulated pulse the stages of the binary counter are set to the logic levels of the binary equivalent of number of clock pulses. The logic levels are transferred to the set and clear terminals of the corresponding stages of the register. This could be achieved by a small duration pulse just before the onset of the clear pulse. It was found convenient to use the gated clock pulse train as the register write-in pulse. That is, the register gates, and hence the register set/clear terminals, are pulsed as the binary count occurs. This method would not be suitable in practice, for the counting of clock pulses in one channel duration would mar the parallel-to-serial conversion of the preceding channel. Of course, this does not matter in the single channel experimental model.

8.2.3. The Decoder Counter Write-in Pulse

It may be seen from fig. 8.1 that the output of the encoder-register is not gated by the binary digit pulses. The coded signal is therefore in logic data form (as distinct from the more usual pulse-form). This signal is applied direct to the decoder register by connecting the Q and $\bar{Q}$ outputs of the encoder register to the J and K inputs respectively of the

decoder register. A code-pulse group will be pulsed through the seven stages of the input register by the end of the 7th "bit" pulse. The transfer to the counter stages is arranged during the 8th pulse. The selection of the 8th "bit" pulse is made by gating with the three normal outputs (Q_1, Q_2 and Q_3) of the divider.

8.2.4. Stabilisation of the Swept Frequency Clock Pulses

For a given modulating signal, as represented by a setting of C in the p.l.m. stage, a definite number of clock pulses should be gated to the counter. When the clock pulse frequency is constant, or subject to a sawtooth sweep, there is no difficulty in maintaining a constant number of say 100 clock pulses in one interval.

When a triangular sweep voltage is applied to a v-f converter, it is not generally possible to display a steady trace, unless the v-f converter itself is synchronised with the channel pulse. It is considered that the absence of an abrupt edge in a triangular pulse can result in timing errors. For there will be small variations in the slope of a triangular waveform from one sweep period to the next, resulting in a variation in the numbers of clock pulses between sweep intervals. In general, jitter-free traces could only be obtained for short periods for the first 20-30 clock pulses. This was true not only for the dual monostable v-f converter, but also for one function generator*, to which a sweep input may be applied. It may be thought that synchronisation may be achieved by the addition of a narrow rectangular pulse to

* Function Generator TG501 (Feedback Ltd.)

the triangular waveform. The polarity and position of the pulse could be such as to decrease the frequency of the v-f converter to the lower-limit, and to stop pulse generation at the end of the sweep. When this was attempted, the pulses ceased towards the end of the sweep, but the operation was still subject to jitter.

It was then found that an excellent gating action could be obtained by applying the sequencer output Q to the AND gate inputs (A) of the dual monostable circuit. It will be recalled that clock pulses will only be generated when there is a logical 0 level on the A input. Hence, stable clock pulse waveforms as shown in the oscillograms of fig.8.4 were obtained when the synchronising connections, shown in fig. 8.1 were made. The simplicity of this method of synchronisation was a further justification for the development of the dual monostable v-f converter.

The synchronisation tended to be less effective when the compression parameter (μ) was increased. The sweep waveform then had regions of high slope (i.e. high df/dt values). It is considered that the variations from one sweep period to the next were too great for synchronism to be maintained.

8.3. Tests upon the Encoder

The tests upon the encoder were of two kinds, to show:

(a) that the model was operating correctly, and

(b) that the required transfer characteristic was obtained.

8.3.1. Tests for Correct Operation

To check that the model was operating correctly, the output waveforms of the various stages were monitored, for various values of C in the p.l.m. stage.

The system shown in fig. 8.1 however, was developed from a 4-channel system, and these initial tests were made upon the earlier system. There were two other differences between the models:

(i) the frequency of the binary digit pulses were 4KHZ instead of 8KHZ;

(ii) the register output was gated by the binary digit train so that a pulse output, instead of a logic level output was obtained.

These differences may be seen in the oscillograms shown in figs. 8.3 to 8.5 inc. and comments are now made upon these observations.

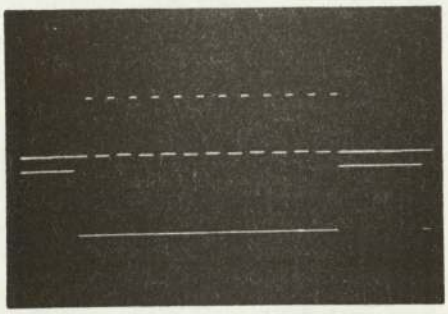
Fig. 8.3 Observation of Waveforms in a Frame.

(i) Sequencer and Binary Digit Pulse Trains.

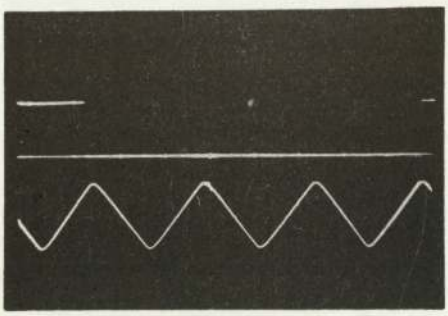
The lower trace is a four-channel sequencer (Q_1) waveform while the upper trace shows the 4KHZ binary pulses when gated by the sequencer output Q_1.

(ii) Integrator and Gated Clock Pulse Trains.

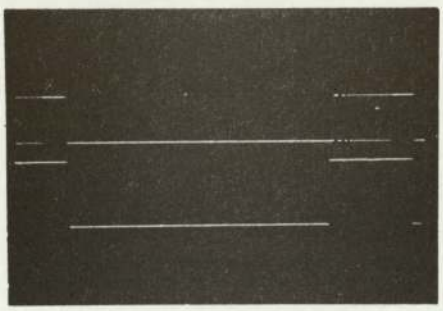
The lower trace is the triangular waveform output of the O.A. integrator, while the upper trace shows the high-frequency clock pulses after gating by the length-modulated pulses. (The value of C was set to give a pulse-length a little smaller than that from the sequencer.)



(1) 4KHz BINARY DIGIT PULSES (upper)
4 CHANNEL SEQUENCER PULSES (lower)



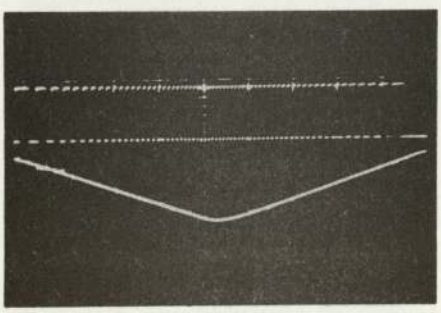
(2) GATED CLOCK PULSES (upper)
INTEGRATOR OUTPUT (lower)



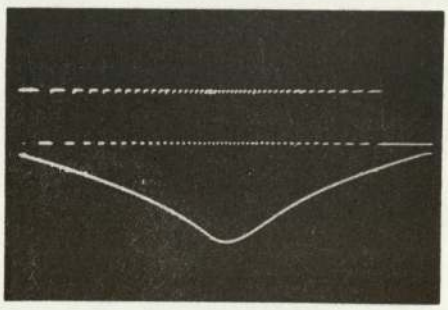
(3) COUNTER STAGE B
Q OUTPUT (upper)
4 CHANNEL SEQUENCER PULSES (lower)

FIG. 8.3 WAVEFORMS IN A FRAME

Time base setting: 500 u s cm^{-1}



(i) GATED CLOCK PULSES (upper)
FOR A TRIANGULAR SWEEP (lower)



(ii) GATED CLOCK PULSES (upper)
FOR A COMPANDED SWEEP (lower)

FIG. 8.4 WAVEFORMS IN A CHANNEL PULSE DURATION

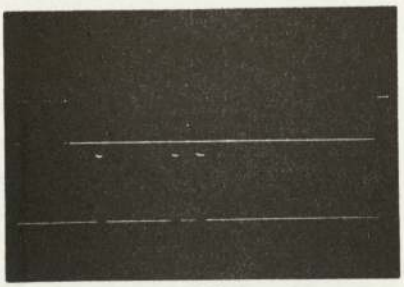
Time base setting 100 u s cm^{-1}

(iii) Sequencer and Counter Stage (B) Pulse Trains.
The lower trace is the sequencer pulse, while the upper trace is the waveform of the counter stage output, B. The time base setting (500 μS cm^{-1}), required to display one frame, does not allow visual counting of the number of pulses. It may be seen, however, that the divided clock-pulses are frequency modulated and that Q_B has a logic 1 level at the end of the channel pulse.

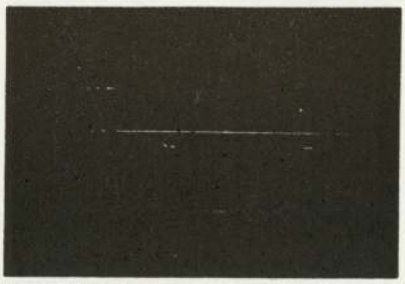
Fig. 8.4. Observation of Waveforms in the Channel Pulse Duration.

(i) The Integrator and Gated Clock Pulse Trains.
These traces are expansions of fig. 8.3 (ii) with a time-base setting of 100 μS cm^{-1}. The compandor stage has been omitted so that the integrator output, suitably inverted, (lower trace) was applied to the v-f converter. The sweep amplitude was adjusted to give a trace in which the clock pulses can be counted visually. It may be seen that in this case the clock p.r.f. was swept from 20 to about 120KHZ, giving some 60 pulses in the channel pulse duration.

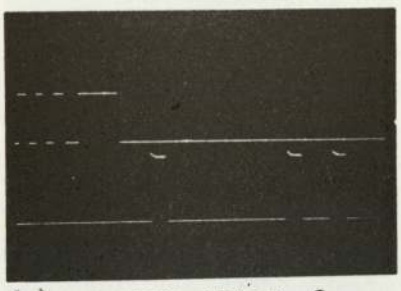
(ii) The Compandor and Gated Clock Pulse Trains.
The lower trace is the output waveform of the single-ended companding element of fig. 7.3 for a triangular input. The upper trace shows the corresponding frequency-modulated clock pulses. The sweep amplitude has again been adjusted to give a trace in which the pulses could be visually counted.



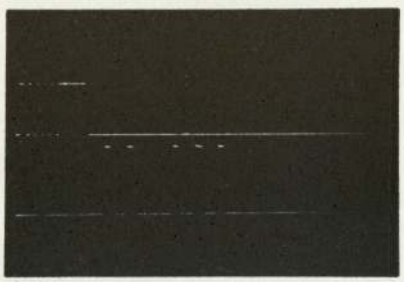
(i) GATED CLOCK AND BINARY CODE PULSES FOR 38 LEVELS



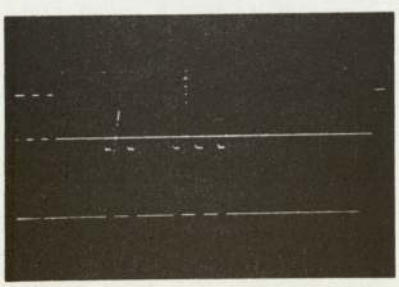
(ii) COUNTER STAGE A AND BINARY CODE PULSES FOR 38 LEVELS.



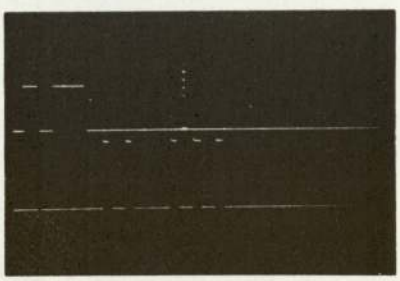
(iii) COUNTER STAGE C AND BINARY CODE PULSES FOR 38 LEVELS



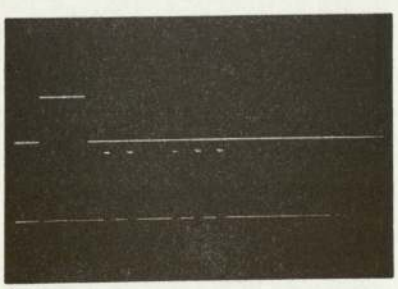
(iv) COUNTER STAGE C AND BINARY CODE PULSES FOR 55 LEVELS



(v) COUNTER STAGE D AND BINARY CODE PULSES FOR 55 LEVELS



(vi) COUNTER STAGE E AND BINARY CODE PULSES FOR 55 LEVELS



(vii) COUNTER STAGE F AND BINARY CODE PULSES FOR 55 LEVELS

FIG. 8.5 WAVEFORM IN THE COUNTER [upper traces] AND AT THE REGISTER OUTPUT [lower traces]

Time Base Setting 500 $\mu s\ cm^{-1}$ (i, iv–vii)
250 $\mu s\ cm^{-1}$ (ii, iii)

It may be noted that both sweep waveforms of fig. 8.4 (i) and (ii) exhibit rounded minima. This suggested that limiting occurred in the input circuit of the constant current transistors of the v-f converter. Nevertheless, the full range of clock frequencies 30-450KHZ could be easily obtained and it was considered that the clock pulse generation was satisfactory.

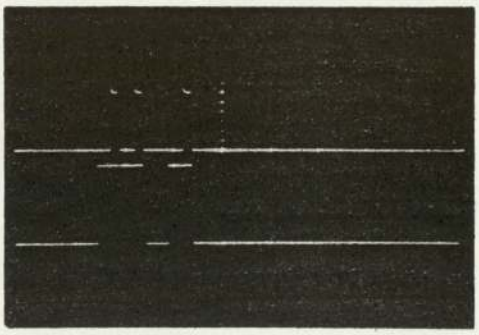
Fig. 8.5. Waveforms in the Counter.

These oscillograms show the waveforms at various stages in the counter, for two clock pulse trains, containing 38 and 55 clock pulses respectively. The number is identified in each oscillogram by the binary coded pulse group in the lower trace, which is the gated output of the register.

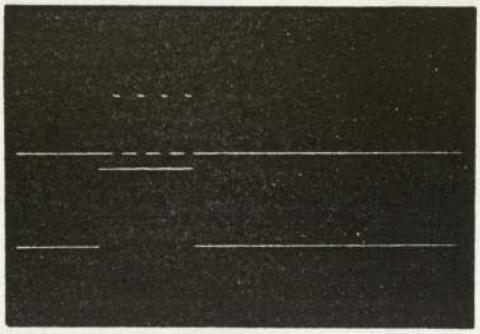
It will be noted from oscillograms (ii) and (iii) that the first 5 mm. of the sweep has not been reproduced. Hence, when account is taken of this, it will be seen that the stage waveforms (ii - vii) correspond respectively with the binary code pulse groups shown, and that therefore the counter is operating correctly.

Fig. 8.6(a) Waveforms in the Output Register.

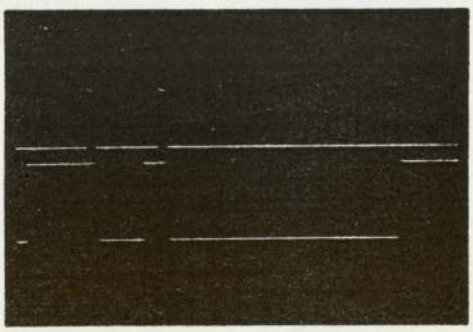
The four oscillograms (i - iv) inc. are the waveforms at the normal output (Q_U) of the register. The upper traces are the binary code pulse groups, obtained by gating the output Q_U with the gated binary train shown in fig. 8.3 (i).



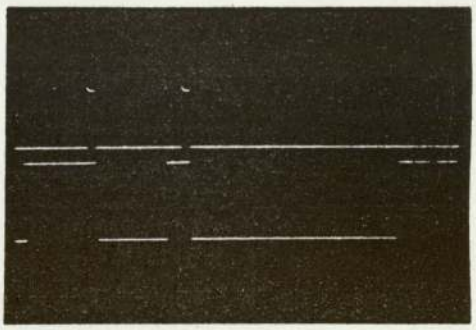
(1) 26 QUANTA



(2) 30 QUANTA



(3) 68 QUANTA



(4) 72 QUANTA

FIG. 8.6(a) WAVEFORMS IN THE OUTPUT REGISTER

BINARY CODE PULSE GROUPS (upper traces)

REGISTER OUTPUT (Qu) (lower traces)

Time base setting: 500 μs cm^{-1}

Inspection of the upper traces would suggest that the corresponding level numbers contain up to 5 digits and that they form one of the sequences:

(13, 15, 17, 18); (26, 30, 34, 36), (52, 60, 68, 72).

The choice of the sequence (26, 30, 34, 36) may be inferred if it were given that the 2^0 digits were zero in each case. In fact, the numbers were 26, 30, 68 and 72 which correspond with the Q_U waveforms, given in the lower traces.

The way in which pulses are formed in parallel entry register is shown in fig. 8.6(b). It will be seen that when a 7-digit number such as 1101101 is set into the 7 stages 0 - U, that the most significant digit is not generated in the output pulse train. It is shown, further, in fig. 8.6.(b) that an 8th binary stage (V) is required to generate a 7-digit code pulse group.

The inability to generate 7 digits does not, however, mean that numbers $>$ 63 cannot be counted. Providing that the high frequency clock pulse number is increased to just below 64 and registered, any further increases up to 127 may be registered, assuming the presence of the 2^6 "bit". Hence, the initial tests indicated that the encoder was operating correctly.

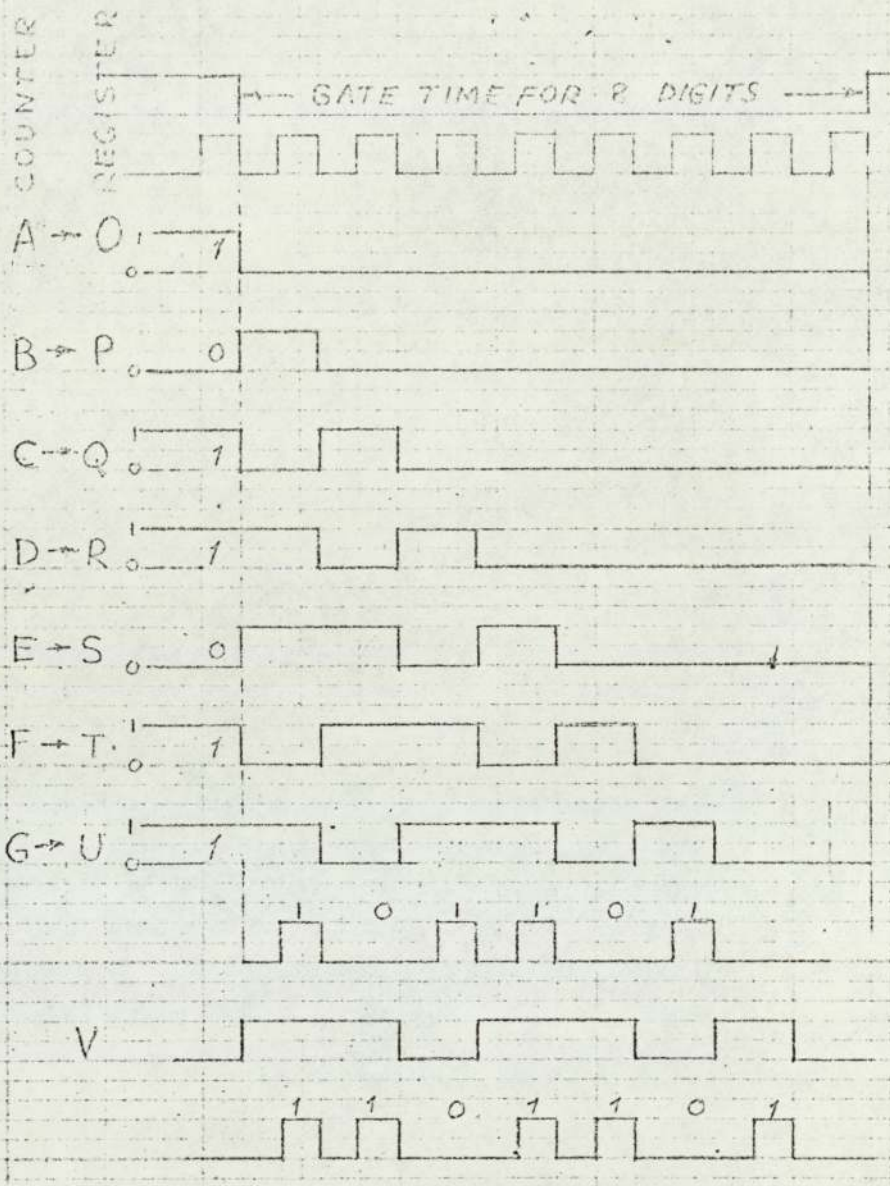


FIG 8.6(b) PULSE WAVEFORMS IN A 7-STAGE PARALLEL ENTRY REGISTER.

(note that an 8th Stage (V) is required to generate a 7-digit serial)

8.3.2 Testing the Transfer Characteristic

To determine the transfer characteristic of the encoder shown in fig.8.1, the following procedure was followed:-

(1) The values of C in the p.l.m. stage, giving minimum and maximum channel pulse lengths of 100 and 900μs respectively, were determined.

(2) The d.c. and then the a.c. levels of the waveform at the input to the v-f converter were adjusted to give:

(a) a maximum count of 100 when T = 900μs

(b) a count of 50 at T $\simeq$ 500μs.

The values of C were then increased from the minimum value, the duration of the channel pulse was measured, and the weight of the corresponding binary code observed from the register output waveform. The binary weight (or level number) was also observed from the expanded trace of the gated clock pulse. The variation of level number against channel pulse duration is shown in fig.8.7. To test the symmetry of this curve the mean level number was determined and used as origin. The numerical values of the deviation from the new origin of points on the curve are shown in fig.8.8. The two curves are the companding characteristics for positive and negative modulation signals. To test the similarity to the logarithmic characteristic given in equation (2.1), the normalised values of the theoretical characteristic were calculated and are also shown in fig.8.8. An attempt was made to increase the companding action by adjustment of d.c. and a.c. levels at the v-f converter input. There was, however, a "jitter" in the clock pulse waveform. Two further transfer characteristics were obtained for the two conditions:

(i) triangular sweep input to the v-f converter.

(ii) rectangular sweep input to the v-f converter.

The positive modulation characteristics for all three sweep input conditions are shown in fig.8.9.

8.3.3 Discussion of the Transfer Characteristics

Examination of the graphs in figs. 8.7 and 8.8 shows that the transfer characteristics are correct in shape and exhibit a good degree of symmetry. It may be seen that some experimental values do not lie on a smooth curve. This feature is to be expected since the characteristic has a staircase shape in which the height of a step is one quantum (or one clock pulse) and the width is the duration of a clock pulse. Clearly, a given pulse-number is observed throughout a time interval. Hence, the experimental values may deviate by a half-step from the smooth curve which passes through the middle of each step.

At large modulation values there appears to be less symmetry. Closer inspection, however, reveals that the pulse-number for maximum positive modulation is two fewer than that for maximum negative modulation. It is considered that this difference may be due to asymmetry in the sweep waveform (examination of the oscillogram in fig.8.4 (ii) indicates asymmetry).

It will be observed from fig.8.8 that the experimental transfer characteristic is similar to the theoretical logarithmic characteristic for $\mu = 15$. It would appear that this is the maximum amount of compression which may be given by this method. The characteristics shown in fig.8.9 are further evidence that the encoder is operating correctly. The curve for the triangular sweep input shows the inherent companding action of the Method 5 encoder. The straight line for the rectangular sweep input shows the linearity of the encoder when operating with constant frequency clock pulses.

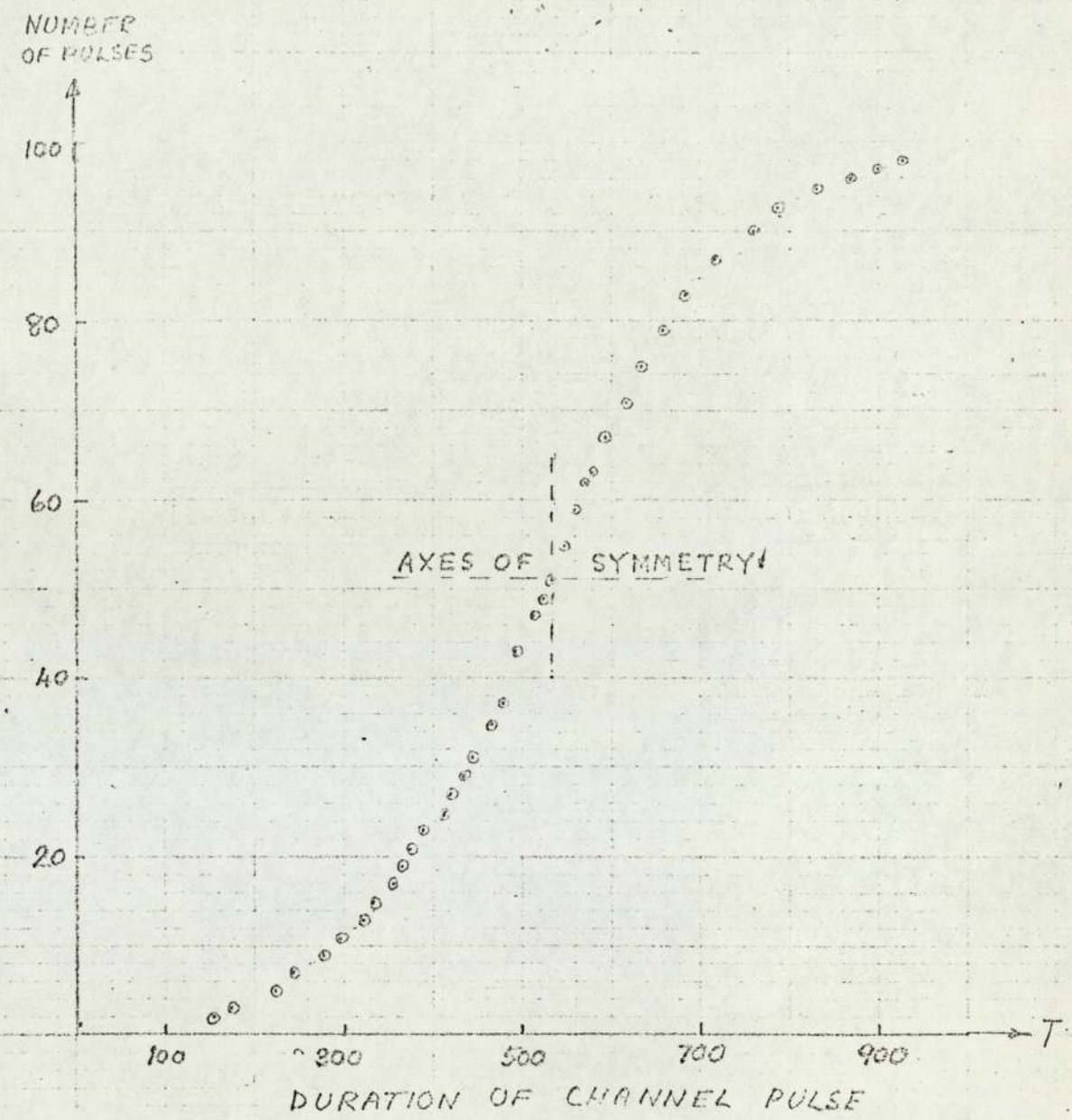


FIG. 8.7 TRANSFER CHARACTERISTIC OF THE EXPERIMENTAL ENCODER.

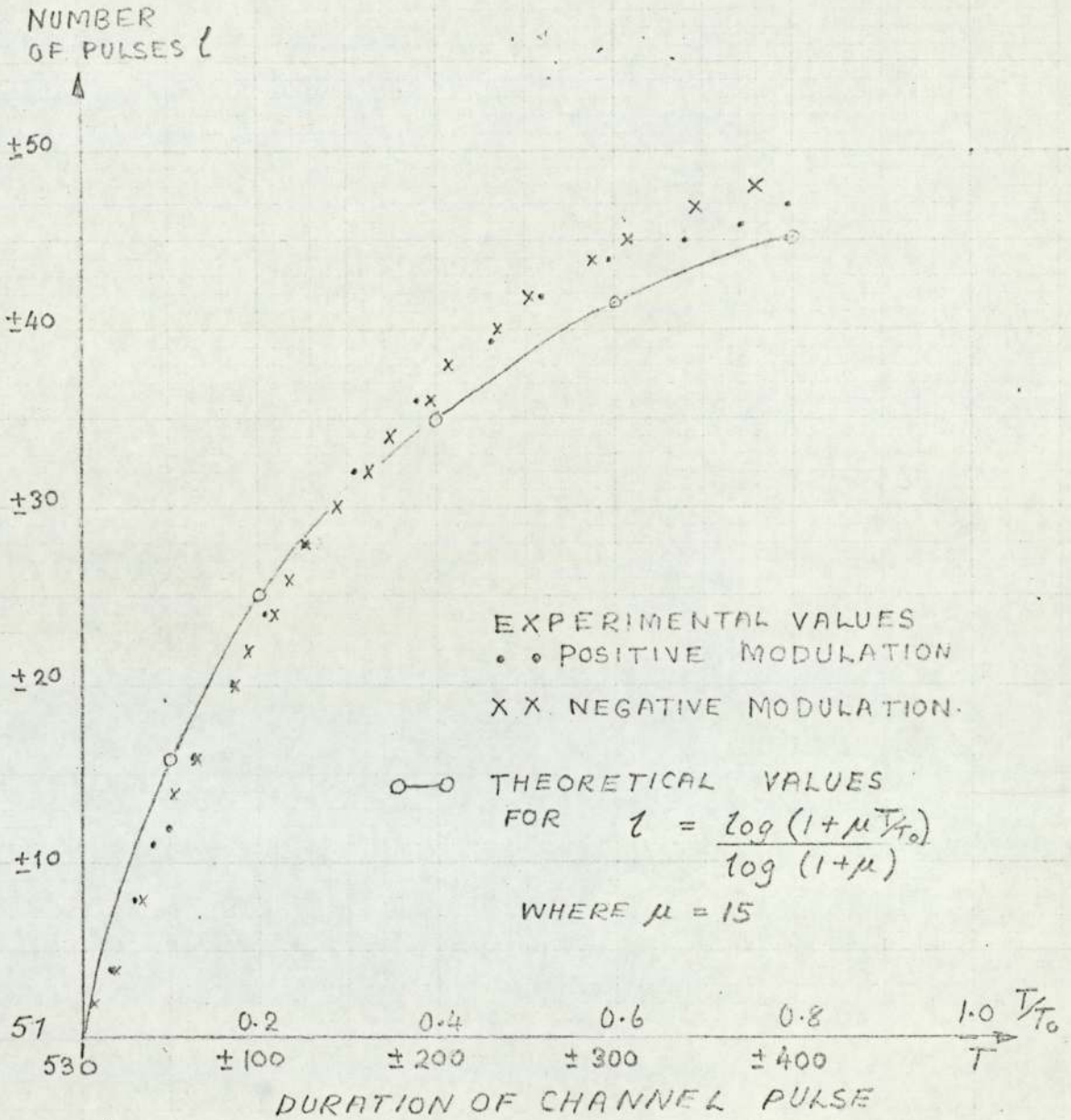


FIG. 8.8 SYMMETRY OF THE ENCODER TRANSFER CHARACTERISTIC.

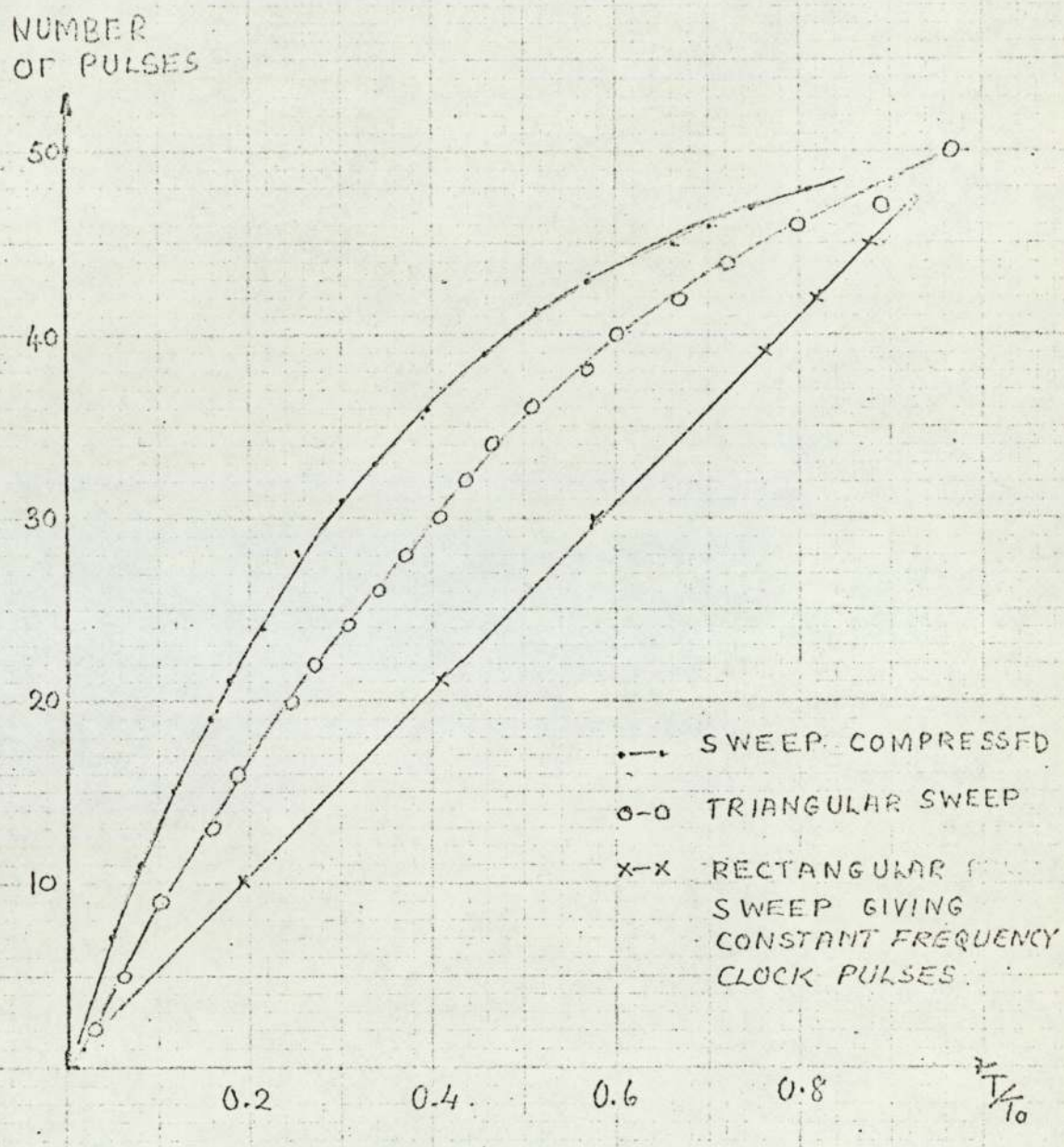


FIG 8.9 TRANSFER CHARACTERISTICS FOR THREE TYPES OF CLOCK PULSE SWEEP WAVEFORM. (POSITIVE MODULATION ONLY)

8.4 The Encoder and Decoder in Tandem

8.4.1 The Overall Test

Two tests were carried out on the overall system.

Firstly, both the encoder and decoder counters were operated from one v-f converter, and the measured pulse durations of the encoder length-modulated pulse were compared with those generated by the decoder start-stop bistable.

Secondly, the system with two independent v-f converters (as shown in fig.8.1) was tested in the same way.

The aim of the first test was to show that the decoding principle was correct. To maintain the correct encoding-transmission-decoding sequence, however, the waveform from the common v-f converter required synchronising at the commencement of channel pulses (1) and (3). This was provided by combining the sequence outputs $\overline{Q_1}$ and $\overline{Q_3}$ in an AND gate for connection to the A input on the dual monostable-astable circuit. The encoder channel pulse duration was varied in steps from 200 to 900μs and the corresponding times for which the decoder bistable was set, were measured. The results are shown graphically in fig.8.10.

The aim of the second test was to assess the effectiveness of the coding method. The arrangement shown in fig.8.1 was used. Care was taken to ensure that the two indpendent v-f converters had similar transfer characteristics. The test, outlined in the previous paragraph, was made. It was observed that the duration of the decoder output pulses were frequently subject to random variations (i.e. timing jitter), which made the results of successive tests inconsistent. The results of one set of measurements are shown graphically in fig.8.10.

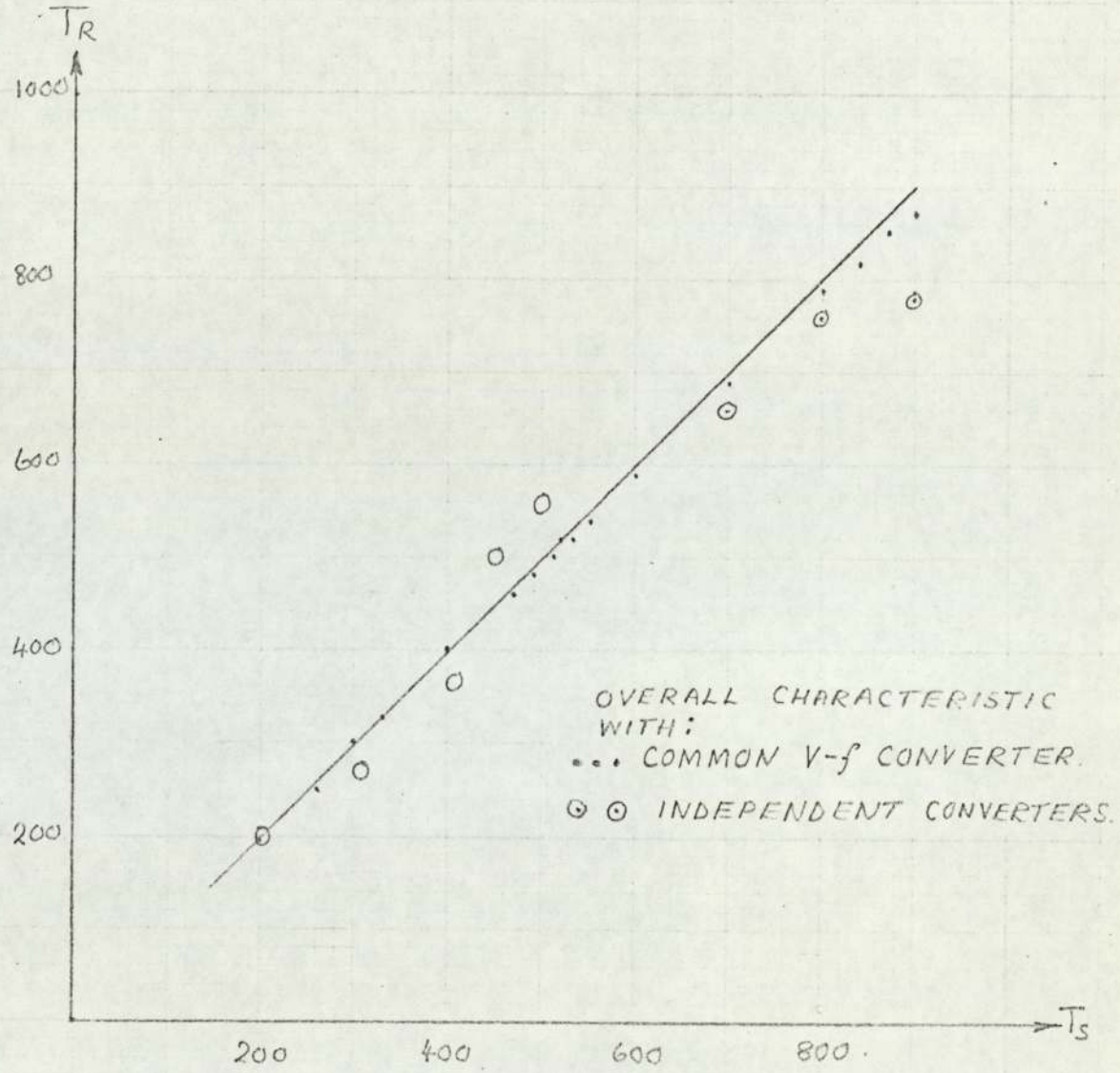


FIG. 8.10 THE OVERALL CHARACTERISTIC

8.4.2 Discussion of Results of Overall Tests

The graph in fig.8.10 indicates that, with a common v-f converter, the overall characteristic is linear to within 1%. The output and input pulse durations were not exactly equal particularly at large pulse durations. The differences, however, are about the size of a quantum step, and are not therefore considered to be significant.

The results of one test with two independent v-f converters showed a scatter of some $\pm$ 10% from the straight line obtained previously. Clearly, because of the random variations in the decoder pulse the experimental points may not be joined to form a smooth overall characteristic. The waveforms of the v-f converters were monitored to see how effectively they were synchronised when subject to a sweep voltage. When the oscilloscope time base was synchronised from the sequencer (Q_1) output, it was observed that there were irregular variations in the number of clock pulses in the sweep waveform of the decoder converter. The waveform of the encoder was stable, as in the tests upon the encoder given in 8.3. These observations were not unexpected, however, as the encoder waveform is nearer in time to the time base synchronising pulse. The first overall test results (with the common v-f converter) were consistently stable. It must, therefore, be concluded that independent v-f converters subject to a triangular sweep input, may not be easily synchronised.

8.5 Asynchronism in the Coding Model

The tendency to lose synchronisation between the channel and clock pulses has been evident during the tests. It is worthwhile now to recall the occasions when it occurred. Firstly, it tended to occur during the initial tests for synchronism upon the v-f converter (section 8.2.4), and in the test opon the transfer characteristic of one coder (section 8.3.2) when the compression was increased. Secondly, intermittent synchronisation occurred in the overall test, when independent v-f converters were used. These two aspects of asynchronism are now considered.

In the first case the synchronisation was satisfactory with sweep waveforms which gave $\mu < 15$. When the dc and ac levels at the v-f converter input were adjusted to increase the μ-value the waveform showed a large variation in df/dv (or df/dt). Under such a condition, a timing jitter was observed in the gated clock pulse waveform, that is, a tendency to lose synchronism between the channel gating and clock pulses. It should be recalled that the channel pulse controls the operation time of the dual monostable-astable circuit. When, however, there is a large variation in df/dv, there tends to be a variation in the number of clock pulses from one sweep period to the next. This is especially true if the channel pulse has a duration T in the range $T_o < T < 2T_o$. This asynchronism could be due to variations in the amplitude of the sweep between periods. It is not understood, however, how such variations are only significant when the sweep waveform has a large df/dv variation.

In the second case, loss of synchronism was evidenced by two factors:-

(a) Variations in the set time (i.e. timing jitter) of the

decoder bistable when the a steady voltage was applied at the encoder.

(b) Unstable gated clock pulse waveforms at the decoder, when the encoder and decoder waveforms were displayed together.

It was stated in the previous section (8.4.2) that this asynchronism was not unexpected, for in previous tests it had been observed that asynchronism tended to occur when the time between pulse bursts was a large part of the time base period. Further thought, however, suggests that this argument is not entirely valid. For, if the pulses from the encoder p.l.m. and decoder bistable stages have their leading edges determined by the sequencer, and if one gated clock burst is steady, then the other should also be stable. It is now considered that asynchronism was due to the instability of the decoder v-f converter when driven by a distorted triangular waveform, (even though $\neq 15$).

This tendency to asynchronism appears to be inherent to a design which has two independent v-f converters driven by such waveforms.

CHAPTER NINE

A METHOD 5 CODER WITH SEGMENTED COMPANDING

9.1 Case for a Segmented Companding Characteristic

9.2 A Method 5 Coder with Segmented Companding

9.3 Conclusion to Chapter 9

9.1 The Case for a Segmented Companding Characteristic

The results of tests upon the coding models of Chapter 8 revealed two causes for the loss of synchronism between the channel and clock pulses. Firstly, it occurred in one coder when $^{df}/_{dv}$ for one v-f converted has a large continuous variation. Secondly, it tended to occur between sending and receiving coders when two independent v-f converters were used. It was then concluded that the loss of synchronism was inevitable in a design which utilized separate v-f converters subject to continuous sweep waveforms. In this context, a continuous waveform is one which has no sharp edge; i.e. a triangular or a distorted triangular waveform is regarded as continuous.

The continuous sweep waveform is necessary, however, to give a smooth companding characteristic. A question , which must arise, is whether the application of a smooth companding characteristic is justified. The principle of amplitude quantisation does not permit the transfer characteristic to be absolutely smooth, for it will have at the most 2^n steps, where n is the number of binary digits. Indeed, as reported in Chapter 2, non-linear quantisation may be given by a few segments, with each covering a number of quantised levels. Moreover, segmented companding with four or more segments is becoming the preferred method. It is capable of greater accuracy, because it is substantially independent of the I/V characteristics of devices. The application of this type of companding may be applied to Method 5 coding, as will be shown, by arranging for the clock frequency to be varied in discrete steps. It must now be asked whether this practice can result in better synchronisation. Cattermole has recognised the advantage of what amounts to time quantisation in a system where the clock pulse is varied. In reference (33), he gives an example of a system in which the clock

frequency has two values, giving a two-segment characteristic. Furthermore, he points out that these clock frequencies may be conveniently generated from one clock pulse source. Hence, because the clock and channel p.r.f.s. could be harmonically related, synchronisation should be maintained more easily. The instrumentation principles of such a system are considered in the next section.

9.2 A Method 5 Coder with Segmented Companding

To complete the investigation of the Method 5 coder, a brief description is given of the instrumentation of a system which gives a four-segment characteristic. A block diagram of such a system is shown in fig.9.1, while the waveforms at various points in the encoder are shown in fig.9.2.

The clock pulse train is made up of "bursts" or trains of 32 pulses of each of four frequencies, obtained by division of 512 KHZ. A nine-stage binary divider is used so that a 1 KHZ channel synchronising pulse is also given. Each of the four "bursts" are obtained by gating certain of the outputs of the divider. The bursts are combined in an OR gate to produce the discretely variable frequency clock pulse train. The number of clock pulses is then 4 x 32 = 128 in the full 1ms channel pulse, 3 x 32 = 96 in 500μs, 2 x 32 = 64 in 250μs and 32 in 125μs. Hence the system would operate as a pulse-count segmented encoder. The corresponding decoder will be very nearly the reverse of the encoder.

The synchronous operation of encoder and decoder in a practical system, would require that information about the clock p.r.f. be extracted from the incoming p.c.m. This may be conveniently arranged by choosing a binary digit rate which is harmonically related to the

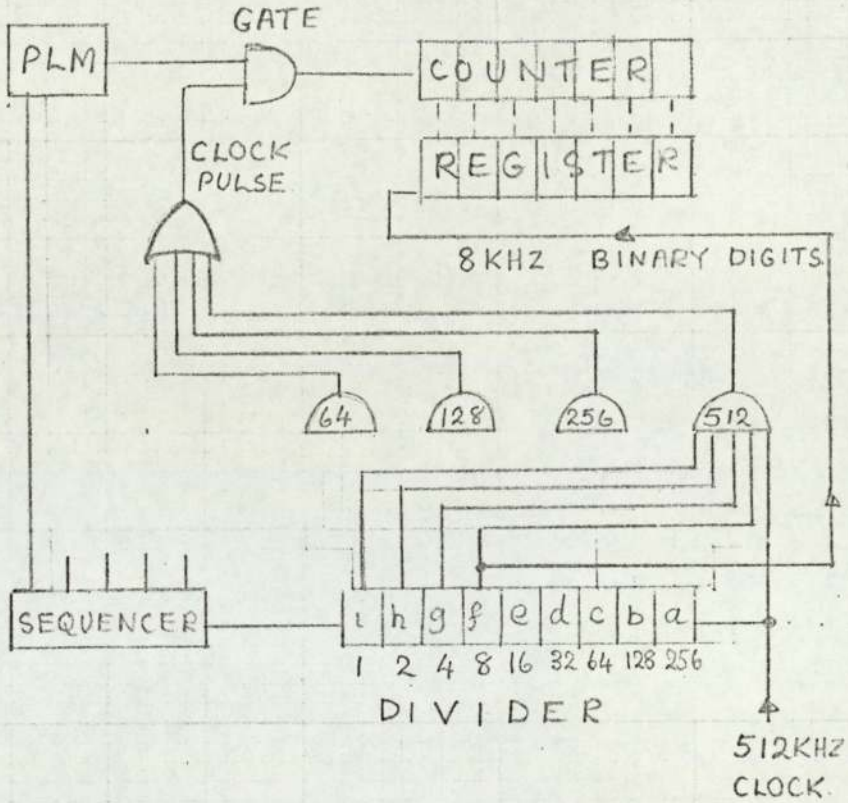


FIG 9.1 METHOD 5 ENCODER WITH 4-SEGMENT COMPANDING.

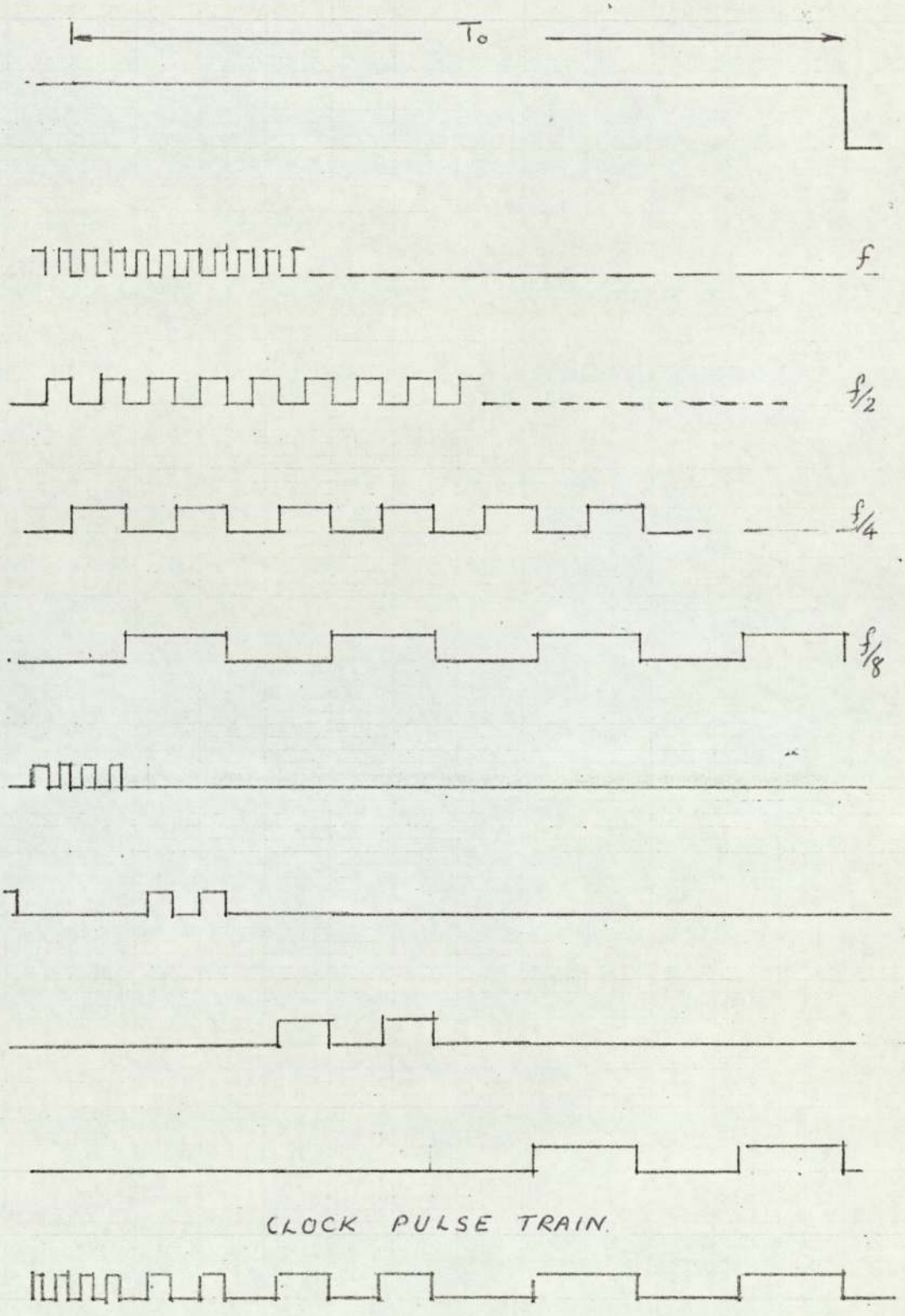


FIG 9.2 WAVEFORMS IN SEGMENTED METHOD 5 ENCODER.
(2 pulses in each of 4 trains, giving 16 levels)

clock p.r.f.

It may be seen therefore that, because the system does not use swept frequency clock pulses, and because the channel, clock and binary digit pulses are harmonically related, jitter-free operation should occur. It may also be noted that although the system contains more integrated circuits, these are, except for the p.l.m. stage, of two types only, namely binary and gate circuits. Such a system is inherently simple and capable of stable operation.

9.3 Conclusion to Chapter 9

A case for a pulse-count coder, which has a segmented companding characteristic, has been made. The instrumentation principle of a system, which gives a four-segment characteristic, has been described briefly. It has been shown that a simple and stable system may be designed.

CHAPTER TEN

CONCLUSIONS

10.1 General

10.2. Experimental Evaluation of Method 1 Coder

10.3 Experimental Evaluation of Method 5 Coder

10.4 A Segmented Method 5 Encoder

10.5 Realisability of a Method 5 Coder

10.6 Concluding Remarks

10.1 General

An investigation has been made into methods of coding, which use a binary counter, for p.c.m. It has been stated in Chapter 1 that logarithmic compression of signals is desirable to give adequate signal : error ratio at small signal levels. It has also been stated in the historical review that in the early pulse-count encoders, the compression was given by a separate stage. Moreover, in each of the three different coders, described in Chapter2 there was provision for a separate-stage compandor, if compression was required. The aim of this work therefore, has been to design a pulse-count coder in which non linear compression is incorporated.

The sequence of operations in a pulse-count coder has been described as follows:-

(i) Conversion of signal into length-modulated channel pulses.

(ii) The gating of a number of clock pulses proportional to the variable-length channel pulses.

(iii) The counting of the clock pulses and the conversion into binary code-pulse groups.

It has been shown that four methods of logarithmic compression are theoretically possible if the signal (v) is made to modulate either one, or both, of the channel pulse-length (T) and the clock pulse frequency (f) as given below:-

(1) T to be a logarithmic function of v, with f constant.

(2) f to be a logarithmic function of v, with T constant.

(3) $T \propto v$, and f to be a non-linear function of v.

(4) $f \propto v$, and T to be a non-linear function of v.

When, however, the instrumentation of these methods was

considered it was found that while the encoders for Methods (1) and (2) may be realised simply, those for Methods (3) and (4) require devices which have negative resistance characteristics. Furthermore, in all four methods the complementary decoders are extremely difficult to instrument.

The problems may be simplified considerably if the signal modulating - and companding - functions are separated. Hence a fifth method was defined as follows. The signal v linearly modulates the channel pulse duration T (as in Method (3)), and the companding function is provided by clock pulses, whose frequency is varied by an independent sweep generator. In an m-channel system the clock pulse would be swept at a frequency of $2mf_m$ where f_m is the highest modulation frequency. This apparently complex method is, in principle, more convenient to instrument than the other four methods, because the decoder is very nearly the encoder in reverse, requiring the same type of clock pulse generation.

10.2 Experimental Evaluation of the Method 1 Encoder

An experimental evaluation of the simplest of the above encoders, namely that for method 1, has been made. Since the clock p.r.f. is constant for that method, the p.l.m. stage, only, required simulation. It has been shown that a monstable multivibrator, in which the timing elements are transistors, may give a quasi-logarithmic companding characteristic. It was, however, not possible to obtain a characteristic which was sufficiently symmetrical on positive and negative modulation. Three methods were used and the one which gave the greatest degree of symmetry, is considered to be original. This method consisted in using two transistors, one of which modulated

the timing resistance, while the other, in effect, modulated the timing capacitance.

10.3 Experimental Development of the Method 5 Coder

To evaluate experimentally the fifth coding method, a model for the system was designed. To simplify both the design and the ultimate determination of the transfer characteristics, the model had the following features:-

(i) Five channels, one of which was instrumented.

(ii) A channel p.r.f. of only 200HZ.

(iii) Direct modulating voltages, only, were simulated at the p.l.m. stage by the settings of a timing capacitor.

(iv) The maximum number of steps in the companding characteristic was 127.

(v) The demodulated output from the decoder was the duration for which a bistable was set by a reversing counter.

(vi) Integrated circuits having the dual-in-line base were used.

Those stages which are common to pulse count coders generally, have been described in Chapter 5. These are the divider, sequencer, gates, binary counter, shift register and decoding bistable. The stages of clock pulse generation are, however, peculiar to the Method 5 coder, and consist of a sweep generator which feeds a linear voltage-to-frequency converter.

A detailed treatment of one type of converter has been given in Chapter 6, because it will generate a stable swept frequency wave-form from a distorted triangular sweep waveform. An integrated circuit form, based on the dual monostable-astable circuit has been developed, and it is considered to be original.

The development of the distorted triangular waveform generator has been given in Chapter 7. Two methods were considered, namely (A) a Triangular sweep method and (B) a differential sweep method. The former required a single-ended compandor only, and had one stage less than method (B) and hence the triangular sweep method was adopted. The junction f.e.t. was selected as a compandor for it has at least one advantage over the diode as a smooth companding element. That is, the f.e.t. i/v characteristic may be varied by gate bias to permit matching between encoder and decoder elements. An analysis of the companding errors for the Method 5 encoder has shown that they should be smaller than those given by an encoder using a separate stage compandor. This is because of the inherent companding given by the swept frequency method, which therefore, reduces the dependency upon the characteristic of the companding element.

The setting-up and testing of the two coders have been described in Chapter 8. It has been shown that the encoder may be operated to give a symmetrical quasi-logarithmic companding characteristic. The maximum value of the compression parameter (μ) which could be obtained was about 15, the limit being set by the loss of synchronism between the clock and channel pulses. It is considered that asynchronism was due to the large continuous variation in $^{df}/_{dv}$ with almost zero values at the low frequency end of the sweep.

Tests upon encoder and decoder when they are connected in cascade, have been made. The results show that, when the encoder and decoder v-f converters are synchronised, a linear input/output relation is obtained. It must be admitted that some difficulty was experienced in synchronising two converters which are driven by distorted triangular waveform generators even when the latter are synchronised from a common source. It is considered that this asynchronism is an inherent feature of a system containing independent v-f converters driven by distorted triangular waveforms. It is concluded therefore that the principle of coding by Method 5 has been validated. The failure to maintain synchronism is due to the limitations of the design for the model.

10.4 A Segmented Method 5 Coder

To complete the work consideration was given to a Method 5 coder in which the clock frequency varied discretely to give a four-segment companding characteristic. It has been shown that such a system is likely to be simpler in instrumentation, and to be capable of more stable operation.

10.5 Realisability of a Method 5 Coder

The evaluation of the coding principles has been made on the basis of a low frequency model. It has been stated in section 4.1.1 that the results obtained from the model are only valid if the devices used in the model, behave similarly at the higher operational frequencies. Consideration is now given to see if Method 5 coding may be applied to telephony.

In an m-channel, n-binary digit system having a maximum modulating frequency fm, the channel p.r.f. is 2.fm, and the maximum channel pulse duration is $1/2mf_m$

The maximum clock pulse frequency, using smooth companding is given by equation(3.10) :

ie $$f_{max} = \frac{\mu f_o}{\log(1+\mu)}$$

where f_o is that constant frequency which will give 2^n clock pulses in the maximum channel pulse.

i.e. $$f_o = 2^{(n+1)} m f_m$$

Assuming typical values as follows :- $n = 8$, $\mu = 15$, $f_{max} = 100\text{MHZ}$,

$$mf_m = 34{,}000$$

Hence, if the highest modulating frequency is 4 KHZ, the largest number of channels which may be accommodated is only 8 or 9.

The S-segment coder will give a similar figure, for the maximum clock frequency is given in Appendix L :-

$$f_{max} = \frac{1}{S}\left[(2^S-1).\,2^{n+1}.\,m f_m\right].$$

If $S = 4$

$$mf_m = 52{,}000$$

The segmented coder, however, may be realised more readily than one which contains a voltage-frequency converter. This advantage arises because of the lower frequencies at which IC monostables tend to operate,

10.6. Concluding Remarks.

The aims of the investigation were to consider methods of pulse count coding in which non-linear smooth companding is incorporated, and to experimentally evaluate the most convenient method. This has been done.

The performance tests upon the experimental model revealed a disadvantage which was inherent in a design for smooth companding. An alternative approach which gives a segmented companding characteristic, has been outlined. It is considered that it will not have the above disadvantage and that it may be more realisable in practice.

APPENDIX A

A.C.Measurement Methods

In the initial feasibility tests upon Method 1 coding an a.c. system of measurement was considered.

When, however, an a.c. signal modulates the duration of a pulse (the a.c. signal and pulse are derivedfrom independent sources) , a steadysingle-line trace cannot be observed on an oscilloscope screen, even though the timebase is synchronised by the pulse. The situation is shown in fig A1 where a sinewave signal is sampled at the peak value in a p.l.m. system. Because the sinewave and pulse are independent signals there will be a random variation in phase so that the pulse deviates from the time position of the sinewave peak. If the leading edge of the pulse is synchronised to the timebase, and if the modulation varies the trailing edge only, thenthe latter will be as shown in fig A1. The C.R.O. screen persistence enables observation of trailing edge for a number of samples, for which there have occurred phase variations between the pulse and sinewave. In effect, the variation of phase appears as an amplitude variation, and hence as a variation in duration T. The lack of synchronism between the modulating signal and the signal to bemodulated always prevents the observation of a steady trace in any modulation experiment. Hence, a system of measurement was designed where the channelpulses are derived from a sinusoidal modulating signal.

A block diagram of the system is given in fig.A2. while the corresponding circuit diagram is shown in fig A.3. It may be seen that the modulating signal is doubled by the diode bridge.

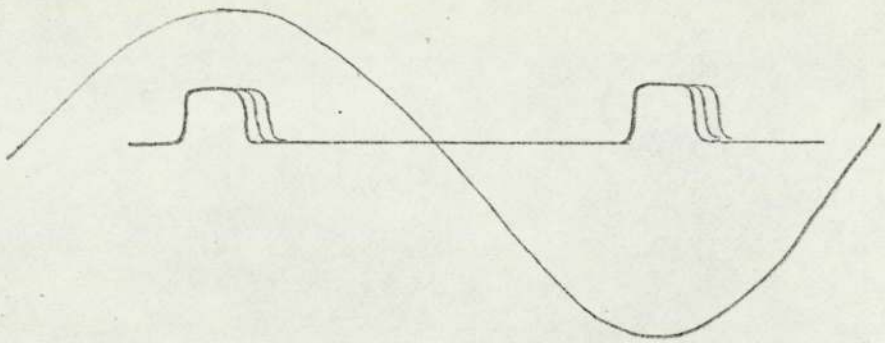


FIG. A1. ASYNCHRONISM BETWEEN MODULATING SIGNAL AND CHANNEL PULSE

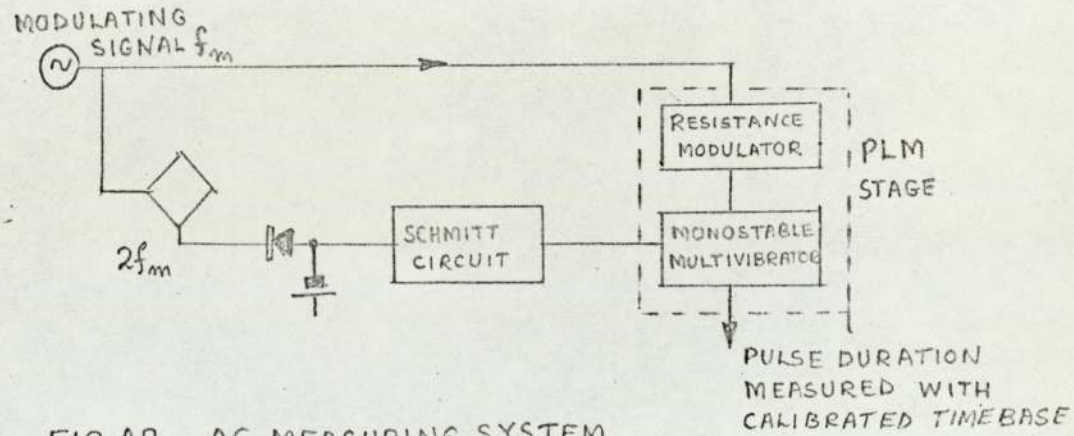


FIG. A2 AC MEASURING SYSTEM

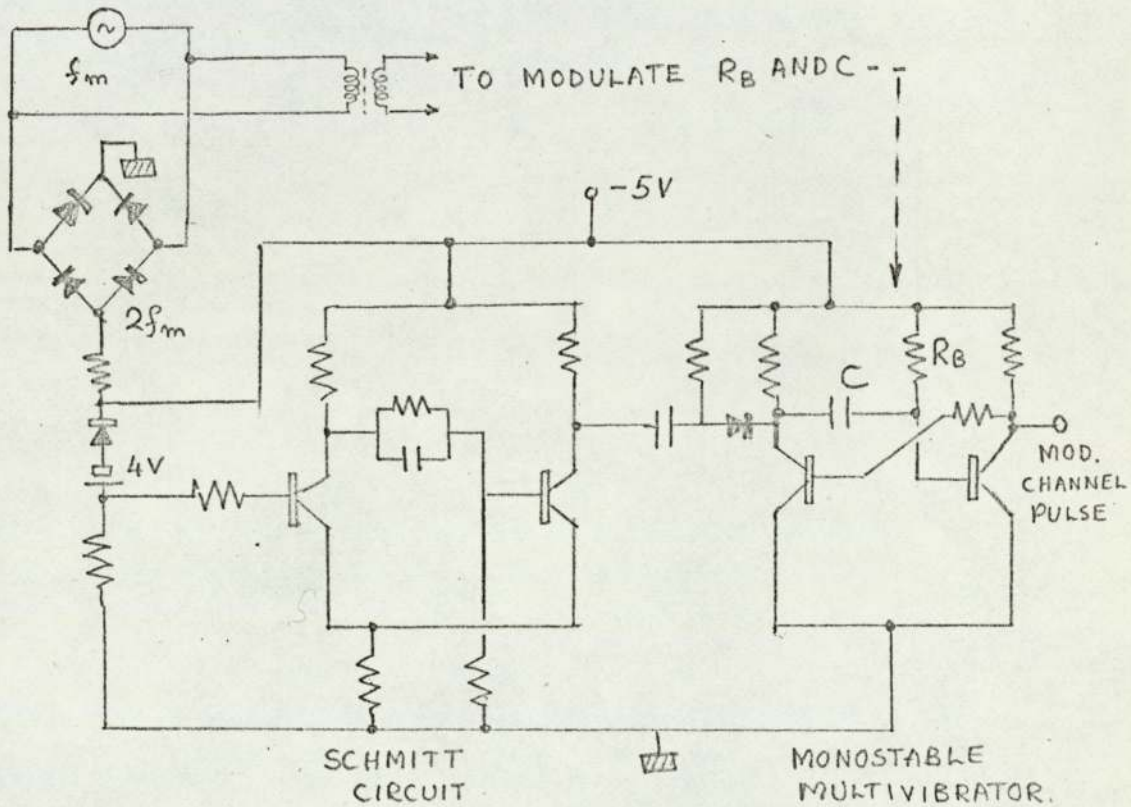


FIG A3 AC MEASURING SYSTEM.

A portion of the amplitude is then selected by the two-level diode clamp. The clamped waveform is used to synchronise a Schmitt trigger, whose output thenconsists of square waves at twice the modulating signal frequency. The square waves are differentiated, to synchronise the monostable multivibrator which forms the p.l.m. stage. Hence channel pulses are generated, having a frequency twice that of the modulating signal, with the pulses occurring near to the peak value. The modulating signal is also applied, via a transformerto the transistor resistance modulator so that the channel pulse duration depends upon the peak value of the modulating signal.

To test the companding characteristics the rms value of the modulating signal ismeasured and the corresponding value of the channel pulse duration T observed.

The initial test results compare closely with those obtained for the d.c. tests shown in figs 4.3 and 4.7. Major errors arose, however, when the channel pulse duration became comparable with the half-period of the modulating signal.

The latter difficulty could have been overcome if a sample-and-hold technique had been used. In view of the complexity, however, of the system, the method of d.c. measurement was followed.

APPENDIX B

ANALYSIS OF THE COMPOUND C R COUPLING

In the multivibrator shown in fig. C1 the capacitances C_1 and C_2 charge up via R and the base-emitter resistance of transistor T_2. During the quasi-stable state C_1 and C_2 discharge towards V_{cc} through R_1 and the collector-emitter resistance of T_1. The following analysis shows how the pulse duration varies with C_1, C_2, R_1 and R_2.

The Charging Process

It may be reasoned that the smaller capacitance C_2, charges quickly to some maximum value, and then discharges through R_2. C_1 charges more slowly, finally acquires the charge of C_2. Hence for most of the normal state of the multivibrator, Ucl - Vcc., and $V_{c2} = 0$

The Discharge Process

Let i_1 and i_2 be the currents in R_1 and R_2 respectively.

Application of Kirchoffs Voltage Law to fig.C1 gives:-

$$V_{cc} = i R_1 + \frac{1}{C_1}\int i_1\,dt + \frac{1}{C_2}\int (i_1 - i_2)\,dt$$

$$= i R_1 + \left(\frac{1}{C_1} + \frac{1}{C_2}\right)\int i\,dt - \frac{1}{C_2 R_2}\int\left[V_{cc} - iR_1 - \frac{1}{C_1}\int i\,dt\right]dt.$$

Differentiate twice w.r.t. t to eliminate integrals, and let $p = \partial/\partial t$, this results in:

$$0 = \left[p^2 + \left(\frac{1}{C_1R_1} + \frac{1}{C_2R_1} + \frac{1}{C_2R_2}\right)p + \frac{1}{C_1C_2R_1R_2}\right] i \qquad ---(4.6)$$

The general solution equation (4.6) is :-

$$i = A \exp(-\alpha_1 t) + B \exp(-\alpha_2 t)$$

where α_1 and α_2 are the roots of the p-quadratic in equation (4.6), and A and B are the integration constants determinable from the initial conditions.

The expressions for α_1 and α_2 may be simplified if

$$\left[\frac{1}{C_2}\left(\frac{1}{R_1} + \frac{1}{R_2}\right) + \frac{1}{C_1R_1}\right]^2 \gg \frac{4}{C_1C_2R_1R_2}$$

Let $n = C_1/C_2$, $m = R_2/R_1$

$$\alpha_1 \text{ or } \alpha_2 = -\frac{1}{2C_2R_1}\left(\frac{1}{n}+1+\frac{1}{m}\right) \pm \frac{1}{2}\sqrt{\left(\frac{1}{n}+1+\frac{1}{m}\right)^2 - \frac{4}{mn}}$$

i.e. $\alpha_1 \simeq -\frac{1}{C_2R_1}\left(\frac{1}{n}+1+\frac{1}{m}\right)$.

i.e. $\alpha_2 \simeq \frac{1}{C_2R_1}\left(\frac{1}{m+n+mn}\right)$

The initial conditions are that :-

(a) at $t=0$, $v_{c2} \simeq 0$, $v_{c1} = V_{cc}$

$$i = 2V_{cc}/R_1 = A + B$$

(b) at $t=0$, C_1 and C_2 are being charged in series

$$\therefore \quad di/dt = -\frac{2V_{cc}}{R_1^2}\left(\frac{1}{C_1}+\frac{1}{C_2}\right)$$

$$= -\frac{2V_{cc}}{R_1.C_2R_1}\left(\frac{1}{n}+1\right)$$

i.e $$-\frac{2V_{cc}}{R_1.C_2R_1}\left(\frac{1}{n}+1\right) = \alpha_1 A + \alpha_2 B$$

$$\frac{2V_{cc}}{R_1}\left(\frac{1}{n}+1\right) = \left(\frac{1}{n}+1+\frac{1}{m}\right)A + \left(\frac{1}{m+n+mn}\right)B$$

substituting $2V_{cc}/R_1$ from (a)

Hence $$B = 2V_{cc}/R_1\, m(\alpha_1-\alpha_2)$$

$$A = \frac{2V_{cc}}{R_1}\left[1 - \frac{1}{m(\alpha_1-\alpha_2)}\right]$$

APPENDIX C

The duration of the quasi-stable state for the monostable multivibrator with compound C R coupling, is given by the solution of equation (4.8):-

$$V_{cc} - i R_1 = 0 \qquad \text{----------(4.8)}$$

where i is given by equation (4.7) of Appendix.

$$\text{i.e.} \quad 1 = \frac{2}{m(\alpha_1 - \alpha_2)} \cdot \exp(-\alpha_2 t) + \left(2 - \frac{2}{m(\alpha_1 - \alpha_2)}\right) \exp(-\alpha_1 t)$$

Values of t which satisfied the above equation were computed, for values of m ranging from 0.1 to 10 and values of n from 1 to 25. The resulting values of t/C_1R_1 are tabulated below.

m	VALUES OF t/C_1R_1 for n-VALUES					
	n=1	n=2	n=3	n-5	n=12	n=25
0.1	0.7	0.68	0.676	.667	.663	.66
0.2	0.66	.64	.633	.625	.62	.616
0.3	0.596	.575	.573	.569	.563	.56
0.4	0.544	.5	.5	.5	.5	.5
0.5	0.51	.443	.424	.422	.422	.43
0.6	.48	.4	.368	.341	.349	.352
0.7	.46	.366	.329	.274	.262	.268
0.8	.445	.343	.288	.232	.177	.178
0.9	.434	.327	.268	.206	.129	.094
1	.425	.315	.255	.19	.107	.063
1.11		.305	.244		.094	
1.25		.295	.233		.084	
1.43		.265	.225		.078	
1.667		.276	.214		.073	
2	.385	.268	.217	.142	.0675	.035
2.5		.26	.2		.0645	
3	.372			.132		.0314
3.33		.25	.192		.0612	
4	.366			.127		
5	.362	.245	.185	.125	.058	.029
10	.354	.237	.178	.12	.056	.028

APPENDIX D

To show how the channel resistance (r) of a junction fet varies with drain current (i) and gate-source voltage (Vg), consider fig. D., with $V = 0$.

As Vg is increased, the channel width 2w decreases with the increase in width of the depletion regions.

Consider fig D, with $Vg = 0$, and with a large series resistance R_1 to maintain a current (i) which is independent of r.

The channel will show an approximate linear taper, for thepotential difference from source to drain progressively increases the bias between gate and source.

It is required to find an expression for the resistance (r) in terms of i and Vg.

The thickness (d) of the depletion region depends upon the effective p.d. (v) between gate and source. This dependence for a reverse-biased p.n. junction has been given [36] as $d = a\sqrt{V}$

It may be reasoned that in a f.e.t. $V = ir + Vg$.

Assuming a cylindrical geometry, the resistance r is then given by :-

$$r = \frac{4\rho b}{\pi (W_1 - a\sqrt{V})^2} = \frac{4\rho b}{\pi W_1^2 (1 - a\sqrt{V}/W_1)^2}$$

ρ = resistivity, b = length, W_1 = maximum width

APPENDIX D

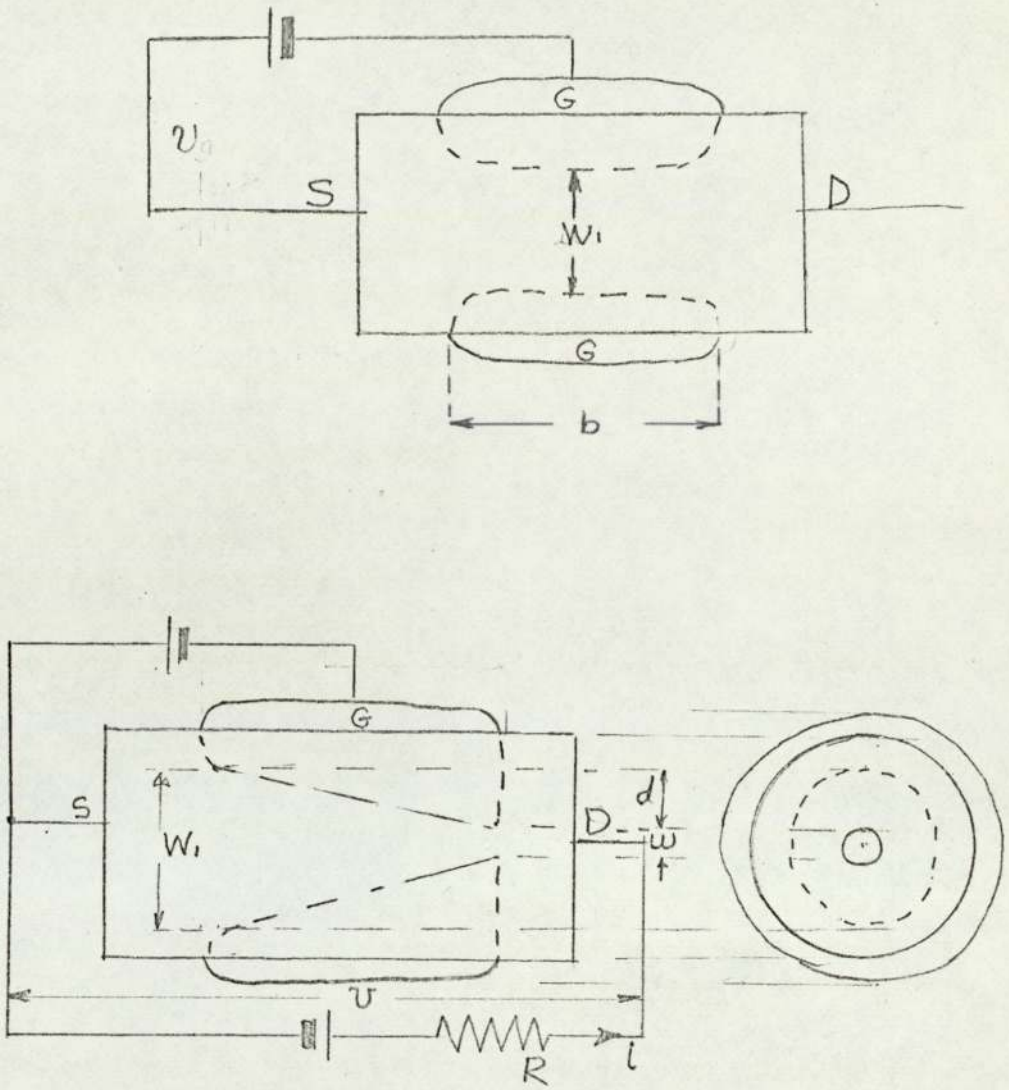


FIG.D THE JUNCTION FET

The initial resistance (r_o) when V = 0 is then $\frac{4\rho b}{\pi W_1^2}$

i.e. $$\frac{r_o}{(1 + \frac{a}{W_1}\sqrt{V})^2}$$

The drain resistance (Rp) when ir = pinch off (Vp), and when Vg = 0 , is approximately 3 r_o for the f.e.t. s tested.

i.e. $$0.33 = (1 - \frac{a}{W_1}\sqrt{V_p})^2$$

and $$a/W_1 = 0.425/\sqrt{V_p}$$

i.e. $$r = \frac{r_o}{[1 - 0.425\sqrt{V/V_p}]^2}$$

Hence $$\frac{R_p}{r} = 3\left[1 - 0.425\sqrt{(ir + v_g)/V_p}\right] \quad \text{--------(D)}$$

This equation is difficult to analyse for the dependent variable is on both sides. The term (ir) is the drain voltage (V) however, and when this is substituted, equation (7.18) results.

Hence it may be seen that the conductance is a function of $\sqrt{V + Vg}$. This function is similar to that derived from the Shockley equation and given in equation (7.17). Both functions are shown in fig. 7.11.

It may be noted that equation 7.18 correctly predicts that the initial conductance (i.e. when V= 0) will depend upon Vg. This dependence, which may be noted in the experimental results in Appendix J, is not given by the "shockley" equation.

To account for the difference between two f.e.t. s operating under the same conditions, the coefficient of V in the surd may be written in the form (1 + σ), where σ represents the departure from the ideal characteristic.

That is, the contribution from the drain voltage V to the depletion region width may be assumed to vary from one f.e.t to another. Hence, the compensation by adjustment of gate bias may be explained.

The Shockley-derived formula represents the behaviour of the f.e.t more accurately, but a similar correction may be applied. The departure from the ideal characteristic may be represented by writing $(1 + \sigma)V$ for V.

The matching of compressor and expander may be explained by supposing that the conductance of the compressor at Vg = 0 is given by:-

$$\frac{R_p}{r_c} = \left[3\sqrt{V/V_p} - 2(V/V_p)^{1.5}(1+\sigma)^{1.5}\right]\frac{V_p}{V} = \left[3 - 2\sqrt{V/V_p}\,(1+\sigma)^{1.5}\right]$$

The conductance of the expander is then assumed to be ideal and given by :-

$$\frac{R_p}{r_e} = 3 - 2\sqrt{V/V_p}\left[(1+V_g/V)^{1.5} - (V_g/V)^{1.5}\right]$$

APPENDIX E

Emitter - follower connection.

Transconductance independent of parameters

A bipolar transistor in common emitter configuration, with a collector load resistance R_L, will have a collector current given by:-

$$I_c = h_{fe}/(1 + h_{oe} R_L) \qquad \text{(E1)}$$

where h_{fe} and h_{oe} are hybrid parameters for current gain and output resistance respectively. Equation (E1) is only approximately true under large signal conditions, but nevertheless, shows the dependance upon the transistor parameters. The parameters tend to vary with current and in particular h_{oe} tends to decrease for higher collector currents.

The transconductance $\frac{\partial i_c}{\partial v_i}$ of the transistor with its load R_L is then given by :-

$$g_m' = I_c/V_i = \frac{h_{fe}/h_{ie}}{1 + h_{oe} R_L} = h_{fe}'/h_{ie}$$

When an emitter resistor Re is used to replace R_L the input resistance is very much greater than h_{ie} so that :-

$$g_m' = I_e/V_i = \frac{(1 + h_{fe}')}{h_{ie} + (1 + h_{fe}')Re} \simeq \frac{1}{Re}$$

Hence the transconductance is independent of h_{fe}' and therefore of h_{oe}.

APPENDIX F

Effect of Reverse Leakage current and junction voltages upon pulse duration.

In the linear V - f converter the pulse duration is given approximately by the time taken for a linear discharge of a capacitance charged to the supply voltage Vcc.

It may be seen, however, from figs 6.4 and 6.6, that the duration will be modified by the saturation values of the junction voltages of T1 and T2 (i.e. by V_{CES} and V_{BES}), by the cut-in value of base-emitter voltage (V_γ) and by the reverse base leakage current I_{CBO}

A more exact analysis may be made by noting :-

(i) C charges to $V_{cc} - V_{BES}$

(ii) C discharged by twoconstant components :

$h_{fb} V_1/R_e \simeq V_1/R_e$ and I_{CBO}

(iii) C discharges to $-(V_\gamma - V_{CES})$

In a linear discharge $i_c T = C v_c$

Hence $C(V_{cc} - V_{BES} + [V_\gamma - V_{CES}]) = (I_{CBO} + V_1/R_e) T$

and equation (6.3) results :-

$$T = \frac{(V_{cc} - V_{BES} - V_{CES} + V_\gamma) C R_e}{I_{CBO} R_e + V_1} \quad \text{---(6.3)}$$

APPENDIX G

The clamping levels of the differential source-coupled clipper.

The limits of the transfer characteristic of fig.7.7 may be calculated with reference to fig. 7.6, by noting that :-

(1) The "lower" limit is set by Q_B being cut-off, and hence giving an output: V_{DD}

(2) The "upper" limit is set by Q_A being cut-off, so that the gate-source voltage of Q_B (v_{g2}) is $i_2 R_S$. This gives an output of $V_{DD} - i_2 R_D$

Hence the difference in the clamping levels $= i_2 R_D$

An expression for i_2 may be obtained from equation (4.9) as follows :-

$$i_2 = I_P (1 - v_{g2}/V_P)^{1.5}$$

$$= I_P (1 - i_2 R_S / V_P)^{1.5}$$

Now, $i_2 R_S \ll V_P$ and $V_P / I_P = R_P$,

Where R_P is the resistance of the f.e.t. drain-source channel when $v_{g2} = 0$ and $v = V_P$; i.e $i_2 (1 + 1.5 R_S / R_P) = I_P$

$$\therefore \; i_2 R_D = \frac{I_P R_D}{1 + 1.5 R_S / R_P}$$

The experimental values were $I_P = 10 mA$, $R_D = 3.9 K\Omega$

giving a voltage $\dfrac{10 \times 3.9}{1 + 1.5 \times 15/0.3} \simeq 0.5 V.$

i.e $i_2 R_D \simeq 0.5 V$

APPENDIX H

Integration of the "Shockley" f.e.t. equation (7.11)

The current/voltage characteristic of a junction f.e.t. with zero gate-bias is represented closely by the equation:

$$I = 3V - 2V^{1.5}$$

where I is the normalised drain current ($= i/I_p$), and V is the normalised drain voltage ($= v/V_p$).

To predict the companding characteristic which will be obtained when a f.e.t. is current-driven in a Method 5 coder, the $\int V dI$ is required. It is to be noted, however, that if the lower limit of integration is zero, the resulting compression curve will be that for negative modulation.

The normal compression curve may be arranged in the first quadrant by -

(i) inserting lower and upper limits of I and 1 respectively and (ii) making the abscissa $(1 - I)$

The Shockley equation, however, gives I as a function of V. To determine the $\int V dI$, the expression may be rearranged as follows:-

$$\int_I^1 V.dI = \int_V^1 V.\left(\frac{dI}{dV}\right).dV$$

$$= \int_V^1 3(V - V^{1.5}).dV = 0.3\left[1 - V^2(5 - 4\sqrt{V}\right]$$

The term within the square bracket has been calculated for various values of V from 0.1 to 0.8, and its variation with the corresponding values of $(1 - I)$ has been given in fig. 7.10.

Evaluation of $\left[1 - V^2 (5 - 4\sqrt{V})\right]$ and (1 - I) values.

V	0.1	0.2	0.4	0.5	0.6	0.7	0.8
3V	0.3	0.6	1.2	1.5	1.8	2.1	2.4
$\sqrt{V}$	0.316	0.447	0.632	0.707	0.773	0.837	0.894
$V^{3/2}$	0.032	0.089	0.253	0.353	0.465	0.585	0.712
$2V^{3/2}$	0.063	0.179	0.506	0.707	0.93	0.17	1.42
I	0.231	0.421	0.694	0.793	0.87	0.93	0.98
$1.2\sqrt{V}$	0.38	0.537	0.76	0.846	0.93	1	1.07
$1.5 - 1.2\sqrt{V}$	1.12	0.963	0.74	0.654	0.57	0.5	0.43
V^2	0.01	0.04	0.16	0.25	0.36	0.49	0.64
$V(1.5 - 1.2\sqrt{V})$	0.011	0.038	0.118	0.164	0.205	0.245	0.275
INTEGRAL	0.289	0.262	0.182	0.136	0.095	0.055	0.025
$3.3\int$	0.967	0.875	0.608	0.455	0.317	0.183	0.083
			RELATIVE COMPRESSED OUTPUT				
1 - I	0.763	0.579	0.306	0.207	0.13	0.07	0.024
			RELATIVE INPUT				

APPENDIX I

The following paper (Reference 39) was published in I.E.E. Letters, 28th May 1970, and is submitted as Appendix I.

COMPANDING WITH JUNCTION F.E.T.

Indexing terms: Compandors, Field-effect transistors

As companding elements, field-effect transistors have advantages over p-n diodes; they have suitably shaped i/v characteristics which are controllable by gate bias. Tests show that a departure from linearity of compressor and expander in cascade can be corrected to have an error of less than 1%.

Compression of signal amplitudes at the sending end and their corresponding expansion at the receiver is carried out in some telephony systems to limit the range of amplitudes in transmission. The overall process is known as 'companding', and is used to maintain adequate signal/noise ratios at low signal levels. There are two types of companding: 'syllabic' and 'instantaneous.'[1] The latter is the subject of this letter.

It has been shown[2] that, for some systems, a logarithmic companding characteristic is desirable, and that if v and u are, respectively, the normalised input and output (compressed) amplitudes, u is given by

$$u = \frac{\log (1 + \mu v)}{\log (1 + \mu)} \quad \ldots\ldots\ldots\ldots\ldots\ldots \quad (I.1)$$

In this expression μ is the compression parameter (usually having a value between 5 and 100) and gives the degree of companding. The companding characteristic given by eqn. I1 is shown in Fig. I1.
In those analogue systems where the signal amplitude is compressed directly, a balanced compandor is used to compress positive and negative half-cycles equally. In this letter only the principle is of interest, and only companding on positive-going signals is considered.

Clearly, the curved transfer characteristic of the compressor causes considerable harmonic distortion of the signal. To remove this distortion from the received signal, the expander must have a characteristic which is the inverse of that of the compressor. Hence, to serve as a companding element, the device must not only have a particular shape of characteristic, but this characteristic must be reproducible. Thus, either all devices of the same type must have the same characteristic, or the characteristic must be controllable to allow matching of the expander to the compressor.

The p-n junction diode has an approximate logarithmic current/voltage characteristic, and this has been a much used companding element.[3] The variation in characteristics (i.e. spreads) among devices of the same type, however, has been a serious disadvantage, and has led to the development of special gold-doped diodes.[4] The authors consider that there are at least three further factors which limit the usefulness of diodes as companding elements:

(i) The i/v characteristic of a 2-terminal device cannot be conveniently varied by external bias; therefore the compression parameter cannot be readily controlled.

(ii) The small range of junction voltages ($\sim$ 700 mV for silicon) required to give a change of current from maximum to minimum implies precise control of voltage at the expander.

(iii) The forward-biased junction is temperature sensitive for $\log i \propto V/T$. This suggests that temperature control is desirable to maintain matching of characteristics at the sender and the receiver.

The junction field-effect transistor (f.e.t.) is a 3-terminal device with a similar i/v characteristic, which is also temperature sensitive and which exhibits spreads. It will be seen, however, that these disadvantages may be more easily overcome with f.e.t.s, and that they may be more accurate companding elements.

The junction f.e.t. consists of a lightly doped silicon channel whose ends are called the source S and drain D, and whose resistance may be varied by a bias voltage applied between a gate electrode G and the source. The variation of drain current I with drain-source voltage V is shown in Fig. I2, and it will be noted that the initial range of the characteristic is similar to the characteristics shown in Fig. I1. An indication of the spread in characteristics may be obtained from Fig. I2 by noting that two units of the same type, giving the same values of I/V, may have gate voltages differing by 0.5 V.

The circuits shown in Figs. I3 and I4 were used as a compressor and an expander, respectively. The resistances R_2 and R_1 have such values that the compressor output follows the drain current, while the expander output follows the drain voltage. The two circuits thus have inverse transfer characteristics, and when they are cascaded the final output should vary linearly with the original input. The fractional departure from linearity is the companding error. To determine this error, the null method of measurement shown in Fig. I5 was developed. A direct voltage was applied to the input of the expander and compressor connected in cascade. The expander preceded the compressor (the reverse order occurs in practice) to enable the elements to be current- and voltage-driven, respectively. The output voltage of each was compared with the input voltage using d.c. potentiometers. The error in measurement was estimated to be less than $\pm$ 0.05 %. This was considerably better than could be achieved using a.c. signals and a wave analyser, or using direct voltages measured on analogue or digital voltmeters.

The measured characteristics of the compressor and expander approximated to the law given by eq.I1 for $\mu = 15$. The overall performance of the expander and compressor in cascade (i.e. the companding error) is shown in Fig. I6.

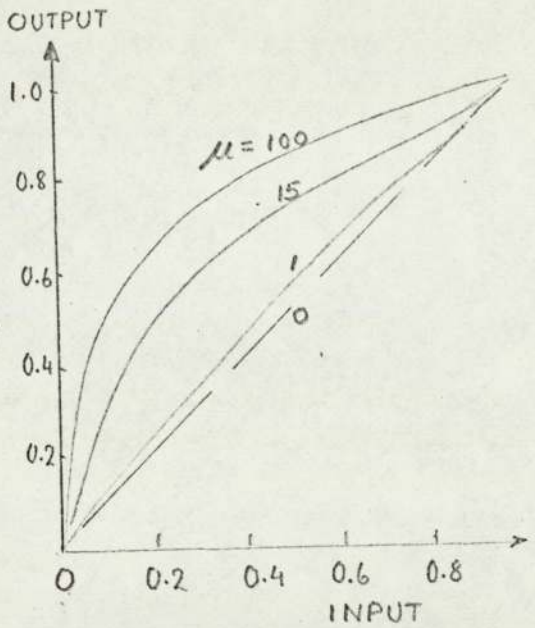


FIG. I.1 LOGARITHMIC COMPRESSION CHARACTERISTIC

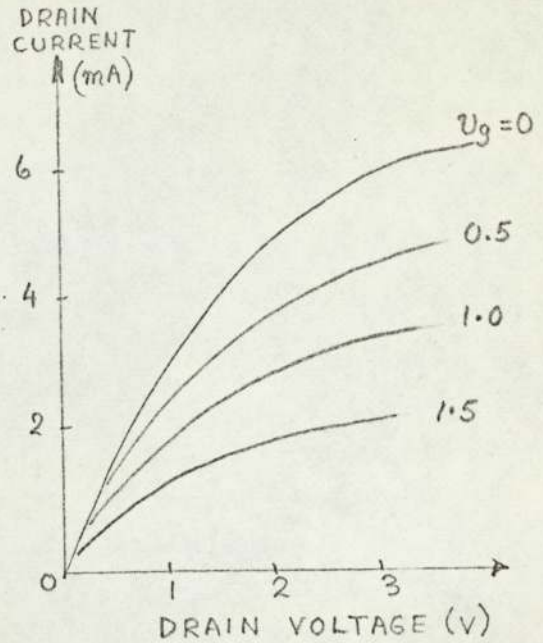


FIG. I.2. DRAIN CHARACTERISTIC OF A JUNCTION FET.

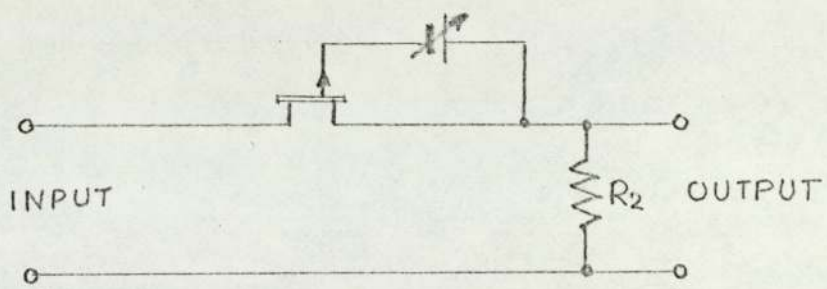


FIG I3. COMPRESSOR.

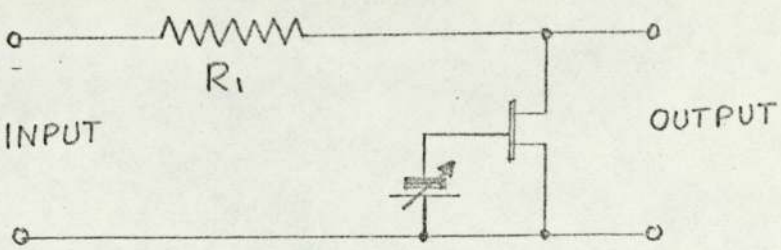


FIG I.4 EXPANDER.

To explain these results consider the overall voltage ratio. This is given by

$$\frac{v_1}{v_2} = 1 + \frac{R_1}{r_e} + \frac{r_e}{R_2} + \frac{r_c R_1}{r_e R_2} \quad \ldots\ldots\ldots \quad (I\,2)$$

Here r_e and r_c are, respectively, the resistances of expander and compressor. The second and third terms are relatively small (~ 50), while the term $r_c R_1/(r_e R_2)$ is large (~ 1000). We are concerned with the variation in v_1/v_2 as v_1 is varied. As v_1 increases, both r_e and r_c increase, causing variations in the three terms. The test showed that the ratio $r_c/r_e = m$ remained remarkably constant when the drain voltages were varied over a 2.5V range and when m had values in the range 1-0.7 Nevertheless a small variation in m can cause a significant variation in v_1/v_2, resulting in a companding error which may not be predictable. The errors due to the other two terms, however, may be predicted and controlled. If m were constant, the fractional error in v_1/v_2 due to a change of f.e.t. resistance r_e may be shown to be given by

$$\left(\frac{r_e}{R_1} - \frac{R_2}{m r_e}\right) \cdot \frac{\delta r_e}{r_e}$$

i.e. the overall error is the difference of two larger errors. Hence the net effect of these two error components may clearly be reduced by increasing R_1 and decreasing R_2, thus fulfilling the respective requirements for current- and voltage-driving. The total error then is the algebraic sum of three errors of the same order.

To show the variation of the total companding error, values of v_1/v_2 were measured for four values of v_1 and six values of v_{gc} (v_{ge} held constant at 0.6V). By noting the values of R_a, R_b, R_1, R_2 etc. (see Fig.I5) the corresponding values of r_e and r_c were obtained. The error in v_1/v_2 was expressed as the fractional departure from the value when the normalised input was 0.2. Hence measured values of this fractional error, together with values calculated from eqn. 2, were plotted in Fig. I6.

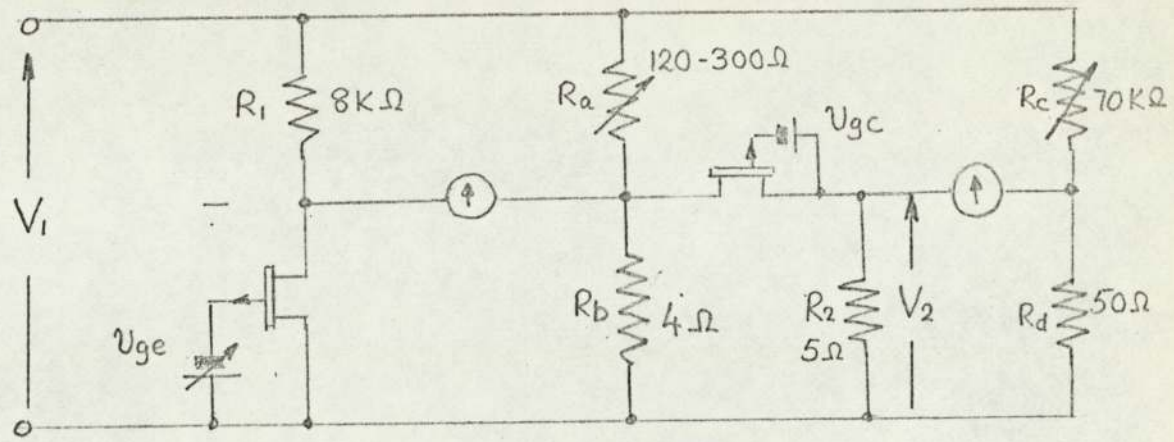


FIG. I.5 CIRCUIT TO MEASURE COMPANDING ERROR.

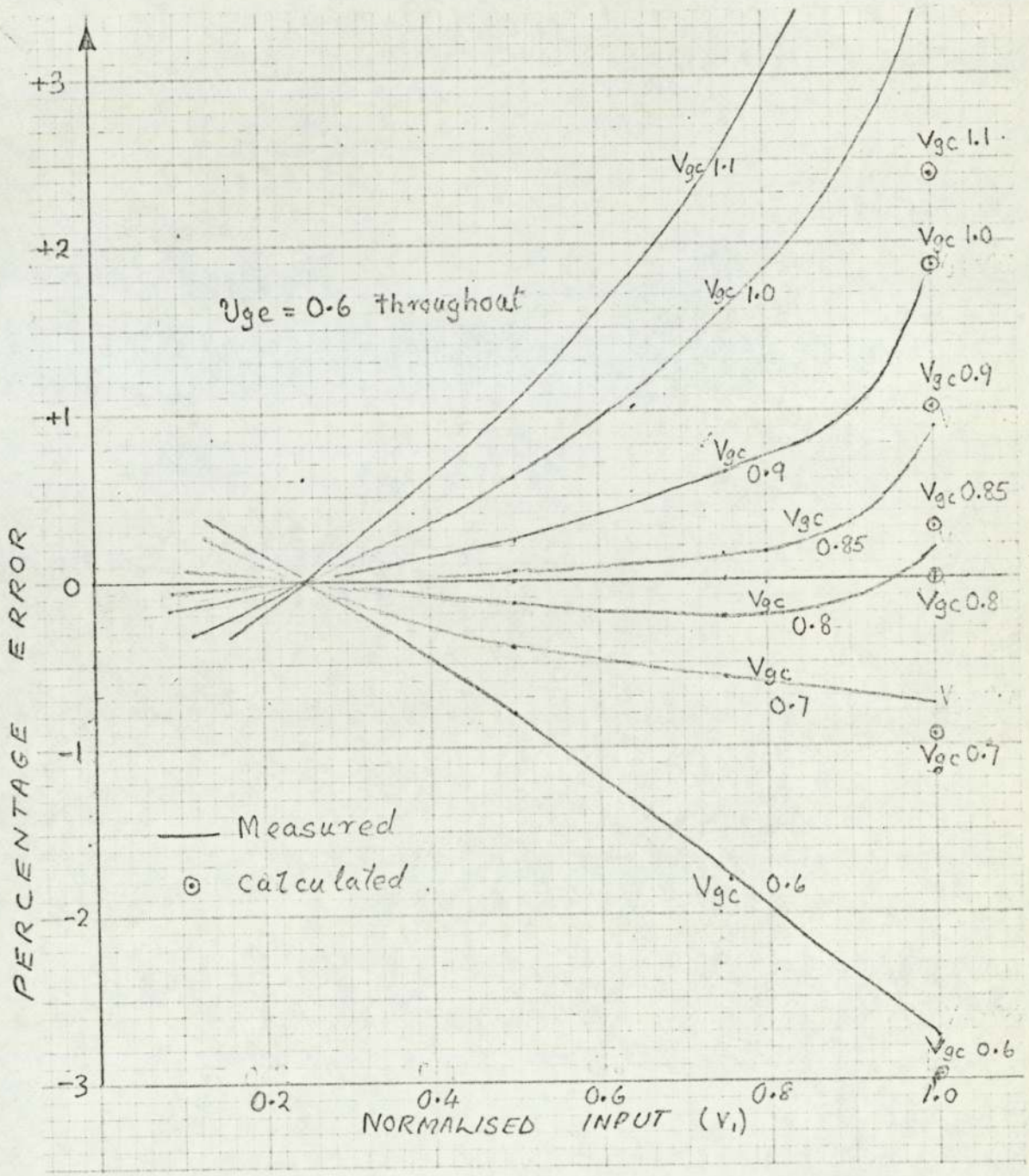


FIG. I.6 VARIATION OF COMPANDING ERROR

The following observations may be made:

(a) The smallest errors, of less than 0.2%, were measured when the gate-bias voltages were such that $r_c = 0.8\ r_e$.

(b) The calculated errors differ somewhat from the measured values, but follow the same trends.

The first result is surprising, for one would suppose that minimum error would occur when the i/v characteristics were inverse (i.e. when $r_e = r_c$ for all v_1). It is characteristic of the f.e.t.s. used that, at m = 0.8, the variation in m cancelled the net variation of the other two components. Further examination of these variations suggest that a low error at m = 1 may be achieved by a threefold increase in R_1. This may be conveniently arranged by replacing R_1 with a bipolar transistor of high output resistance.

Hence it has been shown that the f.e.t. may be used as an accurate companding element with the convenient feature that the characteristic may be controlled by the gate bias. It is admitted that:

(i) Precise control of gate voltage is required.

(ii) The characteristic is temperature-dependent.

In fact, other tests have shown that the fractional change in drain voltage under constant-current conditions is about 0.01 K^{-1} (a value approximately twice that of a silicon diode).

The authors consider, however, that temperature compensation of drain voltage or current may be arranged by the use of silicon p-n diodes to control the gate bias.

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APPENDIX J.

Errors in Separate - Stage Companding.

The use of a junction f.e.t as a separate stage compandor has been suggested in Appendix. I

It has been shown that :-

(a) The companding error may be reduced to less than 0.2% by adjustment of gate-bias.

(b) The calculated errors differ somewhat from the measured values, but follow the same trends.

The first result was unexpected and to clarify it, measured values of error, together with values calculated from equation I2, were plotted against values of Vgc in fig. J1.

It may be seen that errors due to voltage and current driving are of opposite sign and are nearly independent of Vgc while the error due to the variation in m tends to vary linearly with Vgc, passing through zero-value when Vgc = 0.85v. It may also be seen that zero error around Vgc = 0.8v occurs, because the error due to the variation in m cancelled the net effect of the other two errors. Although the gate bias-values were only 0.2v different, the drain resistances (γ_c and γ_e) were markedly different, the value of m being 0.8.

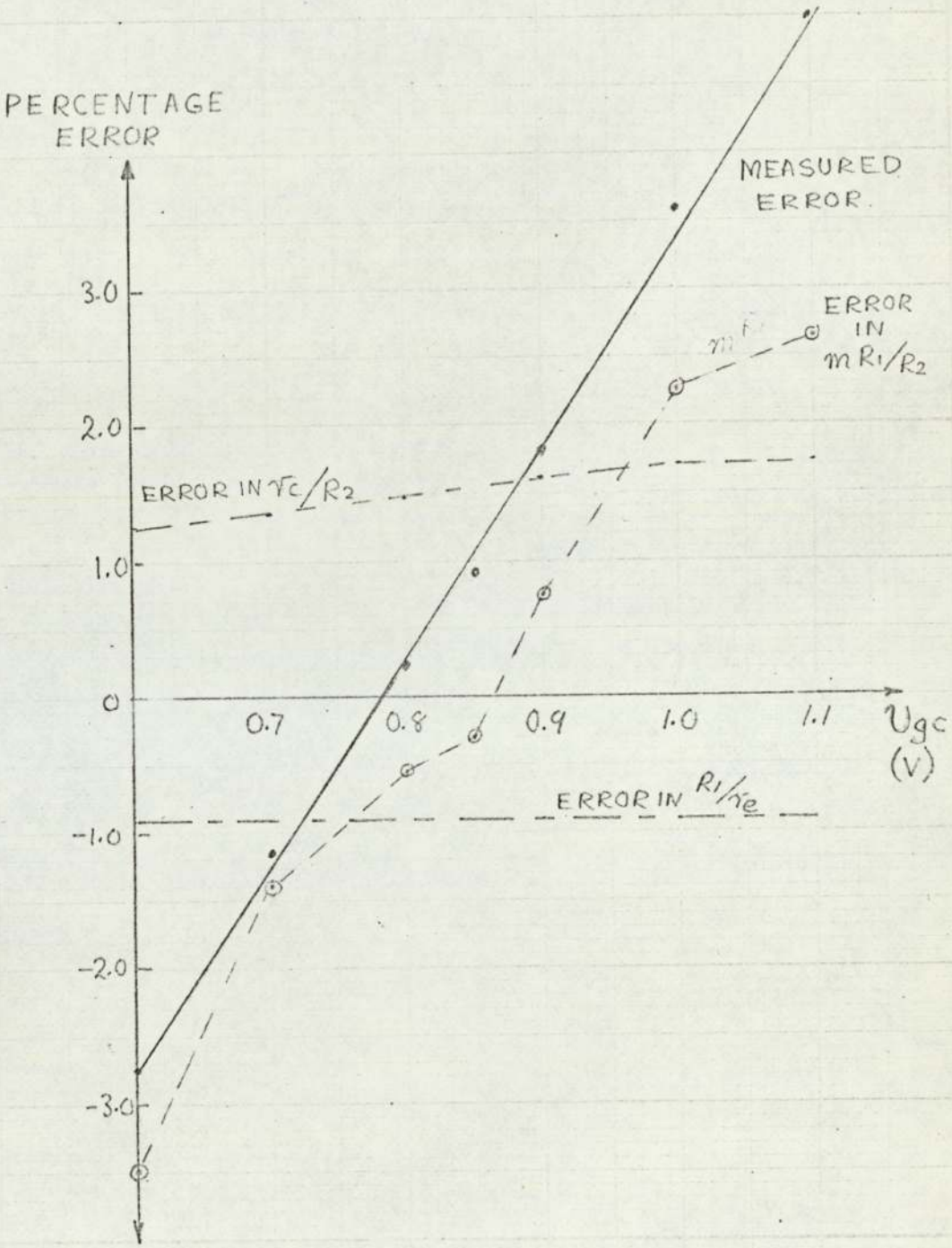
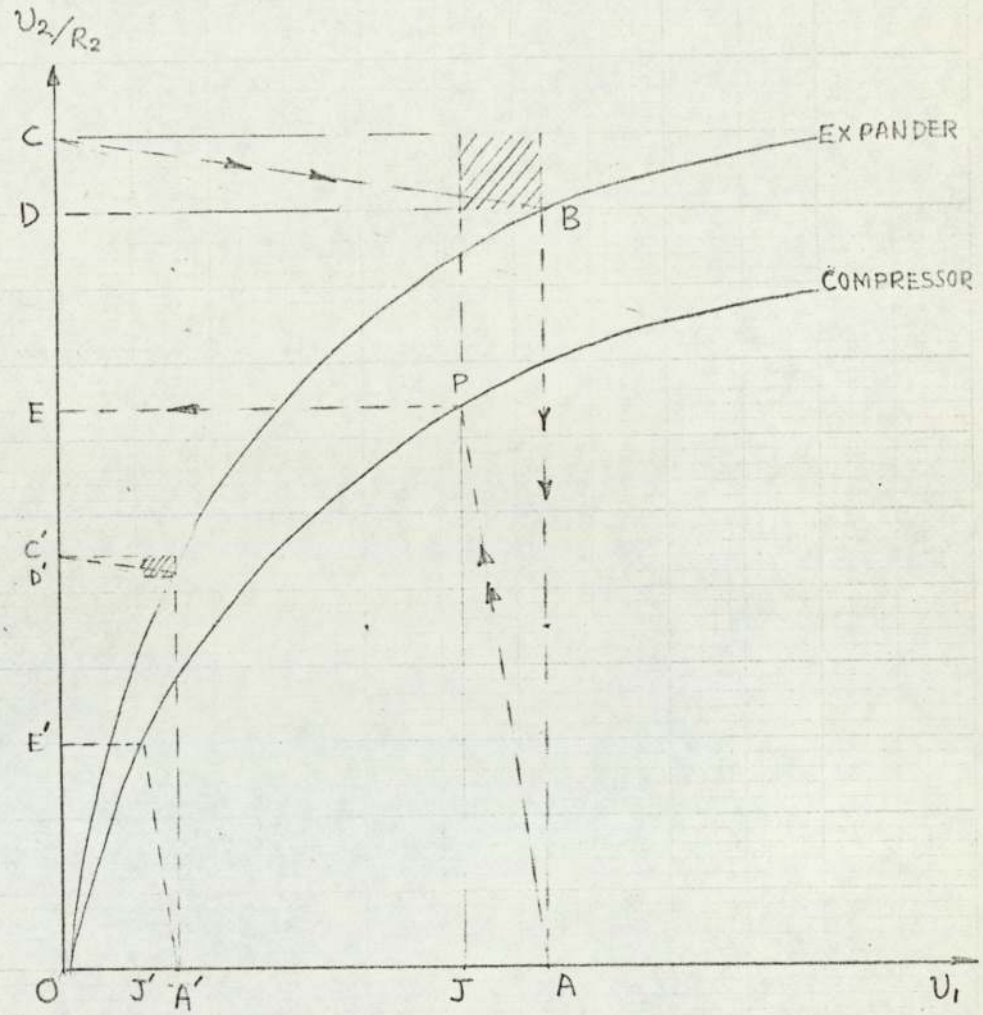


FIG J 1. VARIATION OF COMPONENTS OF COMPANDING ERROR WITH GATE BIAS WHEN NORMALISED INPUT CHANGES FROM 0.25 TO 1.0 (see also fig. I6)

If it were required that zero error occur when m has the value unity (i.e. Vgc = 1.1V and Vge = 0.6v), the ratio R_1/r_e would need to be increased by a factor of four. This could be conveniently arranged by using a bipolar transistor as a constant-current source in place of R_1.

The physical significance of these errors is illustrated in fig. J.2. Firstly, it may be observed that the operation of the expander-compressor cascade follows the arrows on the dashed lines. Secondly AP and BC are the resistance-lines for voltage and current driving respectively. Hence the current in the expander is reduced by amount CD due to its resistance r_e, while the voltage applied to the compressor is reduced by the amount AJ due to the resistance R_2. The error due to current-driving is then the variation of the ratio CD : OD which increases as V_1 is increased. The error due to voltage-driving is the variation of the ratio AJ : OJ which decreases as V_1 is increased. The product of the two gives the third error. That is, the third term shown in equation (I2) as $\frac{r_c}{r_e}\frac{R_1}{R_2}$ may be represented by the ratio of rectangular areas, shown in fig. J.2. The variation of this error with V_1 may be appreciated from the variation of the ratio of these rectangular areas.



$$T_e/R_1 = \frac{CD}{OD}, \quad R_2/T_c = \frac{AJ}{OJ}$$

$$\frac{T_e}{R_1} \times \frac{R_2}{T_c} = \frac{1}{m} \cdot \frac{R_2}{R_1} = \frac{CD \times AJ}{OD \times OJ}$$

The variation $\left[\frac{CD.AJ}{OD.OJ} - \frac{C'D'.A'J'}{OD'.OJ'}\right]$ is the major error.

FIG. J.2 ILLUSTRATING COMPONENTS OF COMPANDING ERROR

A study of fig J2, suggests that it is not necessary for

(i.e. equal resistances). As long as the ratio m = r_c / r_e is constant, only errors due to non-ideal voltage- and current -driving arise.

Maximum Companding Error.

The companding errors determined for the expander-compressor cascade in Appendix I were the fractional deviations of the input : output ratio V_1/V_2 from the values when the normalised input was 0.2. The maximum possible companding error should occur when the input varies from zero to a maximum, and may be written as :- $$\frac{(V_1/V_2)_1 - (V_1/V_2)_0}{(V_1/V_2)_0} = \left(\frac{V_1}{V_2}\right)_1 \left(\frac{V_2}{V_1}\right)_0 - 1 \quad \text{....(J1)}$$

The ratio V_1/V_2 has been given in equation (I2) and is repeated below. $$V_1/V_2 = 1 + R_1/r_e + r_c/R_2 + r_c R_1/r_e R_2 \quad \text{-----(I2)}$$

If r_{c0}, r_{c1} and r_{e0}, r_{e1} are the resistances of compressor and expander at $V_1 = 0$ and 1 respectively, the maximum companding error may be expressed approximately as follows.

$$\frac{R_2}{r_{c0}}\left(\frac{r_{e0}}{r_{e1}} - 1\right) + \frac{r_{e0}}{R_1}\left(\frac{r_{c1}}{r_{c0}} - 1\right) + \left(\frac{r_{c1}}{r_{c0}}\cdot\frac{r_{e0}}{r_{e1}} - 1\right) \quad \text{-----(J2)}$$

The first two terms are the errors due to voltage- and current-driving and it may be noted that the first term is negative ($r_{e0}/r_{e1} \simeq 0.3$) It has been stated previously that the net error from these two terms may be reduced to negligible amount, and that the main component is the third term.

It is of interest now to estimate the maximum error in separate-stage companding(for comparison with the Method 5 compandor). For convenience, the third term only is considered.

Using the Shockley-derived expression for r given in equation (7.17) and (D2), assuming that Vg = 0 at both ends, and that the compandor at one end isideal (σ=0) then

$$R_p/r = 3[1 - 0.66\sqrt{V}(1+\sigma)]$$

$$\text{i.e error } (\varepsilon) = \left(\frac{1 - 0.66(1+\sigma)}{1 - 0.66} - 1\right) = -1.98\sigma.$$

Hence the maximum error with no gate bias correction is 1.98σ for separate-stage companding.

Reduction of Companding Error with Gate Bias.

It has been shown experimentally in Appendix I fig I6 that the companding errors may be reduced by gate bias adjustment at one end. The minimum error is also shown to be nearly independent of input (i or v).

An attempt is now made to confirm these facts. The major error arises from the variation of r_c/r_e with V_1

As in the previous section the f.e.t compandor at one end(r_c) is considered to be non-ideal having a term (1 + σ) but with Vg = 0.

At the other end (r_e), the f.e.t is ideal with a gate bias of Vg. The ratio r_c/r_e, which is to be tested for constancy, is then given by :-

$$\frac{r_c}{r_e} = \frac{V - 0.66\,V^{1.5}\left[(1 + V_g/V)^{1.5} - (V_g/V)^{1.5}\right]}{V - 0.66\,V^{1.5}(1+\sigma)^{1.5}}$$

The test for constancy of r_c/r_e is given in the table below.

V	0.2	0.4	0.6	0.8	1.0	
$V^{1.5}$	0.089	0.254	0.465	0.72	1.0	a
$0.66\,V^{1.5}$	0.059	0.166	0.306	0.474	0.66	b
$0.76\,V^{1.5}$	0.073	0.193	0.355	0.547	0.76	c
$V - 0.76\,V^{1.5}$	0.127	0.207	0.245	0.253	0.24	d
$V - 0.66\,V^{1.5}$	0.141	0.234	0.294	0.326	0.34	e
$(1 + V_g/V)$	1.5	1.25	0.166	1.125	1.1	f
$(1 + V_g/V)^{1.5}$	1.83	1.36	1.26	1.2	1.153	g
$(V_g/V)^{1.5}$	0.353	0.125	0.068	0.044	0.0316	h
$[(1 + V_g/V)^{1.5} - (V_g/V)^{1.5}]$	1.48	1.235	1.192	1.154	1.121	i
$\{0.66V^{1.5}[\text{" "}]\}$	0.0875	0.204	0.365	0.548	0.75	j
$V - \{$ " $\}$	0.112	0.196	0.235	0.252	0.25	K
$(r_c/r_e)_{V_g=0.1}$	0.88	0.96	0.96	0.996	1.04	l
$(r_c/r_e)_{V_g=0}$	1.11	1.13	1.2	1.29	1.42	m

Row d is the denominator (i.e. re which has a departure σ from the ideal)

Row e is the numerator when Vg = 0 : i.e. no correction.

Row m is the ratio r_c/r_e when no compensating gate bias.

Row m is the numerator when Vg = 0.1 : i.e. correction

Row l is the ratio r_c/r_e when compensating gate bias is applied.

Note : the variations in row l are smaller than those in row K.

APPENDIX K

Maximum companind error in Method 5 coding

The maximum companding error in Method 5 coding is given by euqation (7.16 repeated below.

$$\varepsilon = \left[\left\{ \frac{K_s}{K_r} \int_0^{T_s} \frac{\gamma_s}{\gamma_r} dT \right\} \frac{dT_s}{dT_r} - 1 \right] \quad ----(7.16)$$

The channel pulse durations at the encoder and decoder under zero modulation conditions are equal ($T_{s0} = T_{r0}$) andalso $dT_s/dT_r = 1$

Furthermore, if the channel pulse duration is directly proportional to the modulating signal, and if the f.e.t. companders at both ends are current-driven, then :-

$$\varepsilon = \left[\frac{K_s}{K_r} \int_0^1 \frac{\gamma_s}{\gamma_r} dI - 1 \right]$$

Where I is the normalised current input.

As in Appendix J the Shockley-derived formula is used with the sending-end compandor ideal ($\sigma = 0$) Hence,

$$\varepsilon = \left[\frac{K_s}{K_r} \int_0^1 \left\{ \frac{1 - 0.66\sqrt{V}(1+\sigma)}{1 - 0.66\sqrt{V}} \right\} dI - 1 \right]$$

Integration w.r.t. normalised voltage V ($= v/V_p$) is arranged by differentiating the Shockley equation for draincurrent, equation (7.11) i.e. $dI = 3(1-\sqrt{V})dV$. Hence, the maximum error is given by :-

$$\varepsilon = \left[\frac{3K_s}{K_r} \int_0^1 \frac{[1 - 0.66\sqrt{V}(1+\sigma)(1-\sqrt{V})]}{[1 - 0.66\sqrt{V}]} dV - 1 \right]$$

Evaluating the integral :-

$$\varepsilon = 3\frac{K_s}{K_r} \int_0^1 \left[1 - \sqrt{V} - \frac{2}{3}\sqrt{V}\sigma + \frac{2}{9}\frac{V\sigma}{(1-0.66\sqrt{V})} \right] dV - 1$$

Now $0.66\sqrt{V} < 1$ and hence

$$\varepsilon = 3\frac{K_s}{K_r} \int_0^1 \left[1 - \sqrt{V} - \frac{2}{3}\sqrt{V}\sigma + \frac{2}{9}V\sigma\left(1 + \frac{2}{3}\sqrt{V} + \frac{4}{9}V + \frac{8}{27}V^{3/2}\right) \right] dV - 1$$

$$\varepsilon = 3\frac{K_s}{K_r} \left[V - \frac{2}{3}V^{3/2} - \frac{4}{9}V^{3/2}\sigma + \frac{1}{9}V^2\sigma + \frac{8}{135}V^{5/2}\sigma + \frac{8}{243}V^3\sigma + \frac{32}{1701}V^{7/2}\sigma \right]_0^1 - 1$$

$$\varepsilon = 3\frac{K_s}{K_r}\left[+\frac{1}{3} - \sigma\left(\frac{4}{9} - \frac{1}{9} - \frac{8}{135} - \frac{8}{243} - \frac{32}{1701}\right)\right] - 1$$

$$\varepsilon = \frac{K_s}{K_r}\left[1 - 0.637\sigma\right] - 1$$

If the voltage-frequency converter at the two ends are identical,
$K_s/K_r = 1 \quad \therefore \quad \varepsilon = -0.637\sigma$

This should be compared with $\varepsilon = -1.98\sigma$ given in Appendix J for separate stage companding.

APPENDIX L.

Expression for maximum clock pulse frequency in a Method 5 segmented encoder.

Let s = number of segments in a n- bit, m-channel system having a maximum modulating signal frequency of fm.

Maximum channel pulse duration is $\frac{1}{2mf_m}$

In this duration there are S bursts of $2^n/s$ pulses each having frequencies $f, f/2 \ldots f/2^{s-1}$ respectively.

The durations of the bursts are then $2^n/sf,\ 2(2^n/sf), \ldots (2^{s-1}.2^n/sf)$

i.e. $\frac{1}{2mf_m} = (1 + 2 + \ldots + 2^{s-1})2^n/sf$

$\therefore \quad f = \frac{1}{s}\left[(2^s - 1)2^{n+1}.mf_m\right]$.

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