STUDY OF EPITAXIAL SILICON LAYERS WITH REFERENCE TO THE TECHNOLOGY OF SEMI-CONDUCTOR DEVICES

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by

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SUMMARY

Epitaxial silicon layers have been studied, with reference to the technology of semiconductor devices, in order to determine the possibility of developing a new method, which overcomes the limitations associated with the conventional methods for forming PN junctions by introducing impurities into the crystal during growth from the melt or by diffusion.

The mechanisms governing epitaxial growth, by silicon vapour and vacuum deposition are reviewed and the most promising adopted for further study and development. This involved the design and construction of apparatus for the growth of layers by the hydrogen reduction of silicon tetrachloride and for control of crystal perfection, layer thickness, layer type and resistivity, as determined by the doping element and its concentration respectively.

Methods of evaluating the conductivity, thickness, resistivity, structure, impurity and doping concentration were assessed and the most suitable methods developed.

The dependence of the growth of epitaxial layers of controlled properties on nucleation,gaseous impurities in the system and on the type and concentration of the doping elements in the gas system and the substrate, have been established.

Lattice defects originating mainly at the substrate-layer interface giving rise to inferior electrical characteristics, can be eliminated by gaseous polishing of the substrate surface and control of the purity of the reaction system.

Difficulties have been encountered in controlling the layer thickness in multi-layer structures during the formation of the base and collector regions of a transistor, and thereby producing transistors with consistent characteristics.

The control of the properties of single epitaxial layers is satisfactory for the subsequent fabrication of transistors by diffusion within the layer.

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1. INTRODUCTION

One of the outstanding developments of the post-war era originated with the discovery of transistor action by Bardeen & Brittain (1). This has formed the basis of the development of the technology of semi-conductor devices that has developed into an industry with a turnover of $500 million per annum in the U.S.A., and about a tenth of that magnitude in the U.K. This industry has been established as a result of the exploitation of the properties of the elemental semi-conductor materials germanium and silicon.

Germanium and silicon elements of Group IVB of the periodic table, have a valence of 4 and crystallise with the diamond type of structure where each atom forms a co-valent bond with four other atoms in a three dimensional lattice. Such a structure is extremely stable and is a perfect insulator at absolute zero of temperature. At higher temperatures thermal agitation causes some electrons to break away from the atoms that are free to diffuse within the crystal structure. When an electric field is applied the electrons drift and a current flows.

At room temperature silicon and germanium conduct electricity because of the presence of a number of electrons, but the magnitude of the current is low since the number of mobile electrons is only a very small proportion of the total number of atoms present. At room temperature silicon has an intrinsic resistivity of the order of 230,000 ohm cm.

In a practical application, such as the preparation of rectifiers and transistors, single crystals are used because they have a high degree of lattice perfection and uniformity of structure. The conductivity of a silicon single crystal, however, may be greatly enhanced by the addition of trace of impurities of two different types either elements of Group III, or elements of Group V. When a silicon atom is replaced by phosphorus of Group V, the one electron that is not required to form the crystal structure bonds is free to diffuse through the single crystal thereby increasing the conductivity. This type of impurity is known as a "donor" and the semi-conductor is called N-type because the current is carried by a negative charge carrier or electron. When boron, an element of Group III, replaces

a silicon atom, the lattice bonds are incomplete since the boron atom can only satisfy three of the four bonds. The fourth bond is made by attachment of an electron from a neighbouring atom. The migration of the electron to complete the crystal bond structure transfers the vacancy or hole to another part of the structure and gives an effective movement of positive charge. Conduction by the movement of holes, gives a positive or P-type semi-conductor and the boron atoms are referred to as "acceptors".

Increasing the number of impurity atoms will decrease the resistivity and Figure 1.1 indicates the relationship between the number of impurity atoms present and the resistivity of silicon. It is relevant to note that silicon contains 5×10^{22} atoms/cc and the difference in N and P type impurity concentration arises from the difference in hole and electron mobilities.

When P and N type impurities are deliberately introduced into a semi-conductor crystal a PN junction will be formed at the interface, where the number of acceptors and donors are equal. A PN junction is illustrated in Figure 1.2, where the region on the right is P-type, and the conduction is mainly by positive holes, and that on the left is N-type where conduction is mainly by electrons. When biased on the forward direction, the P-region is positive and a comparatively large current flows because under the influence of the voltage positive holes from the hole rich P-type region and negative electrons from the electron rich N-type region cross the junction. On the other hand, when biased in the reverse direction, the P-region is negative and very little current flows since the polarity is such as to attract across the barrier only the minority carriers from each side. Since a larger current flows in one direction than in the other, for a given voltage, the system rectifies. When the junction is biased in the reverse direction, a constant low current is drawn which is independent of voltage over a wide range of voltage. However, at a critical voltage the current increases sharply, Figure 1.3, and breakdown occurs which is designated the peak inverse voltage.

When biased in the reverse direction, the P-N junction acts as a collector where minority carriers injected into either side sufficiently close to the barrier can reach it by drift or diffusion, and be collected by the field across the junction. Consequently, such a junction is photosensitive to light of a sufficiently short wavelength, because the light excites electrons from the valence band to the conduction band, thus creating hole electron pairs on whichever side of the barrier the light falls. When biased in the forward direction the junction is an emitter, since the motion of charge carriers is such that holes enter the N-side while electrons enter the P-side. Finally, under forward bias the minority carriers which have been injected can be stored in the end regions if their lifetimes are sufficiently long. A certain number can be recaptured if the voltage is quickly reversed. This property of charge storage is analogous to that found in a capacitance.

More complex structures may be found and described as a multiplicity of PN junctions. When two PN junctions are formed close together in one single crystal so that either a PNP or an NPN configuration is formed as shown in Figure 1.4 a junction transistor is established. The two PN junctions separate three homogeneous regions called (1) the emitter region because it emits or injects carriers (2) a base region and (3) a collection region, because it collects carriers from the base region.

Voltages applied to the emitter-base and collector-base junctions determine the minority carrier densities at the two ends of the base region. With a forward bias applied to the emitter-base junction, the density of minority carriers at the emitter and of the base region is raised above the equilibrium density. A reverse bias applied to the collector junction lowers the minority carrier density at the collector end of the base region, and if the current level is not too high, the minority carrier distribution (electrons in an NPN transistor) in the base region is illustrated in Figure 1.5. The carrier gradient indicates a flow of current by diffusion from the emitter to the collector. Since the gradient in the base region is in part determined by the bias voltage on the emitter junction, the

current through the collector junction is in part a function of the emitter base voltage. This is the basis of transistor operation where the current from emitter to collector is controlled by the bias applied to the emitter junction.

When the emitter is biased negatively with respect to the base in an NPN transistor, in order to forward bias the emitter junction, and the collector is biased positively to reverse bias the collector junction minority carriers - electrons, flow through the P type region.

Although the electron current is the important parameter, the applied bias voltages also modify the electron densities in the N type emitter and collector regions and give rise to currents of holes from base to emitter and also from collector to base. For efficient transistor operation these currents should be small compared with the important electron currents. To ensure this the emitter and collector regions are more heavily doped with donors than the base is with acceptors, thus producing an N^+PN^+ configuration.

The heavy doping of the emitter region is much the more important of the two. As the forward bias of the emitter is increased the ratio of the hole and electron currents stays roughly the same, and is dominated by electrons in the N^+P junction. The collector junction, however, is reverse biased and the currents flowing through it are simply determined by the rates at which the minority carriers can reach it. The electrons coming from the base region are provided by the emitter and, at all but the lowest current levels swamp the small number of thermally generated holes coming from the collector region, even if the collector is not very heavily doped. Thus, it is not so important to heavily dope the collector region and many transistors have an N^+PN configuration where the N^+P structure forms the emitter-base junction and the PN structure forms the base collector junction.

The electron current which leaves the emitter junction will only reach the collector unmodified if there is no recombination in the base region. In practice, some recombination takes place although it can be made exceedingly small by the use of a thin base width, and material having a

high life time, so that the collector electron current is slightly less than the emitter electron current.

Two factors contribute to the collector current being less than the emitter current. Firstly, some of the emitter current does not consist of electrons; the ratio of the electron current to the total emitter current is called the emitter efficiency γ . Secondly, not all the electrons leaving the emitter reach the collector; the proportion of electrons leaving the emitter and reaching the collector is called the transport factor δ . The production of the two factors $\alpha n = \gamma\delta$, where αn is current gain and determines the proportion of the emitter current which reaches the collector. In order to maximise the current gain the lifetime of base region should be high, the base thickness should be small, the emitter resistivity should be very low, and the surface recombination should be small.

The fabrication of P-N junctions may be divided into two general classes, where either the impurities leading to the desired properties are incorporated into the crystal during growth or a section of a homogeneous crystal is heat treated when the desired regions of conductivity are formed. In the first case the crystal is grown from an N-type doped melt to which further doping elements are added to the melt at the appropriate stage in the growth of the crystal - Figure 1.6. The surface of the junction produced is not usually regular because of the influence of various growth factors.

In principle, a large number of P-N junctions could be grown in the crystal by continual reversal of type through doping the melt with the proper amounts of donors and acceptors. However, in practice this has the result that with each reversal the impurity content continually increases and the lifetime and mobility of charge carriers deteriorate. In addition accurate compensation to produce the desired resistivities becomes progressively more difficult to achieve as the total impurity content increases.

In the second case P-N junctions are formed by heating a wafer of a semi-conductor in contact with an impurity element which forms a liquid alloy with the semi-conductor at the heating temperature. Aluminium has

been used to make P-N junctions in N-type silicon as illustrated in Figure 1.7. On heating a pellet of aluminium resting on an N-type silicon wafer, the aluminium will melt at 660°C and start to attack the silicon, to form a silicon aluminium liquid. At a particular temperature equilibrium will be reached between the liquid silicon and aluminium. When the wafer is cooled, the liquid solution is super-cooled and begins to freeze. The silicon crystallises out in the form of a single crystalline layer deposited upon the undissolved silicon.

Because of the high concentration of aluminium the re-crystallised silicon layer is doped with aluminium and a junction is formed at the interface between the unmelted N-type silicon and the re-crystallised P-type silicon. Variation of the temperature-time cycle will produce junctions of controlled depth and impurity concentration; however, regular junctions are not generally obtained.

Another example of this second case is the formation of diffused junctions made by exposing a P-type wafer of a semi-conductor to the vapour of an N-type impurity (or vice versa) at an elevated temperature. Junctions produced by diffusion of a vapour into the solid semi-conductor move uniformly into the crystal surface, retaining the contour of the crystal surface. Hence, if the surface is very flat, the junctions will also be very flat. The depth beneath the surface at which the junction is formed is determined by the time and temperature of exposure to the impurity vapour. The depth of penetration together with the initial impurity content of the semi-conductor crystal determine both the location of the junction and its thickness.

With this method, accurate control of junction depth and impurity concentration gradient can be obtained, and hence it is the most common method used for the production of P-N junctions in diodes and transistors.

Recently Marinace (3), Wajda (4) and Theuerer (5), have demonstrated that layers of controlled resistivity, type and thickness can be grown epitaxially on to a single crystal substrate. In semi-conductor technology, an epitaxial layer is defined as a film of single crystal semi-conductor

material that has been deposited on a single crystal substrate, and is coherent with the substrate. The layer is produced by the thermal or chemical decomposition of a germanium or silicon compound about the single crystal substrate under conditions which allow the layers to grow epitaxially.

In the formation of mesa transistors the selection of the proper resistivity for the collector body is a compromise dictated by the necessity for a low collector capacitance and a high breakdown voltage (factors which require high collector resistivity) and a low series ohmic collector resistance (which requires a low collector resistance). On the other hand in the formation of an epitaxial transistor, it is possible to select two structure parameters independently, which makes it possible to meet all these design requirements, without a design compromise. A transistor can be fabricated using a high resistivity epitaxial layer (in order to achieve the low collector capacitance and high breakdown voltage requirements) and a very low resistivity substrate (which for all practical purposes makes the series collector resistance zero).

Theuerer (6) has produced a more ideal transistor structure as shown in Figure 1.8 by diffusing the base and emitter layers into a thin high resistivity epitaxial layer. The main body of the collector region is very low resistance material. Such an epitaxial transistor has the following advantages over the normal diffused mesa transistor -

(a) low saturation resistance,

(b) saturation resistance independent of temperature,

(c) greater linearity of characteristics,

and (d) reduced minority carrier storage time.

These improvements have been shown in the case of small mesa transistors using very thin epitaxially deposited layers, but little is known about the advantages in properties that can be obtained when epitaxial layers are used for the production of power (high current) devices.

With the demand for more refined semi-conductor devices it is becoming increasingly difficult by present techniques to control the

formation of N and P regions with the required properties and accuracy. The epitaxial technique offers the possibility of creating device structures by the successive deposition of P and N layers that are difficult or not possible with the present techniques.

With the demand for more compact electronic equipment, the greatest packing density of components can be obtained with the use of solid circuits as described for instance by Dummer (7). The basic principle is to form the circuit components-resistors, capacitors, transistors, diodes, etc. in a single solid block of silicon and by suitably shaping the block, isolation can be obtained between the circuit elements so that there are no end connections between the various components functions. It is believed that the reliability of such a unit should be very high.

The epitaxial technique can offer great reward in the formation of these solid circuits. In principle the epitaxial technique offers absolute freedom for controlling impurity distributions in three dimensions in a single crystal, when the technological difficulties have been overcome. It is with the formation and the physical properties and mechanisms occurring in epitaxial layers, in particular in silicon, that this thesis is concerned.

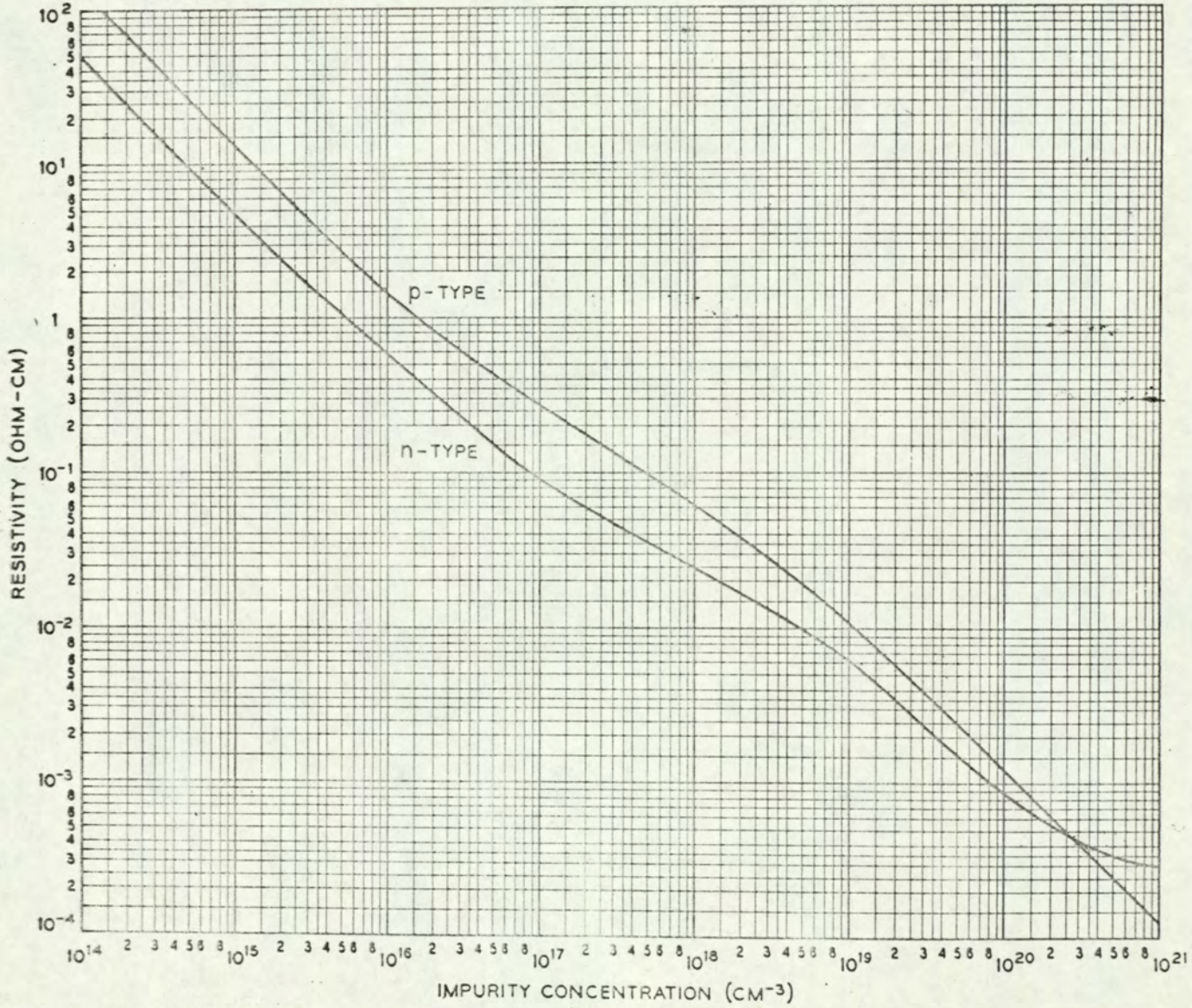


Fig. 1.1 Relationship between resistivity and impurity concentration. Ref. 2

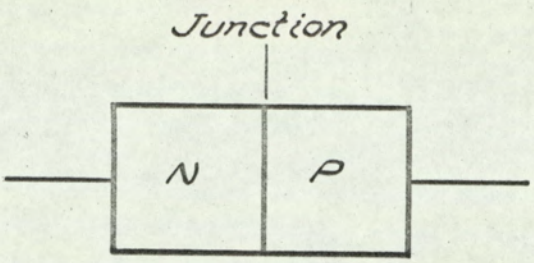


FIG. 1.2 PN JUNCTION

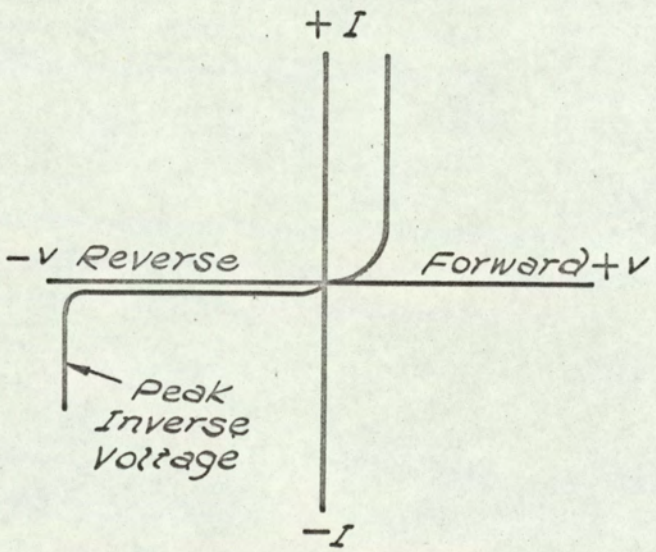


FIG. 1.3. TYPICAL RECTIFIER CHARACTERISTIC.

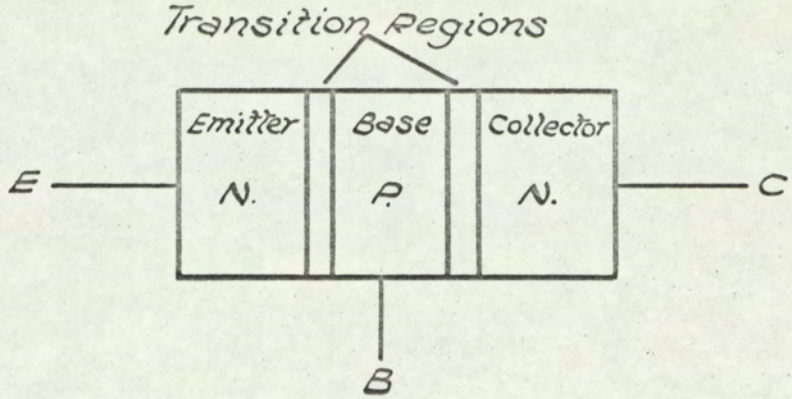


FIG. 1.4 AN IDEALISED STRUCTURE OF A TRANSISTOR.

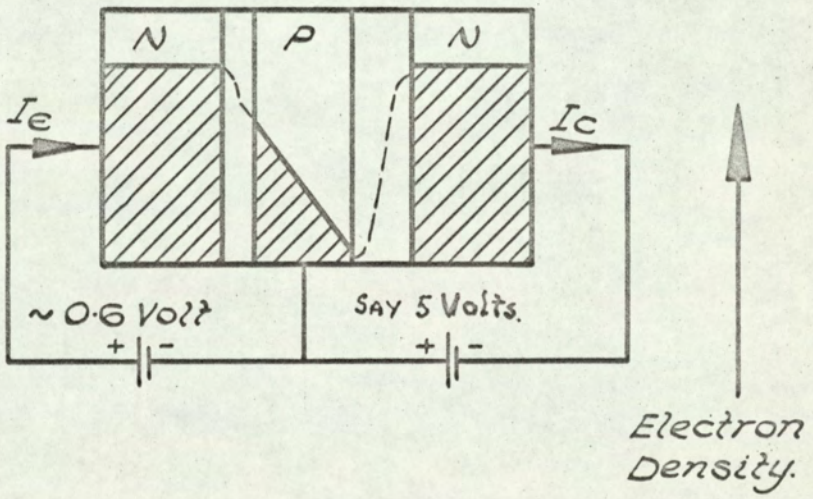


FIG. 1.5. ELECTRON DENSITY DISTRIBUTION IN AN N.P.N. TRANSISTOR.

THE DENSITY PROFILE IS SHOWN DASHED IN TWO TRANSITION REGIONS.

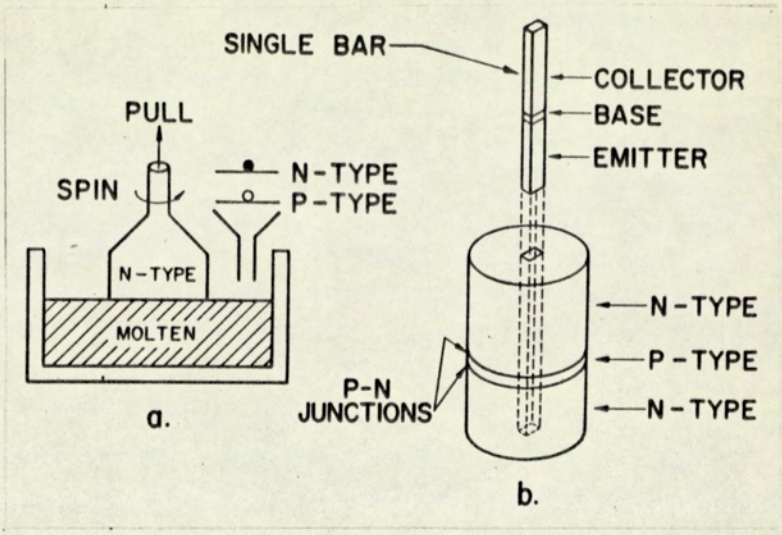


Fig. 1.6 Grown PN junction

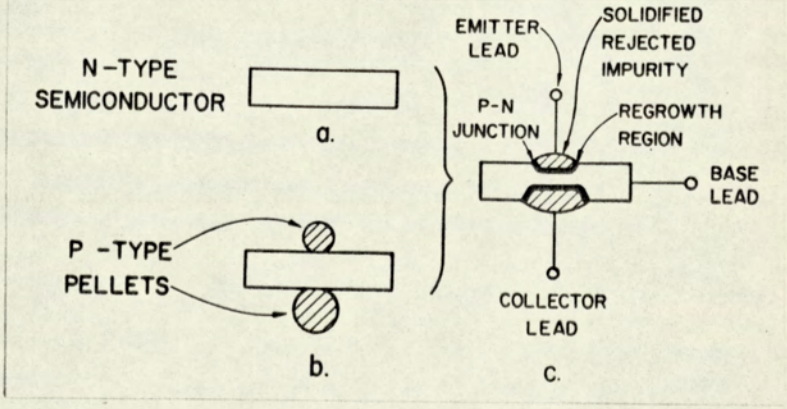


Fig. 1.7 Alloyed PN junction

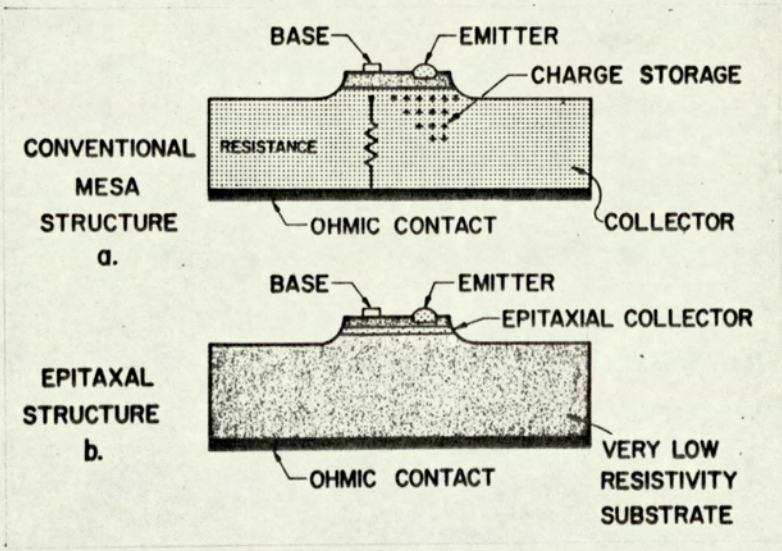


Fig. 1.8 Conventional and epitaxial diffused mesa transistors

2. SILICON EPITAXIAL LAYER FORMATION

The derivation of the word epitaxy from the Greek words epi, meaning "upon", and the past tense of the verb teinen, meaning "arranged", is an apt description of epitaxy. A gas containing silicon atoms is suitably passed over the substrate when the silicon atoms, released from reactant molecules, are deposited and become part of the growing film. Under proper conditions single crystal orientation is obtained and the resulting layer becomes an exact extension of the single crystal lattice of the substrate.

The mechanisms governing epitaxial growth are not completely understood, but simplified models for epitaxial growth have been advanced and are discussed below. Growth mechanisms can be divided into "direct" and "indirect" processes.

2.1 Theory of Epitaxy

In the DIRECT PROCESS, silicon is transferred from the source to the substrate with no intermediate reactions or events. Evaporation, sublimation and sputtering are examples of this technique. It is assumed that silicon atoms impinge on the substrate surface and are held there by interatomic forces. Under certain conditions the atoms are mobile and become attached to a step or ledge or re-evaporate. The growth process, therefore, can be described as the lateral movement of steps across the substrate surface as depicted in Figure 2.1. Steps can be formed either by the two dimensional nucleation of islands on the surface resulting from the initial deposition of silicon or by a spiral dislocation existing on the substrate. Epitaxial growth therefore occurs through the influence of (a) the substrate on two dimensional nucleation and (b) lattice matching as the steps form across the surface.

The rate of two dimensional nucleation can become large at high temperatures and is dependent on the concentration of silicon in the vapour and on the free energy of formation of the nucleus. The rate of nucleation is given by:

$$R_n \propto N_o \exp(-\Delta G/kT), \qquad 2.1$$

where R_n = two dimensional nucleation rate,

N_o = concentration of silicon in the vapour,

ΔG = free energy of formation of the nucleus,

T = temperature of deposition,

k = the Boltzmann constant.

For large values of R_n, many steps are available for propagating the growth of the epitaxial layer and good epitaxial growth would be expected to occur. On the other hand, it may be seen from equation 2.1 that even for large values of N_o, R_n may still be small if the deposition temperature T is reduced.

The steps formed (at low temperature) quickly grow to a maximum and produce a "singular" or low index face. This is illustrated in Figure 2.2 where the surface of the layer is prepared by vacuum sublimination at the comparatively low substrate temperature of 1100^oC. The low index faces, bounded by steps, are clearly defined. Impurities tend to inhibit the movement of steps across the surface and often results in the formation of steps very many atoms high. Impurities on the other hand may increase or decrease the nucleation rate and seriously complicate the growth process.

In the INDIRECT PROCESSES the deposition of silicon atoms, onto a substrate, involves the release of silicon by the decomposition of a vapour of a silicon compound. Examples of such processes are the hydrogen reduction of silicon tetrachloride ($SiCl_4$), silicon tetrabromide ($SiBr_4$), trichlorosilane ($SiHCl_3$) and the pyrolysis of silane (SiH_4). The precise decomposition reactions which produce silicon atoms during epitaxial growth are not clearly understood. One hypothesis (5, 9, 10, 11) proposes that silicon is formed on the substrate by a surface controlled reaction, while another (8, 12) assumes that the silicon is separated from its compound, in the gas phase, in a region of a few microns from the substrate. This results in the deposition of individual atoms, groups of atoms, or overcooled droplets, by diffusion.

For cases where the reaction is surface controlled, as in the first hypothesis, a classical heterogeneous reaction consisting of the following events is proposed (10).

(a) Mass transfer of the reactants to the substrate surface.

(b) Adsorption of the reactant onto the surface.

(c) The reaction or series of reactions which occur on the surface.

(d) Desorption of the by-product molecules.

(e) Mass transfer of the by-product molecules to the main gas stream.

and (f) Addition of atoms to growth steps.

In some cases the last events may be combined with event (c).

Electron micrographs and diffractograms taken of growing layers at short time intervals after growth is initiated, show what are apparently clusters of silicon atoms distributed on the surface before complete coverage has occurred. Figure 2.3 shows a typical electron micrograph of a growing layer 10 seconds after growth has been initiated, where the silicon atoms are released by the hydrogen reduction of trichlorosilane. The surface is covered with a number of discrete islands or clusters about 500 Å in diameter. After growth for a period of 30 seconds, the islands are still present as illustrated in Figure 2.3 but they are not as clearly defined. Layers grown on substrates of different orientation show similar effects.

The most probable sequence of events involved in the reaction is the sorption of trichlorosilane on the substrate followed by its reduction by the hydrogen impinging on the substrate and desorption of hydrogen chloride as a by-product. Initially, the silicon does not grow as a monolayer, but rather by the formation of clusters which are much thicker than one atomic layer. Because chemisorption can only occur to a depth of a monolayer, the clusters increase in size either by surface diffusion of silicon, from unfavourable sites, or by preferential chemisorption. Surface diffusion is more probable since layer perfection and surface mobility decrease with decreasing temperature.

The nucleation process as explained above is supported by experimental data (11). It is observed that in the pyrolysis of silane, larger islands or clusters are formed than in the decomposition of hydrogen-trichlorosilane. This is indicative that the mobility of the chemisorbed molecule is the important factor, rather than that of the silicon atoms. Silane is more likely to have a higher mobility (and hence form larger islands) than trichlorosilane since the larger chlorine atoms would be expected to decrease the mobility of trichlorosilane to a large extent.

If one of the events in the heterogeneous process is much slower than the others, it will govern the growth rate. Furthermore, the events may be controlled by different factors: the mass transfer rate is influenced by the gas flow rate, but it is relatively independent of temperature. The other events, however, are strongly dependent on temperature, but practically independent of gas flow rate.

At low growth temperatures, the adsorption rate of the silicon compound appears to be the controlling factor and the reaction is controlled by the surface reaction rate. At high temperatures, however, the mass transfer rate of reactants is the controlling factor. In the alternative hypothesis of epitaxial deposition, silicon atoms are freed from their compounds in the layer of gas adjacent to the substrate. The layer of gas is assumed to be in a state of laminar flow and transport to and from the substrate is governed by diffusion through the layer. After reaching the substrate, the silicon atoms are mobile and can align preferentially to the lattice of the substrate. Under certain conditions, the concentration of silicon atoms in the gaseous region over the substrate is not uniform. This can lead to imperfect epitaxial layers and ledges or pyramids are formed. One method of obtaining this instability is the reduction of the growth temperature which reduces the nucleation rate and causes a rough irregular surface as shown in Figure 2.4.

The study (13, 14) of growth mechanisms on the (111) faces of silicon indicates that the growth proceeds by lateral expansion of the (111) layers in $\langle 211 \rangle$ directions thereby forming steps. The step edges are

perpendicular to the direction of expansion and lie in the <110> directions. Bunching of these steps causes various topographical features which are discussed in Section 7.

In general, the process of silicon deposition is dependent on mass transport, kinetic and equilibrium factors, and experimental conditions such as the geometry of the reaction chamber where the carrier gases are decomposed and the silicon deposited.

2.2 Silicon Deposition Processes

A number of processes of depositing silicon have been developed, namely vapour and vacuum deposition.

In vapour deposition, investigations have proceeded during the past two decades: many processes have been investigated for the purpose of depositing high purity polycrystalline silicon from a gas phase on to a hot surface. All the chemical processes have certain features in common. At a temperature T_1, a stable volatile silicon compound is formed that can be purified by fractional distillation, for example. The vapour pressure of the compound may be maintained and controlled by evaporating the compound from a source at a given temperature while it is transferred into a deposition zone maintained at a temperature T_2. In the course of this reaction elemental silicon is deposited onto surfaces exposed to the vapour. Frequently hydrogen gas is added to the vapour as a carrier or reducing agent. Table 2.1, which is by no means complete, gives a number of typical experimental conditions required for various reactions which have been used in order to deposit silicon from the vapour phase. Processes yielding solid reaction products other than silicon, such as obtained in the reduction of silicon tetrachloride with zinc or sodium vapours have not been included.

The reactions listed in Table 2.1 should also be suitable for growing single crystal layers of silicon, since the additional requirements necessary for epitaxial growth, rather than for simple deposition of polycrystalline silicon, are governed by the properties of the substrate such as its surface and deposition temperature.

One of these reactions - the decomposition of silicon tetraiodide to form silicon - is a simple chemical process and because of the ease of purification, the silicon tetraiodide produces extremely high purity silicon. The use of iodine vapour to transport silicon for epitaxial growth has been reported (4). In this process the substrate, source of silicon, iodine vapour and sometimes hydrogen, are enclosed in a sealed tube with provision (Figure 2.5) for the source and the substrate to be heated to different temperatures. The iodine vapour reacts with the silicon to form a volatile compound which migrates to the substrate, where decomposition and deposition occur. For iodine vapour pressures greater than 100 torr the substrate is maintained at a low temperature ($\sim$ 950°C) compared with that of the source ($\sim$ 1100°C). The reaction proceeds according to the chemical equation -

$$2\,SiI_2 \rightleftharpoons Si + SiI_4 \qquad 2.2$$

At low iodine pressures ($\sim$ 1 torr) the reaction in equation 2.2 is reversed and the substrate must be maintained at the higher temperature ($\sim$ 1300°C) and the source at the lower temperature ($\sim$ 1100°C). For low pressures the reaction

$$SiI_4 \rightleftharpoons Si + 4I \qquad 2.3$$

can occur which in combination with equation 2.2 gives the net reaction

$$SiI_2 \rightarrow Si + 2I \qquad 2.4$$

The disadvantages of this process are (i) only a limited number of substrates can be enclosed in the tube for simultaneous layer growth during one cycle, (ii) a sealed tube must be used in the process resulting in a serious disadvantage when simultaneous deposition of layers on to a number of substrates is required, (iii) the tube cannot be purged under operating conditions resulting in impurities being introduced into the transporting gas stream, (iv) the resistivity and type of the deposited layers will be directly dependent on that of the silicon source.

Reactions involving silicon tetrachloride and trichlorosilane are also used in the manufacture of silicon. Trichlorosilane thermally decomposes at a slow rate to produce silicon, but silicon tetrachloride is

stable up to at least 1200°C. With hydrogen however both these compounds react to produce silicon with reasonable efficiency and rates. The overall chemical reaction for silicon tetrachloride is

$$SiCl_4 + 2H_2 \longrightarrow Si + 4HCl \quad \text{---------- 2.5}$$

but other products e.g. $SiCl_2$; $SiHCl_3$ and long chain polymers also occur in the reaction.

The overall reaction for trichlorosilane is represented by the following equation -

$$SiHCl_3 + H_2 \longrightarrow 3HCl + Si \quad \text{---------- 2.6}$$

The kinetics of the H_2 - $SiCl_4$ process in equation 2.5 are complicated and a quantitative account of the ingoing $SiCl_4$, in terms of total deposited silicon and other reaction products in an epitaxial growth system, have not been discussed (16). However, Lever (17) has shown that in the range of variables most frequently used for the vapour growth of silicon by the H_2 - $SiCl_4$ process, the principal species expected during the reduction reaction are H_2, HCl, $SiHCl_3$, $SiCl_2$ and Si. This indicates that the reduction of $SiCl_4$ to Si may be a two step process with an intermediate reduction and formation of $SiHCl_3$ as the reaction gases approach the deposition temperature, i.e.

$$H_2 + SiCl_4 \longrightarrow SiHCl_3 + HCl \quad \text{---------- 2.7}$$

A further increase in temperature, as the $SiHCl_3$ comes into contact with the hot silicon then results in the reduction of $SiHCl_3$ to Si according to equation 2.6.

$$H_2 + SiHCl_3 \longrightarrow Si + 3HCl \quad \text{---------- 2.6}$$

The possibility of a two step reduction process should be taken into consideration in any kinetic analysis of the reaction.

The reaction kinetics of the hydrogen reduction of trichlorosilane are believed to be similar to those of the H_2 - $SiCl_4$ process. The application of these compounds to epitaxial growth has been reported (9, 18) and the process has been carried out in an open tube where silicon is produced at the heated substrate surface. Control of the chemical reaction and nucleation allows the epitaxial growth of the silicon onto the substrate to

occur while the gaseous products of the reaction are removed from the reaction zone. The process should also have the advantage that deposition of layers onto single or multi-substrates can occur and the resistivity and type can be controlled by introducing suitable traces of impurity into the silicon compound, that undergo similar hydrogen reduction or thermal decomposition reactions. In this manner impurity atoms may be incorporated into the growing layer and furthermore alternative layers of different resistivity or type can be deposited to produce multi-layer structures.

The pyrolysis of silane in principle is very simple and follows the reaction:

$$SiH_4 \longrightarrow Si + 4H_2 \qquad 2.8$$

The silane may be obtained by the hydrolysis of calcium or magnesium silicide or from the reaction of silicon tetrachloride with lithium aluminium hydride.

Silane is a colourless gas which ignites spontaneously when released into the atmosphere. Mixtures of silane and air are explosive, over a wide range of composition. When prepared by either of the methods mentioned above, the silane usually contains traces of other hydrides, such as arsine, borane and phosphine. It can be purified by chemical absorption, by condensation and distillation, by the use of suitable cold traps or by a molecular sieve; borane impurities can also be removed catalytically by contact with platinum or Raney nickel. The pyrolytic reaction

$SiH_4 \rightarrow Si + 2H_2$ is appreciable at temperatures above $600^{\circ}C$ and is probably accompanied by the formation of small amounts of polymers, such as disilane (Si_2H_6) and trisilane (Si_3H_6). The decomposition of pure SiH_4 at reduced pressure has been used for the production of hyper pure silicon in reasonably large quantities for the semiconductor device industry, but because the process is dangerous and requires burdensome safety precautions, most manufacturers have turned to the use of methods involving silicon tetrachloride and trichlorosilane. However, if SiH_4 is diluted with hydrogen or a rare gas to a concentration of less than 5% by volume, it is

not pyrophoric and can be stored at a pressure of 1000 psi in a standard gas cylinder.

The pyrolysis can be carried out in a system, similar to that used in the decomposition of silicon tetrachloride, with the exception that the system must be capable of being evacuated.

The most common method of vacuum depositing silicon is by electron bombardment (19, 20, 21, 22). The electron beam locally heats a small portion of a solid silicon block forming molten silicon. The molten silicon then acts as a source of vapour; the solid silicon is supported on a water cooled hearth. A typical electron bombardment arrangement is shown in Figure 2.6. The substrate is held at a positive potential with respect to a filament, placed behind it, emits electrons which heats the substrate by electron bombardment. Radiant heating can also be used but it is less effective.

In a practical system the source of silicon is at ground potential and is heated by bombardment with electrons from another filament. The high negative potential surrounding the filament accelerates and directs the electrons to the desired area of the silicon. The focusing of the beam is a very sensitive function of the geometry of the system but when correctly constructed the heating is confined to an area less than 3 mm. in diameter. Both the source and the substrate are shielded optically from the electron source to limit contamination from the outgassing and evaporation of the filament.

The molten silicon is supported by the solid silicon; this prevents contamination of the vapour since it is only in contact with silicon. This method also permits the temperature of the evaporating silicon to be maintained at several hundreds of degrees centigrade above its melting point. The increased vapour pressure at these temperatures allows higher deposition rates, up to 4μ/minute with a minimum of contamination, to be achieved with systems similar to the type illustrated in Figure 2.6. In practice the source of silicon is bombarded for several minutes to allow

the initial outgassing to be pumped away and to remove surface contamination. A thoroughly cleaned substrate is then heated rapidly to over 1200°C to remove occluded gases and then placed in position over the source. Deposition pressures of 10^{-7} to 10^{-10} torr are used.

Epitaxial growth of silicon by vacuum sublimation (evaporation directly from a solid) avoids the problem of retaining molten silicon, but lower deposition rates (0.3μ/min.) are obtained; suitable apparatus for growing silicon layers by this method using induction heating is illustrated in Figure 2.7. Silicon vapour is transferred from the hot solid (about 1350°C) to the cooler substrate (about 1100°C) at a residual pressure of less than 10^{-8} torr. To prevent contamination all metallic parts are excluded from the system which is made of quartz. Controlled amounts of impurities are added to the films by using a source of silicon of known resistivity. The transfer rate of the dopant from the source reaches a steady state after several hours of heating. The physical arrangement of this technique requires a specially designed vacuum system and is not easily adapted to the fabrication of multi-layer devices or the simultaneous deposition of layers on to a number of substrates.

Although epitaxial films have been obtained by vacuum methods, this type of process does not appear to have the facility for progressive development to meet the following requirements: (i) simultaneous deposition of layers onto a number of substrates, (ii) growth of layers of either type and a range of resistivity, (iii) growth of alternate layers of different resistivity or type to produce a multi-layer structure.

The work which will now be reported in this thesis will be primarily concerned with epitaxial growth by vapour deposition processes, where an ideal epitaxial deposition process should achieve uniform reproducible results at a low temperature, while maintaining crystalline perfection, have a high yield, be safe and economical and use easily obtainable chemicals. The three vapour processes, involving silane, silicon

tetrachloride and trichlorosilane appear to satisfy certain of the criteria, but the dangers associated with the pyrolysis of silane has eliminated this process from the initial investigation. The iodine transfer process appeared to have the same limitation as the vacuum method. The choice of the silicon tetrachloride process was made for the primary investigation of the growth of silicon epitaxial layers, in preference to trichlorosilane, because it was available in small quantities and in extremely pure form.

The apparatus developed for depositing epitaxial layers will now be described.

Table 2.1 Silicon deposition processes. Ref. 15

Deposition reaction	Initial pressure of Si compound, mm Hg	Deposition temp., °C	Flow rate of carrier gas, (liter/min)	Yield, %	Deposition rate, g Si/hr
$SiH_4 \longrightarrow Si + 2H_2$	3-18	770-1335	—	33-85	3-7
$SiI_4 \longrightarrow Si + 4I$	10^{-3} - 2 × 10^{-2}	1000	—	50-80	1-10
$SiCl_4 + 2H_2 \longrightarrow Si + 4HCl$	—	1100	—	small	2.5
$SiBr_4 + 2H_2 \longrightarrow Si + 4HBr$	6	1275	1.5	40	0.36
$SiI_4 + 2H_2 \longrightarrow Si + 4HI$	100	1000	0.5	53	2.6
$2SiHCl_3 \longrightarrow Si + SiCl_4 + 2HCl$	15	1100	13.0	50	10
$2SiCl_2 \longrightarrow Si + SiCl_4$	~240	800-1220	—	—	0.1-0.2
$2SiI_2 \longrightarrow Si + SiI_4$	15-2200	950	—	—	—

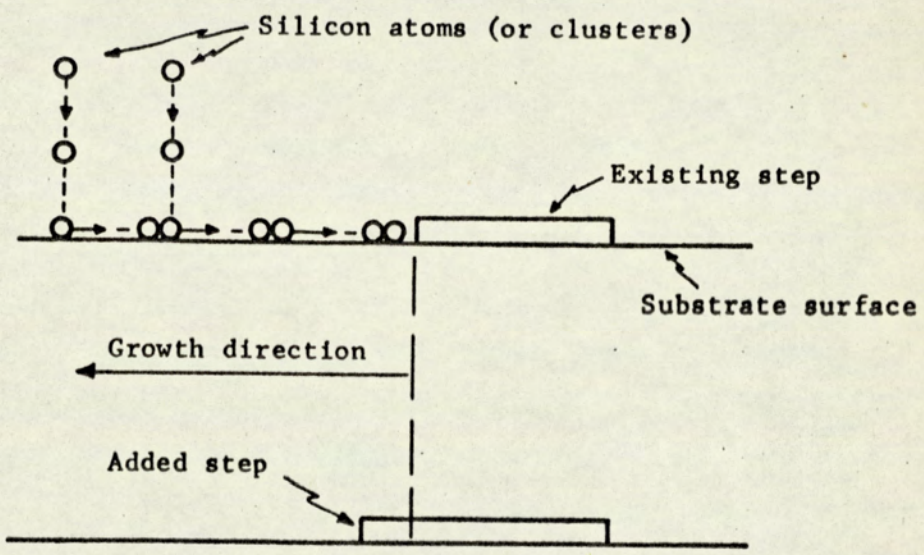


Fig. 2.1 Progress of a step during epitaxial growth

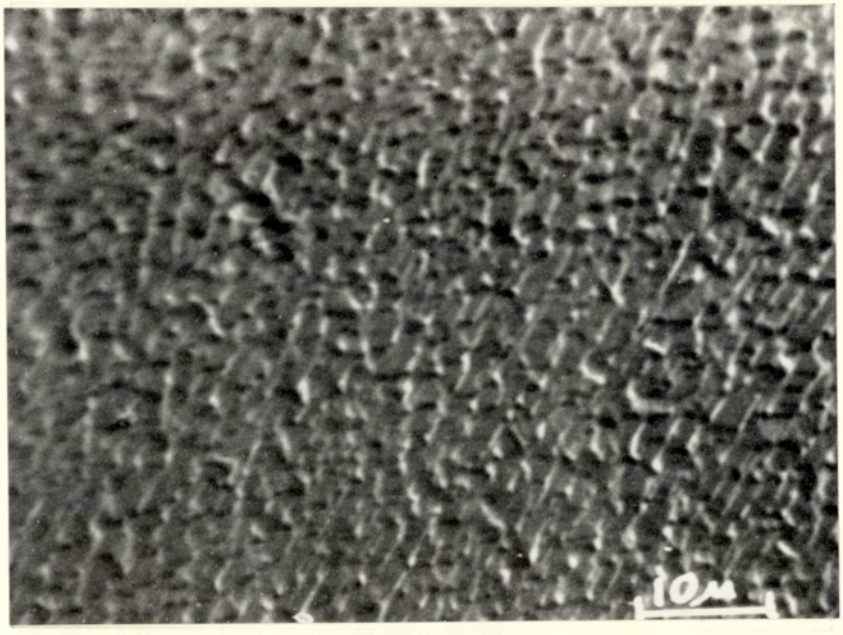
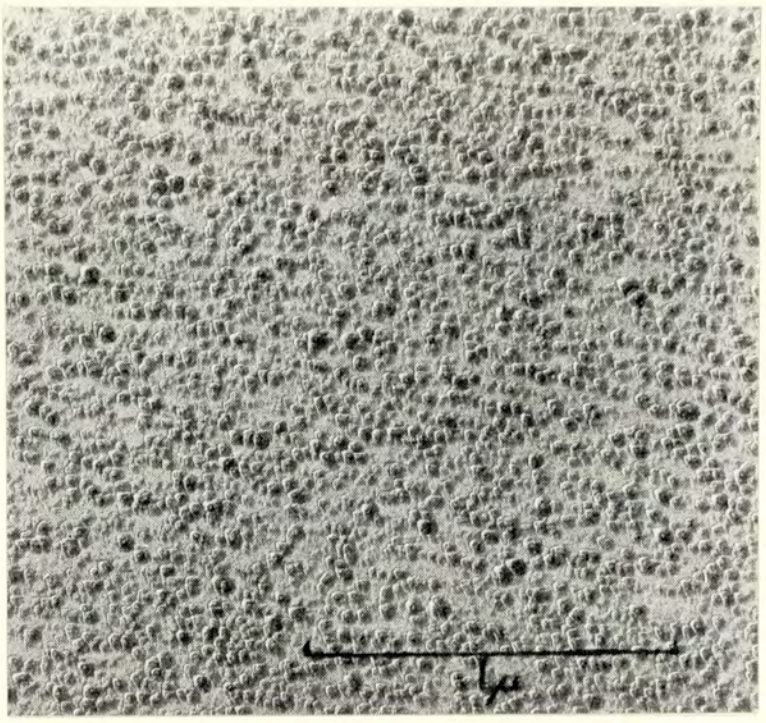
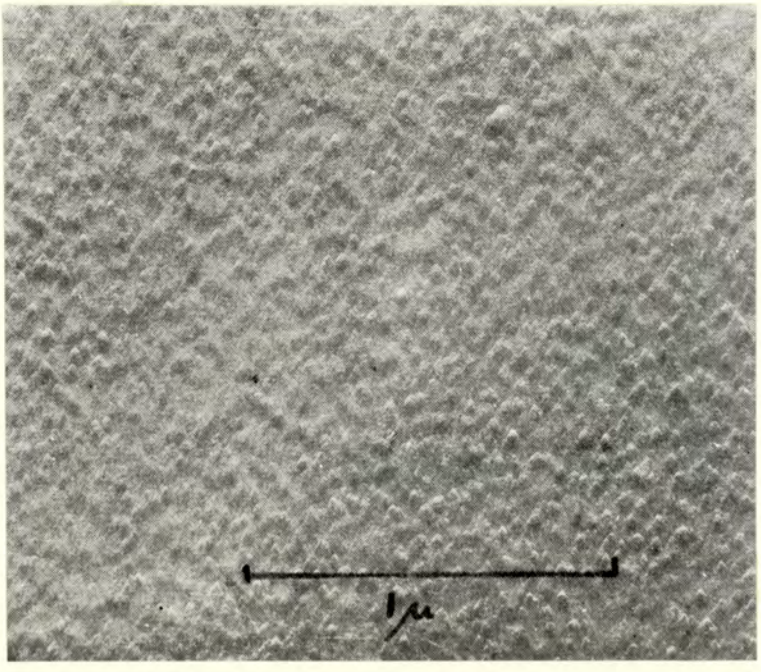


Fig. 2.2 Steps on a layer prepared by sublimation (x500)
Ref. 8



10 sec. of growth



30 sec. of growth

Fig. 2.3 Electron micrograph of Pt-C replica of epitaxial silicon layer on {110} surface after growth at 1250°C. (x40,000) Ref. 9

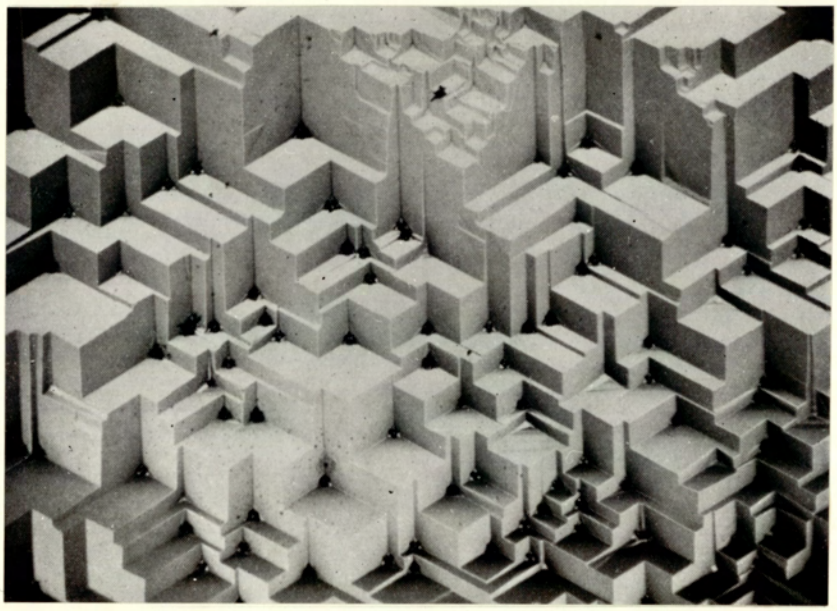


Fig. 2.4 Surface of layer prepared from $SiHCl_3$ at low temperature. (x28) Ref. 8

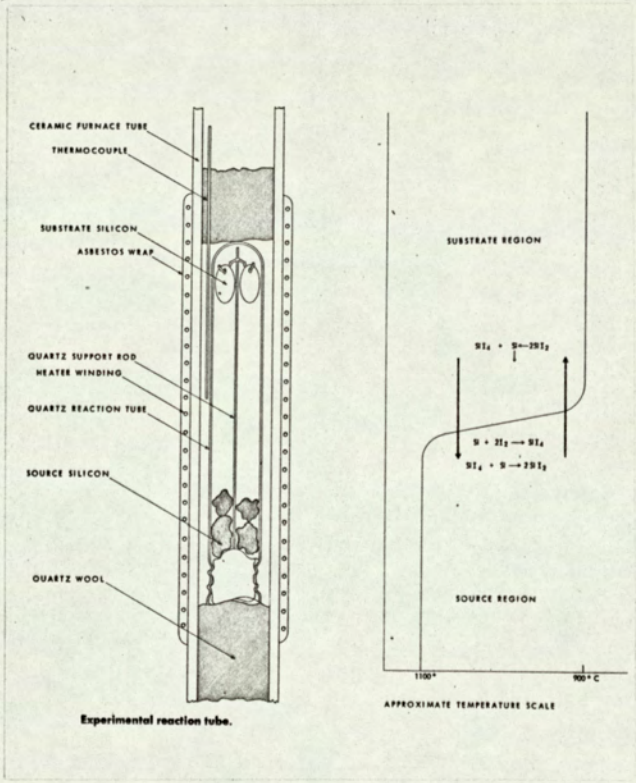


Fig. 2.5 Experimental reaction system. Ref. 4

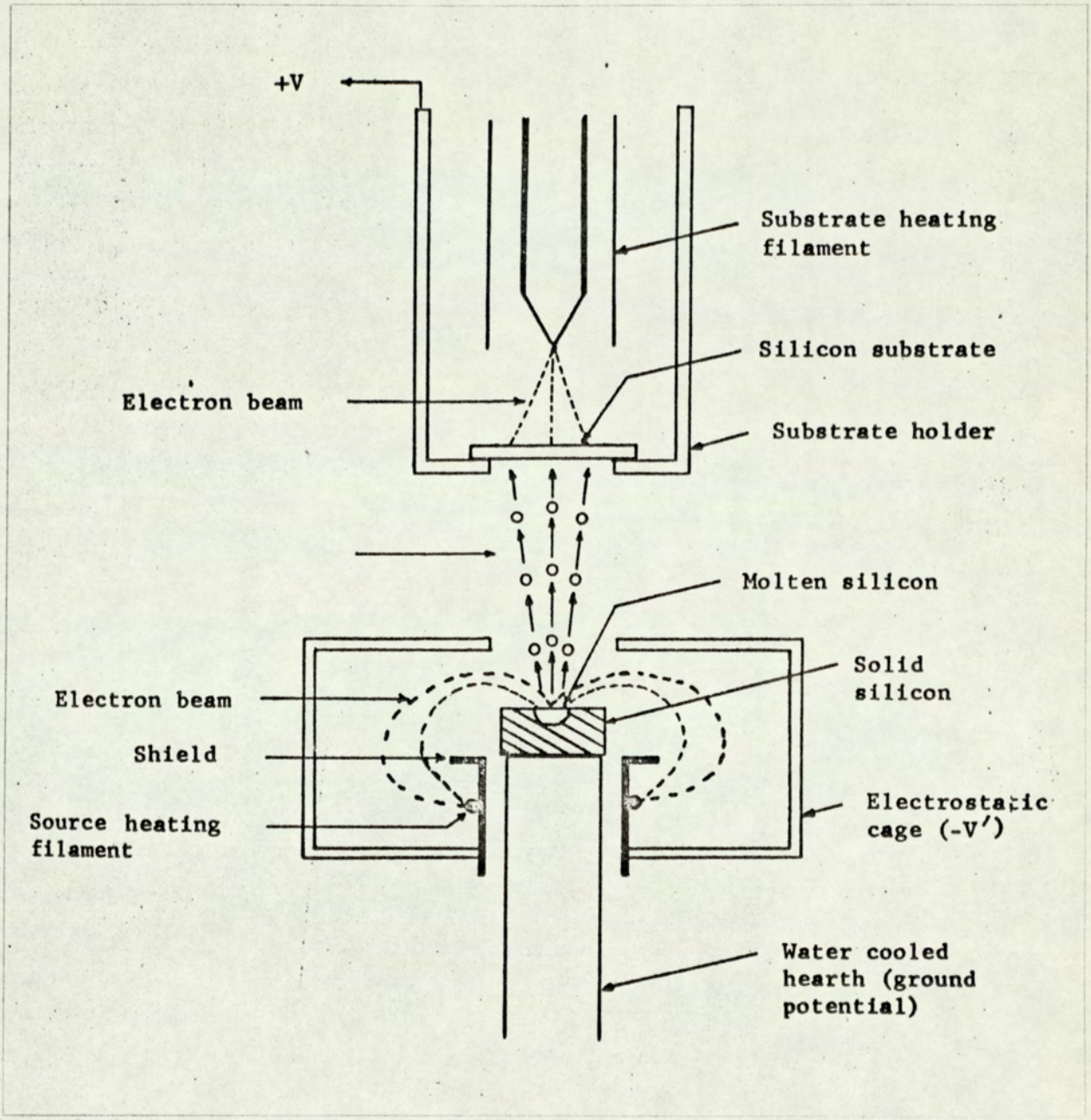


Fig. 2.6 Evaporation and substrate heating by electron bombardment. Ref. 22

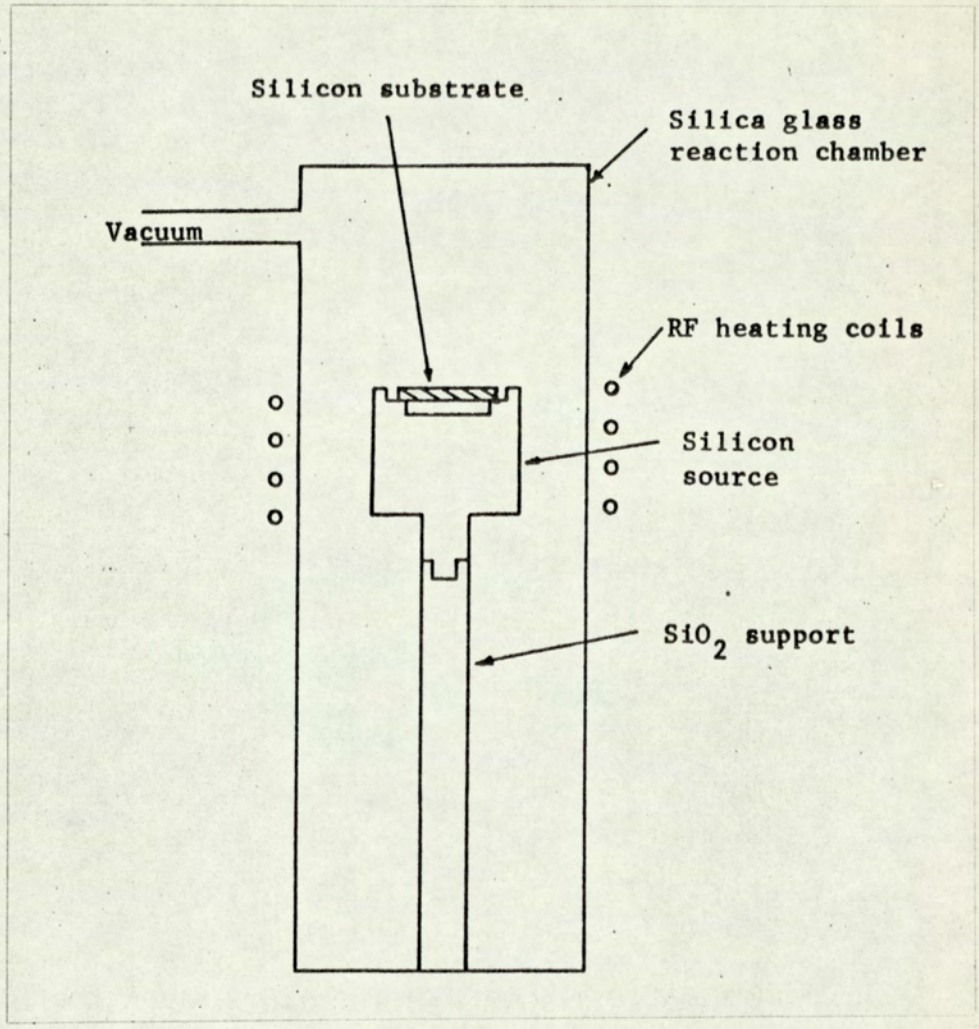


Fig. 2.7 Vacuum sublimation apparatus. Ref. 23

3. DESCRIPTION OF APPARATUS FOR THE DEPOSITION OF EPITAXIAL LAYERS

3.1 Deposition Apparatus

In the deposition apparatus developed initially, it is required to control the flow of hydrogen and silicon tetrachloride to a heated substrate and control the nucleation, growth and impurity level of the growing layer on the substrate. The substrate is supported and heated by radiation from a susceptor which is coupled to an induction heating unit.

The initial apparatus is illustrated in Figures 3.1 and 3.2. Argon and hydrogen gas pressure regulators, with flow control valves, are connected with $\frac{1}{4}$ inch external diameter copper tubing to a deoxo unit and hydrogen flowmeter which is coupled to a gas drying system of one tower of silica gel, three towers of molecular sieve 4A and a liquid nitrogen trap interconnected with P.V.C. tubing. A ball and socket joint connects the liquid nitrogen trap to the evaporator. The silicon tetrachloride evaporator Figure 3.3 consists of two spring loaded three way stopcocks, secured with a small locking pin, connected to the flask so that gas can (A) bye-pass the evaporator and flow into the reaction tube, (B) pass into the evaporator through the silicon tetrachloride and out to the atmosphere and (C) pass into the evaporator through the silicon tetrachloride and into the reaction tube. The quartz flask is connected to the evaporator with a B.24 cone and socket and the quartz inlet tube connected to the cone unit with a graded seal. The evaporator is situated in a vacuum jar containing solid carbon dioxide, methylated spirits and water for temperature control. The evaporator is connected to the reaction tube with a ball and socket joint and graded seal. "Kel-F"* grease is used on all ground glass joints.

The quartz reaction tube of 35 mm internal diameter has an optical flat top for observing the substrate temperature, a D.40 cone at the bottom and an inlet near the top for connection to the evaporator. A pyrex cooling jacket surrounds the quartz tube and is held in position by water cooled clamps which allow compressed air to blow through the jacket. An induction

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* Kel-F registered trade-mark of 3M Company for its fluorocarbon polymers.

heating coil of $\frac{1}{4}$ inch external diameter copper tubing containing 6 turns over a length of two inches is situated at the centre of the tube and connected to a $7\frac{1}{2}$ K Watt 750 Kc/s Delapena Induction heating unit.

A pyrex extension of the reaction tube with D.40 socket and side outlet has a stainless steel end cap, through which passes a quartz support rod joined at the top to a small quartz tube supporting the susceptor. The rod is clamped into position and sealed with an O-Ring allowing its height to be adjusted. Removal of the pyrex extension unit allows the susceptor and substrate to be withdrawn from the reaction tube.

The side arm of the pyrex extension is connected to a trap of activated charcoal in liquid nitrogen, a non-return valve, small silicone bubbling unit and a dreshal bottle.

The complete apparatus is situated in a fume cupboard connected to an extraction unit.

The temperature is monitored with a Land Radiation Pyrometer type QS/100/20, sighted on to the substrate through the optical flat of the reaction tube, and connected to a Leeds and Northrup temperature recorder.

As the investigations of silicon deposition proceeded the following modifications were incorporated in the apparatus Figure 3.4.

1. Gas drying with liquid nitrogen was not necessary and the gas drying towers were replaced with Birlec molecular sieve driers containing internal regenerative heating.
2. Separate control valves, flowmeters and driers for hydrogen and argon were incorporated in the gas circuit.
3. Two evaporator units were connected in series to obtain consecutive evaporation of different types of silicon tetrachloride.
4. The vertical reaction tube was replaced with a horizontal quartz reaction tube Figures 3.5, 3.6. The tube 36 inches long and 50 mm internal diameter, has an induction heating coil, 6 inches long of 9 turns of $\frac{1}{4}$ inch external diameter

copper tubing situated at the tube centre. The ends of the tube are fitted with stainless steel units sealed with O-rings through which the gases can enter and leave. Experiments were made with gases entering (A) at one end of the tube to give gas flow along the tube and (B) through a quartz inlet tube, situated in the top of the reaction tube, of 7 mm external diameter and 5 mm internal diameter containing gas outlet holes Figure 3.7 allowing the gases to enter above the substrate.

The apparatus had a number of limitations:-

1. The gas system was often the source of leaks at the ground glass stopcocks and joints due to the volatile and reactive silicon tetrachloride which affected the sealing greases and reacted with moisture in the atmosphere. The leaks resulted in the deposition of poor quality layers and frequent dismantling of the apparatus for cleaning.

2. Temperature control, of the substrate was difficult and melting of the silicon would occur while temperature control of the silicon tetrachloride was not consistent.

3. During deposition in the vertical reaction tube, yellow-brown films were deposited on the quartz in the hot zone. In order to clean the reaction tube after each run the cooling system had to be dismantled.

4. With the horizontal reaction tube, a number of substrates could be processed in one operation cycle compared with one substrate per cycle in the vertical system. It has not been possible to obtain uniform layers on a number of substrates in the horizontal tube because the maximum gas flow of 3.5 litres/minute at N.T.P. was too low.

5. The number of gas inlet and control lines in the system is inadequate for future work.

To overcome the above limitations and to further investigate and develop the process, a completely new "Multideposition apparatus" was designed and constructed. This apparatus has a horizontal reaction tube

and uses improved gas plumbing techniques.

A schematic layout of the multideposition apparatus is shown in Figures 3.8, 3.9 and 3.10.

The gas lines from gas pressure regulators are connected in turn to Millipore filters, Fischer and Porter series 10A3200 flowmeters with 5 inch scale length interchangeable meter tube and float and integral needle valve. The needle valves are connected to a PTFE manifold Figure 3.11. The argon, hydrogen and hydrogen chloride have a common inlet line while the silicon tetrachloride and doped gases have individual gas lines to the manifold. The outlet of the manifold is connected to the reaction tube.

Silicon tetrachloride is introduced into the system by bubbling hydrogen through a quartz evaporator Figure 3.12. This evaporator is a sealed unit with a gas inlet connected to a sintered bubbling unit within the evaporator. The gas outlet is of larger diameter to enable it to be used for filling the evaporator with silicon tetrachloride. The inlet and outlet are connected to Springham High Vacuum Greaseless stopcocks with Viton A diaphragms which completely sealed the evaporator gas lines. The evaporator has an approximate capacity of 1 litre and is sited in a Grant's low temperature bath containing odourless kerosene.

The quartz reaction tube of 50 mm internal diameter and 36 inches long is integrally constructed with an outer jacket for water cooling. The gas inlet of the reaction tube is coned to the same diameter as the quartz tubing, while the outlet has a stainless steel cap sealing with an O-ring through which the outgoing gases pass into a PTFE tube and finally to an extraction system. A quartz sledge supports the susceptor at a small angle to the incoming gases in the reaction tube.

The reaction tube is situated inside an induction heating coil of $3\frac{1}{8}$ inches internal diameter constructed from 5/16 inches external diameter copper tubing and length 6 inches and coupled to a Wild Birfield $7\frac{1}{2}$ K Watt 500 Kc/s induction heating unit. Temperature control was automatic via a Land Radiation Pyrometer Type QS/100/20, sighted on to the susceptor through

the coil and connected to a Kent Potentiometric temperature indicator, recorder and temperature controller with a feed back to the generator.

The equipment was housed in two fume extracted cabinets and the entrances around the reaction chamber were fitted with safety glass.

All the gas lines were constructed from $\frac{1}{4}$ inch external diameter stainless steel tubing connected by Ermeto compression fittings while the silicon tetrachloride gas line from the needle valve via the evaporator to the PTFE manifold was of 8 mm external diameter quartz tubing. Quartz tubing also connected the PTFE manifold to the reaction tube. PTFE coupling units containing O-ring seals, which are shown on the gas inlet and outlet of the evaporator Figure 3.12, were used to make all the connections not joined by Ermeto fittings. After experiments with sealing materials, Viton 75 was found to be the most satisfactory and hence used for all O-ring seals.

The hydrogen and argon gas lines are connected to Puridriers which contain Deoxo catalysis units and molecular sieve driers. All gases were filtered with 0.8μ MF Millipore filters of mixed esters of cellulose with the exception of the hydrogen chloride which reacted with these filters and was passed through a 5.0μ Teflon filter.

The gas control section, once assembled, was a sealed unit and only the gas line from the evaporator had to be broken when it required filling. The reaction tube can easily be removed for cleaning by disconnecting one PTFE coupling. When this coupling is broken, argon purge gas flows through the gas system to prevent in diffusion of gases from the atmosphere.

In practice and with the requirement for development of the process it was found that gases contained in the inlet arms to the PTFE manifold diffused out. This resulted in (A) contamination of the gases flowing into the reaction tube and (B) the halide vapour present in the manifold reacting with the stainless steel inlet lines.

To overcome these problems, the PTFE manifold was replaced with a quartz manifold so that the argon purge gas and hydrogen gas flushed out all other gases entering the manifold. The volume of the side arms of the

manifolds connected to the needle valves were kept to a minimum to reduce the possibility of out diffusion from the side arms.

The design of the susceptors was important; they have the general shape shown in Figure 3.13. The substrate rests on the top of the susceptor which was slightly recessed to stop the substrate sliding off. A number of susceptor materials were investigated.

High purity silicon cannot be coupled directly into an induction heating coil below approximately 600°C and hence a composite silicon susceptor Figure 3.13(1) which could be coupled at room temperature was made by joining high resistivity and low resistivity silicon rods together in a float zone apparatus and machining the composite rod to the required shape. The high resistivity end being used to support the substrate. The first type of susceptor was expendable because it was found to melt easily and required remachining, as silicon layers were deposited on its surfaces. This operation was very difficult because the silicon had become brittle and easily fractured during machining.

A second type was a graphite susceptor enclosed in quartz Figure 3.13 (2). A graphite cylinder was sealed in vacuum into a quartz container, so that the top face of the cylinder was against an optical quartz disc which formed the supporting surface of the substrate. In practice the required temperature of the substrate was not obtained before the quartz distorted producing an uneven supporting surface and temperature distribution.

While these two types of susceptor enabled the impurity contamination to be minimal they were unsatisfactory in practice. This led to the development of a graphite susceptor which is easily coupled to an induction heating coil.

Hawker Siddeley Supergraph graphite produced from Morgan Crucible type EYX600 graphite and impregnated by the Hawker Siddeley F.A.C. treatment and of density 1.88 was used. This density is higher than that obtained with conventional graphites. In use the material contaminated the substrate surface and retarded epitaxial nucleation. The contamination was overcome

by precoating the susceptor with approximately 15 micron layer of silicon Figure 3.13(3)-in the deposition apparatus. When the surface of the susceptor became uneven or contaminated it was possible to etch off the silicon with CP_4* and deposit a new coating.

This type of susceptor was also used in the horizontal reaction system Figure 3.14.

Further development involved the use of Le Carbone graphite Type 5890 PT, coated with silicon. This material had a total purification treatment resulting in a total ash content of the graphite of less than 5 ppm which contained an average of 0.5 ppm boron with silicon, vanadium and magnesium.

With the development of the epitaxial process it became necessary to use a susceptor whose surface had not previously supported substrates for deposition. Thus after each deposition of silicon on to the substrate the susceptor had to be cleaned and a new silicon coating deposited. In order to eliminate the recoating an alternative protective layer of silicon carbide for the susceptor was investigated.

Experiments were made to deposit silicon carbide by introducing carbon tetrachloride vapour, silicon tetrachloride and hydrogen into the deposition apparatus. Small test samples supported on the main susceptor were coated with silicon carbide at approximately 1400°C. Unfortunately due to the power limitations of the induction heating generator it was not possible to obtain the graphite susceptor to 1400°C for coating with silicon carbide.

Silicon carbide susceptors Figure 3.15 were obtained from Texas Instruments with the trade name "Te-Kote ScS". The surface coating of the susceptor has a fine crystalline structure with smooth surface and is impermeable to gases, has excellent thermal shock resistance and chemical inertness to the reaction products at the deposition temperature and the 3:1 nitric acid and hydrofluoric acid mixture used for cleaning the

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*CP_4 5 parts nitric acid, 3 parts acetic acid and 1 part hydrofluoric acid.

susceptor. Silicon epitaxial material produced using silicon carbide coated susceptors was comparable with material grown on silicon coated susceptors which have now been superseded.

The temperature of the silicon substrate was continuously monitored with the Land Radiation pyrometer type QS/100/20 which had a minimum target area of 0.20 inches when focussed at 20 inches and the output was displayed on a Leeds and Northrup temperature recorder. The deposition apparatus was designed so that the pyrometer could be focussed through the reaction tube on to the substrate surface.

The pyrometer was calibrated under black body radiation conditions, but when used in the present work it was found to read approximately 130°C low. This low reading was due to: (1) Absorption of radiation by the quartz reactor tube and gases and (2) the emissivity of silicon. To calibrate the instrument under the experimental conditions, the silicon melting point was used for the temperature calibration point. At this calibration temperature the difference between the true temperature and the one indicated by the Land Radiation pyrometer is due to the sum of (1) and (2) above. The emissivity correction of silicon at different temperatures has been determined by Allen (24) and thus at the calibration temperature the correction of absorption can be determined. It was assumed that this absorption correction remained constant over the range 1000°C - 1420°C. The true temperature as calculated for emissivity and absorption corrections are shown in Table 3.1.

The output of the Land Radiation pyrometer was not linear with temperature and when displayed on the linear Leeds and Northrup recorder it appeared insensitive to changes in the lower temperature and very sensitive to temperature fluctuations in the high range. The temperature control of the substrate was obtained by manually adjusting the power input of the induction heating unit in conjunction with the visible observation of the recorder, but due to its variable sensitivity this was sometimes difficult to achieve.

The recorder was replaced with a Kent Mark 3 Electronic recorder, which had a partial linearising circuit designed for the output of the Land pyrometer over the temperature range of interest in this work and an adjustment which automatically corrected for emissivity and absorption errors when calibrated at the melting point of silicon.

This recorder resulted in better temperature control being obtained by manual adjustment, but eventually it was modified for automatic temperature control with feed back to the generator.

Before the apparatus was assembled all internal surfaces of the components were scrupulously chemically cleaned.

The Pyrex components of the initial deposition apparatus were treated in boiling ICI Alkaline Degreasing Agent No.I which is mainly caustic soda with a small amount of sodium metasilicate and wetting agent, while the quartz apparatus was swilled in 20% hydrofluoric acid. To remove the deposits in the quartz reaction tube 40% hydrofluoric acid was required, which etches the quartz and hence this cleaning must be used for the minimum of time.

All the components of the multideposition apparatus are cleaned with boiling Decon 75 which is a non-foaming surface-active agent, a 2% solution having a pH of 10. Deposits in the quartz reaction tube were removed with 3:1 mixture of nitric acid and hydrofluoric acid. However, the deposition products in the water-cooled reaction tube tend to ignite in contact with the nitric acid and extreme care must be exercised when carrying out this operation.

After cleaning with the necessary reagents all components were rinsed in deionised water to remove all traces of the cleaning agents and dried at 120^{o}C, with the exception of the PTFE components which were dried at 50^{o}C, in an air circulating oven and allowed to cool where the minimum of dust can enter the components.

When assembling the apparatus care was taken to ensure that the operator or other external factors did not contaminate the internal parts.

Prior to operation of the apparatus for deposition all gas lines and evaporators are purged with their respective gases to ensure that all required flow lines are functioning, evaporators are in equilibrium and no impurities are present in the system. The operation procedure is then as follows:-

1. Clean substrates are loaded on the susceptor which is positioned in the reaction tube, with argon purge flowing.
2. Purge for 5 minutes with argon.
3. Purge for 15 minutes with hydrogen.
4. Substrate brought to required temperature over a period of approximately 15 minutes.

5A. Substrate held at this temperature for 30 minutes to clean surface and anneal defects. This operation was later replaced with (5B).

5B. Hydrogen chloride polish for specified time, followed by 5 minutes hydrogen purge.

6. Silicon deposition for required time.
7. Cool over a period of approximately 15 minutes.
8. Purge with argon.
9. Remove susceptor and substrate from reaction tube with argon purge flowing.

3.2 Substrate Preparation

A clean substrate surface, free of deformation and imperfections is necessary for good single crystal epitaxial growth. Substrates were prepared from Czochralski or Float Zoned silicon single crystal doped with the require element to the specified resistivity by a series of mechanical lapping and polishing operations with successive reduction in particle size of the abrasive followed by chemical polishing.

In order to undertake mechanical polishing, the silicon single crystal was mounted in wax on a wooden block and cut to the required orientation and thickness of wafer on a type TRA10 Felma Automatic cut off

machine. The wafers were then mounted on a lapping block, with the minimum of carnauba wax and the free side lapped with 13μ alumina lapping abrasive on a Lapmaster 12 inch lapping machine to a flat saw cut free surface. The wafers were turned over on the same side of the block and lapped to specified thickness, ensuring that all saw marks were removed.

After lapping the wafers were removed from the lapping plate, ultrasonically cleaned in trichloroethylene, remounted on a polishing plate Figure 3.16 with the minimum of wax and polished on an Automatic Cooke, Troughtman and Simes Polishing unit using diamond compound. Polishing was started on Hyprocel PA-K pad with 8μ diamond, which was successively changed to 6μ, 3μ, 1μ and ½μ diamond and the last three grades of polishing were on a Selvyt pad.

When the substrates had a scratch free, planar mirror surface, as observed by viewing with the naked eye in reflected light, polishing was discontinued and the substrates removed from the polishing plate. The substrates were cleaned in trichloroethylene, wiped with a Kleenex tissue and stored between polythene discs in a suitable container.

Before the substrates were used for deposition, they were cleaned ultrasonically in trichloroethylene and dried in a blast of air.

After the mechanical polishing operation the substrates were chemically polished by one of these methods.

Aqueous Polishing

Individual silicon substrates were immersed in 50 ml of CP_4 etching solution, quenched after polishing with deionised water and dried in hot air. The polishing rate was approximately 25 microns per minute and about 25 microns were removed from the surface.

Electro Polishing

The apparatus used for electropolishing was similar in basic design to that reported by Baker (25) and is shown in Figure 3.17. The lapped surface of the substrate was mounted on a 2 inch diameter quartz disc, ⅜ inch thick which contained holes concentric with the centre of the

substrate. These holes allowed electrical connections to be made to the rear of the substrate by a brass pin held in position with a spring connected to a copper bush which serves as the final anode terminal and as a pivot around which the holder can rotate-Figure 3.18. The cathode is a rotating 9 inch diameter stainless steel plate pieced by closely spaced 1/16 inch diameter holes filled with polystyrene and driven by a variable speed motor. The electrolyte-Table 3.2 is pumped to the plate surface where it spreads and thus supports the work holder on a film of uniform thickness. The difference in velocity of the electrolyte at the inner and outer edge of the work holder causes the disc to rotate. When the electrolyte has spread to the edge of the disc, it is flung off, collected in a surrounding polythene trough and recirculated.

The voltage across the cell was approximately 15 volt with current density of 100 ma/sq.cm. with a rotation speed of the plate of 40 revs/minute.

The electrolyte was prepared at room temperature, but warms up to approximately 30°C during polishing. These conditions remove approximately 0.8 microns per minute and polishing was usually for a period of 30 minutes.

Gaseous Polishing

Gaseous polishing is performed in the epitaxial apparatus, prior to silicon deposition. A 2.5% mixture of anhydrous hydrogen chloride in hydrogen is passed over the substrate at the deposition temperature. After polishing the reaction tube is purged with hydrogen before silicon deposition. The polishing rate is approximately 1.5 microns per minute and approximately 15 microns of the surface are etched off.

The techniques for evaluating the mechanical, electrical and structure of epitaxial layers will now be discussed.

TABLE 3.1

Temperature corrections for emissivity and apparatus absorption

Land Radiation Pyrometer Reading	Emissivity Correction	Apparatus Correction	True Temperature
965°	40°	29°	1034°C
1023°	46°	29°	1098°C
1077°	54°	29°	1160°C
1125°	61°	29°	1215°C
1173°	68°	29°	1270°C
1203°	73°	29°	1305°C
1238°	79°	29°	1346°C
1295°	91°	29°	1415°C

TABLE 3.2

Electrolyte composition for electropolishing
0.01 ohm cm N silicon substrates

20 ml. hydrofluoric acid

200 ml. deionised water

200 ml. glycerol

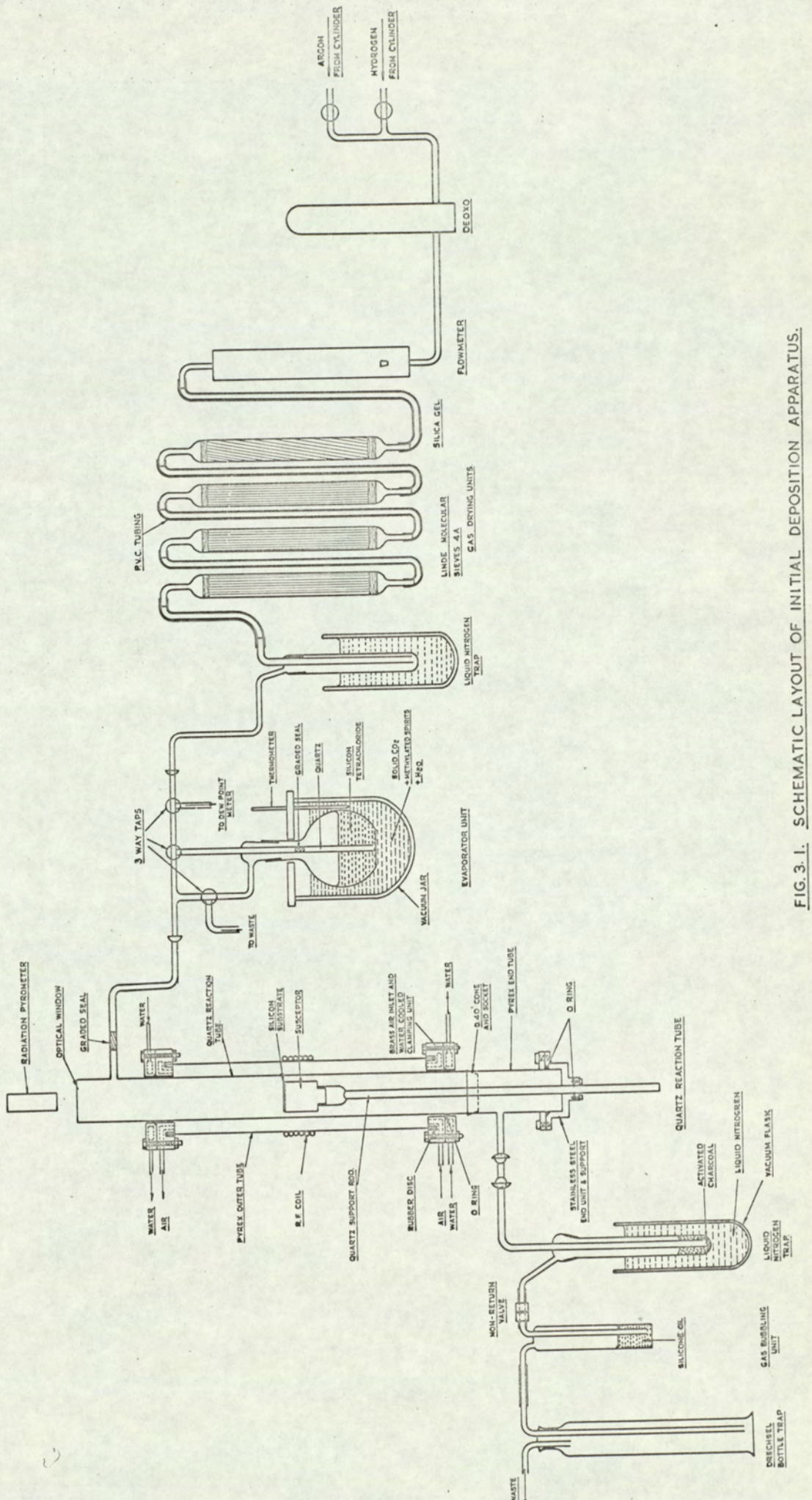

FIG. 3.1. SCHEMATIC LAYOUT OF INITIAL DEPOSITION APPARATUS.

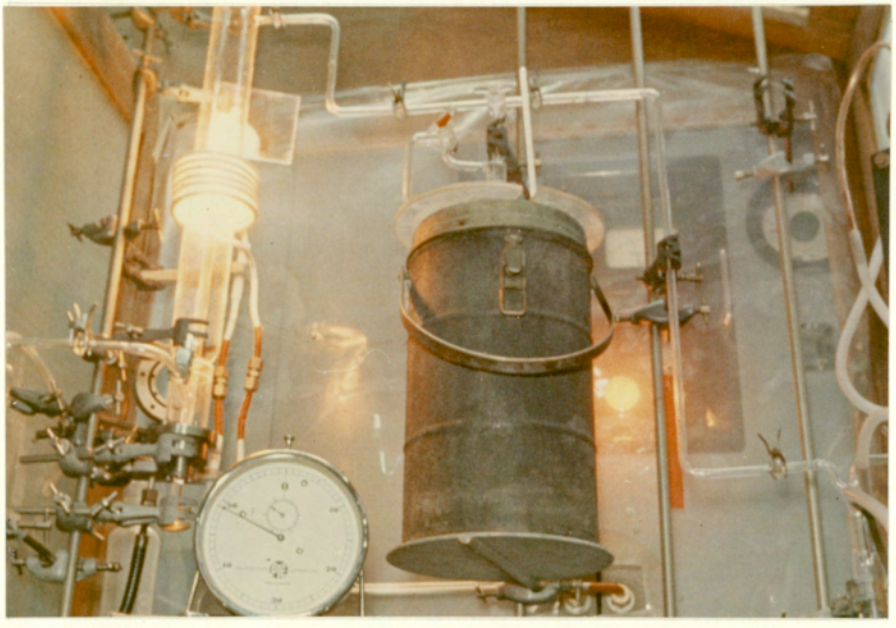

Fig. 3.2 Initial deposition apparatus

Fig. 3.3 Silicon tetrachloride evaporator for the initial deposition apparatus

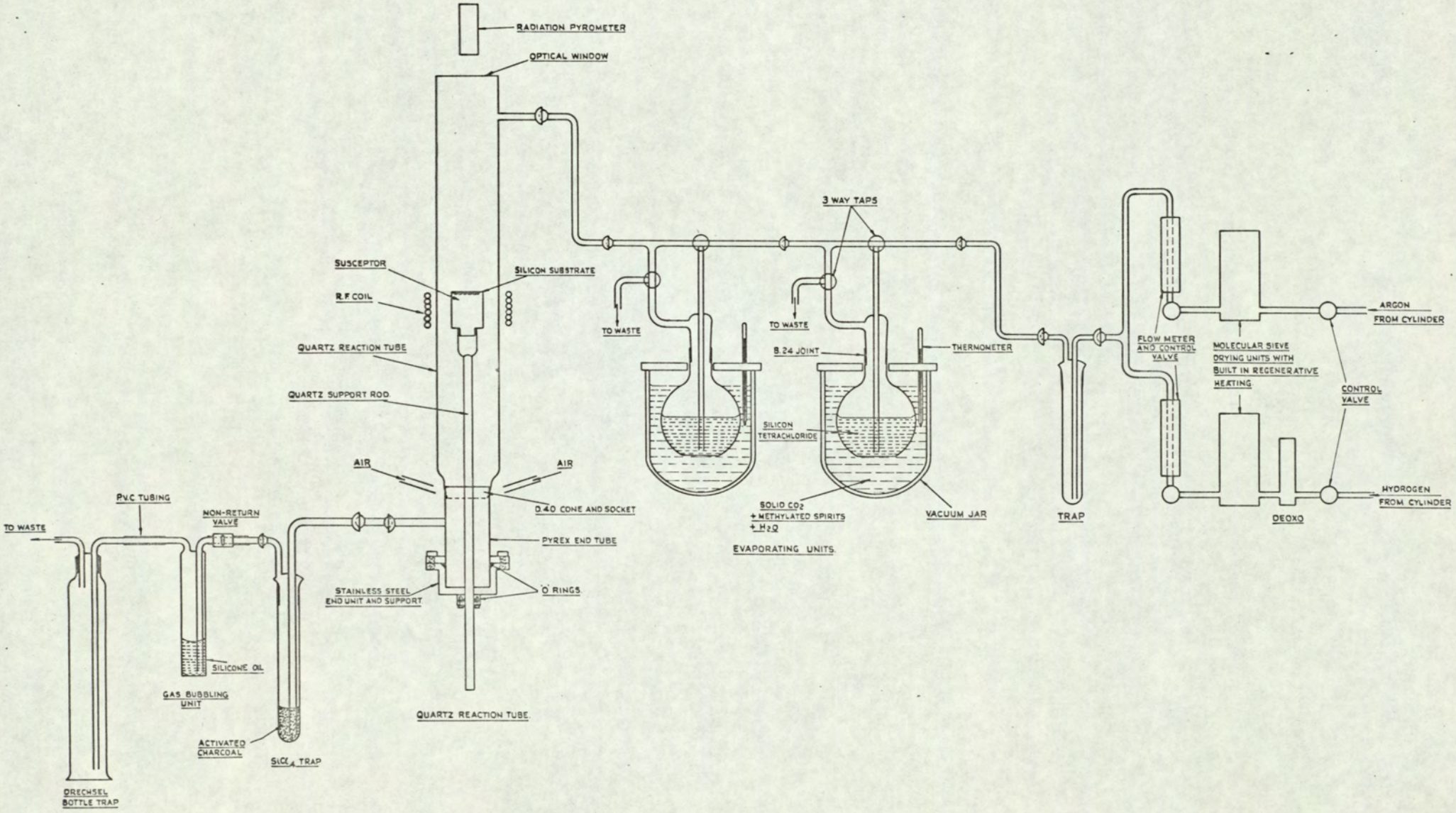

FIG. 3.4. MODIFICATION OF THE INITIAL DEPOSITION APPARATUS.

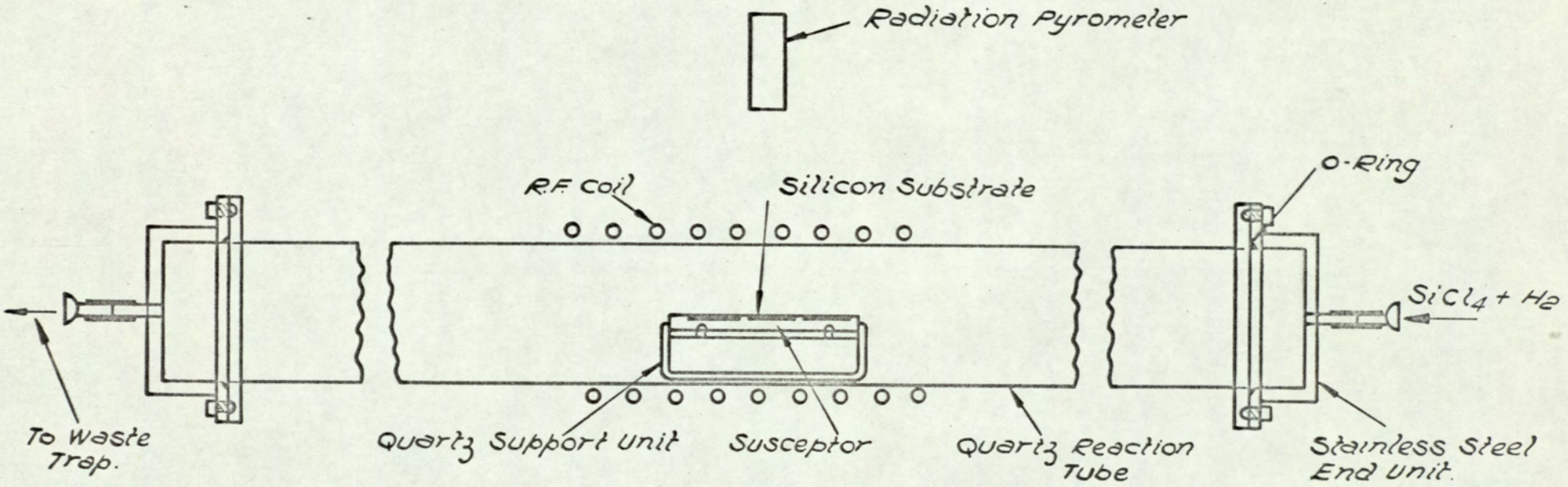

FIG. 3.5. HORIZONTAL DEPOSITION REACTION TUBE - HORIZONTAL GAS FLOW.

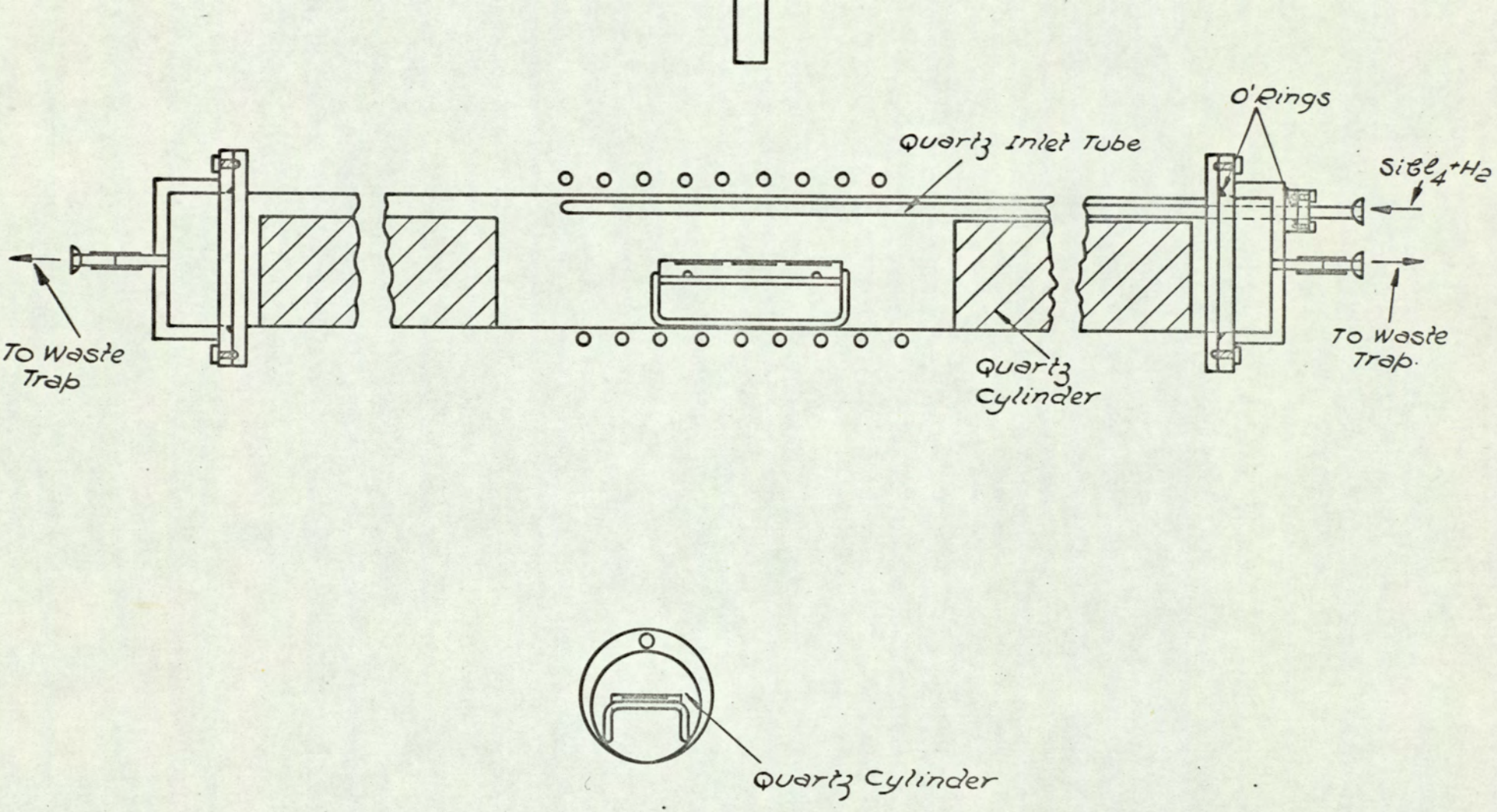

FIG. 3.6 HORIZONTAL DEPOSITION REACTION TUBE – VERTICAL GAS FLOW.

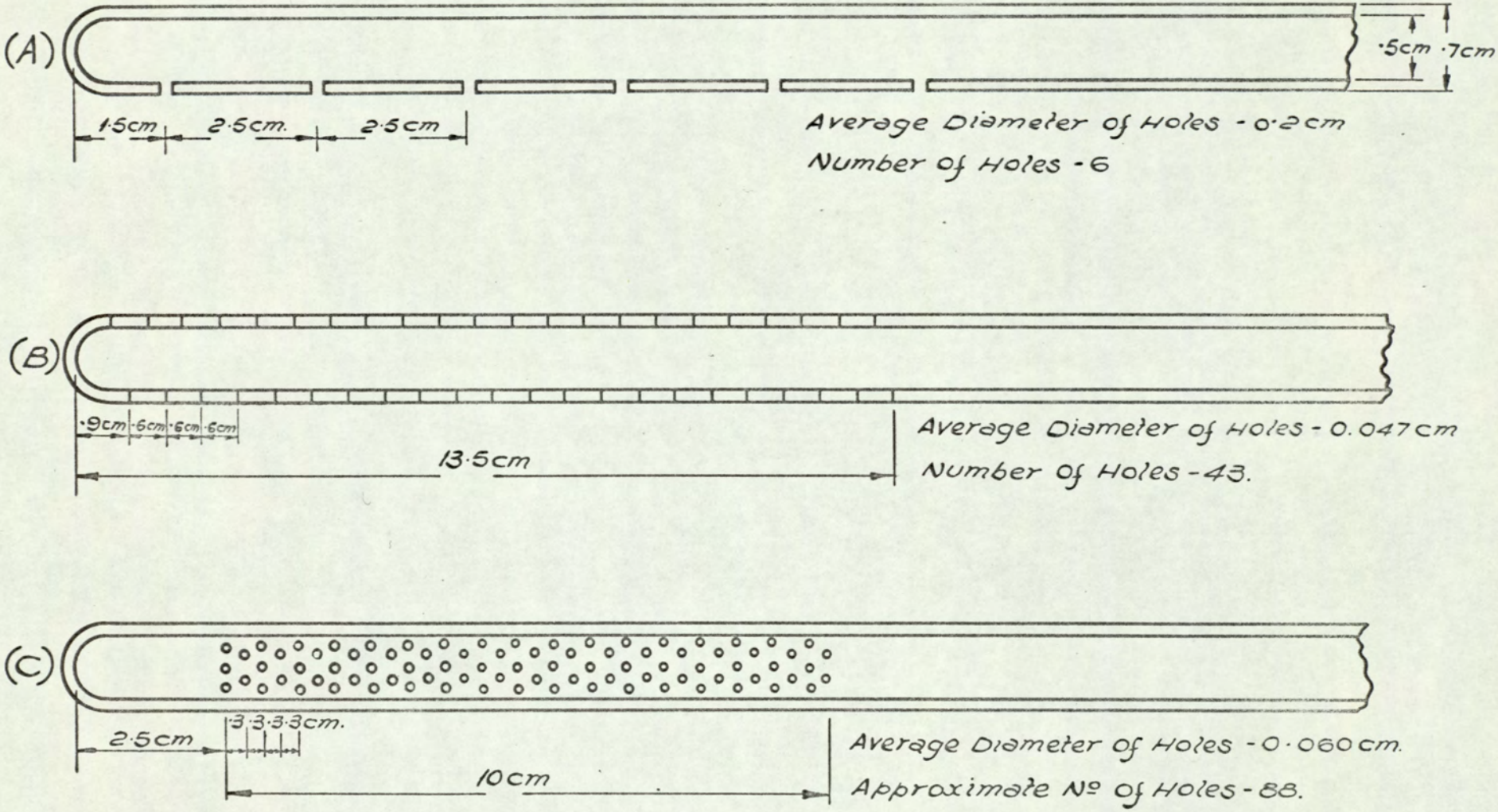

FIG. 3.7. QUARTZ INLET TUBES FOR VERTICAL GAS FLOW IN HORIZONTAL REACTION TUBE.

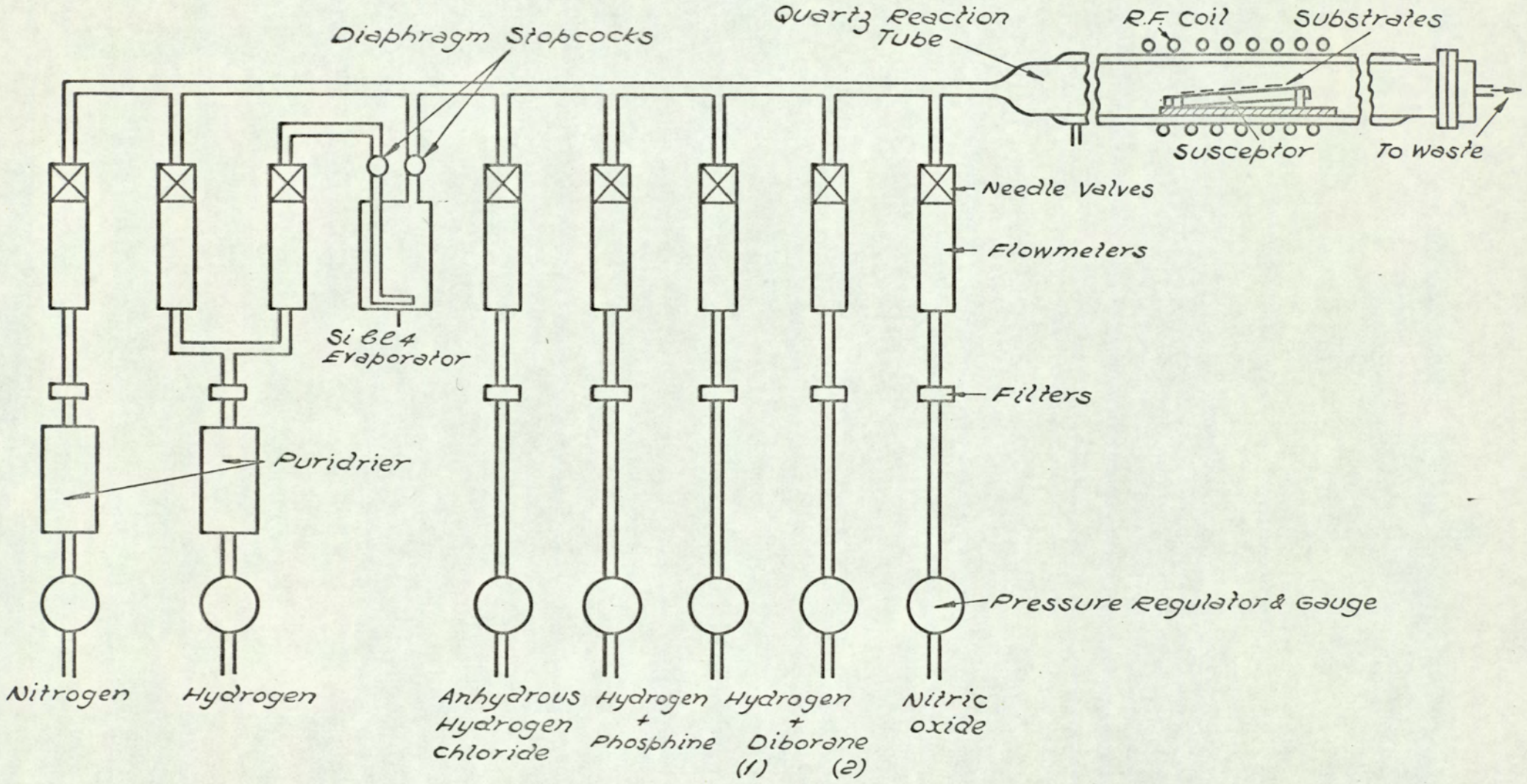

FIG.3.8 SCHEMATIC LAYOUT OF THE MULTIDEPOSITION APPARATUS.

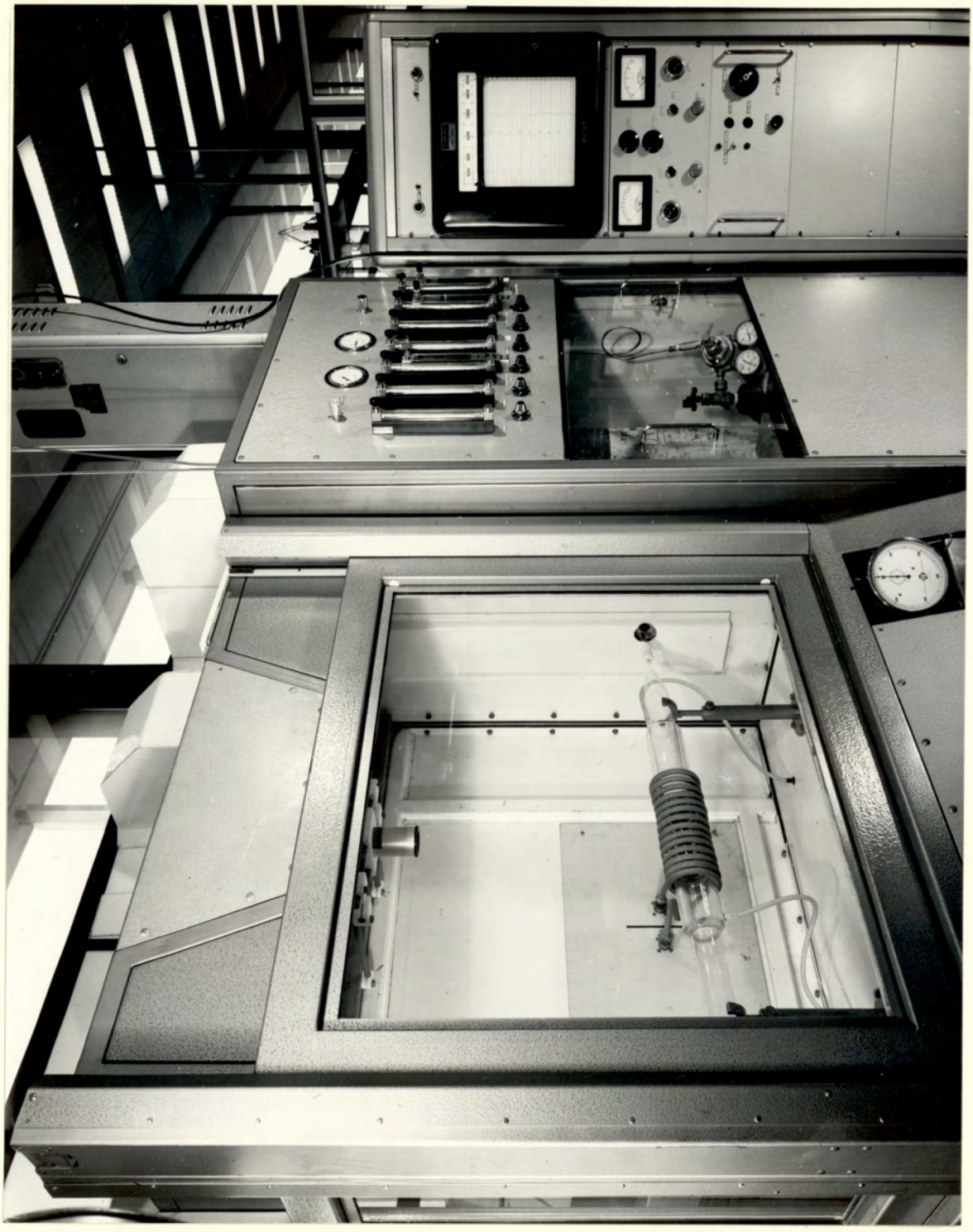

Fig. 3.9 Multideposition apparatus

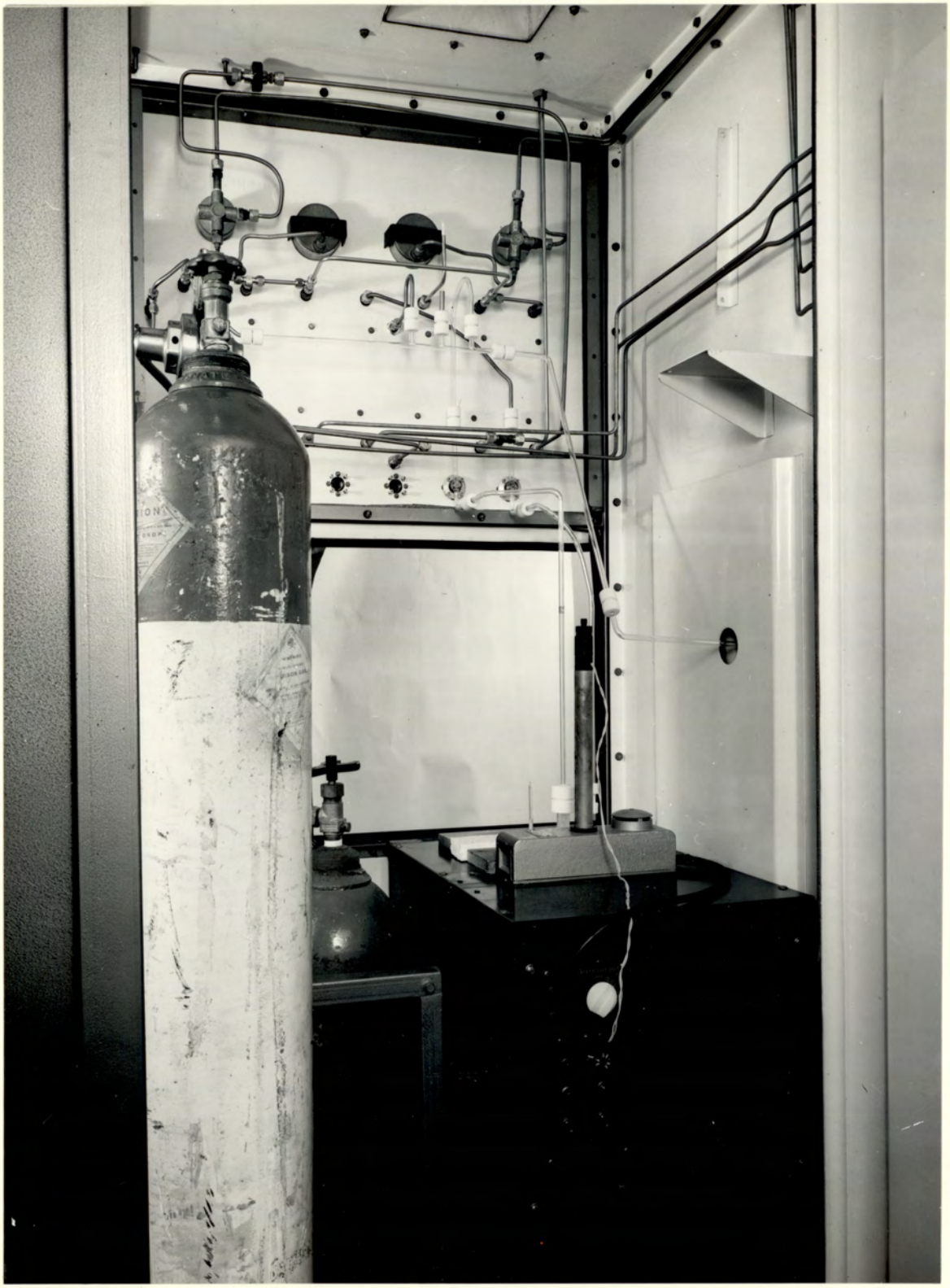

Fig. 3.10 Multideposition apparatus

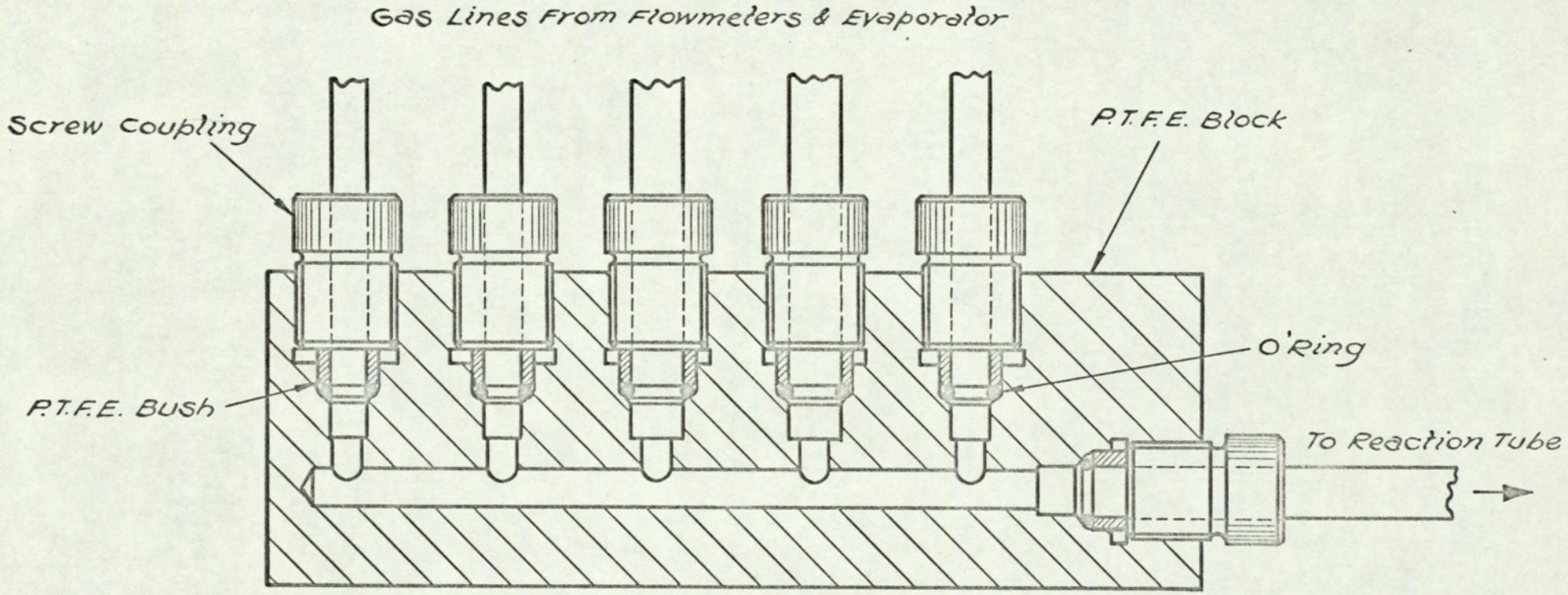

FIG. 3.11. P.T.F.E. MANIFOLD.

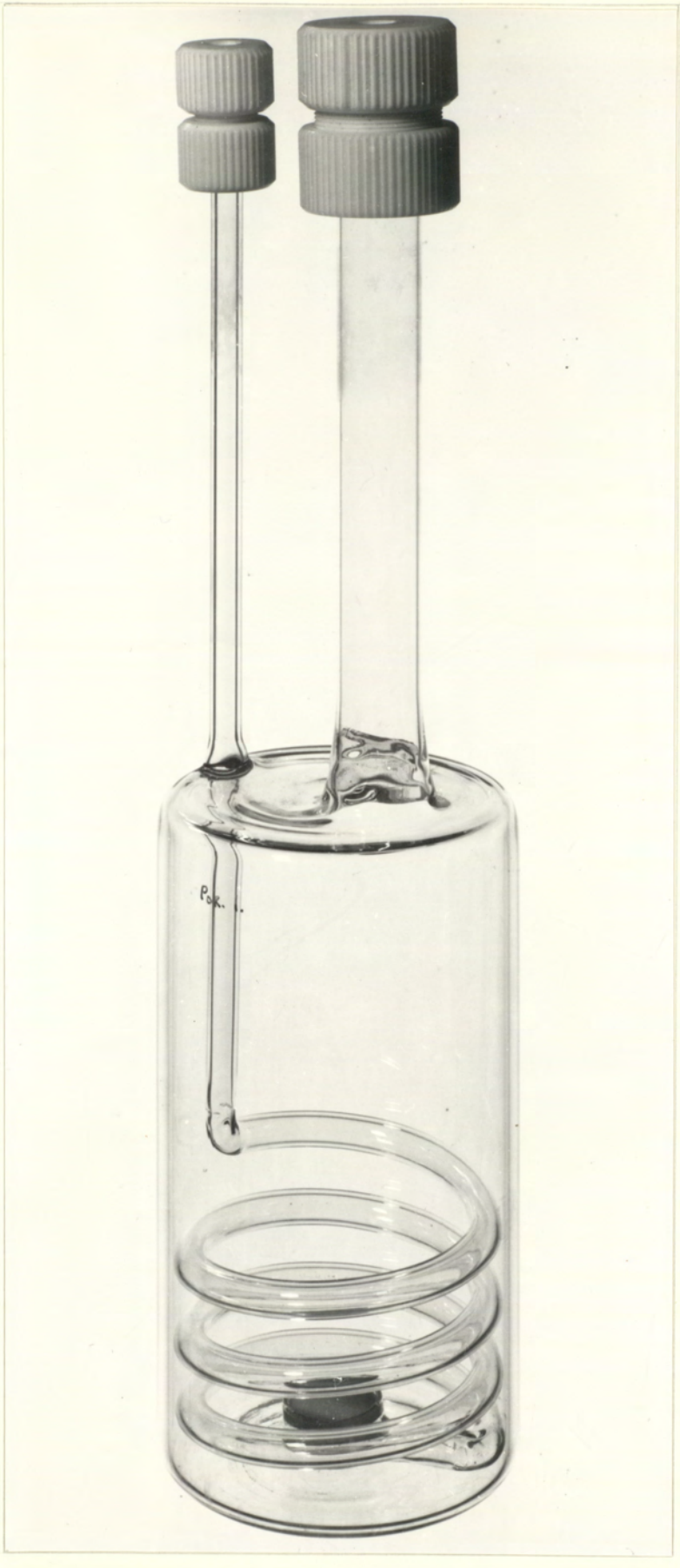

Fig. 3.12 Quartz evaporator and P.T.F.E. couplings used in the multideposition apparatus

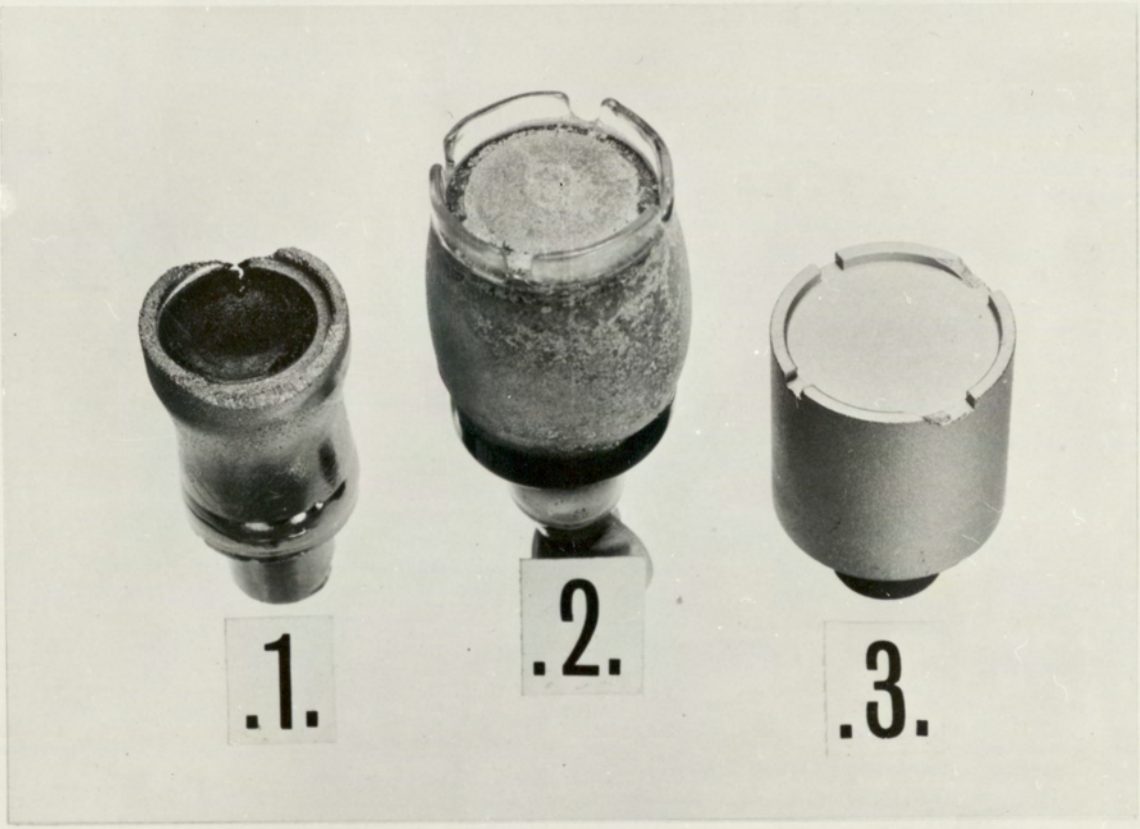

Fig. 3.13 Susceptors for the initial deposition apparatus - vertical system

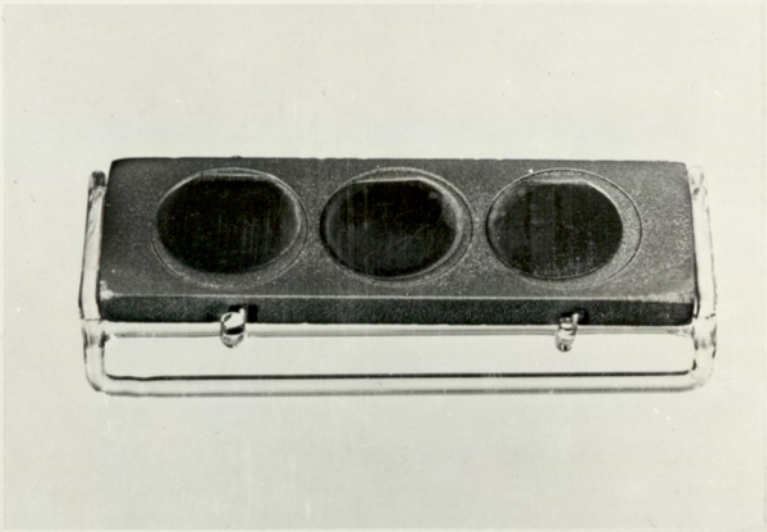

Fig. 3.14 Susceptor for the initial deposition apparatus - horizontal system

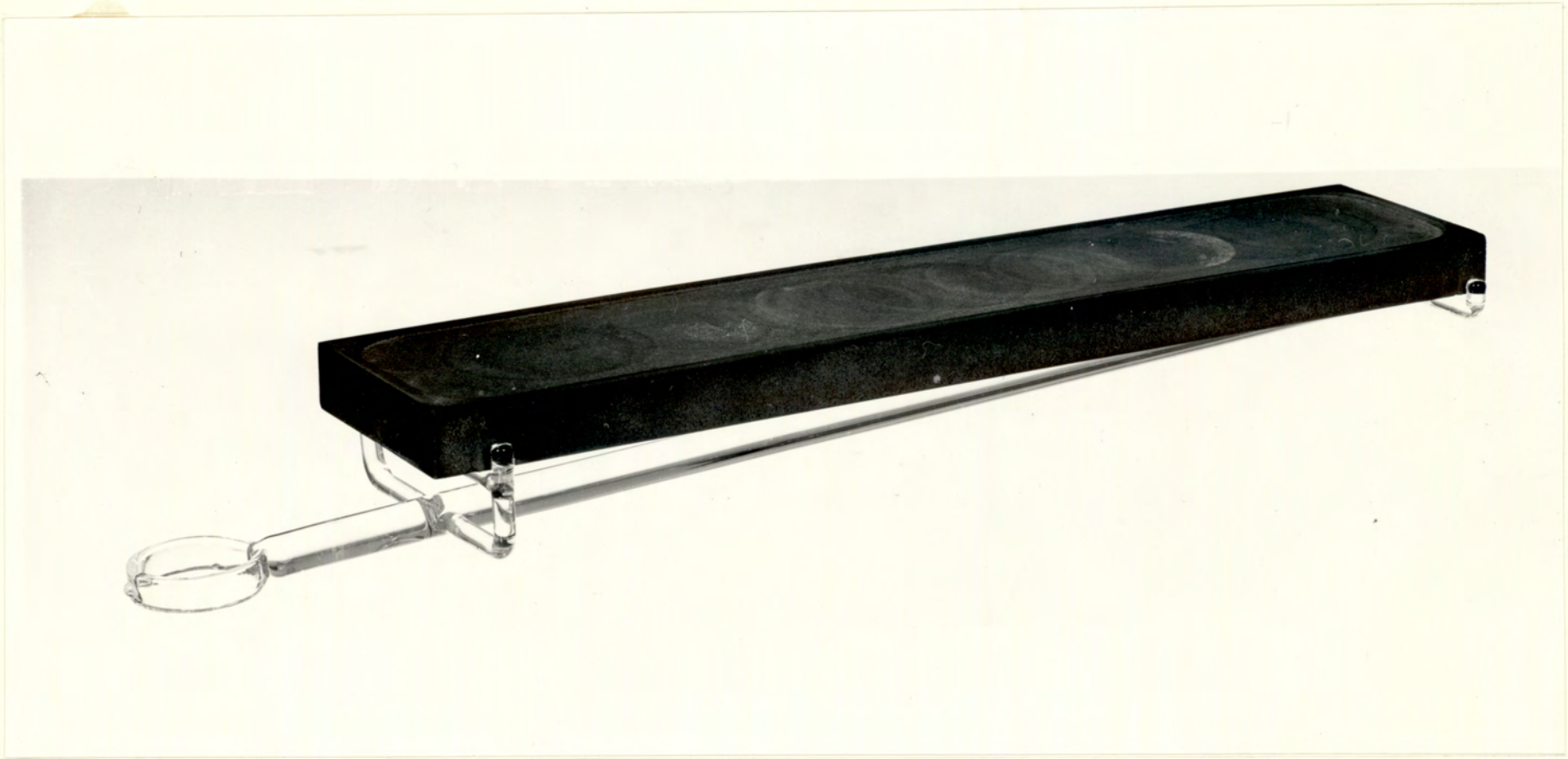

Fig. 3.15 Graphite coated silicon carbide susceptor for the multideposition apparatus

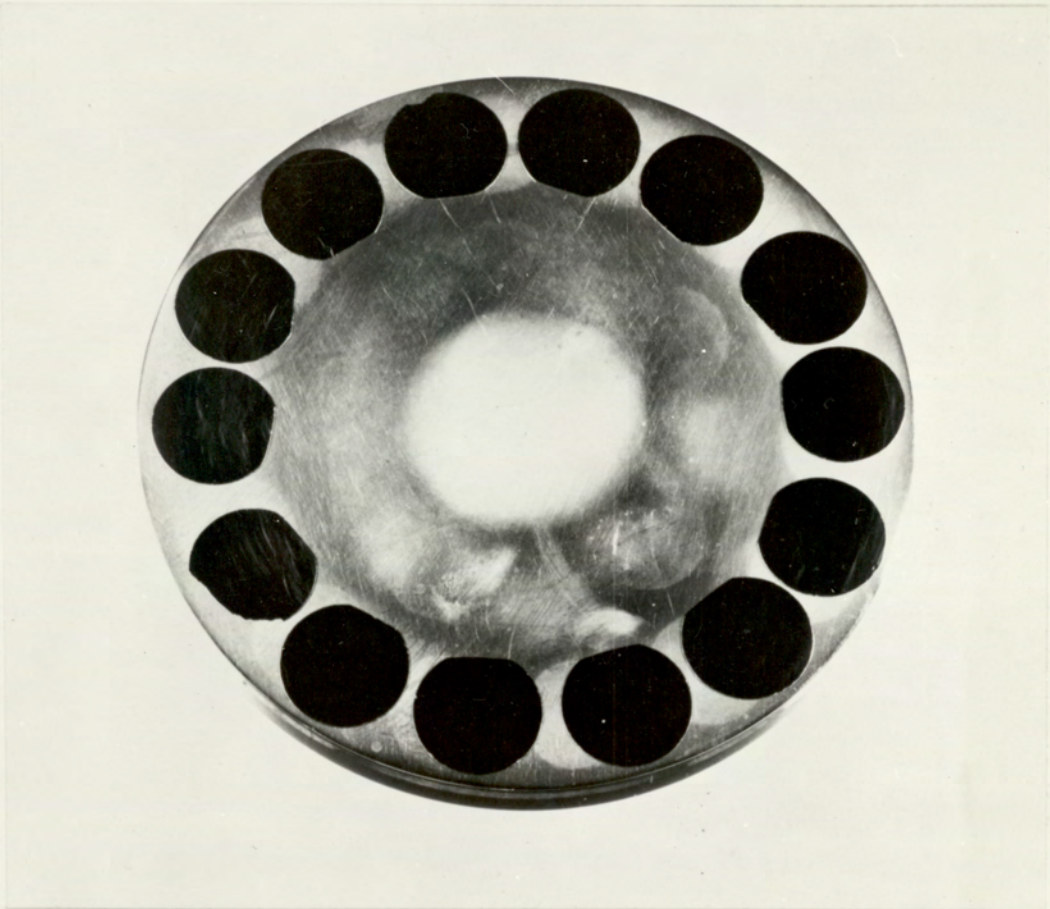

Fig. 3.16 Polishing plate with silicon substrates

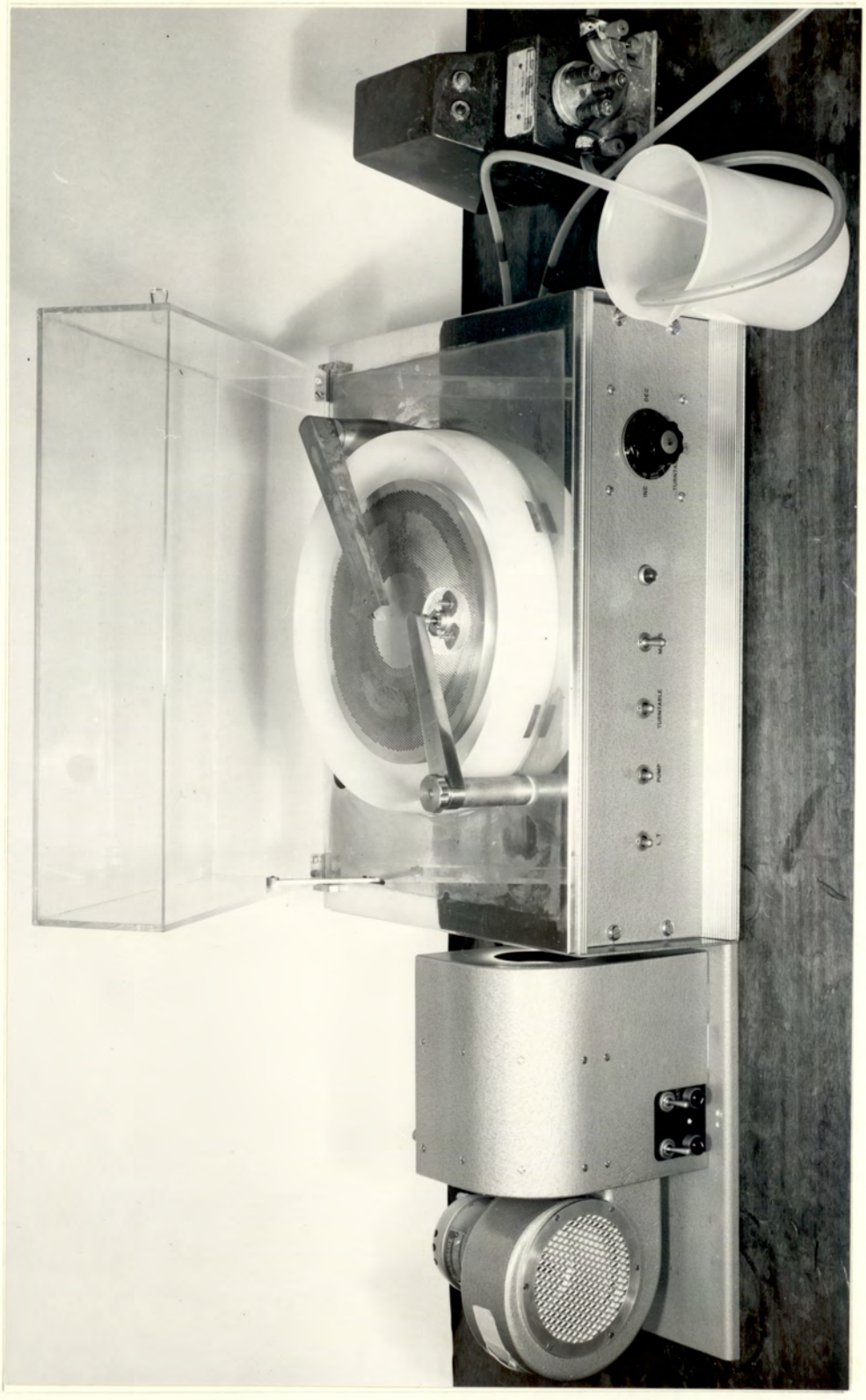

Fig. 3.17 Electro polishing unit

Fig. 3.18 Quartz discs used to support silicon substrates for electropolishing

4. MECHANICAL, ELECTRICAL AND STRUCTURAL EVALUATION OF EPITAXIAL LAYERS

A number of problems are associated with the mechanical, electrical and structural evaluation of epitaxial layers. These arise mainly from the nature of the layers and the methods used in their formation. For example, non-uniform deposition of the layer, non-impurity in the crystal symmetry and the comparative thinness of the layer are only a few of the factors that can lead to erroneous measurements and therefore interpretation. Practical precautions must also be kept in mind since it is essential to ensure that any probes do not penetrate the layers therefore measuring the characteristics of the substrate rather than those of the layers.

The growth of epitaxial material is only an initial process in the manufacture of devices and any method of measuring the properties of the epitaxial layer which affect or damage the epitaxial layer, its surface or substrate render it useless for further device fabrication. Measurement of layer properties can be divided into two groups (A) those used for process evaluation and hence are non-destructive (B) those providing more detailed information about the layer properties and are generally destructive. The three most important parameters required are the layer thickness, conduction type and the concentration of excess donors or acceptors (resistivity).

4.1 Determination of Layer Conduction Type

The thermo-electric method of detecting and identifying regions of silicon of a particular type of conductivity is based on observing the difference in polarity of the thermo-electric power produced when a heated metal probe is placed in contact with a P-type or N-type semi-conductor. The energy (Z) developed between the metal and the semi-conductor is

$$Z = -kT \log \frac{nh^3}{2(2\pi m_n kT)^{3/2}} \quad , \text{ - - - - - - - - - - -} \quad 4.1$$

where k is the Boltzmann constant, T is the absolute temperature, n the number of electrons in the conduction band, h Planck's constant and m_n the effective mass of a free electron.

The thermo-electric power is given by Z/eT where e is the electronic charge and the thermo-electric force V between two junctions at temperature T_1 and T_2 is

$$V = \frac{k}{e} \int_{T_1}^{T_2} \log \left(\frac{nh^3}{2(2\pi mkT)^{3/2}} \right) dT \qquad \text{------4.2}$$

The thermo-electric power developed between a hot and a cold steel probe when placed in contact with a semiconductor changes polarity when the type of conductivity changes. On an N-type semiconductor the heated probe becomes positive with respect to the cold probe and on P-type material it becomes negative with respect to the cold probe. A schematic diagram of the apparatus used is shown in Figure 4.1. As the hot probe is moved across the surface of the silicon the deflection of the galvanometer is reversed when the type of the conductivity changes.

This method is non-destructive and enables the N-type or P-type material of the resistivity encountered for device fabrication to be detected. It does not, however, given an accurate location of the boundaries between the two types of conductivity and is insensitive for material of resistivity higher than approximately 40 ohm cm.

4.2 Measurement of Layer Thickness

A number of methods have been developed to measure the layer thickness. If a substrate is weighed before and after deposition of the layer, the thickness can be calculated from the following equation:-

$$\text{Layer thickness} = \frac{\text{Increase in weight of substrate}}{\text{Cross sectional area of substrate} \times \text{density of silicon}} \qquad \text{---4.3}$$

This equation assumes that the layer is of a uniform thickness and deposition occurs on only one face. In practice the deposited layer is not of a uniform thickness and deposition also occurs to a limited extent on the back of the substrate while there is also a transfer of silicon from the susceptor to the back surface of the substrate. This method will only give an approximate value of the layer thickness.

Another method involves angle lapping and staining of the substrate. Chemical methods have been developed which will produce a permanent stain or plate giving a well defined outline of the boundary arising in the substrate between N and P-type silicon. In order to facilitate accurate visual measurement of the stained region the substrate is bevelled to increase the length exposed for staining to give a magnification of X10 as shown in Figure 4.2.

The bevel is formed by mounting the silicon substrate on wax on a brass plunger with face machined at 5° 44' and forming a good sliding fit into a steel cylinder as shown in Figure 4.3. The edge of the substrate is lapped on grade 600 corosil finishing paper, moving the jig backwards and forwards in straight lines, using methylated spirits as a cutting lubricant. When the bevel is of the required width, it is polished to a mirror finish with $\frac{1}{4}\mu$ diamond lapping compound and fluid on a hardened steel plate, to produce a sharp and well defined edge between the surface and the bevelled region. After delineation of the boundary, the layer width is measured at a suitable magnification with a calibrated eye-piece in a microscope with reflected light.

The most common preferential stain used (26) consists of approximately 0.1% concentrated HNO_3 in concentrated HF. The action of the permanent stain when placed on the bevel is to darken the P-type regions and leave the N-type regions unchanged. Some impurity in the HF is apparently necessary to activate the staining reaction which then proceeds at a rate which is dependent upon the resistivity and conductivity-type of silicon substrate and layer. Illumination of the junction is advantageous, since it increases the rate of staining due to the creation of a photo-voltage across the junction.

Another mechanism by which selective staining can occur is electrochemical displacement plating (27, 28, 29). The electrochemical potential of silicon is such that metallic ions such as copper, silver and gold will be displaced by silicon; that is, silicon ranks higher in the electromotive force series of elements than copper, silver and gold. The displacement is

selective, however, since the electrochemical potential of N-type silicon makes it the preferred area for the initial plating. The plating occurs on N-type silicon and then on P-type, if permitted. The technique is to observe the plating until the junctions are well delineated and then stop the action by flushing or otherwise removing the plating solution from the silicon. Plating occurs best when some HF is present in the plating solution to dissolve the anodic oxide that is initially formed. Hence, too much HF tends to promote immediate plating everywhere so that its concentration is critical. A solution containing 200 gram of copper sulphate per litre with 12 cc of 40% HF is used for copper staining while gold is deposited from a gold cyanide plating solution of 10 gram per litre $KAu(CN)_2$ and 300 gram per litre of KOH. Better preferential deposition of the gold is obtained if plating occurs in the temperature range 30° - $70^{\circ}C$ and in the presence of illumination.

The plating stains have poor adherence to the polished surface and great care in handling is required to avoid damaging the stained region. The stains produced from the HNO_3-HF solutions adhere well and produce sufficient contrast with the unstained regions so as to be easily photographed-Figure 4.4. The delineation of N on P and P on N layers with these stains has been successful but for N on N^+ and P on P^+ layers, very limited delineation has been obtained.

Infrared interference techniques (30, 31) have also been developed for the measurement of layer thickness. This method has the advantage that it is not destructive, as in the previous technique, and is much faster to carry out. However, it is limited to measurements of high resistivity layers (above approximately 0.09 ohm cm) on low resistivity substrates (less than approximately 0.015 ohm cm).

Infrared radiation will produce interference fringes which can be used to measure layer thickness, if reflection occurs both at the surface and at the interface between the layer and the substrate. This condition is satisfied if the carrier concentration in the layer is low enough to permit

transmission of the incident radiation through the layer and the optical constants of the substrate differ sufficiently from those of the epitaxial layer so that reflection occurs at the interface between the layer and the substrate.

Measurements are made by recording the intensity of reflected infrared radiation as a function of wavelength. Wavelengths in the 15 to 40 micron range are used to improve the infrared contrast. A Beckman IR-5A spectrophotometer (caesium bromide optics) or an IR-10 with diffraction grating equipped with a micro-specular reflectance attachment is used.

The relationship between layer thickness and the wavelengths of interface fringe maxima can be determined from Figure 4.5 The incident ray strikes the layer at A with an angle of incidence ϕ. Part of the incident radiation is reflected as ray (I) and the rest is refracted at an angle ϕ' until it strikes the interface B. Some of this radiation is absorbed by the substrate, but most of it is reflected to the layer surface C, where it emerges as ray (2) parallel to ray (I). Varying the wavelengths causes alternating bright and dark interference fringes in the reflected light whenever rays (I) and (2) differ in phase by an integral multiple of half wavelengths.

The optical path difference δ is given by

$$\delta = n_I(AB+BC) - AD \qquad \text{---- 4.4}$$

The refractive index n_I, multiplies the apparent optical path in the layer AB+AC, converting it to an equivalent air path using Snell's Law ($\sin\phi = n_I \sin\phi'$) equation 4.4 becomes

$$\delta = 2\,T\,n_I \cos\phi' \qquad \text{---- 4.5}$$

where T is the layer thickness and ϕ' the angle of refraction.

At point A the reflected ray undergoes a phase change of π or $\lambda/2$ while the transmitted ray remains in phase with the incident ray. At point B the reflected ray undergoes a phase change which is between 0 and π depending on the optical constants at the layer-substrate interface. For cases of layers of low carrier concentration on highly doped substrates, the phase change at point B is very small. At point C, both the transmitted

and reflected waves are in phase with the incident wave BC. For some wavelength λ_o, the optical path difference will be

$$\delta = \lambda_{o/2} \quad \text{— — — — — — — — — — — — — —} \quad 4.6$$

At this wavelength ray (I) is advanced by $\lambda_o/_2$ and ray (2) retarded by $\lambda_o/_2$ giving a net difference of λ_o. It is assumed that maxima will occur at wavelengths where ray (2) is in phase with ray (I). The first (zero order) fringe will occur at λ_o, the next fringe (first order) will occur at λ_I, where

$$\delta = \lambda_I + \lambda_I/2 \quad \text{— — — — — — — — — — — —} \quad 4.7$$

and the M^{th} order fringe maxima will occur at λ_m where

$$\delta = (M+\tfrac{1}{2})\lambda_m \quad \text{— — — — — — — — — — — —} \quad 4.8$$

Minima occur at intermediate wavelengths $\delta = m\lambda$ (where m is an integer). A convenient thickness relationship can be obtained from equations 4.5 and 4.8 utilising two wavelengths corresponding to the fringe maxima λ_m and λ_{m+x} where

$$T = \frac{x(\lambda_m \lambda_{m+x})}{2N_I \mathrm{Cos}\phi^I \ (\lambda_m - \lambda_{m+x})} \quad \text{— — — — — — —} \quad 4.9$$

T is the thickness of the layer in microns, x the number of complete cycles between maxima and λ_m and λ_{m+x} and N_I is the value of the refractive index of silicon extrapolated for the range 11-35u that is 3.41.

The angle of incidence, ϕ for the Beckman specular reflectance attachment is 30^o, which corresponds to an angle of refraction ϕ' of 8.4^o and $\mathrm{Cos}\phi^1 = 0.99$. The rays within the film are nearly normal to the surface, which makes the measurement relatively insensitive to ϕ. The constant $2N_I\mathrm{Cos}\phi^I$ equal to 6.77, when used with equation 4.9, gives layer thickness in the same units as those used for wavelengths.

A typical infrared reflectance spectrum obtained in the thickness measurement of an epitaxial layer is reproduced in Figure 4.6. For intensity fringes that increase in size the peak wavelengths should be chosen at points where the fringe curve envelope function is tangent to the fringe curve. For cases where more than three fringes are present simple maxima may be used. Non-uniform layer thickness or out-diffusion from the interface caused by high growth temperature and low growth rates may lead to poor interference

The non-destructive method together with the small sampling area 0.18 sq. cm. of the Beckman micro specular reflectance attachment allows individual substrates to be scanned for layer thickness determination.

The stacking fault method of measuring layer thickness is unique to epitaxially grown layers. Stacking faults in the growing epitaxial layer propagate throughout the layer and upon application of an appropriate etch form line etch figures at the layer surface. A diagram of a common type of etch figure for epitaxial layer grown on (111) substrate is shown in Figure 4.7.

The intersection of three (111) planes within the epitaxial layer forms a tetrahedron in the growing layer with an apex at the layer-substrate interface, which provides a means of measuring layer thickness (32). The thickness of the layer is related geometrically to the length of one side of the equilateral triangle. If l is the length of one side and t is the thickness of the layer,

$$t = l\sqrt{2/3} = 0.816\, l \qquad \text{4.10}$$

The stacking fault figure varies with substrate orientation, but each fault originating at the layer-substrate interface is geometrically related to the layer thickness regardless of orientation.

When this technique is used, only those etch figures originating at the interface should be measured, since stacking faults can originate in the growing layer. Those originating at the interface will be the largest figures delineated by the etch.

4.2.1 Comments on the Measurement of Layer Thickness

Of the four methods (Increase in weight; Angle lapping and staining; Infrared Interference and Stacking Fault Dimensions) that have been investigated for layer thickness measurements, the increase in weight method gives an average thickness of the layer on the substrate, while the other three methods provide measurement of thickness from a small sample area of the layer, but all methods are subjected to different limitations. Before

and during epitaxial growth (A) silicon is removed from the substrate surface with the hydrogen or hydrogen chloride polishing (B) deposition of silicon also occurs on the edge and back of the substrate and (C) silicon is transferred from the silicon coated susceptor to the back of the substrate. Thus the measurement of the increase in weight of the substrate is not an accurate measure of the silicon used to form the layer and is the reason why this method does not provide results consistent with the other methods (Table 6.1).

The angle lapping method relies on the delineation of a boundary between areas containing different impurities or concentration of impurities. However results obtained in this work indicate that the metallurgical interface does not necessarily coincide with the boundary formed by impurities (Figures 6.5 and 6.6.). This method is only suitable for the measurement of the thickness of layers produced with minimum impurity contributions from the substrate, but is satisfactory for layer thickness measurements for resistivity calculations and junction depths.

The infra-red method is simple, quick and non-destructive but is limited to the measurement of a boundary between a high and low impurity concentration which in practice is for layers of resistivity above approximately 0.09 ohm cm. on substrates less than 0.015 ohm cm. resistivity. Again the measured boundary need not coincide with the grown substrate/layer interface.

The stacking fault method measures the layer thickness from the metallurgical substrate/layer interface, but with the development of this investigation stacking faults have almost been completely eliminated from the epitaxial layer.

The comparison of the results for measuring layer thickness indicate that it is possible within experimental error to obtain similar layer thickness measurements of layers, produced with certain process conditions, by the angle lapping, infra-red and stacking fault methods. The agreement of these methods has resulted in the calibration of the growth rate of the epitaxial system from infra-red thickness measurements of layers grown from

intrinsic silicon tetrachloride on 0.01 ohm cm. N type antimony doped substrates.

4.3 Measurement of Layer Resistivity

The most common method of measuring sheet resistivity is that employing a four point probe. Four equally spaced metal probes are used to contact the silicon surface, Figure 4.8. A measured current I is passed through the two outside probes, inducing a voltage drop V across the two inside probes which can be measured. From the measured current and voltage, the resistivity can be calculated allowing for the appropriate correction factors for the sample and probe geometry from the following equation (33).

$$\rho = \frac{V}{I} .W.C\left(D/S\right).F\left(W/S\right) \qquad \text{---------- 4.11}$$

where V is the voltage, I the current, W the thickness of the layer in centimeters, D the diameter of substrate and S is the probe spacing. $C\left(D/S\right)$ is a correction for area: if $D > 20S$, $C\left(D/S\right)$ is approximately equal to 4.5 $F\left(W/S\right)$ is a correction for thin samples: if $W \leqslant \frac{1}{2} S$, $F\left(W/S\right)$ is equal to 1.

This method is suitable for the measurement of epitaxial layers of known thickness grown on substrates of the opposite type, when the junction effectively isolates the layer from the substrate. However, this method is unsuitable for N on N^+ or P on P^+ structures.

The three point probe technique (34, 35) consists of calibrating the reverse breakdown voltage of the point contact diode made from single crystal silicon of known resistivity and a metal probe. Measurement of the reverse diode breakdown on an epitaxial layer is then related to resistivity by means of a calibration curve.

Two probes, Figure 4.9, one of tungsten and the other of osmium, are brought into contact with the silicon surface and a voltage applied between them. Since the epitaxial layer is generally of higher resistivity and much thinner than the substrate, the path of current flow is primarily through the substrate. The osmium probe I will form a forward biased PN junction with the epitaxial layer, while the tungsten probe 2 will form a reverse

biased PN junction. The only potential difference of significant magnitude occurs at the reverse biased point. There is significant ohmic resistance across the osmium probe I and to enable the reverse bias breakdown voltage to be measured a third osmium probe is added. The location of the third probe is not critical provided that the distance between probes 2 and 3 exceeds the width of the depletion layer associated with the reverse biased PN junction of probe 2. This distance is achieved under practical conditions as the width of the depletion layer is of the order of microns, whereas a probe spacing of this order is impossible to achieve in practice.

Measurement is made by increasing the reverse biased voltage and displaying the breakdown voltage on an oscilloscope. If the depletion layer width, which is proportional to the square root of the applied voltage, penetrates through the epitaxial layer to the substrate before breakdown occurs a phenomenon known as "punch through" is observed. Voltage measurements depend on the area of contact, the probe material and the pressure applied to the probe. If the conditions of measurement are standardised, reproducible results can be obtained.

This non-destructive method is primarily used for measuring the resistivity of N on N^+ or P on P^+ epitaxial layers and does not require a knowledge of layer thickness.

The apparatus for making three point probe measurements consists of a Fell three point probe head with the two outer probes of osmium and a centre probe of tungsten with a radius of 0.005 inches accommodated in a standard Fell resistivity unit with lever loading of the probe on to the substrate. The probes are spring loaded and result in reproducible loading in contact with the substrate. The loading pressure can be adjusted within the probe head.

The circuit used is shown in Figure 4.10 and consists of a Variac with 240 volts AC input connected to a transformer, to isolate the mains input from the osmium probe, via a 2,200 ohm resistor for limiting the current and a diode for half wave rectification. The tungsten probe is connected to earth, the transformer via 560 ohm current monitoring resistance and the

vertical input of the oscilloscope. The third probe is connected to the horizontal input via 10,000,000 ohm resistance which eliminates probe contact potential. The voltage is measured on a Type CD.513.2 Solascope oscilloscope with a 1 mm graduated scale which has been accurately calibrated for voltage with a standard supply.

Breakdown voltage is obtained by bringing the 3 point probe head into contact with the substrate surface and applying an increasing voltage by adjustment of the variac. The increased voltage is displayed on the oscilloscope and when breakdown is reached the current-voltage trace stops increasing, hooks back and exhibits negative resistance Figure 4.11. The maximum voltage indicated on the oscilloscope is the breakdown voltage and the average of several readings on the substrate surface is taken as the mean breakdown voltage.

The calibration of the reverse breakdown voltage is determined from a series of polished silicon substrates with resistivity in the range of 0.1 to 10.0 ohm cm N type which has previously been accurately determined with the four point probe method. The mean of eight readings from the surface of each calibration substrate is taken as the representative breakdown for that substrate. From these results (A) a calibration curve can be plotted-Figure 4.12 or (B) for a more exact correlation the equation of the curve fitting the data can be obtained by the method of least squares and from this equation a computer print out of resistivity and breakdown voltage can be obtained, Table 4.1.

A further method of measuring layer resistivity involves the application of a sinusoidally alternating bias to a PN junction that gives rise to certain capacitive effects, which are not apparent under direct current operation. The physical causes of these effects are two-fold.

1. Modulation of the space charge width which is important under reverse bias conditions.

2. Reactive or inertial effect due to the injected excess carriers and therefore important under forward bias conditions.

The measurement of the former provides a method of determining the doping level of a junction and its gradient.

The total width l of the space charge region i.e. the region from which the free carriers have been swept away, is a function of the potential barrier height V_D. The same relation applies in the presence of an external bias V if $V_D - V$ is substituted for V_D. The application of a forward bias positive V, reduces the width of the space charge region by reducing the barrier height, while a reverse bias, negative V, has the opposite effect. These changes are indicated qualitavely in Figures 4.13, 4.14 and 4.15.

When a reverse bias -V is applied to a junction, the corresponding widths of the space charge region in the P and N regions is lp and ln. When the bias is changed to $-V^1$, the widths of the space charge region change to l^1p and l^1n respectively. This entails the removal of a certain charge ΔQ by the removal of holes from the left hand edge of the space charge region, and of an equal and opposite charge $-\Delta Q$ of electrons from the other edge. This transfer of charge accompanying the change of bias appears as a current in the external circuit, and gives rise to a capacitive effect.

For infinitesimally small variations in the bias, a capacitance may be defined as

$$C_S = \frac{dQ}{dV} = lN_A \frac{d\ell_p}{dV} \qquad \text{---------- 4.12}$$

and it can be shown that this capacitance is

$$C_S = \frac{K}{l_p + l_n} = \frac{K}{l} \qquad \text{---------- 4.13}$$

in MKS units where K is the dielectric constant of silicon equal to 10.6×10^{-11}.

The formula $C_S = \frac{K}{l}$ is valid irrespective of the junction profile and is equivalent to the capacitance of a parallel plate condenser of dielectric constant K and thickness l. The capacitance C_S is known as the space charge capacitance and it shunts the direct current conductance of the junction.

The latter may become very small at reasonably high reverse bias voltages and the space charge capacitance then becomes the dominant element in alternating current work.

It can be shown (36) that for abrupt PN junctions

$$C \propto (V_D - V)^{-\frac{1}{2}} \qquad 4.14$$

and in the particular case of strong asymmetrically doped junctions

$$\frac{1}{C^2} = \frac{2}{K_1 N_{AD}} \left(V_D - V \right) \qquad 4.15$$

The measurement of C_S as a function of the applied reverse bias V provides a means of obtaining information about the doping level N_{AD} of a junction. If $1/C_S^2$ plotted against V is a straight line, then the junction may be regarded as abrupt and the slope of the graph is a measure of the doping level N_A or N_D on the higher resistivity side. The intercept on the V axis is equal to the diffusion potential V_D.

Similarly for a linear gradient junction

$$1/C_S^3 \propto \frac{V_D - V}{K^2_1 \alpha} \qquad 4.16$$

and provides a means of determining the impurity gradient α.

When junctions that are shallow and nearly abrupt are produced by diffusion in N-type epitaxial layers on N^+ substrates and mesa diodes are subsequently formed, the measurement of junction capacitance as a function of reverse bias voltage will give the doping level of the epitaxial layer. The measurements will also provide information about the impurity gradient existing in grown epitaxial PN junctions.

The circuit for measuring the junction capacitance, Figure 4.16, consists of a radio frequency generator, Radiometer Type MS 111a feeding a signal into a Wayne Kerr Radio Frequence Bridge Type B601 and from which a signal is detected with an AR88 radio receiver and displayed on an oscilloscope. An additional circuit is used to provide the bias voltage and consists of dry cells, the number of which provides a coarse adjustment for voltage, connected to the RF bridge in series with a 470,000 ohm

resistance and a variable 1,000,000 ohm resistance which gives fine bias voltage adjustment. A meter for measuring bias voltage is connected in parallel with the dry cells and the bridge. In series between the voltmeter and the common terminal of the bridge is a 15 Henry 200 ohm choke and a 1.0μF condenser. The former is to isolate the voltmeter from the diode thus preventing any erroneous readings and the latter to isolate the bridge from the DC bias given by this additional circuit.

The test diode is connected between the choke and condenser to the R and C range terminal of the bridge and capacitance measurements made at 1 megacycle.

It is important that there is a high voltage drop in the part of the circuit containing the dry cells in comparison with that part containing the diode, so that the true voltage across the diode is measured by the voltmeter and is achieved by the use of the 470,000 ohm resistance.

A plot of Log C against Log (V_D-V) will result in a straight line if the junction is abrupt and from a graph of $^1/_C2$ against V, the value of $^1/_C2/V$ can be determined and used to calculate the value of N_{AD} in equation 4.15 and hence the resistivity. The calculations are tedius and have been replaced by a slide rule reported by Amron (37) for computing Dopant profiles.

The diodes required for determining the layer resistivity by the junction capacitance method are prepared by a boron predeposition and diffusion into the epitaxial layer followed by plating and dicing of the substrates and finally soldering and cleaning of the discreet devices.

Initially the composite substrate is cleaned in hot chromic acid, washed in deionised water and dried in acetone vapour. Predeposition of boron on to the layer surface is made in a tube type furnace at 900°C by passing a small concentration of boron trichloride in nitrogen over the substrate for five minutes, followed by a further nitrogen purge for ten minutes and finally withdrawing the substrates from the furnace. The deposited boron is diffused into the silicon in a clean alumina tube

furnace for five minutes at 1250°C and air-cooled by withdrawing the substrate from the furnace. These deposition and diffusion conditions result in a junction depth of approximately 2.6 microns and a surface concentration of 1.3×10^{19} atoms per cc.

After diffusion the oxide layer is removed with hydrofluoric acid from the substrate which is rinsed in water, dried and mounted with the epitaxial layer surface in Apiezon W Wax on a microscope slide. The P layer on the substrate surface is etched off with CP_4 and its removal confirmed with the thermoelectric probe.

The substrate is removed from the slide, cleaned in toluene, hydrofluoric acid, water and finally agitated for one minute in a solution of palladium chloride ($PdCl_2$), followed by a rinse in water and immersed in electroless nickel plating solution at 80°C for two minutes followed by washing in water and drying on a filter paper. The nickel plate is sintered at 800°C in an atmosphere of oxygen free forming gas flowing at two litres per minute at N.T.P. After sintering, the substrates are rinsed in dilute hydrofluoric acid, washed in water and immediately replaced in the hot nickel plating solution for a further eight minutes followed by washing in water and electroplating with gold for five minutes in "Autronex C.I."* solution and finally washed and dried.

After the plating, the substrate is remounted on a microscope slide with Apiezon W wax with the epitaxial layer containing the junction uppermost. A mask with 0.070 inch diameter holes is positioned over the substrate and clamped with a magnet and a solution of Apiezon W wax in trichloroethylene sprayed through the holes in the mask. The mask is removed by tapping the backside of the slide and the wax dried and fused to ensure that the edges of the dots are clean and sharp. The gold and nickel plate with the exception of that protected by the wax mask is etched off in a mixture of 3 parts of hydrofluoric acid and one part of nitric acid. The black wax spots are removed and a mask with 0.090 inch diameter

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* Trade name of Sel-Rex Corporation for Gold-Acid-Cyanide plating solution.

holes positioned and clamped on the substrate so that the centres of these holes coincide with the centre of the gold islands and a solution of Apiezon W wax again sprayed through the holes followed by removal of the mask, drying and fusing of the wax.

The smaller diameter mask is used to facilitate the removal of the gold and nickel in order to reduce the possibility of the deposition of these metals at the PN junction during dicing.

The substrate is diced while still positioned on the slide by agitating in a solution of CP_4 and in order to lessen the possibility of contamination of the exposed junctions after dicing, a further etch for five seconds in fresh CP_4 is made followed by washing in water and drying with an acetone rinse. The dice are removed from the slide by dissolving the Apiezon wax in cold toluene and after separation the dice are washed in clean toluene. The substrate surface of the dice is soldered onto a TO5 transistor base and the epitaxial layer surface soldered to a connecting wire with a high temperature Alcho-Re 298 solder.

The devices are finally cleaned to remove any impurities at the exposed junction by the following sequence of five minutes ultrasonically cleaning in toluene, an acetone rinse, ten minutes cleaning in water, a further acetone rinse and finally drying in a dust-free atmosphere. The device junctions are finally protected with Midland Silicones ESP 2618 varnish, applied with a rounded pyrex rod and cured for two hours at 200°C.

The device is not encapsulated and measurement of the junction capacitance is made after it has cooled.

Another method of measuring the layer resistivity involves the measurement of the breakdown voltage of a diode. A single PN junction has a forward and reverse current voltage relationship as shown in Figure 1.3. The forward current increases rapidly after an initial application of a fraction of a volt. On the other hand a very small current flows in the reverse direction until sufficient voltage is applied to cause a sharply defined breakdown. This voltage is known as the peak inverse voltage

which is dependent on the gradient of the excess donors or acceptors at the junction and the resistivity on either side of the junction.

If a junction is produced in the epitaxial layer by diffusion the peak inverse voltage of the junction can be related to that obtained from similar PN junctions produced by diffusion of impurities into single crystal silicon of known resistivity grown from the melt. This method can be used for monitoring the resistivity of epitaxial material used in the fabrication of transistors under conditions where all fabrication processes are repeatable when the breakdown voltage is dependent on the epitaxial layer resistivity.

4.3.1 Comments on the Measurement of Layer Resistivity

The measure of resistivity of the layer is a measure of excess donor or acceptor impurity atoms within the layer. The four point probe method is non-destructive and can be used for measuring layer resistivity of known thickness isolated by a PN junction from the substrate. The method provides a measure of the bulk resistivity of the layer and does not take into account changes in impurity concentrations through the layer profile.

The three point probe method measures the reverse breakdown voltage of a point contact diode, which is compared with that obtained from silicon of known resistivity. The method does not require a knowledge of the layer thickness and measures the resistivity only in the region occupied by the depletion layer at breakdown. The width of the depletion region depends on the resistivity and resistivity gradient in the layer and hence the layer thickness must always be greater than the depletion region at breakdown. If the depletion region extends to the substrate, many different combinations of layer thickness can yield the same breakdown. The use of this method in the present work has been very limited because generally the layers produced had a resistivity and thickness which resulted in the depletion layer penetrating to the substrate.

With the capacitance method a junction is formed by shallow diffusion into the epitaxial layer and diodes fabricated. The epitaxial layer must be lightly doped so that the depletion region spreads primarily into the epitaxial layer. Again this method can only measure the impurity concentration within the distance covered by the depletion region of the reverse biased PN junction and this distance is limited by the electrical breakdown of the junction. The calculations to obtain the resistivity from the capacitance measurements require an accurate measurement of the diode area but the method used in this work to produce the diodes does not result in reproducible or uniform area. This method is time consuming and not readily applicable for process control and requires further processing of the layer which can result in possible structure changes. This method is very suitable however for measuring the impurity profile within the layer section.

The material used to make comparisons of the four point probe, capacitance and breakdown voltage methods of measuring resistivity contained more than 750 stacking faults per sq. cm. and junctions produced in this material have soft breakdown characteristics. It is probable that the true breakdown voltage of the diodes produced in this material was not measured and accounts for the difference in resistivity obtained by this method compared with the four point probe methods. However only fair agreement is obtained between the four point probe and capacitance methods which is probably due to inaccurate measurement of the diode area and/or the difference in sampling area of the two methods.

The structure of material often required for device processing consists of an N epitaxial layer on an N^+ substrate and because of the problems associated with the capacitance and three point probe methods, the N layer resistivity is monitored from a high resistivity (1.0 ohm cm) P substrate processed at the same time as the N^+ substrates. A four point probe resistivity measurement can be obtained because of the effective isolation of the N layer from the P substrate by the PN junction. This method does not give an absolute measure of the N layer resistivity because

of the influence of the different types of substrates; however in practice it is found to be near the true resistivity and serves as a standard for monitoring or changing the N layer resistivity.

4.4 Structure Examination

Macro examination of the surface of the deposited layer reveals the crystalline nature of the deposited layer. An epitaxial layer will have a shiny polished surface identical to the original substrate surface while a polycrystalline layer appears matt or grey and individual crystallites may be observed. Small irregularities due to the substrate surface, grain boundaries, small protruding defects and other defect areas can be observed on the shiny layer surface.

Micro examination of the surface layers reveals the finer structure of the matt or grey polycrystalline layers observed with macro examination, while the shiny epitaxial surface provides information about the protruding defects and other surface imperfections. Examination of the surface after chemical etching with suitable etches (Table 4.2) reveals the presence of crystal imperfections such as dislocations and stacking faults in the epitaxial layer. Estimation of the number of these defects is obtained by counting the number present in a calibrated area of the field of view of the microscope at a number of positions on the layer surface as illustrated with the results and relating the average of these counts to the number per sq. cm. of layer surface.

The structure of the epitaxial layer can be examined also by an electrochemical plating process to detect preferential electrical leakage at the line etch figures. The surface of the epitaxial layer is made the cathode in a copper plating solution and preferential deposition of copper occurs at the line etch figures if electrical leakage occurs.

An N type epitaxial layer on a P type substrate was etched in the Sirtl etch to reveal the position of the line etch figures on the layer surface. A gold film was vacuum deposited on to the centre of the P substrate and a contact wire soldered on to the gold. The periphery of

the substrate, the P surface and the uninsulated portion of the contact wire were coated with Apiezon W wax as illustrated in Figure 4.17 in order to isolate the substrate with the exception of the epitaxial layer surface. The plating solution consists of 0.5M copper sulphate, 0.5M sulphuric acid and 10^{-5}M di - thio - oxamide ($CSNH_2$) and the electrical plating circuit shown in Figure 4.18.

Plating of the sample was carried out below the breakdown voltage of the PN junction for a few seconds, followed by washing in deionised water and drying in cool air and examining microscopically for the deposition of copper at the line etch figure. This process was repeated a number of times until preferential deposition of copper was detected or uniform plating of the layer surface occurred.

The determination of the layer crystal orientation by the Laue X-ray diffraction method involves the presentation of the stationary single crystal to a collimated beam of white radiation X-rays. Because the specimen is a fixed single crystal, the variable necessary to ensure that the Bragg equation $\lambda = 2d_{hkl}\sin\theta$ is satisfied for all the planes in the crystal has to be provided by the range of wavelengths in the beam, i.e. each set of crystal planes chooses the appropriate λ from the white spectrum to give a Bragg reflection. With the experimental arrangement used a back reflection photograph is obtained and the pattern of the spots produced lie on hyperbolae. All spots on any hyperbola are reflections from planes of a single zone i.e. where all the lattice planes are parallel to a common direction, the zone axis, and consequently the Laue pattern is able to indicate the symmetry of the crystal. For example when the beam is directed along a $[111]$ direction in the crystal, the Laue pattern will show three-fold symmetry - Figure 6.4. The orientation of the single crystal is obtained essentially by plotting the zones measured from the film onto a stereogram and comparing the angles between them with a standard projection of the crystal structure.

Confirmation that the shiny polished layer was epitaxial with the

substrate was obtained from X-ray Laue photographs. Initially a Laue photograph was taken of the side of the substrate that had no layer deposited on it. This substrate was then etched from the layer and a Laue photograph taken of the layer, using exactly the same conditions as for the substrate.

4.5 Impurity Analysis

An A.E.I. M.S.7 Spark source mass spectrometer has been used for the chemical analysis of silicon epitaxial layers. The normal electrode arrangement for a solid source M.S.7 analysis is unsuitable for examination of epitaxial layers. However, an electrode arrangement, reproduced in Figure 4.19 and consisting of a scanning probe of high resistivity silicon (1,000 ohm cm), has been developed (38) to form an arc to the surface of the epitaxial layer thereby evaporating and ionising the layer. In practice it has been found that a substrate 0.05 cm thick to provide mechanical support is required and an epitaxial layer at least 20 microns thick is necessary to avoid arcing through the layer into the substrate.

The comparison of gain measurements of transistors, fabricated with exactly the same structure, in different specimens of epitaxial material provides a measure of the relative minority carrier lifetime of the base material and hence the relative concentration of electrically neutral impurity atoms within the silicon.

In the functioning of a transistor-Figure 4.20, electrons are produced at the emitter that diffuse across the first PN junction, which is in forward bias, and drift towards the collector across the second PN junction, in reverse bias. The region between the emitter and collector is known as the base, the number of electrons crossing the base is a measure of the current gain of the device.

$$\text{Gain} = \frac{\text{value of current emerging from the collector}}{\text{value of current entering the emitter}} \quad \text{---4.17}$$

To obtain maximum efficiency of the transistor a thin base region is

required in order to transfer as many electrons as possible across the base without recombination of holes and electrons within the base. The recombination of electrons in the base region is also affected by the lifetime of the minority carrier in the base region. This is dependent on the electrically active and electrically neutral atoms of impurity in the silicon.

The experimental techniques and process variables, influence the deposition and properties of the epitaxial layers and will now be discussed.

TABLE 4.1A

Computer print out of the three probe calibration for resistivity against breakdown voltage.

RESISTIVITY	B/D VOLTAGE	RESISTIVITY	B/D VOLTAGE
0.040	21.49	1.040	83.80
0.060	25.46	1.060	84.46
0.080	28.71	1.080	85.13
0.100	31.51	1.100	85.78
0.120	34.01	1.120	86.43
0.140	36.27	1.140	87.07
0.160	38.35	1.160	87.71
0.180	40.28	1.180	88.33
0.200	42.09	1.200	88.96
0.220	43.80	1.220	89.57
0.240	45.42	1.240	90.18
0.260	46.97	1.260	90.79
0.280	48.44	1.280	91.39
0.300	49.86	1.300	91.98
0.320	51.22	1.320	92.57
0.340	52.54	1.340	93.15
0.360	53.80	1.360	93.73
0.380	55.03	1.380	94.30
0.400	56.22	1.400	94.87
0.420	57.38	1.420	95.43
0.440	58.51	1.440	95.99
0.460	59.60	1.460	96.55
0.480	60.67	1.480	97.10
0.500	61.72	1.500	97.64
0.520	62.74	1.520	98.19
0.540	63.73	1.540	98.72
0.560	64.71	1.560	99.26
0.580	65.66	1.580	99.79
0.600	66.60	1.600	100.31
0.620	67.52	1.620	100.83
0.640	68.42	1.640	101.35
0.660	69.30	1.660	101.86
0.680	70.17	1.680	102.38
0.700	71.03	1.700	102.88
0.720	71.87	1.720	103.39
0.740	72.69	1.740	103.89
0.760	73.51	1.760	104.38
0.780	74.31	1.780	104.88
0.800	75.10	1.800	105.37
0.820	75.88	1.820	105.86
0.840	76.65	1.840	106.34
0.860	77.40	1.860	106.82
0.880	78.15	1.880	107.30
0.900	78.89	1.900	107.77
0.920	79.61	1.920	108.25
0.940	80.33	1.940	108.72
0.960	81.04	1.960	109.18
0.980	81.74	1.980	109.65
1.000	82.43	2.000	110.11
1.020	83.12	2.020	110.57

TABLE 4.1B

Computer print out of the three probe calibration for resistivity against breakdown voltage.

RESISTIVITY	B/D VOLTAGE	RESISTIVITY	B/D VOLTAGE
2.040	111.02	3.040	131.15
2.060	111.48	3.060	131.51
2.080	111.93	3.080	131.86
2.100	112.37	3.100	132.22
2.120	112.82	3.120	132.58
2.140	113.26	3.140	132.93
2.160	113.70	3.160	133.28
2.180	114.14	3.180	133.64
2.200	114.58	3.200	133.99
2.220	115.01	3.220	134.33
2.240	115.44	3.240	134.68
2.260	115.87	3.260	135.03
2.280	116.30	3.280	135.37
2.300	116.73	3.300	135.72
2.320	117.15	3.320	136.06
2.340	117.57	3.340	136.40
2.360	117.99	3.360	136.74
2.380	118.40	3.380	137.08
2.400	118.82	3.400	137.42
2.420	119.23	3.420	137.76
2.440	119.64	3.440	138.09
2.460	120.05	3.460	138.43
2.480	120.46	3.480	138.76
2.500	120.86	3.500	139.09
2.520	121.26	3.520	139.43
2.540	121.67	3.540	139.76
2.560	122.06	3.560	140.09
2.580	122.46	3.580	140.41
2.600	122.86	3.600	140.74
2.620	123.25	3.620	141.07
2.640	123.64	3.640	141.39
2.660	124.03	3.660	141.72
2.680	124.42	3.680	142.04
2.700	124.81	3.700	142.36
2.720	125.19	3.720	142.68
2.740	125.58	3.740	143.00
2.760	125.96	3.760	143.32
2.780	126.34	3.780	143.64
2.800	126.72	3.800	143.95
2.820	127.10	3.820	144.27
2.840	127.47	3.840	144.59
2.860	127.85	3.860	144.90
2.880	128.22	3.880	145.21
2.900	128.59	3.900	145.52
2.920	128.96	3.920	145.84
2.940	129.33	3.940	146.15
2.960	129.69	3.960	146.46
2.980	130.06	3.980	146.76
3.000	130.42	4.000	147.07
3.020	130.79	4.020	147.38

TABLE 4.1C

Computer print out of the three probe calibration for resistivity against breakdown voltage.

RESISTIVITY	B/D VOLTAGE	RESISTIVITY	B/D VOLTAGE
4.040	147.68	5.040	161.97
4.060	147.99	5.060	162.24
4.080	148.29	5.080	162.51
4.100	148.60	5.100	162.78
4.120	148.90	5.120	163.04
4.140	149.20	5.140	163.31
4.160	149.50	5.160	163.57
4.180	149.80	5.180	163.84
4.200	150.10	5.200	164.10
4.220	150.40	5.220	164.36
4.240	150.69	5.240	164.63
4.260	150.99	5.260	164.89
4.280	151.29	5.280	165.15
4.300	151.58	5.300	165.41
4.320	151.87	5.320	165.67
4.340	152.17	5.340	165.93
4.360	152.46	5.360	166.19
4.380	152.75	5.380	166.45
4.400	153.04	5.400	166.71
4.420	153.33	5.420	166.96
4.440	153.62	5.440	167.22
4.460	153.91	5.460	167.48
4.480	154.20	5.480	167.73
4.500	154.49	5.500	167.99
4.520	154.77	5.520	168.24
4.540	155.06	5.540	168.50
4.560	155.34	5.560	168.75
4.580	155.63	5.580	169.01
4.600	155.91	5.600	169.26
4.620	156.19	5.620	169.51
4.640	156.48	5.640	169.76
4.660	156.76	5.660	170.01
4.680	157.04	5.680	170.26
4.700	157.32	5.700	170.51
4.720	157.60	5.720	170.76
4.740	157.87	5.740	171.01
4.760	158.15	5.760	171.26
4.780	158.43	5.780	171.51
4.800	158.71	5.800	171.76
4.820	158.98	5.820	172.00
4.840	159.26	5.840	172.25
4.860	159.53	5.860	172.50
4.880	159.81	5.880	172.74
4.900	160.08	5.900	172.99
4.920	160.35	5.920	173.23
4.940	160.62	5.940	173.48
4.960	160.89	5.960	173.72
4.980	161.16	5.980	173.96
5.000	161.43	6.000	174.21
5.020	161.70	6.020	174.45

TABLE 4.1D

Computer print out of the three probe calibration for resistivity against breakdown voltage.

RESISTIVITY	B/D VOLTAGE
6.040	174.69
6.060	174.93
6.080	175.17
6.100	175.41
6.120	175.65
6.140	175.89
6.160	176.13
6.180	176.37
6.200	176.61
6.220	176.85
6.240	177.08
6.260	177.32
6.280	177.56
6.300	177.79
6.320	178.03
6.340	178.26
6.360	178.50
6.380	178.73
6.400	178.96
6.420	179.20
6.440	179.43
6.460	179.66
6.480	179.90
6.500	180.13
6.520	180.36
6.540	180.59
6.560	180.82
6.580	181.05
6.600	181.28
6.620	181.51
6.640	181.74
6.660	181.97
6.680	182.19
6.700	182.42
6.720	182.65
6.740	182.88
6.760	183.10
6.780	183.33
6.800	183.55
6.820	183.78
6.840	184.00
6.860	184.23
6.880	184.45
6.900	184.68
6.920	184.90
6.940	185.12
6.960	185.35
6.980	185.57
7.000	185.79
7.020	186.01

RESISTIVITY	B/D VOLTAGE
7.040	186.23
7.060	186.45
7.080	186.67
7.100	186.89
7.120	187.11
7.140	187.33
7.160	187.55
7.180	187.77
7.200	187.99
7.220	188.21
7.240	188.42
7.260	188.64
7.280	188.86
7.300	189.07
7.320	189.29
7.340	189.51
7.360	189.72
7.380	189.94
7.400	190.15
7.420	190.37
7.440	190.58
7.460	190.79
7.480	191.01
7.500	191.22
7.520	191.43
7.540	191.65
7.560	191.86
7.580	192.07
7.600	192.28
7.620	192.49
7.640	192.70
7.660	192.91
7.680	193.12
7.700	193.33
7.720	193.54
7.740	193.75
7.760	193.96
7.780	194.17
7.800	194.38
7.820	194.59
7.840	194.79
7.860	195.00
7.880	195.21
7.900	195.41
7.920	195.62
7.940	195.83
7.960	196.03
7.980	196.24
8.000	196.44
8.020	196.65

TABLE 4.1E

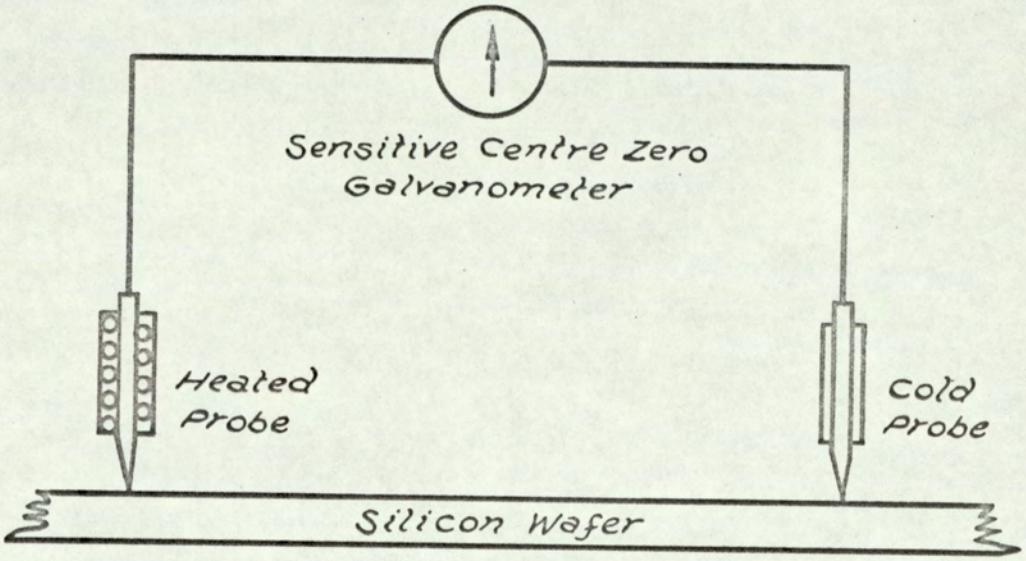
Computer print out of the three probe calibration for resistivity against breakdown voltage.

RESISTIVITY	B/D VOLTAGE	RESISTIVITY	B/D VOLTAGE
8.040	196.85	9.040	206.73
8.060	197.06	9.060	206.92
8.080	197.26	9.080	207.11
8.100	197.47	9.100	207.30
8.120	197.67	9.120	207.49
8.140	197.87	9.140	207.68
8.160	198.07	9.160	207.87
8.180	198.28	9.180	208.06
8.200	198.48	9.200	208.25
8.220	198.68	9.220	208.44
8.240	198.88	9.240	208.63
8.260	199.08	9.260	208.82
8.280	199.29	9.280	209.00
8.300	199.49	9.300	209.19
8.320	199.69	9.320	209.38
8.340	199.89	9.340	209.57
8.360	200.09	9.360	209.75
8.380	200.29	9.380	209.94
8.400	200.49	9.400	210.13
8.420	200.69	9.420	210.32
8.440	200.89	9.440	210.50
8.460	201.08	9.460	210.69
8.480	201.28	9.480	210.87
8.500	201.48	9.500	211.06
8.520	201.68	9.520	211.24
8.540	201.88	9.540	211.43
8.560	202.07	9.560	211.62
8.580	202.27	9.580	211.80
8.600	202.47	9.600	211.98
8.620	202.66	9.620	212.17
8.640	202.86	9.640	212.35
8.660	203.06	9.660	212.54
8.680	203.25	9.680	212.72
8.700	203.45	9.700	212.90
8.720	203.64	9.720	213.09
8.740	203.84	9.740	213.27
8.760	204.03	9.760	213.45
8.780	204.23	9.780	213.64
8.800	204.42	9.800	213.82
8.820	204.61	9.820	214.00
8.840	204.81	9.840	214.18
8.860	205.00	9.860	214.36
8.880	205.19	9.880	214.54
8.900	205.39	9.900	214.73
8.920	205.58	9.920	214.91
8.940	205.77	9.940	215.09
8.960	205.96	9.960	215.27
8.980	206.16	9.980	215.45
9.000	206.35	10.000	215.63
9.020	206.54	10.020	215.81

TABLE 4.2

Chemical etches used for stacking fault delineation

Westinghouse Silver etch	40 ml. hydrofluoric acid 20 ml. nitric acid 40 ml. deionised water 20 gram. silver nitrate
Dash etch	3 parts nitric acid 12 parts acetic acid 1 part hydrofluoric acid
CP_4	5 parts nitric acid 3 parts acetic acid 3 parts hydrofluoric acid
Iodine etch	110 ml. acetic acid 100 ml. nitric acid 50 ml. hydrofluoric acid 0.3 grams Iodine
Sirtl etch	1 part 33 Wt % aqueous solution of chromium trioxide 2 parts hydrofluoric acid
Salier etch	300 ml. nitric acid 600 ml. hydrofluoric acid 2 ml. bromine 24 grams copper nitrate Solution diluted 10:1 with deionised water before use and etch for 4 hours.



6 4.1 SCHEMATIC DIAGRAM OF THERMO-ELECTRIC PROBE.

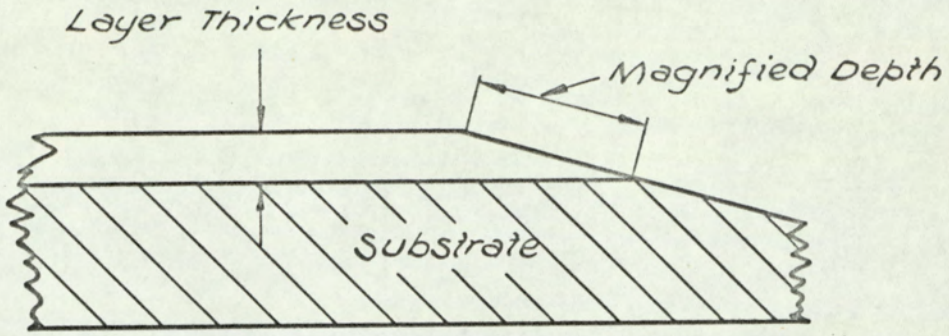


FIG. 4.2. SECTION OF BEVELLED SILICON SUBSTRATE.

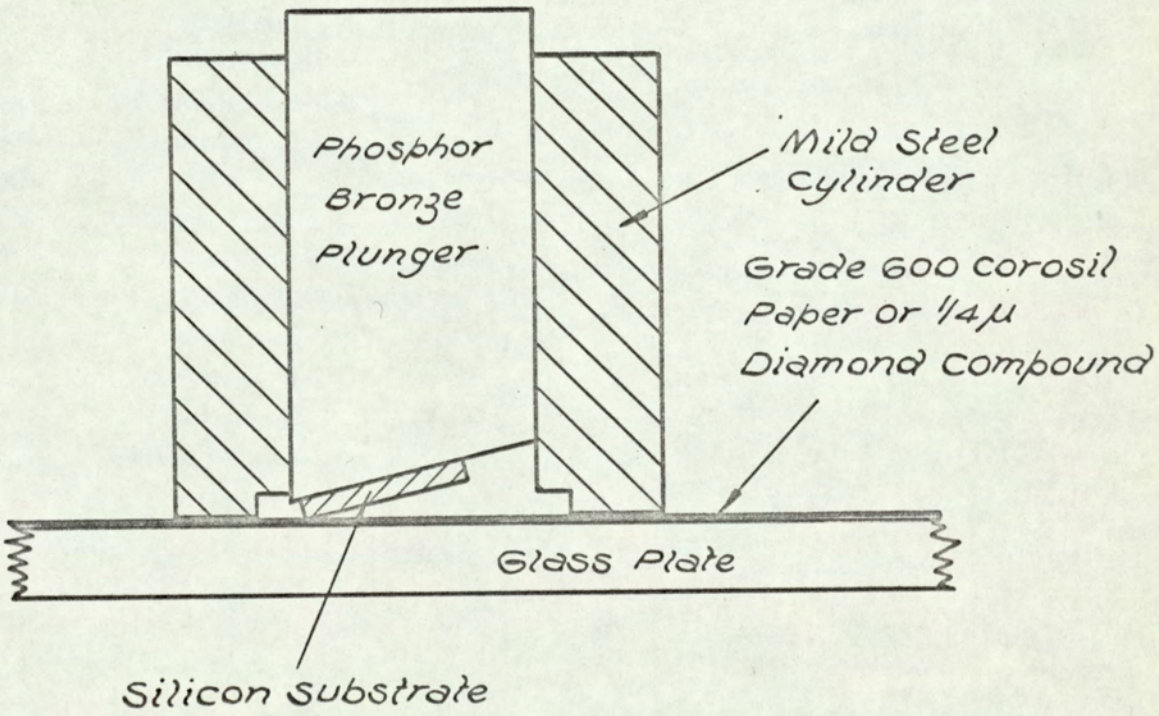
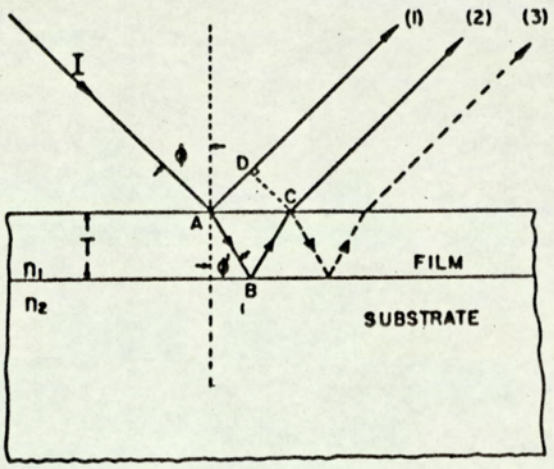


FIG. 4.3 GRINDING JIG ASSEMBLY.

Fig. 4.4 Bevelled and stained substrate surface.

1.0 ohm.cm. P layer on 0.01 ohm.cm. N antimony doped substrate.



Ray diagram for reflection from a film deposited on a thick substrate. The amplitudes of rays 1, 2, 3, etc., add vectorially resulting in maxima and minima in the reflectance spectrum.

Fig. 4.5 Ray diagram for reflection from a film deposited on a thick substrate

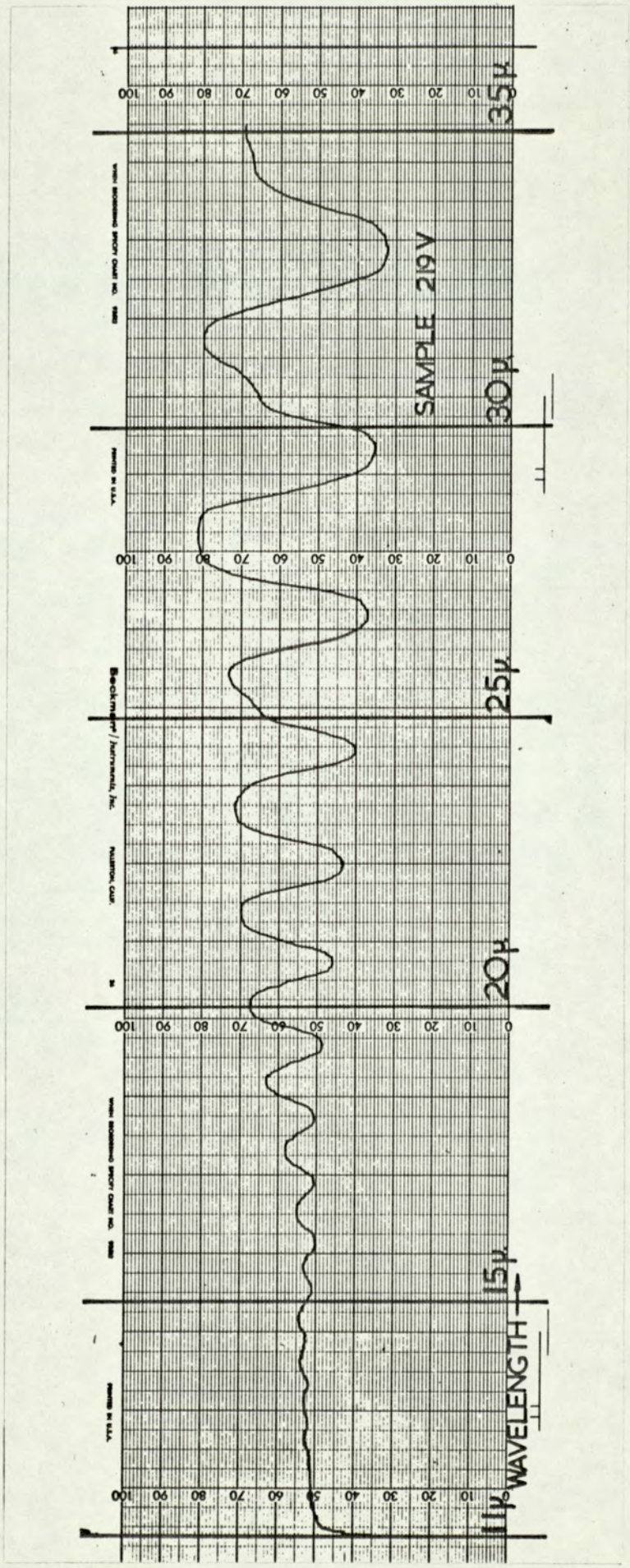


Fig. 4.6 Infrared reflectance spectrum

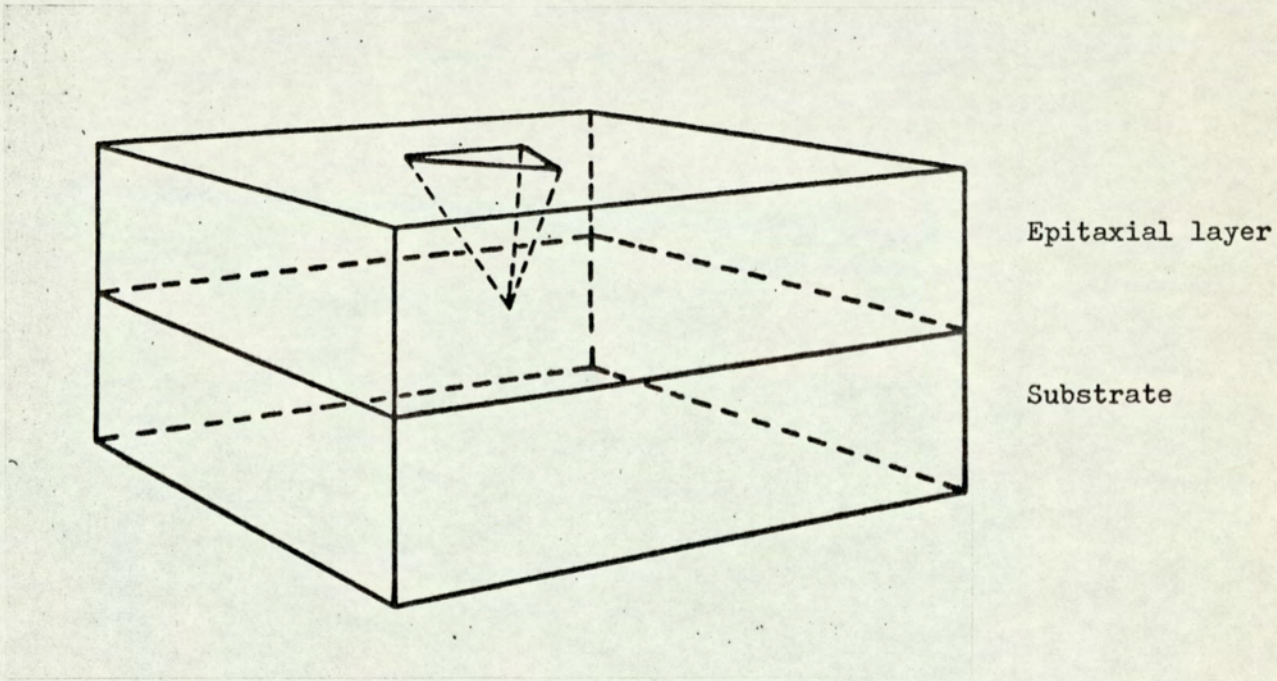


Fig. 4.7 Stacking fault formation on (111) substrate

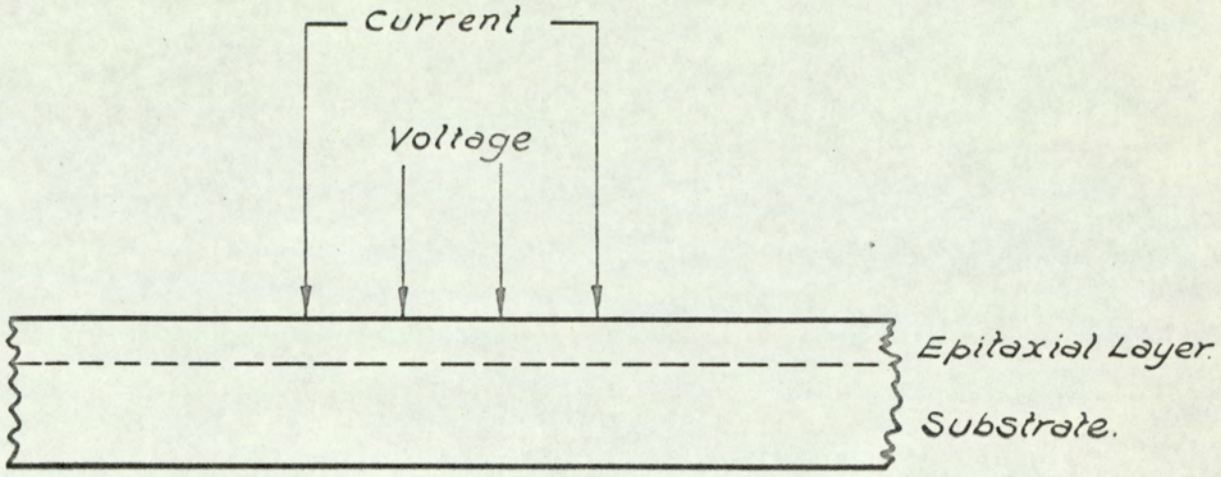


FIG. 4.8 4 POINT PROBE SYSTEM.

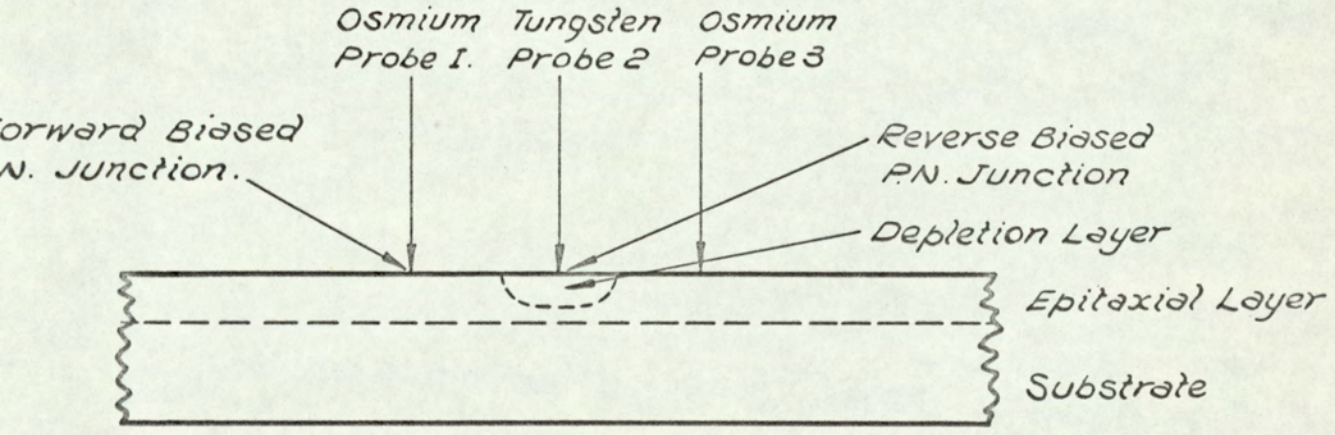


FIG. 4.9. 3 POINT PROBE SYSTEM.

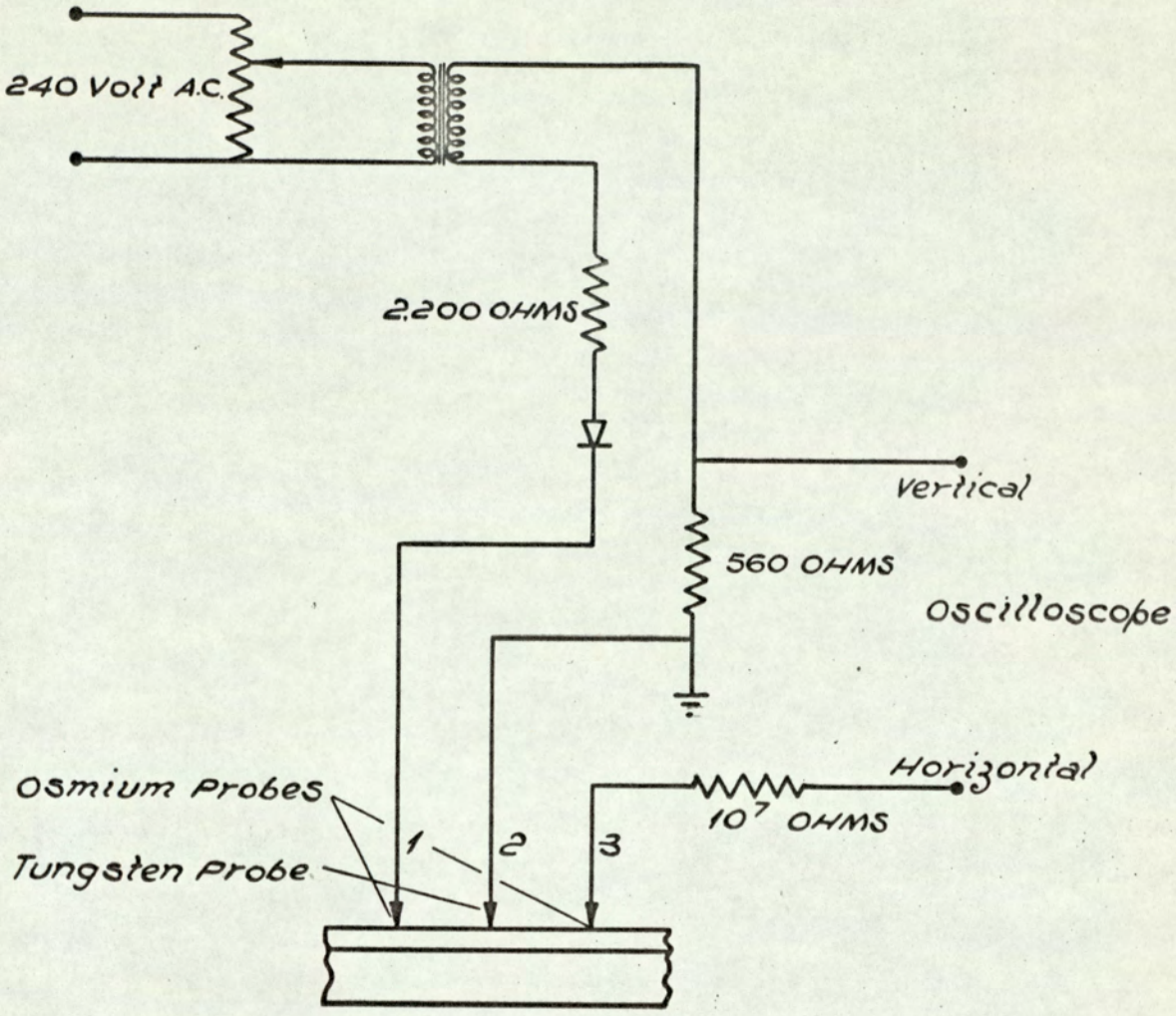


FIG. 4.10. CIRCUIT FOR THREE POINT PROBE MEASURMENTS.

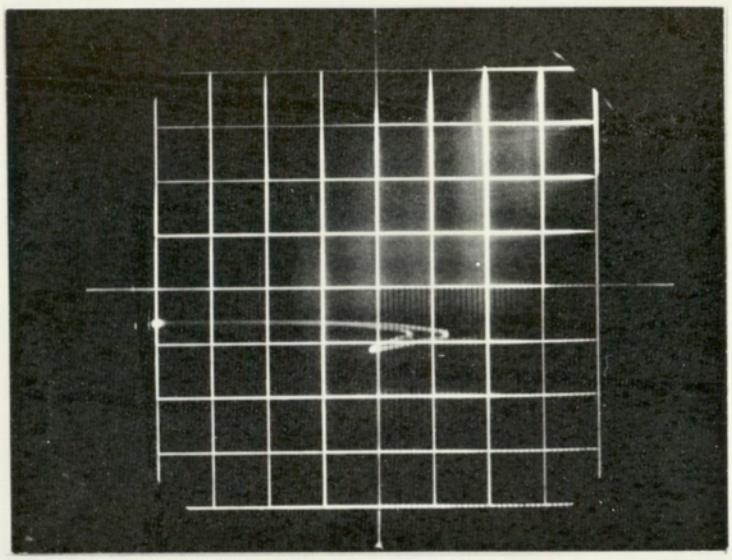


Fig. 4.11 Three point probe current-voltage trace

Calibration 1 cm = 28 volts
Breakdown voltage = 148.4 volts

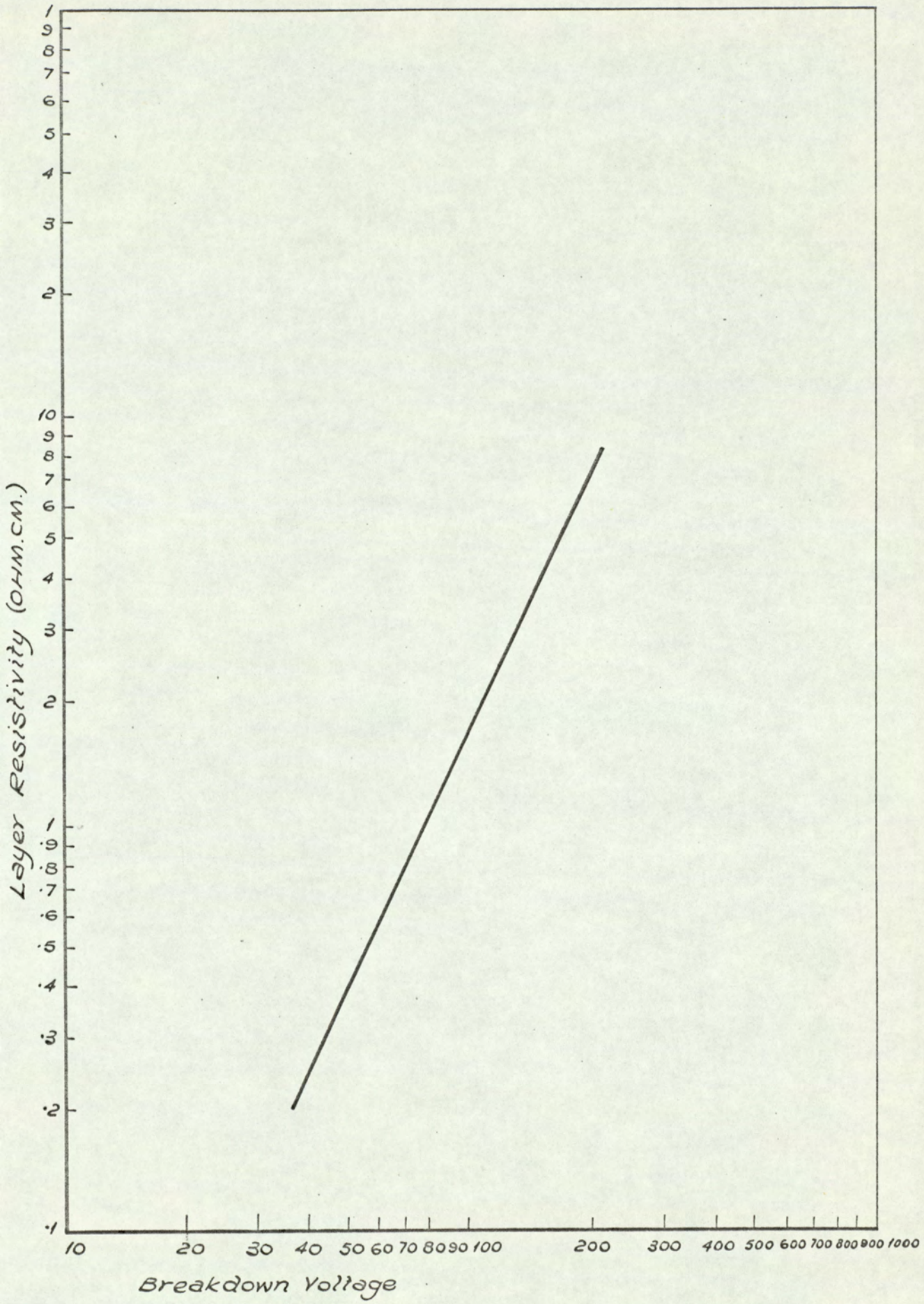


FIG. 4.12. BREAKDOWN VOLTAGE–LAYER RESISTIVITY CALIBRATION FOR THREE POINT PROBE.

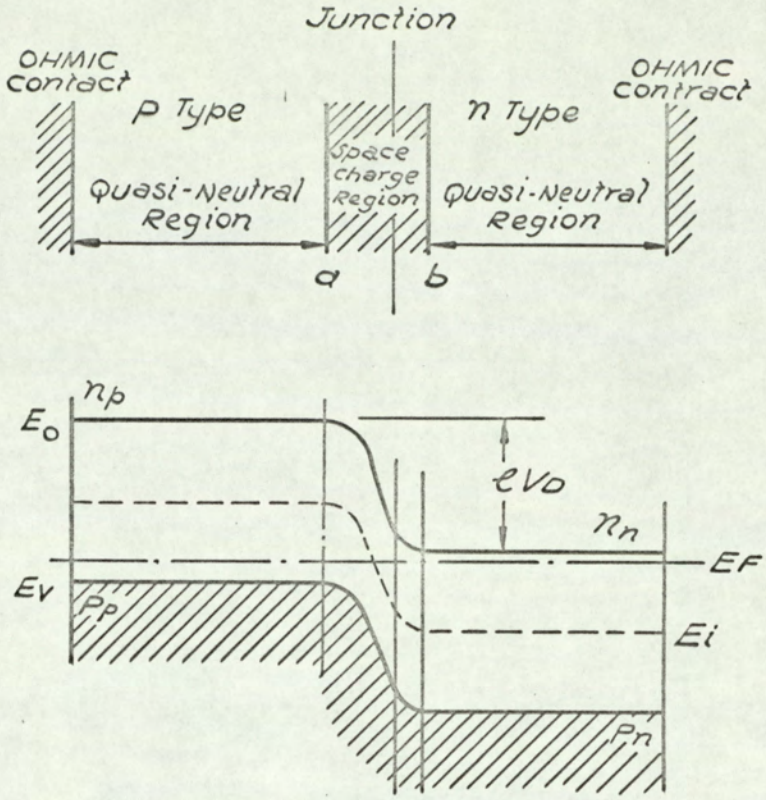


FIG. 4.13. PN JUNCTION IN THERMAL EQUILIBRIUM

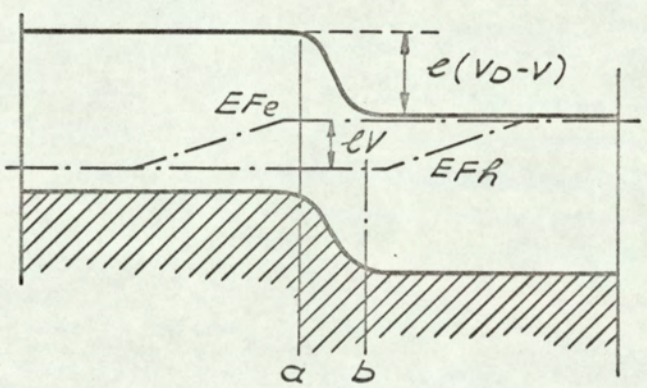


FIG. 4.14. FORWARD FLOW OF CURRENT IN A PN JUNCTION AT LOW INJECTION LEVEL.

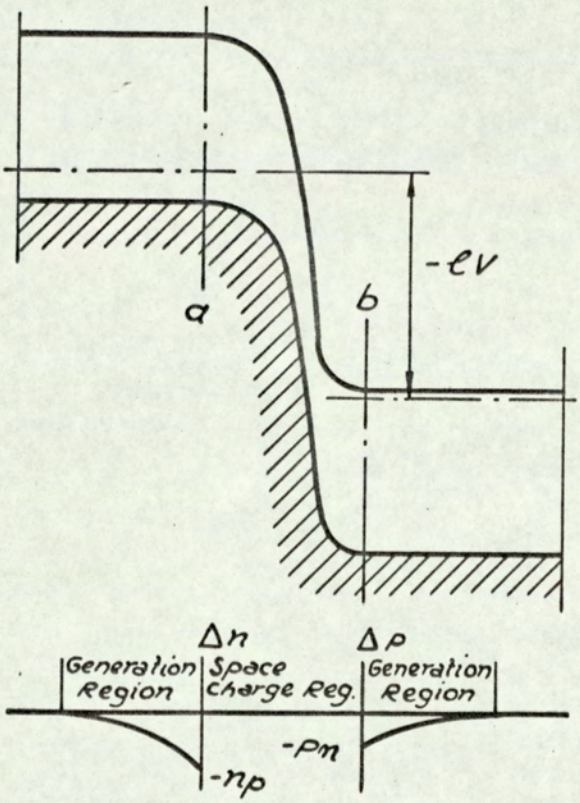


FIG. 4·15. PN. JUNCTION WITH A REVERSE APPLIED BIAS.

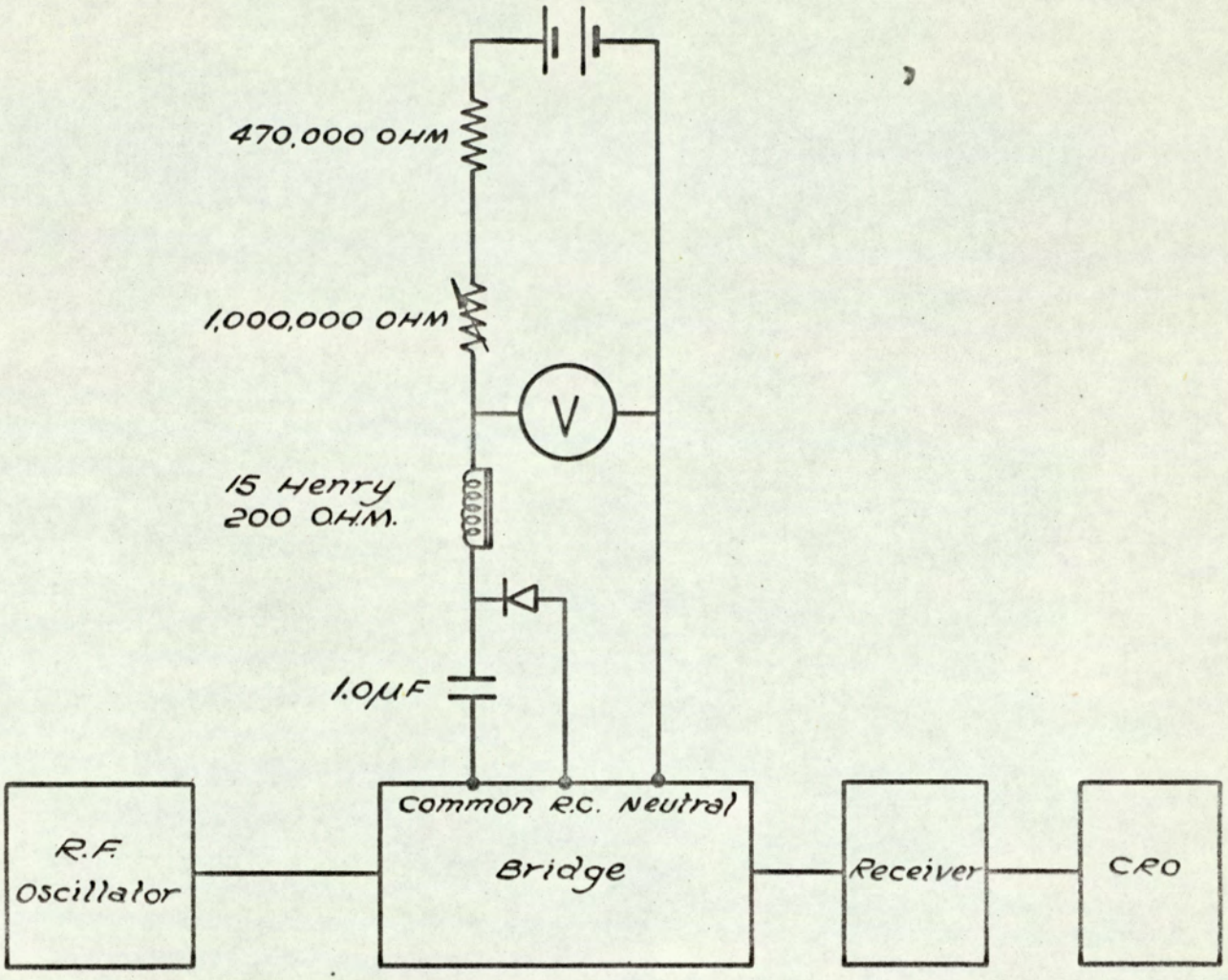


FIG 4.16 CIRCUIT FOR JUNCTION CAPACITANCE MEASUREMENTS.

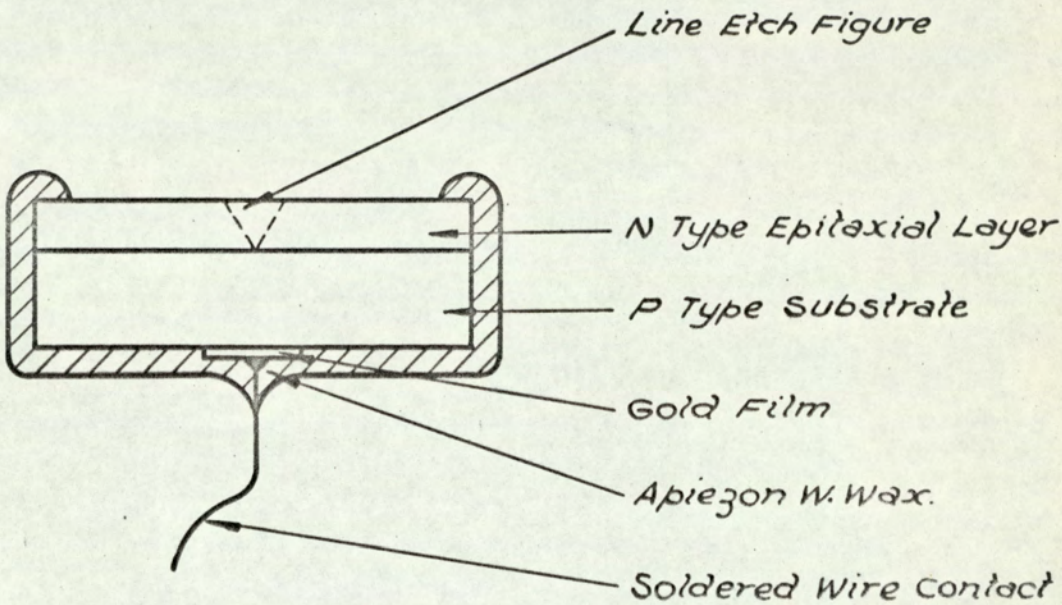


FIG. 4.17. EPITAXIAL SUBSTRATE PREPARED FOR EXAMINATION FOR ELECTRICAL LEAKAGE AT LINE ETCH FIGURES.

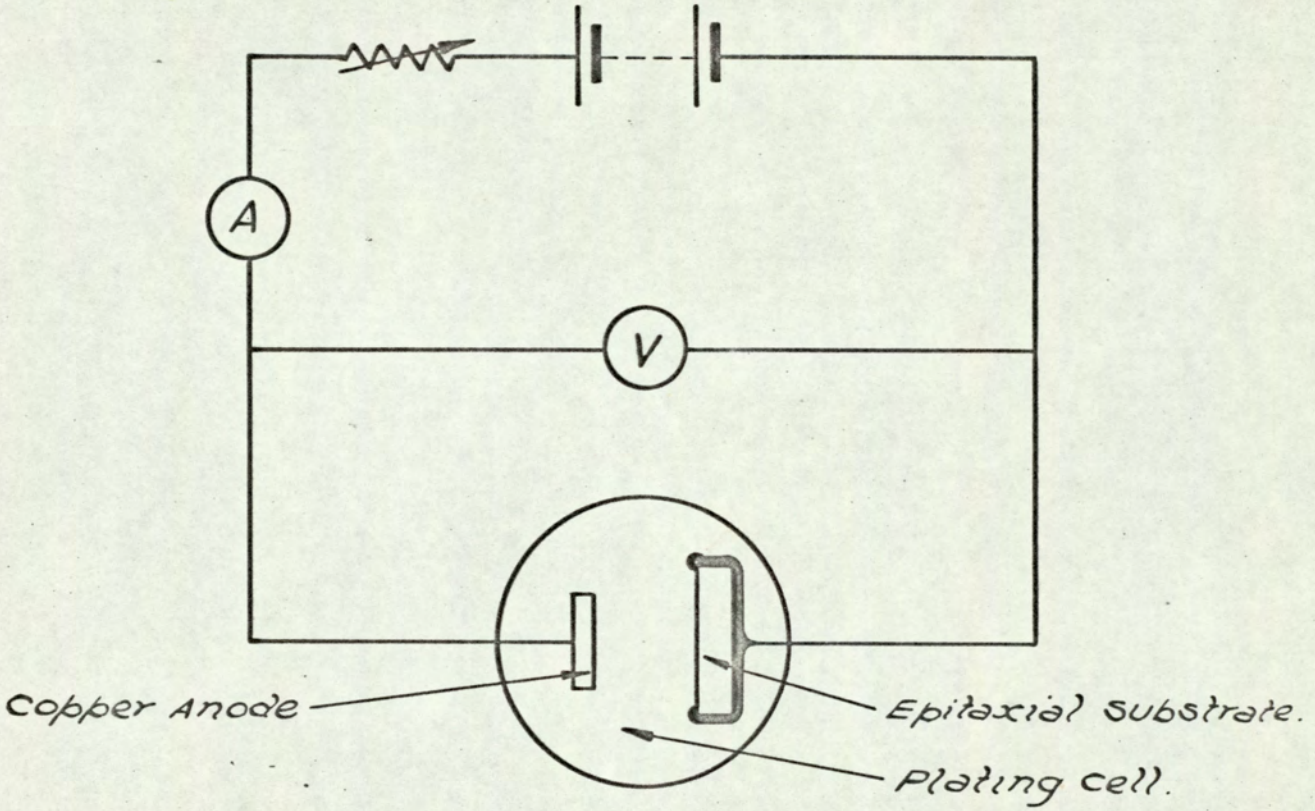


FIG.4.18. PLATING CIRCUIT FOR EXAMINATION FOR ELECTRICAL LEAKAGE.

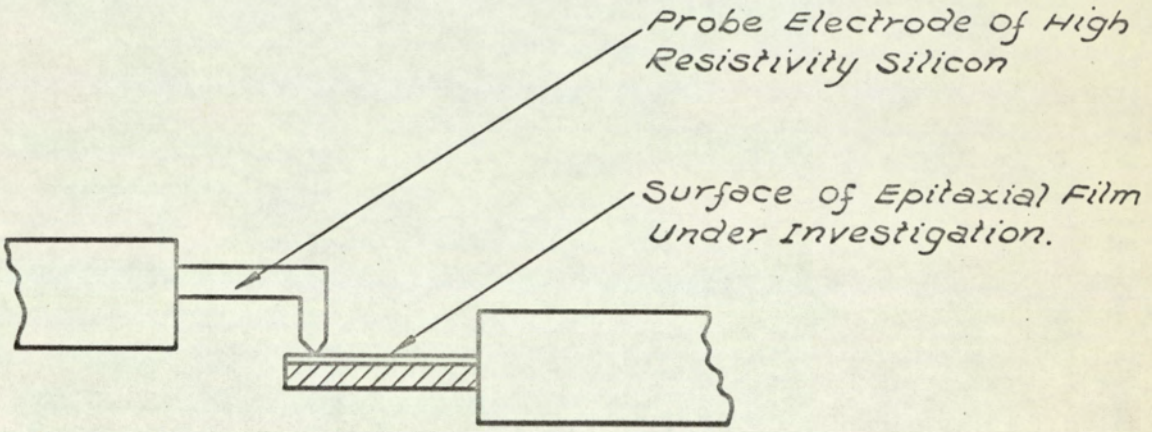


FIG. 4.19. MASS SPECTROMETER ELECTRODE ARRANGEMENT.

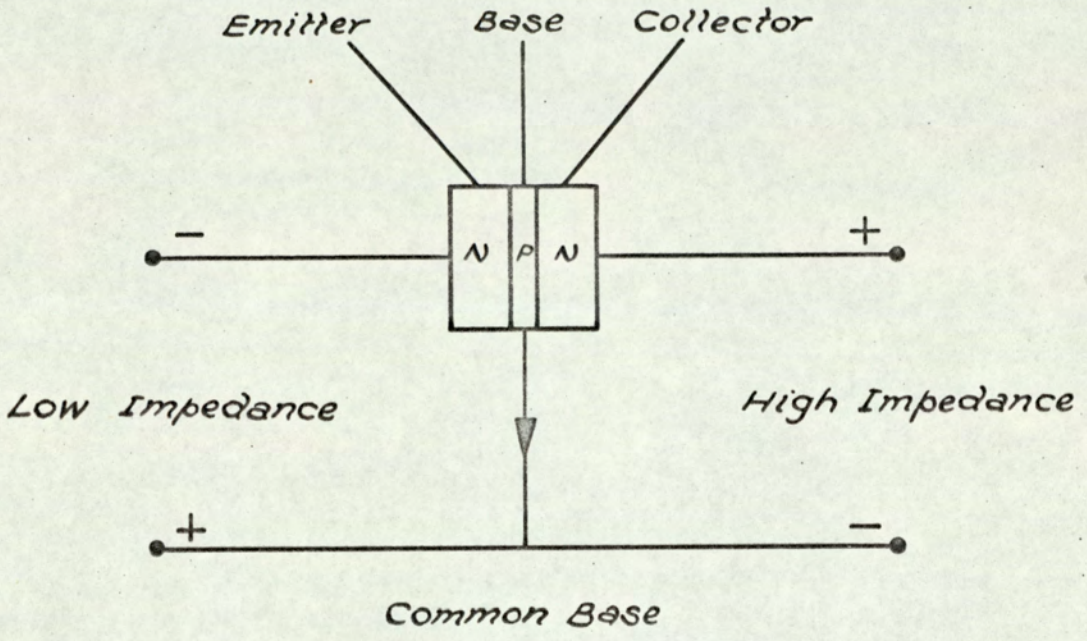


FIG. 4.20. FUNCTIONAL TRANSISTOR.

5. INFLUENCE OF PROCESS VARIABLES AND EXPERIMENTAL TECHNIQUES ON DEPOSITION AND PROPERTIES OF EPITAXIAL LAYERS

5.1 Purity of the Gas System

It is important that the hydrogen gas contains a negligible amount of molecular or combined oxygen because its presence will result in (A) crystal imperfections in the epitaxial layer or (B) inhibit epitaxial nucleation. The commercial high purity hydrogen gas used, a by-product from the electrolysis of brine to produce sodium hydroxide, is purified by a Deoxo Catalytic type purifier which employs a platinum metal catalyst to combine the oxygen impurities with twice its volume of hydrogen to form water and leave less than 1 volume part per million of oxygen remaining. The water vapour is removed from the purified hydrogen, by passing it through a drier containing molecular sieve as the drying agent to less than 1VPM.

Contamination of the purified hydrogen can occur as it flows through the gas system:-

1. if the apparatus is not perfectly clean and dry
2. due to trapped gas impurities resulting from incomplete purging of the gas system prior to epitaxial deposition
3. as the result of leaks in the initial deposition apparatus at the ground glass joints and at stopcocks during manipulation because the halide vapours slowly attack the Kel-F grease used on the ground glass surfaces.
4. from incompletely made compression fittings or O-ring seals in the multi-deposition apparatus
5. from harmful impurities contained in other gases introduced into the system

5.2 Deposition Temperature

The effect of deposition temperature on epitaxial nucleation in the initial vertical reaction system is listed in Table 5.1 and micro-photographs are shown in Figures 5.1 to 5.6. For epitaxial growth of the

layers the substrate temperature must be above 1150°C but for microscopic layer perfection, growth should be at the highest possible temperature. Unfortunately as the growth temperature is increased it is possible that the rate of transfer of impurity atoms from the substrate to the layer will increase. In practice it was found that with substrate temperatures above 1350°C, melting of the silicon susceptor coating could occur and molten silicon would rapidly spread over the susceptor resulting in uncontrolled temperature rise of the substrate and possible melting. For these reasons the majority of layers produced in this report were grown in the temperature range 1200°-1300°C.

Figure 5.7 illustrates the growth rate as a function of temperature. Below 1150°C, growth rate increases with temperature, but above this temperature no significant difference is observed. The growth rate for aqueously etched substrates was slightly lower than that for mechanically polished substrate surfaces.

5.3 Silicon tetrachloride - hydrogen concentration

In the vertical deposition apparatus the two variables for controlling the concentration of silicon tetrachloride in the hydrogen are (A) the hydrogen flow rate and (B) the temperature of the silicon tetrachloride, Figure 5.8, shows that an increase in hydrogen flow rate results in an increase in the concentration of silicon tetrachloride in the hydrogen and similarly an increase in the silicon tetrachloride temperature results in an increased concentration in the hydrogen. As the two variables are increased more silicon atoms are introduced into the gas stream and result in faster growth rates as indicated in Figure 5.9.

In the multi-deposition apparatus the growth rates were derived from the substrate in the position nearest to the gas inlet and the layer thickness measured with the infra-red method. This gas system has a third variable, the main hydrogen flow. This main hydrogen does not flow through the silicon tetrachloride but is mixed with the hydrogen flow

through the silicon tetrachloride. As in the previous section the increase in the silicon tetrachloride temperature or the silicon tetrachloride-hydrogen flow result in faster growth rates (Figures 5.10 and 5.11) while increase of the main hydrogen flow reduces the growth rate (Figure 5.12).

In practice it is found that a high main hydrogen flow is required to obtain uniform growth over a number of substrates on the susceptor and that the silicon tetrachloride temperature and silicon tetrachloride-hydrogen flow are adjusted to give a reasonable growth rate compatible with uniform layer growth. Table 6.13 lists the gas process details that have been used in this apparatus.

5.4 Deposition Time

For both the initial deposition apparatus - vertical system and the multi-deposition apparatus, increase in deposition time results in thicker layers, Figure 5.13. If all deposition conditions are kept constant the overall layer thickness will be a function of the growing time.

5.5 The effect of reaction tube geometry on layer thickness in the initial deposition apparatus

In this section the layer thickness was measured by the angle lapping and staining technique.

The measurement of layer thickness across two diameters D_1 and D_2 of the substrate processed in the vertical reaction tube are shown for 3 samples in Figure 5.14. The gas injection was along the diameter D_2. The measurements indicate that the layer is not uniform in thickness and the largest variation occurs along the diameter normal to the gas inlet and the degree of variation is not constant from one run to another. Also shown is a statistical analysis of these measurements for the range of the mean for 95% confidence which indicates that the possible thickness variation across the diameter of the substrate is larger than the measured variation.

Figure 5.15 shows layer thickness measurements and their statistical analysis obtained on substrates processed in the horizontal reaction tube with horizontal gas flow. The thickest layer is obtained near the gas inlet and the thinnest layer near the exist. As with the Vertical Reaction tube a slightly larger variation occurs across the diameter of the tube in comparison with that in the flow direction. Analysis of the variance indicates that the substrate diameter and not its position influences the thickness uniformity of the layer.

When the gases enter the horizontal reaction tube through the gas inlet tube shown in Figure 3.7A situated above the substrates, the layer on the area of the substrate directly underneath an inlet hole grew at a faster rate and resulted in a layer of thickness shown schematically in Figure 5.16.

For the inlet tube shown in Figure 3.7C and with the gas flowing vertically down onto the substrate, layer thickness measurements and analysis are shown in Figure 5.17. A considerable variation in layer thickness occurs across both diameters of the substrate while the range of variation is not the same for each substrate. When this gas inlet tube is turned through 180°, large variations in layer thickness occur across the substrate in the direction of the diameter of the tube with little variation in the longitudinal direction, while the magnitude of variation is similar for each substrate.

The gas inlet system, Figure 3.7B, had a large variation of layer thickness across both diameters on a single substrate.

In the system, where the gases are introduced into the horizontal reaction tube from above the substrates, the analysis of the variance indicates that the substrate diameter and its position influences the thickness uniformity of the layer.

5.6 Layer thickness variation in the multideposition apparatus

In practice it has been found that (A) by tilting the susceptor 5° to 10° into the direction of the gas flow so that each substrate receives a fresh supply of non-depleted gases, (B) having the front part of the susceptor approximately $20^{\circ}C$ lower in temperature to form a temperature gradient along the first quarter of the length of the susceptor and (C) not positioning the substrate at the very edge of the susceptor near the gas inlet, it has been possible to obtain layers of thickness as shown in Figure 5.18 for layers grown simultaneously on a number of substrates.

The results of layer thickness measurements obtained with the infra-red method indicate that within the limits of layer thickness measurement, uniform layers can be obtained on individual substrates and on simultaneously grown substrates with the experimental conditions used in this reaction system.

5.7 The effect of the substrate on layer properties

The epitaxial layer surface in general is a duplication of the substrate surface. A flat mechanically polished substrate surface results in a layer with a mirror surface. Fine scratches on the substrate tend to disappear in the growing layer, but coarse scratches result in fine lines on the layer surface, and the orange peel effect obtained on aqueous polishing of the substrate is duplicated in the layer surface.

Defects in the epitaxial layer have been observed after etching with Sirtl etch in the form of line etch figures. On (111) orientated substrates they appear triangular, Figures 5.19 and 5.20, and as squares or parts of squares on (100) orientated substrates,

Figure 5.21. The highest concentration at the layer surface, Table 5.2, is obtained on mechanically polished substrate surfaces with a reduction after the surface has been aqueously or electro polished while they were almost completely eliminated with hydrogen chloride polishing.

Another type of defect "etch pits", Figure 5.22, were observed after further etching and their concentration at the layer surface shown in Table 5.3. The number of etch pits appears to be independent of the surface preparation but does appear to be related to the method of growing the original single crystal from which the substrate is prepared.

The substrate doping element and concentration also effects the epitaxial layer. Table 5.4 indicates that the resistivity of epitaxial layers, grown from intrinsic silicon tetrachloride (i.e. contains no doping) on 0.01 ohm cm N substrates is effected by the substrate doping element and that the highest resistivity layers are grown on antimony doped substrates, followed by arsenic and the lowest with phosphorus.

Similarly the resistivity of the substrate affects the type and resistivity of the epitaxial layer when grown from intrinsic silicon tetrachloride. Table 5.5 shows that increase in resistivity of N type antimony doped substrates increases the N layer resistivity while Figure 5.23 indicates that with low resistivity P type boron doped substrates P layers are initially obtained, which change to compensated and finally to N as the substrate resistivity is increased.

5.8 Doping Methods

The type and impurity concentration of the growing silicon layer can be controlled by incorporating impurity atoms into the growing crystal

lattice. The ratio of impurity atoms to silicon atoms in the gas phase is controlled so that the growing layer contains the desired impurity concentration.

Solution doping and gas doping involve the addition of the appropriate Group 3 or Group 5 impurity to the gas stream during the epitaxial growth cycle.

In solution doping, a volatile impurity is added to the silicon tetrachloride and evaporates with it to provide doping of the layer. This method is only applicable when the vapour pressure of the dopant is similar to that of the silicon tetrachloride and there is no chemical reaction between the two. Phosphorus trichloride and boron tribromide have been used for this purpose and a comparison of their vapour pressures together with that of silicon tetrachloride is shown in Figure 5.24. The amount of liquid dopant required in the silicon tetrachloride is very small and is obtained with an "Agla" micrometer precision burette which can measure accurately a volume of 0.001 ml and is used to produce a master doped solution of silicon tetrachloride. This master solution is in turn diluted further until the required resistivity is obtained. Figure 5.25 shows the effect of the phosphorus trichloride concentration in the silicon tetrachloride on the resistivity of the N type epitaxial layer grown on a 9 ohm cm P substrate.

Experiments to grow P type layers of controlled resistivity with boron tribromide doping of silicon tetrachloride were unsuccessful and control of the layer type was erratic.

For dopants of relatively low vapour pressure e.g. antimony trichloride the pure dopant can be incorporated in an evaporator in parallel with the pure silicon tetrachloride and the relative hydrogen flow rate and evaporator temperature used to control the concentration of dopant in the gas stream.

Gas doping involves the introduction of dopants by means of an independent gas stream. The dopants used are hydrides e.g. diborane and phosphine diluted in hydrogen to the parts per million range. The control

of the concentration of the dopant in the main gas stream is achieved by accurate control of the small gas flow. Figure 5.26 shows the relationship between N type epitaxial layer resistivity and the phosphine/hydrogen doped gas flow. Similarly Figure 5.27 shows the relationship for P type layers and diborane/hydrogen doped gas.

5.9 Summary

The preceding results indicate:-

1. Impurities in the gas system effect the nucleation, the type and impurity concentration of the growing layer and result in lattice defects.
2. The temperature of deposition influence the type of nucleation and growth rate.
3. The hydrogen flow rate, silicon tetrachloride temperature and reaction tube geometric effect the growth rate and layer thickness uniformity.
4. The method of preparation of the substrate, its type of doping element and concentration influence the epitaxial layer type, its impurity concentration and crystal imperfections.

TABLE 5.1

Influence of Temperature on Layer Morphology

Figure No.	Deposition Temperature	Surface Preparation	
5.1	1000°C	Mechanically polished.	Small crystallites nucleated at points on the surface.
	1000°C	Mechanically polished and etched.	No deposit.
5.2	1100°C	Mechanically polished.	Increase in the number of crystallites on the substrate surface and in certain areas the crystallites had started to coalesce (dark area).
5.3; 5.4	1100°C	Mechanically polished and etched.	One area of the substrate has polycrystalline growth, while another area has epitaxial growth. The macro photographs indicate the transformation across the substrate from polycrystalline crystals which first coalesce to an undefined structure and then to typical three-fold symmetrical pyramids that are characteristic of (111) growth and epitaxial with the substrate. It is possible that this change from polycrystalline to epitaxial growth on the substrate surface at this temperature is due to one or both of the following:- 1. A variation in concentration of the gas above the substrate due to preferential flow down one side of the susceptor, 2. A slight variance in temperature across the substrate resulting from (A) uneven contact between the substrate and susceptor or (B) the susceptor being slightly nearer the coil at this position.
5.5	1200°C	Mechanically polished.	Epitaxial layer as indicated by the high reflectivity of the surface. The layer surface has areas of facet growth.

Continued.....

TABLE 5.1 (CONTINUED)

Figure No.	Deposition Temperature	Surface Preparation	
5.6	1200°C	Mechanically polished and etched.	Epitaxial layer. The surface contains a number of triangular pyramids having various shapes. The edge of the substrate shows a grain boundary, separating a small area containing a large number of triangular defects, from the main epitaxial layer containing less pronounced defects. This small area which does not appear to have the same orientation as the main layer probably results from nucleation and growth on the edge of the wafer.
	1300°C	Mechanically polished.	High reflectivity epitaxial layer.
	1300°C	Mechanically polished and etched.	Epitaxial layer indicating pattern of etched surface.
	1350°C	Mechanically polished.	High reflectivity epitaxial layer.
	1350°C	Mechanically polished and etched.	Epitaxial layer indicating pattern of etched surface.

TABLES 5.2 and 5.3

Positions for counting line etch figures and etch pits at the epitaxial layer surface on the silicon substrate

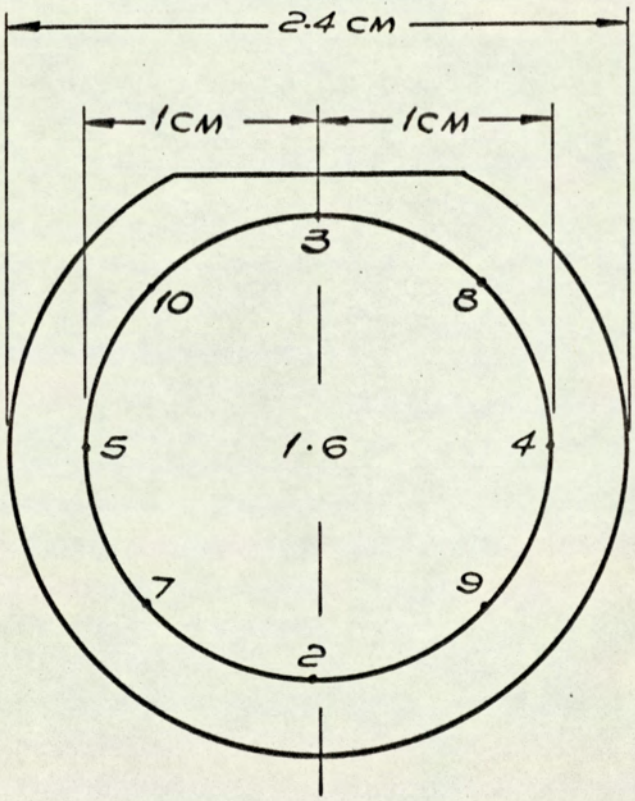


TABLE 5.2

Line etch figure (stacking fault) counts in the epitaxial layer

Substrate Number	Method of Growing Substrate	Final Surface Preparation	Substrate Resistivity (ohm cm) and type	Substrate Doping Element	Layer Thickness (microns)	Substrate Counting Position 1	2	3	4	5	6	7	8	9	10	Mean	Density of Line etch figures per sq.cm.
						Sampling Area 0.015 sq. cm.											
172	Float Zoned	Mechanical Polished	18-25P	Boron	21.2	213	98	316	177	169						195	1.3×10^4
187	Pulled	Mechanical Polished	0.0094-.019N	Arsenic	13.4	85	64	78	61	107						78	5.2×10^3
173	Float Zoned	Aqueously Etched	18-25P	Boron	20.4	7	12	3	8	10						8	5.4×10^2
186	Pulled	Aqueously Etched	0.0095-.019N	Arsenic	15.4	9	17	9	11	10						11	7.4×10^2
						Sampling Area 0.0245 sq. cm.											
EF1	Float Zoned	Gaseous Hydrogen Chloride	1500P	Boron	21.6	1	Nil	2	Nil	Nil	Nil	1	2	Nil	Nil	0.6	24
EF2	Float Zoned	Gaseous Hydrogen Chloride	1500P	Boron	21.6	3	Nil	1	Nil	2	3	Nil	4	Nil	2	1.5	61
EP1	Pulled	Gaseous Hydrogen Chloride	0.01N	Antimony	21.6	Nil	Nil	Nil	Nil	Nil	Nil	Nil	Nil	Nil	Nil	Nil	Nil
EP2	Pulled	Gaseous Hydrogen Chloride	0.01N	Antimony	23.4	Nil	Nil	Nil	1	Nil	Nil	Nil	Nil	1	2	0.4	16

TABLE 5.3

Etch Pit Counts in the Epitaxial Layer and Substrate

Substrate Number	Method of Growing Substrate	Final Surface Preparation	Substrate Resistivity (ohm cm) and type	Substrate Doping Element	Layer Thickness (microns)	Substrate Counting Position 1	2	3	4	5	6	7	8	9	10	Mean	Density of Line etch figures per sq. cm.
						Sampling Area 0.00375 sq.cm.											
-	Float Zoned		18-25P	Boron		166	185	51	60	38	151	81	83	66	34	77.5	2.07×10^4
-	Pulled		0.0095-.019N	Arsenic		Nil	Nil	1	Nil	Nil	Nil	1	Nil	1	2	0.4	1.07×10^2
	Epitaxial Layer																
172	Float Zoned	Mechanical Polished	18-25P	Boron	21.2	92	160	60	80	76	121	101	46	114	142	99.2	3.29×10^4
187	Pulled	Mechanical Polished	0.0095-.019N	Arsenic	13.4	Nil	17	30	20	9	Nil	6	12	18	1	11.3	3.02×10^3
173	Float Zoned	Aqueously Etched	18-25P	Boron	20.4	100	137	87	70	60	92	96	52	76	77	84.7	2.24×10^4
186	Pulled	Aqueously Etched	0.0095-0.019N	Arsenic	15.4	11	35	20	13	8	5	11	19	27	24	11.3	4.61×10^3
	Substrate																
						Sampling Area 0.001 sq.cm.											
-	Float Zoned			Boron		12	7	7	25	5	12	9	12	13	5	10.7	1.1×10^4
-	Pulled			Antimony		Nil	Nil	1	Nil	Nil	Nil	Nil	Nil	Nil	Nil	0.1	1.0×10^2
-	Pulled			Antimony		Nil	Nil	Nil	Nil	Nil	Nil	Nil	Nil	Nil	Nil	Nil	Nil
	Epitaxial Layer																
EF1	Float Zoned	Gaseous Hydrogen Chloride	1500P	Boron	21.6	7	16	19	22	5	7	2	16	5	42	14.1	1.4×10^4
EF2	Float Zoned	Gaseous Hydrogen Chloride	1500P	Boron	21.6	3	10	40	10	57	6	8	25	73	6	23.8	2.4×10^4
EP1	Pulled	Gaseous Hydrogen Chloride	0.01N	Antimony	21.6	Nil	14	3	8	6	Nil	14	Nil	1	4	5.0	5.0×10^3
EP2	Pulled	Gaseous Hydrogen Chloride	0.01N	Antimony	23.4	Nil	5	Nil	11	6	Nil	5	Nil	20	6	5.3	5.3×10^3

TABLE 5.4

The effect of the N type substrate doping element on layer resistivity

Substrate No.	Substrate Resistivity ohm cm	Doping Element	Mean epitaxial Layer Resistivity ohm cm
268	0.01-0.012	Antimony	12.8
272	0.0095-0.019	Arsenic	1.9
273	0.013-0.029	Phosphorus	0.55

TABLE 5.5

The effect of N type antimony doped substrate impurity concentration on layer resistivity

Substrate No.	Epitaxial Layer Thickness microns	Substrate Resistivity ohm cm	Substrate Doping Element	Mean Epitaxial Layer Resistivity ohm cm
268	24.2	0.01-0.012	Antimony	12.8
269	22.5	0.14	Antimony	14.6
271	25.0	1.1-1.7	Antimony	30.0

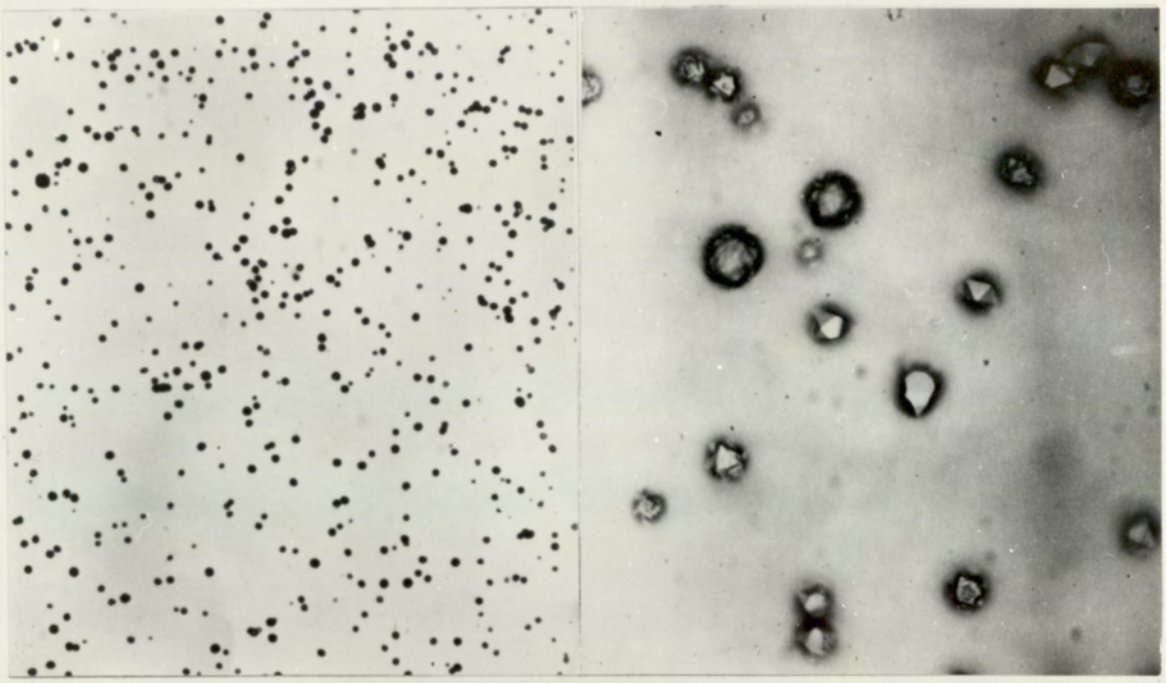
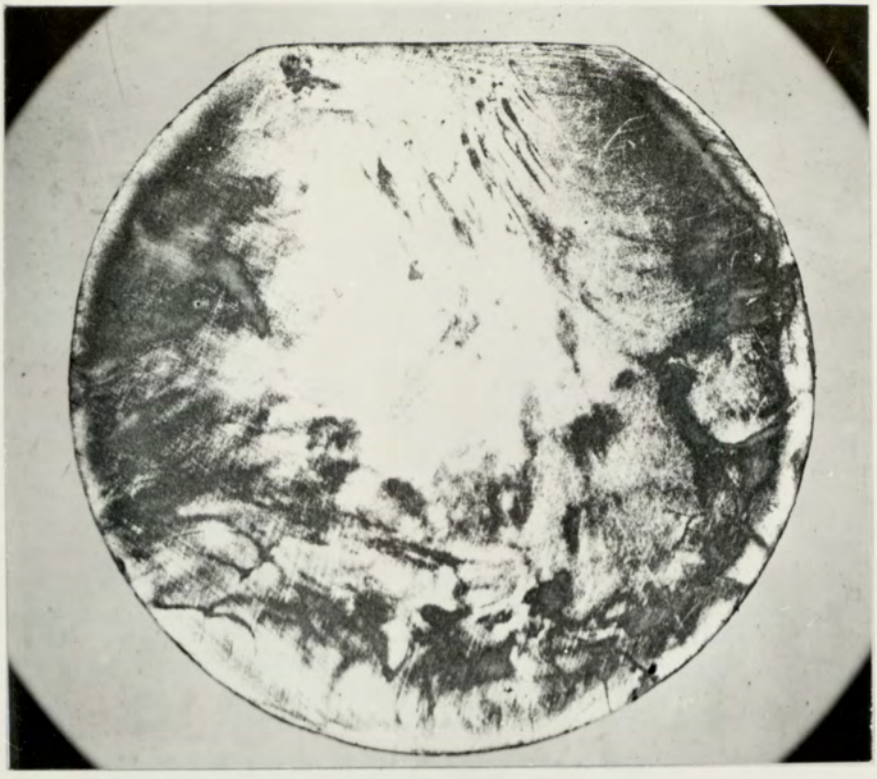
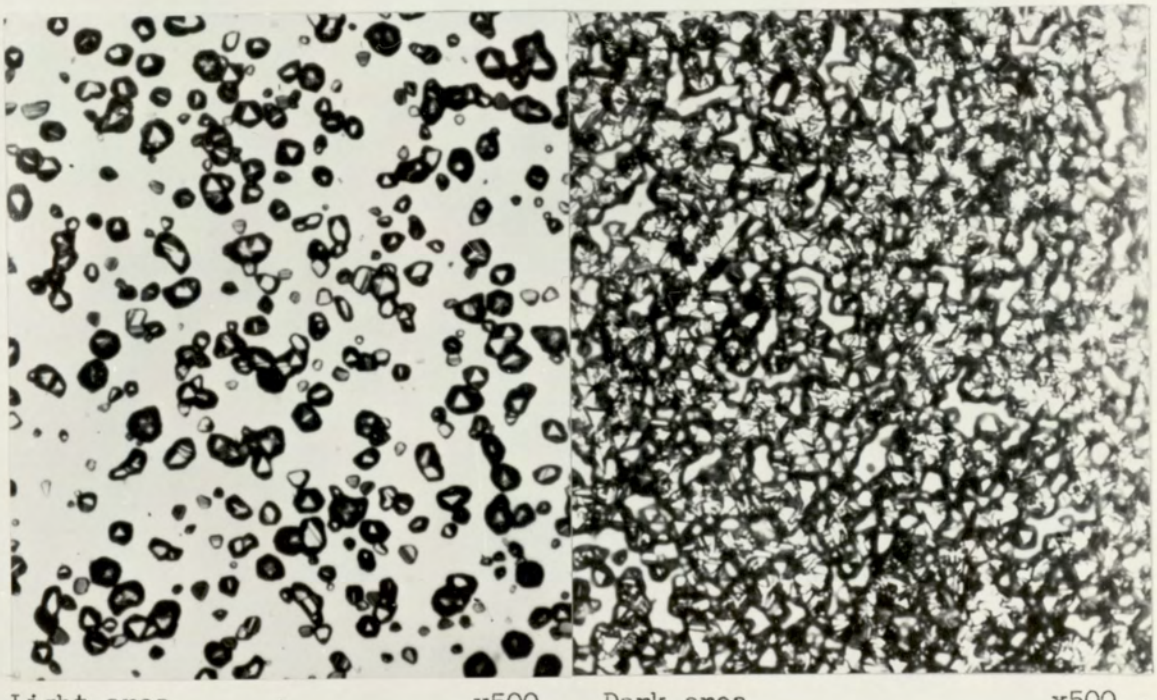


Fig. 5.1 Mechanically polished substrate surface after deposition at 1000°C

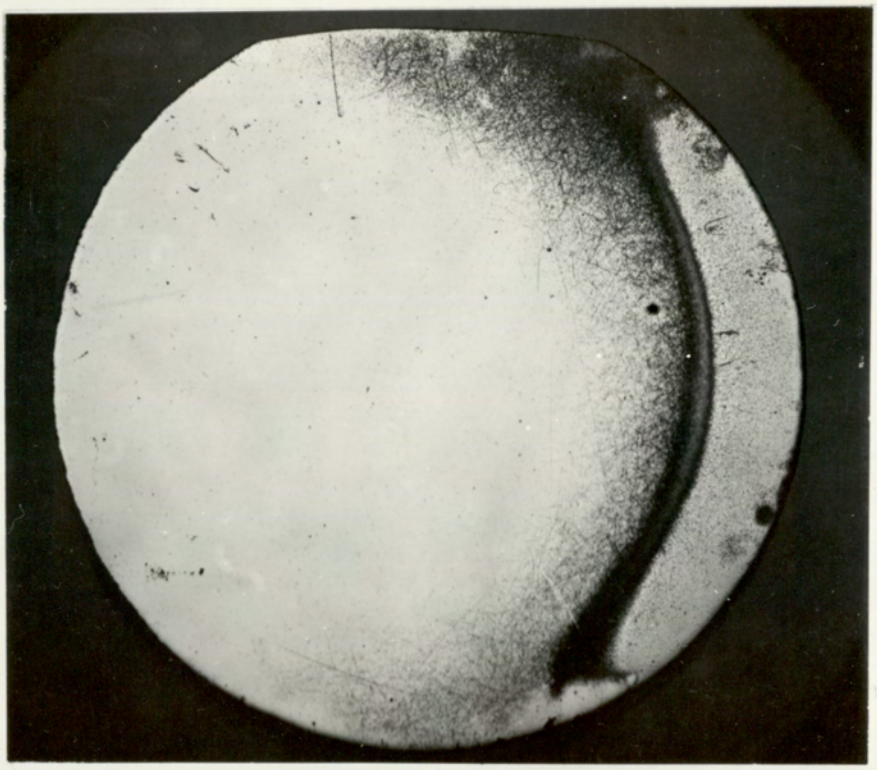


x5



Light area x500 Dark area x500

Fig. 5.2 Mechanically polished substrate surface after deposition at 1100°C



x5

Fig. 5.3 Etched substrate surface after deposition at 1100°C

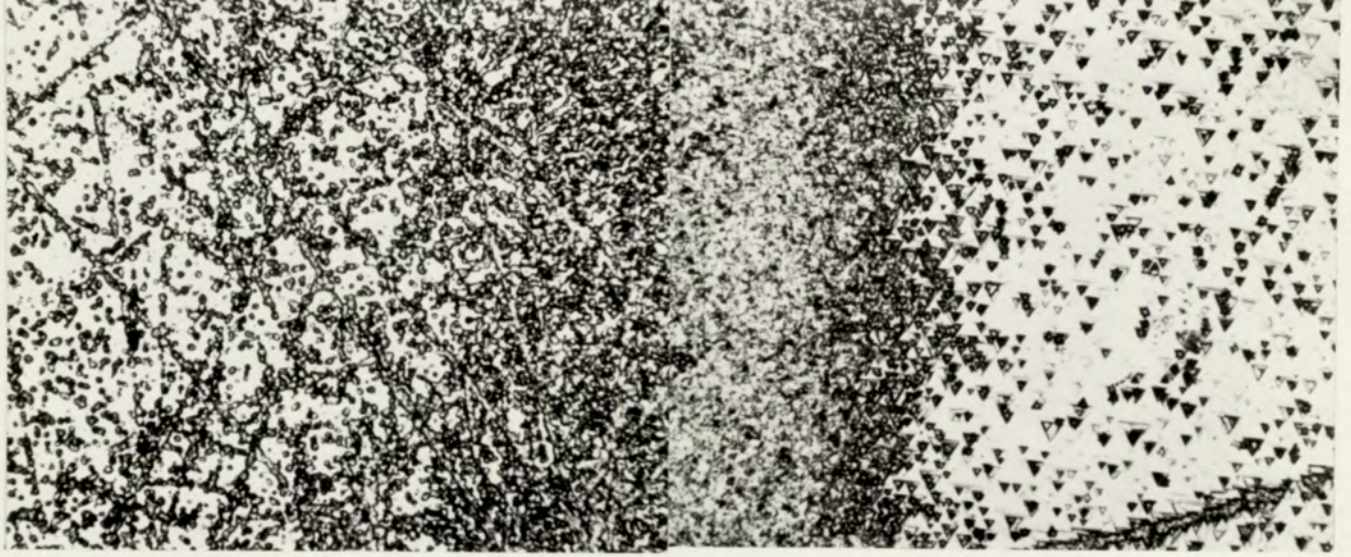
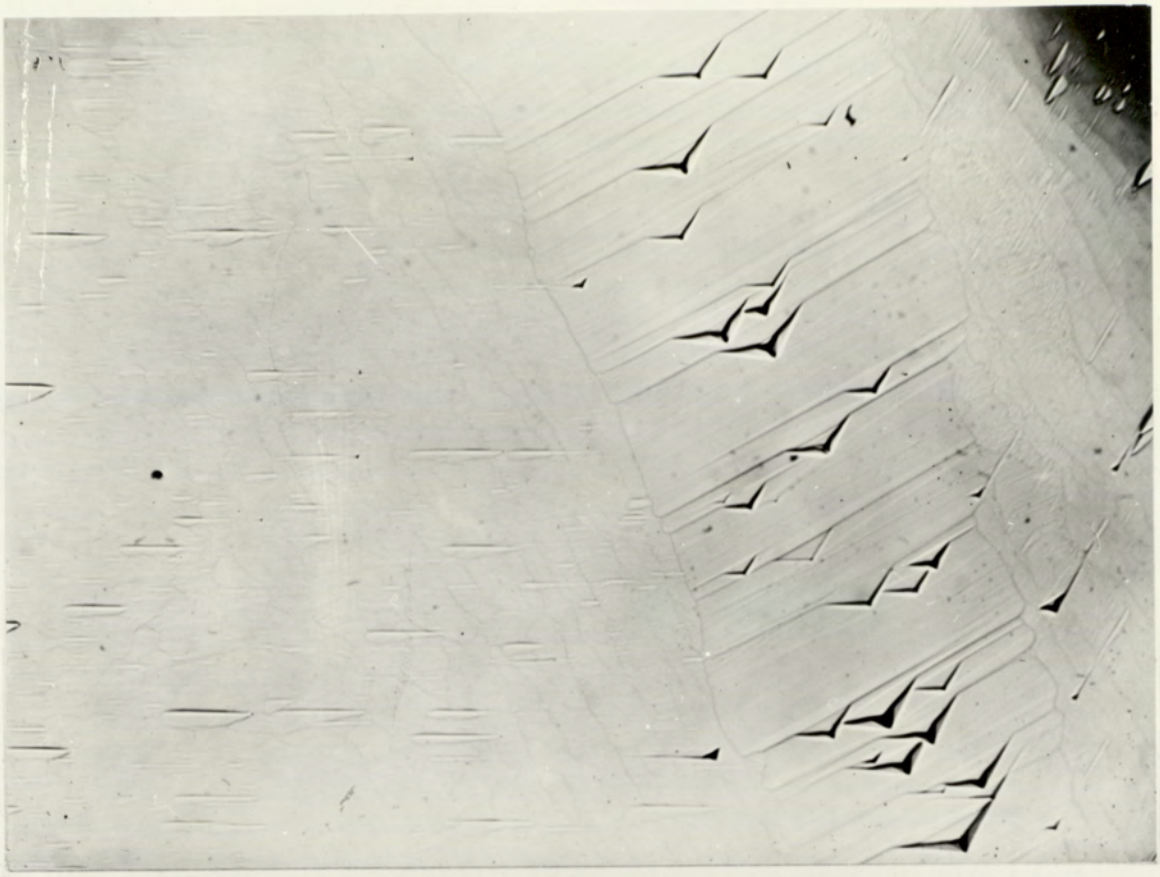


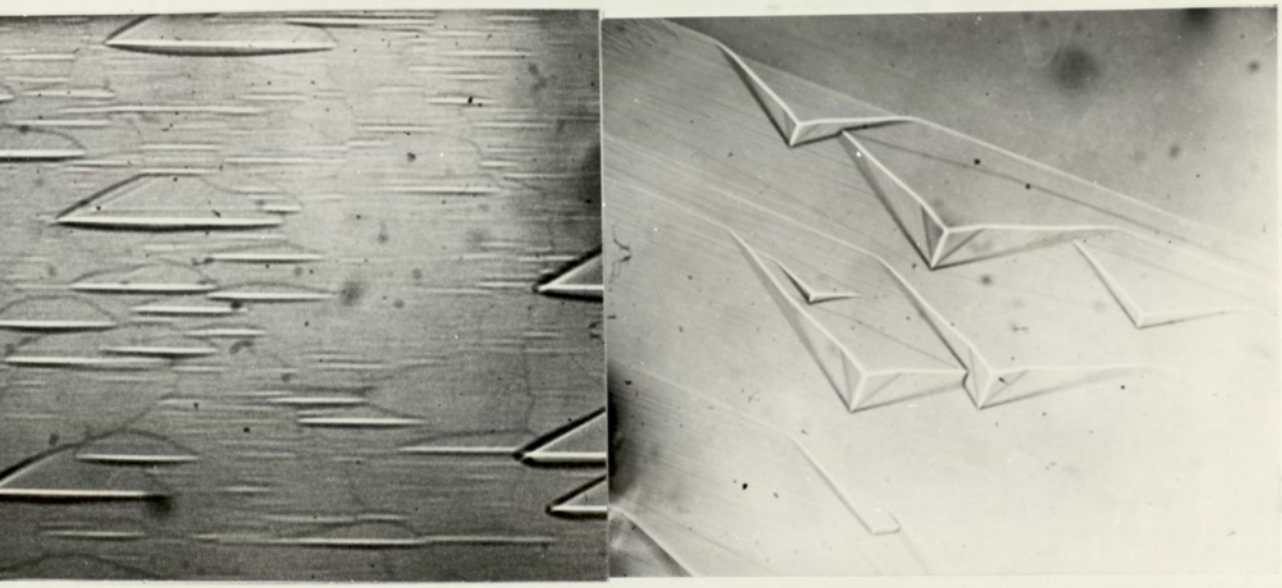
Fig. 5.4 Dark area on the substrate surface of Fig. 5.3 at higher magnification

x15

Fig. 5.5 Mechanically polished substrate surface after deposition at 1200°C



x15



x40

Fig. 5.6 Etched substrate surface after deposition at 1200°C

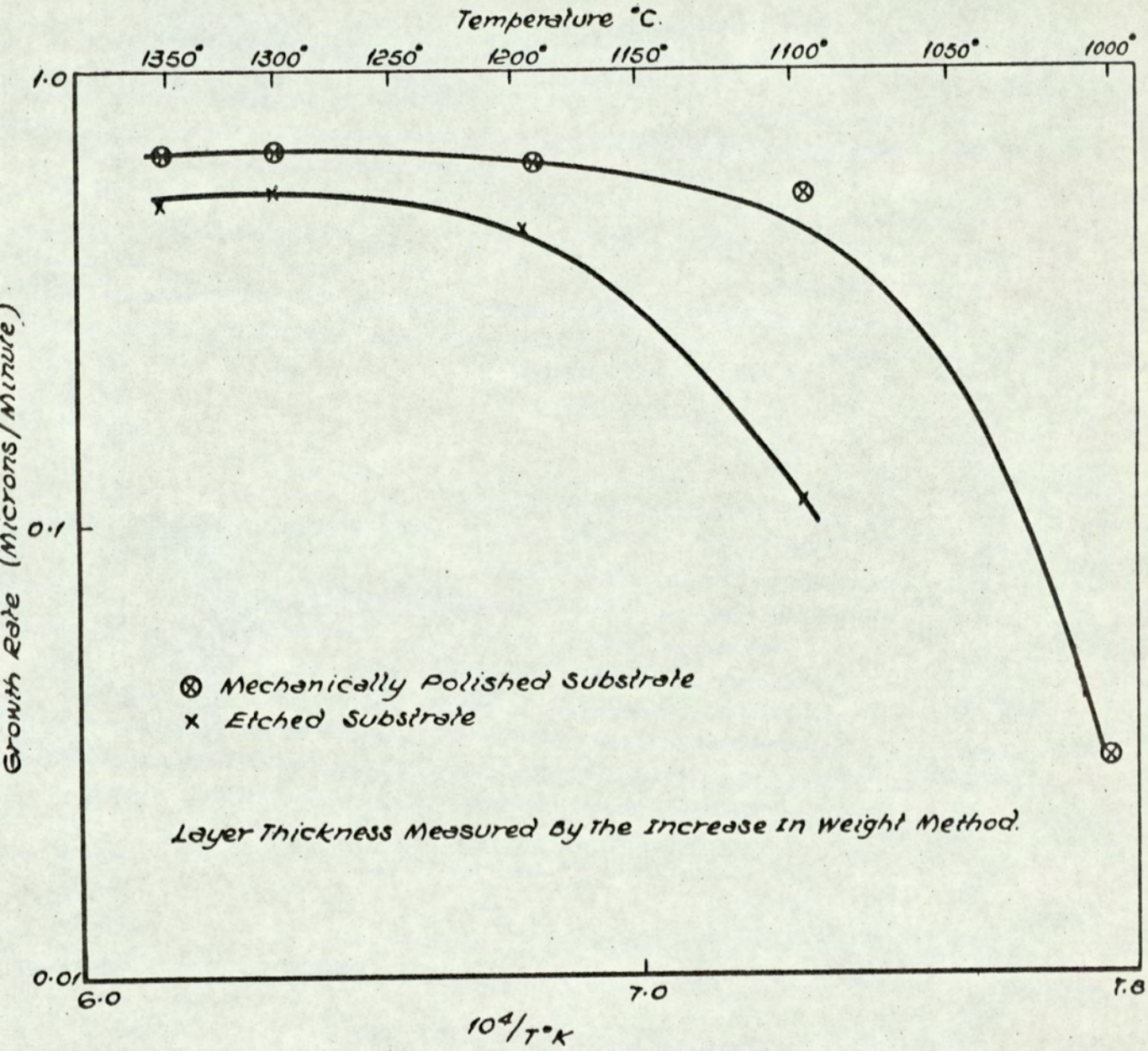


FIG 5.7 GROWTH RATE AS A FUNCTION OF TEMPERATURE.

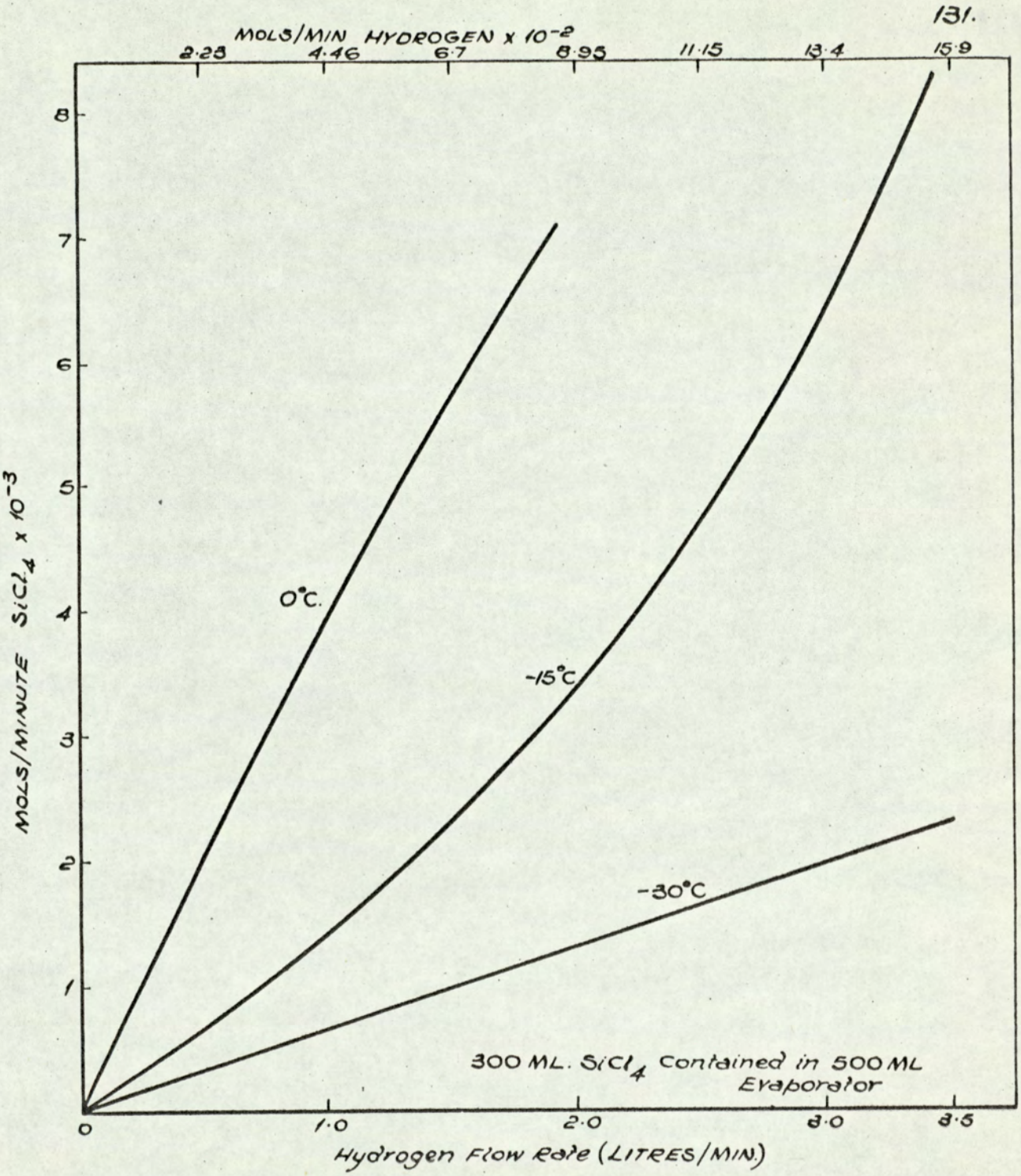
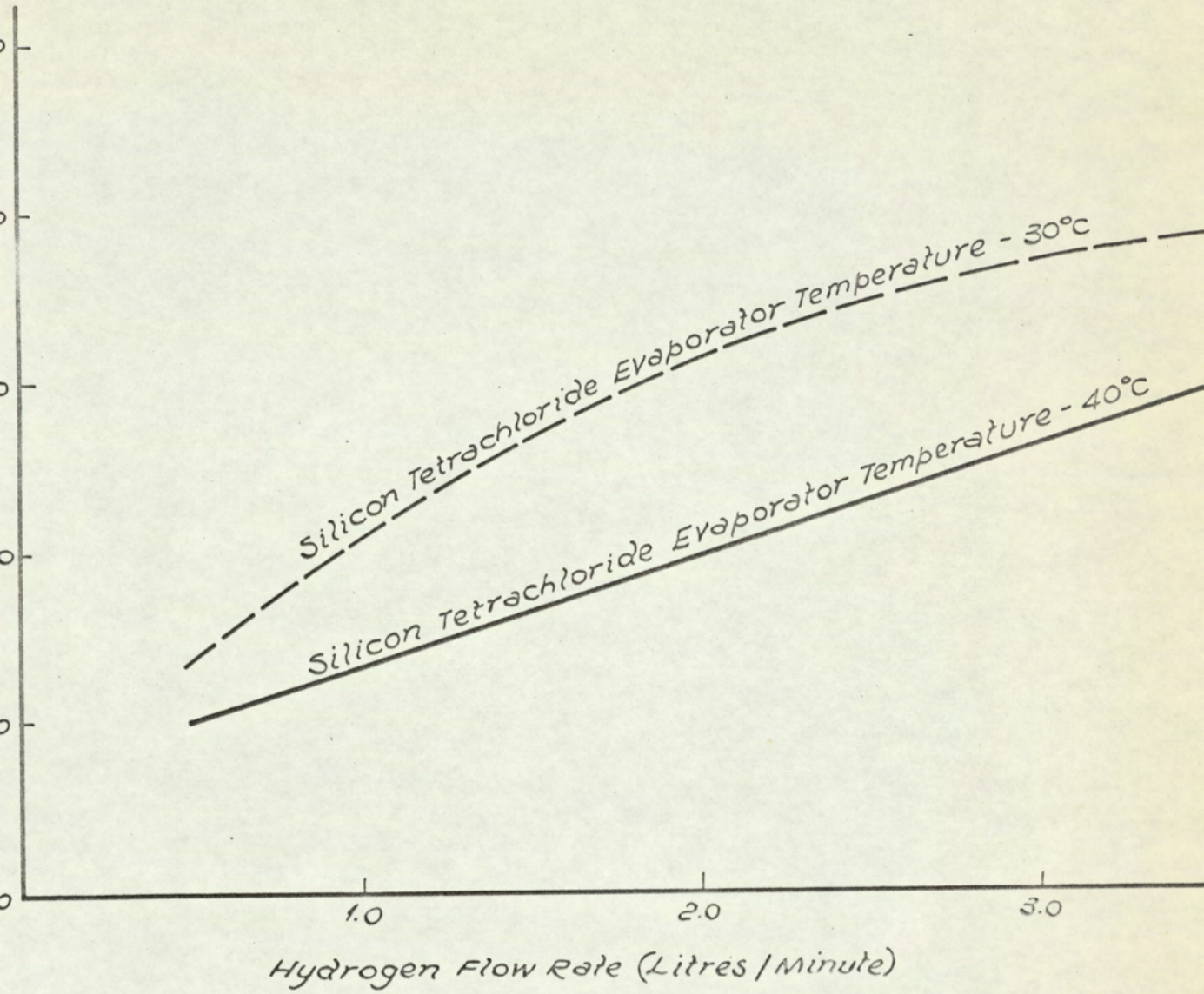


FIG.58. EFFECT OF HYDROGEN FLOW RATE ON THE CONCENTRATION OF $SiCl_4$ IN THE GAS STREAM OF THE INITIAL DEPOSITION APPARATUS.



6.5.9. EFFECT OF HYDROGEN FLOW RATE ON THE LAYER GROWTH RATE IN THE INITIAL DEPOSITION APPARATUS.

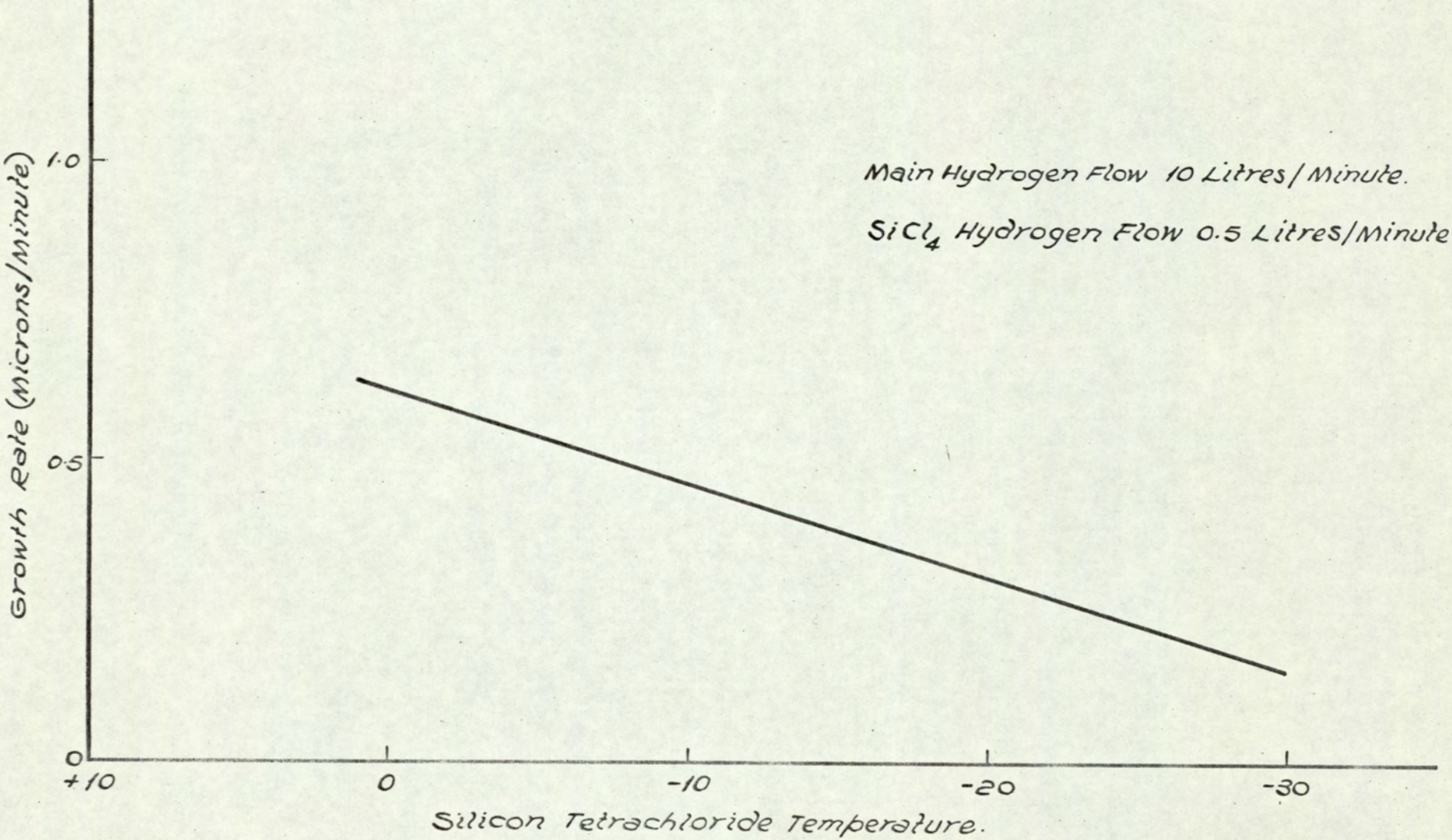


FIG. 5.10. INFLUENCE OF SILICON TETRACHLORIDE TEMPERATURE ON THE GROWTH RATE IN THE MULTI-DEPOSITION APPARATUS.

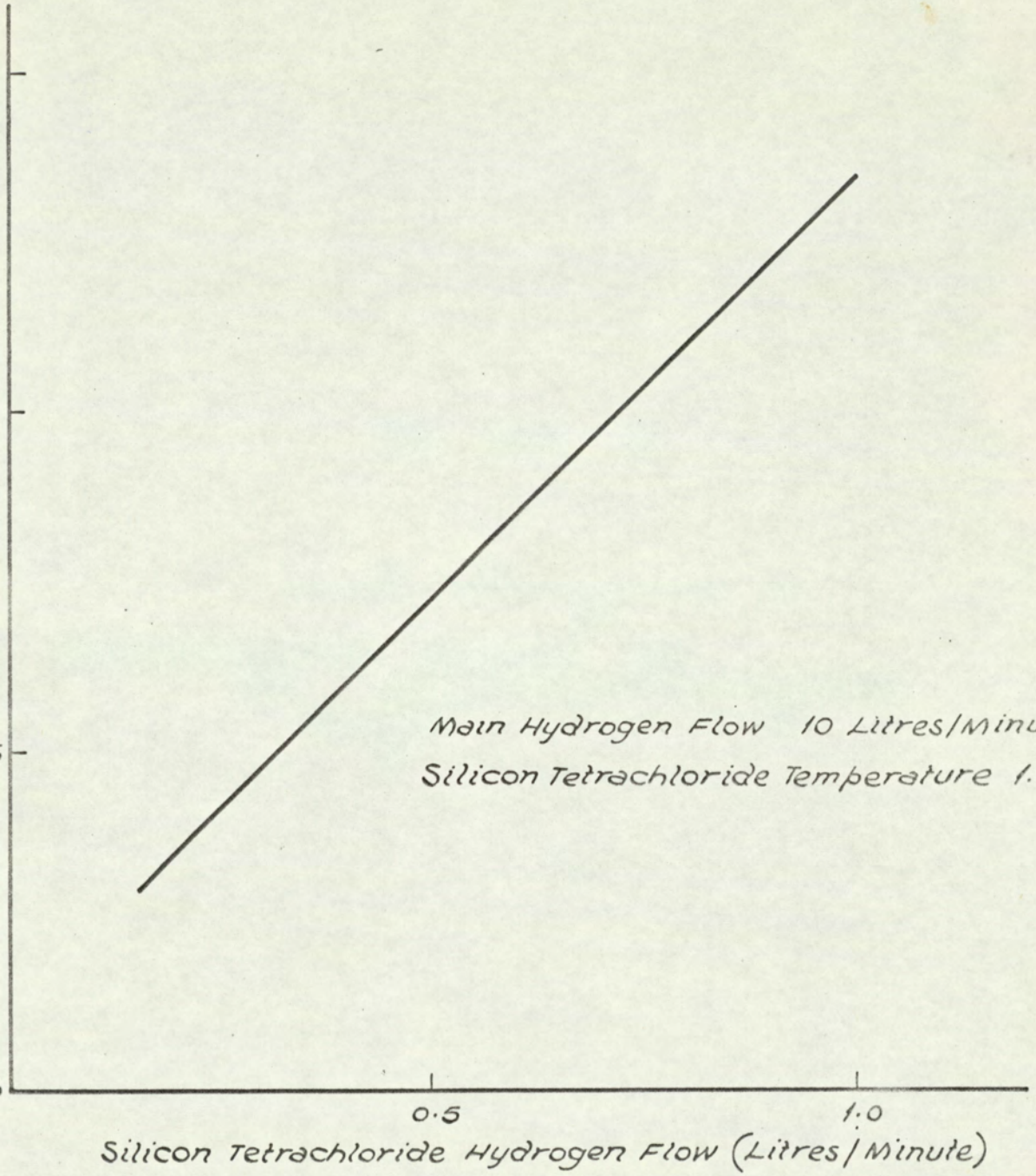


FIG. 5.11 INFLUENCE OF SILICON TETRACHLORIDE - HYDROGEN FLOW ON THE GROWTH RATE IN THE MULTIDEPOSITION APPARATUS.

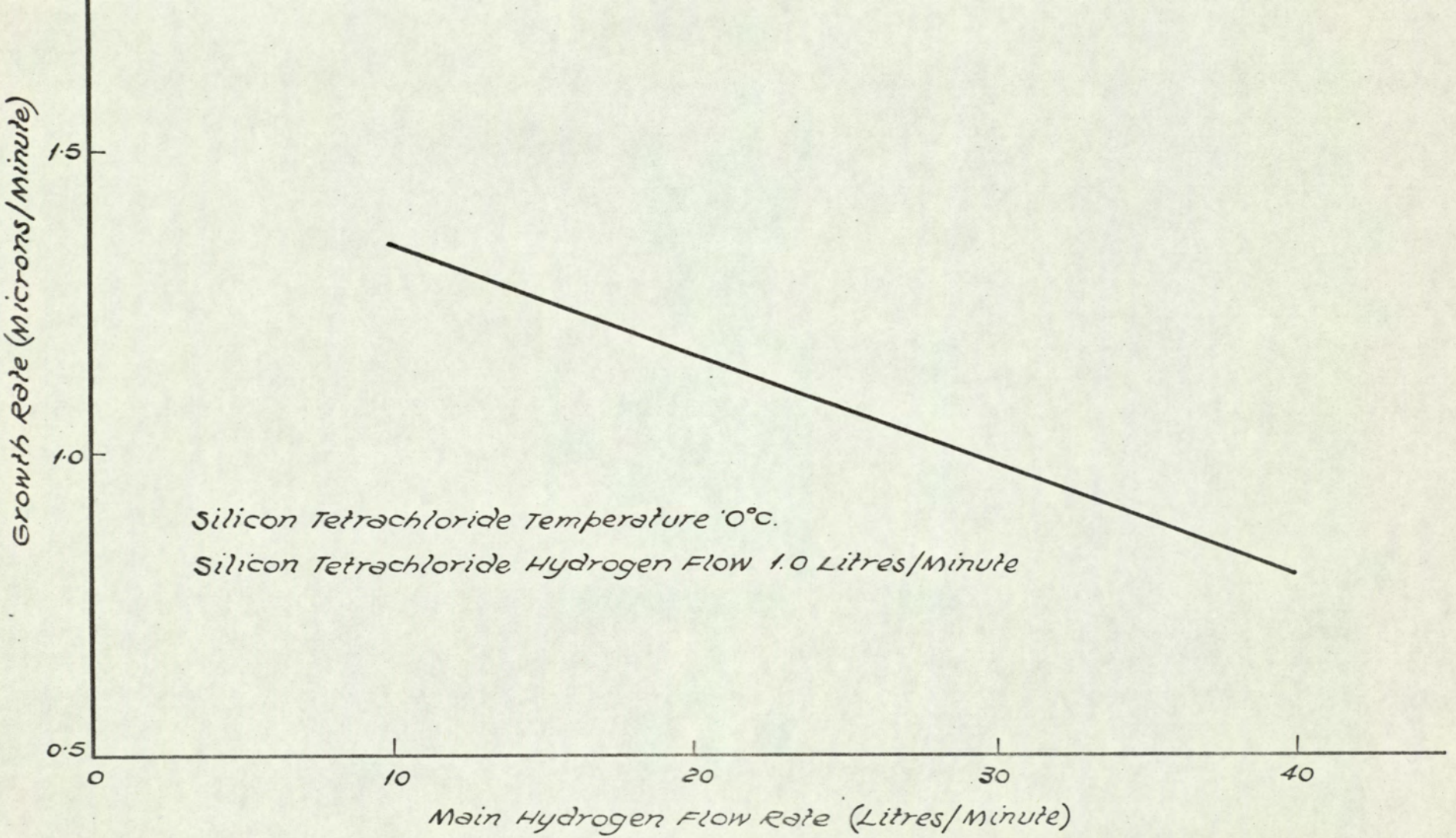
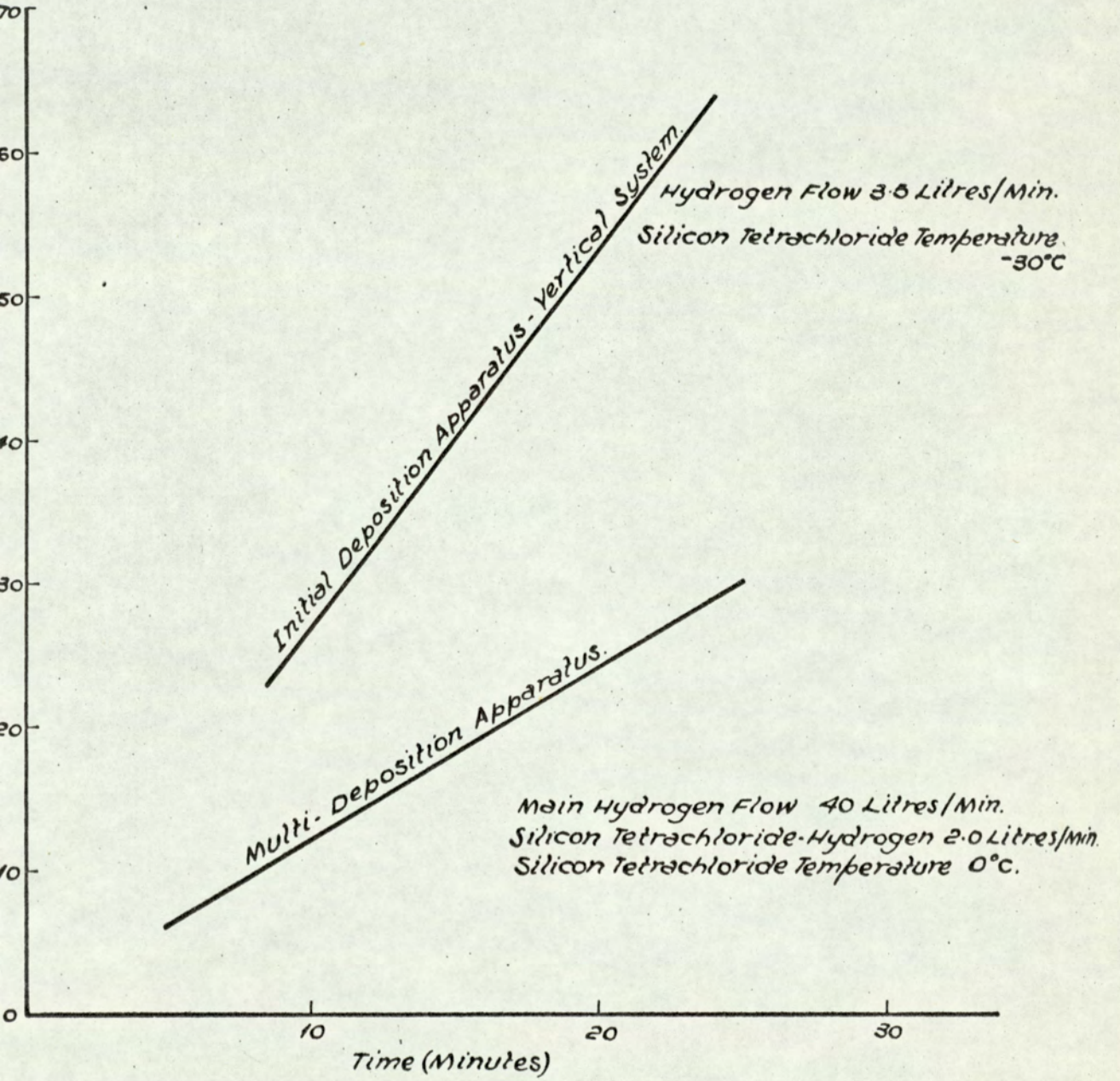


FIG. 5.12. INFLUENCE OF THE MAIN HYDROGEN FLOW RATE ON THE GROWTH RATE IN THE MULTI-DEPOSITION APPARATUS.



G. 6. 13. LAYER THICKNESS AS A FUNCTION OF DEPOSITION TIME.

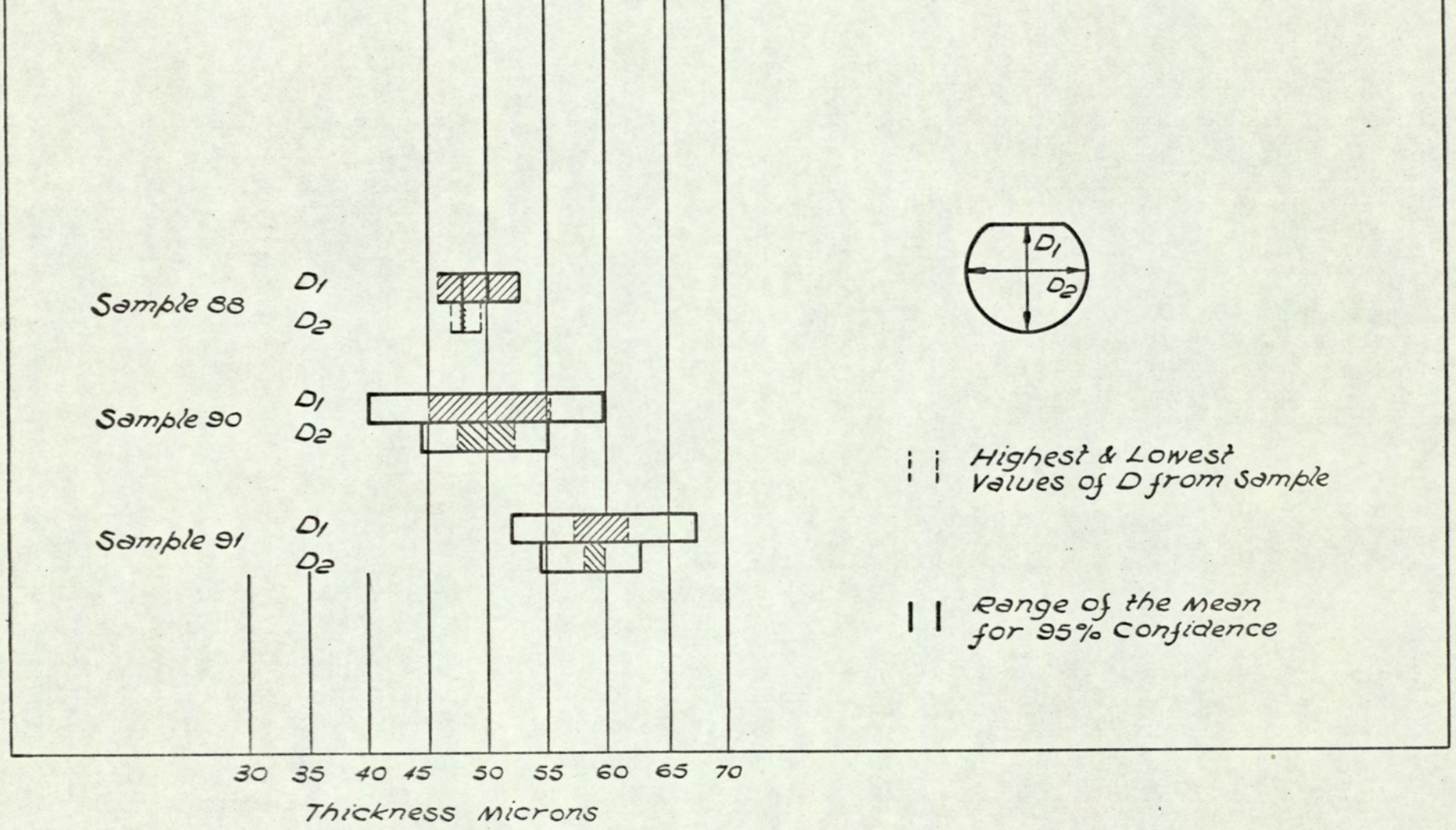


FIG. 5.14. LAYER THICKNESS VARIATION IN THE INITIAL DEPOSITION APPARATUS - VERTICAL SYSTEM.

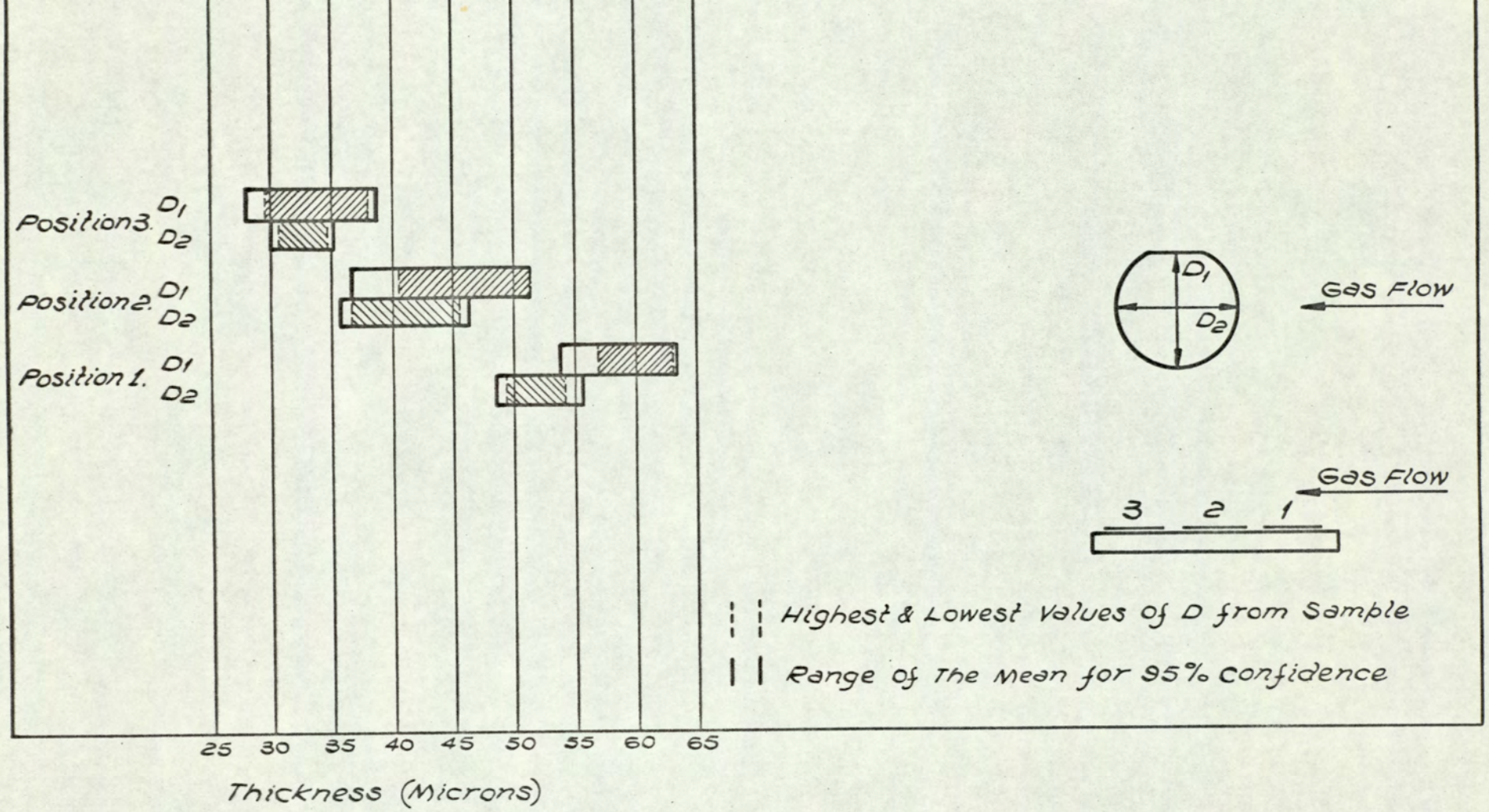


FIG. 5.15. LAYER THICKNESS VARIATION IN THE INITIAL DEPOSITION APPARATUS

HORIZONTAL SYSTEM – HORIZONTAL GAS FLOW.

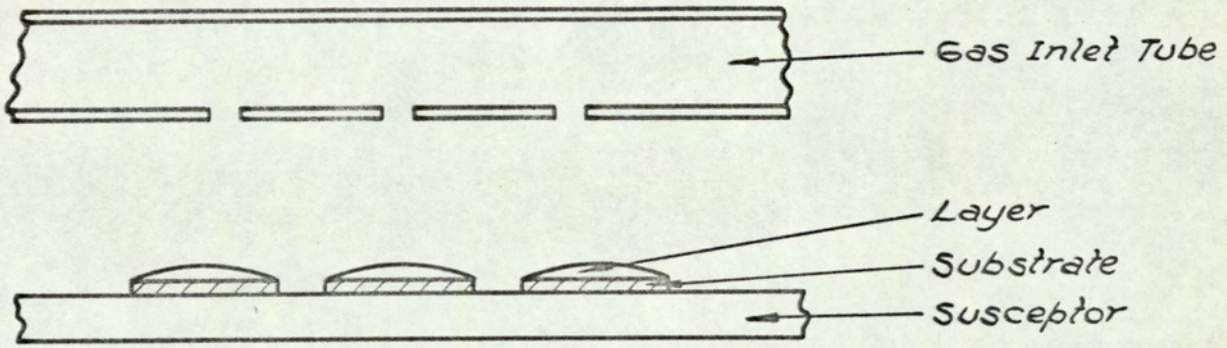


FIG. 5.16. SCHEMATIC VARIATION OF LAYER THICKNESS IN THE INITIAL DEPOSITION APPARATUS HORIZONTAL SYSTEM - VERTICAL GAS FLOW WITH LARGE DIAMETER HOLES IN THE GAS INLET TUBE.

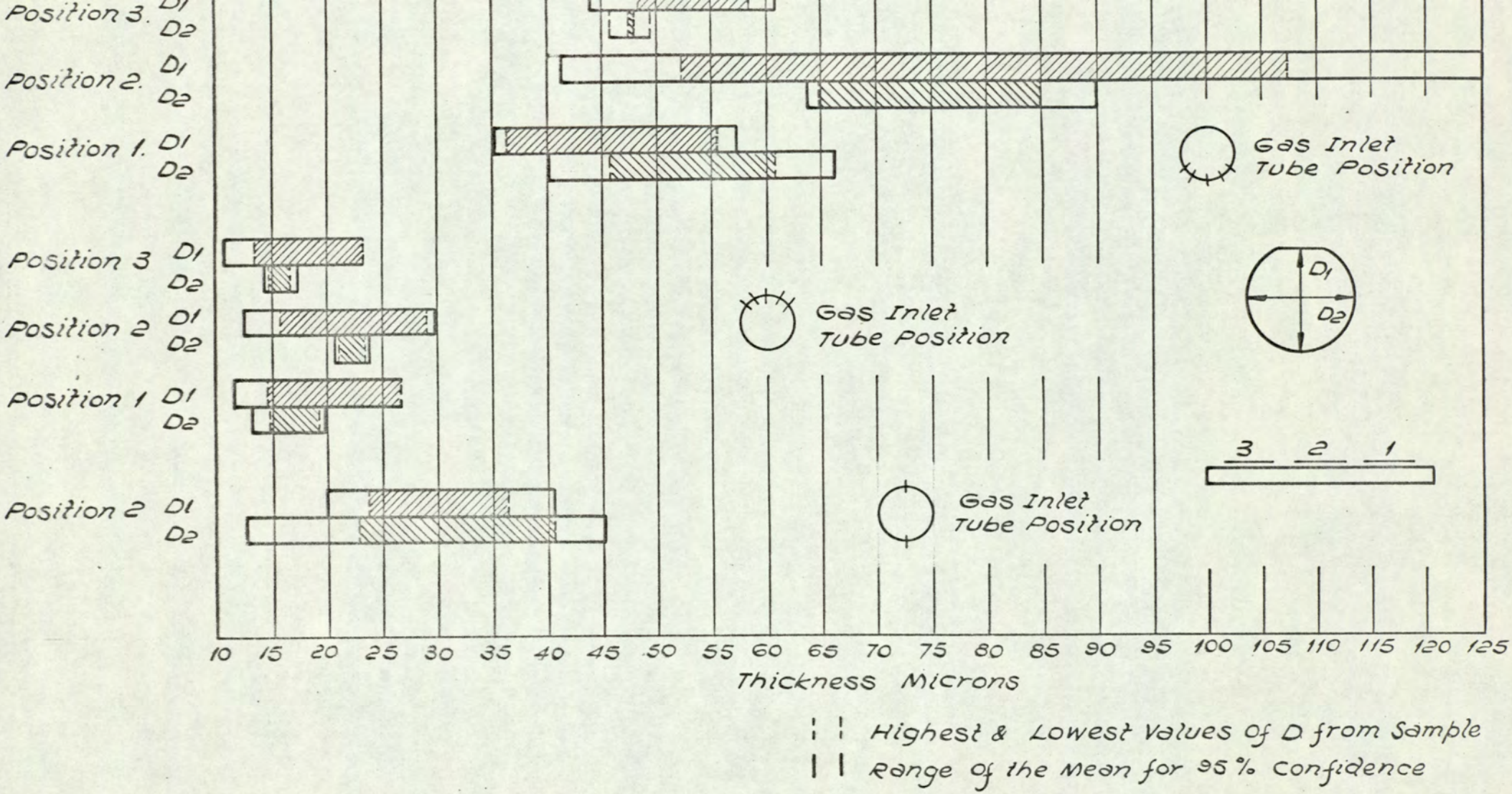


FIG. 5.17 LAYER THICKNESS VARIATION IN THE INITIAL DEPOSITION APPARATUS. HORIZONTAL SYSTEM - VERTICAL GAS FLOW WITH SMALL DIAMETER HOLES IN THE GAS INLET TUBE.

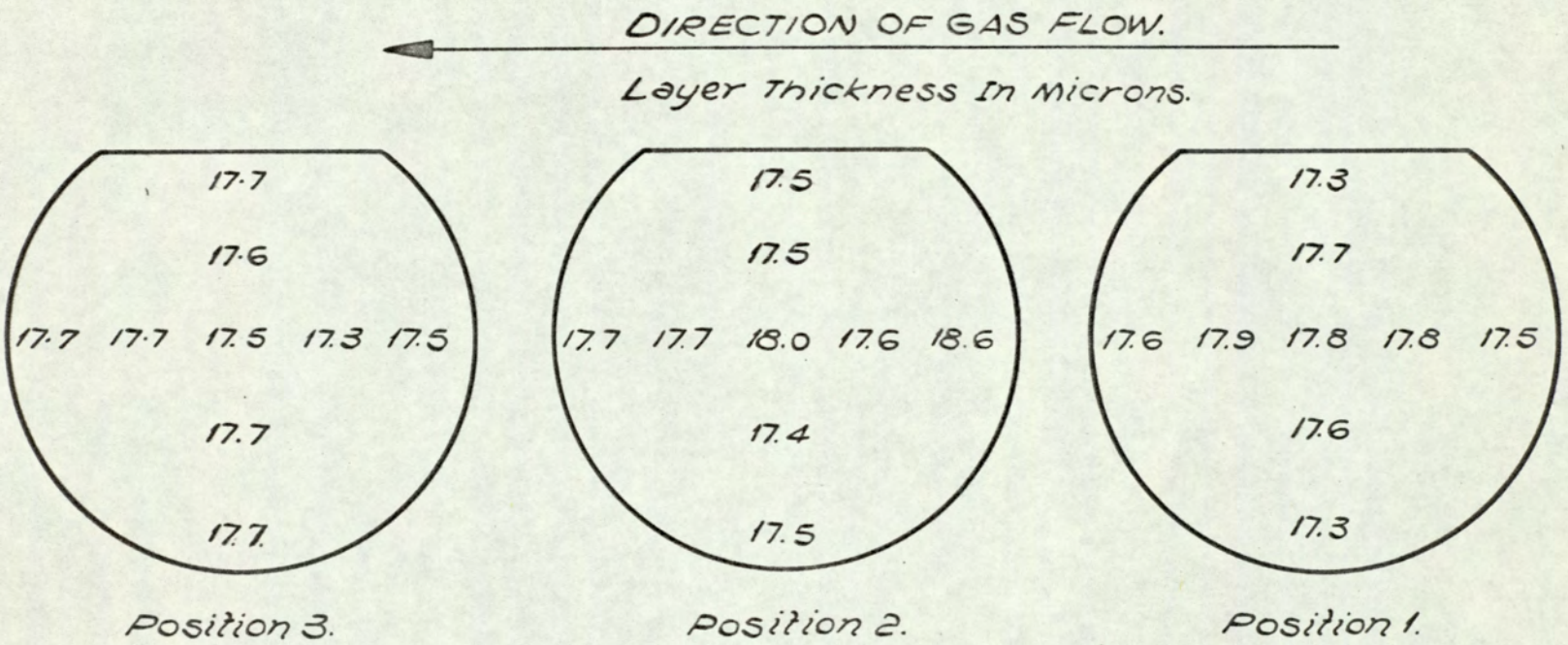


FIG. 5.18. LAYER THICKNESS VARIATION IN THE MULTIDEPOSITION APPARATUS MEASURED BY THE INFRARED METHOD.

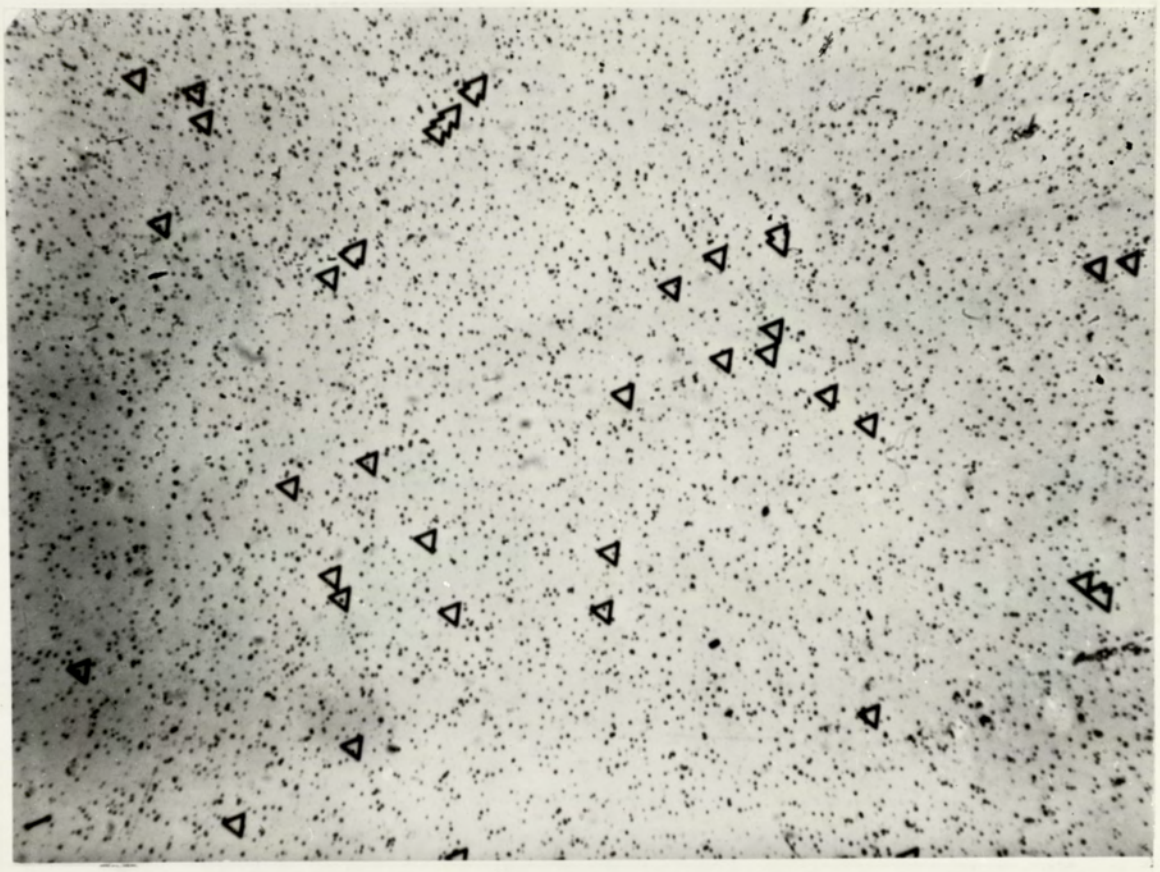


Fig. 5.19 Line etch figures on the epitaxial layer surface grown on (111) orientated pulled crystal substrate

x100

Fig. 5.20 Line etch figures on the epitaxial layer surface grown on (111) orientated float zone crystal substrate

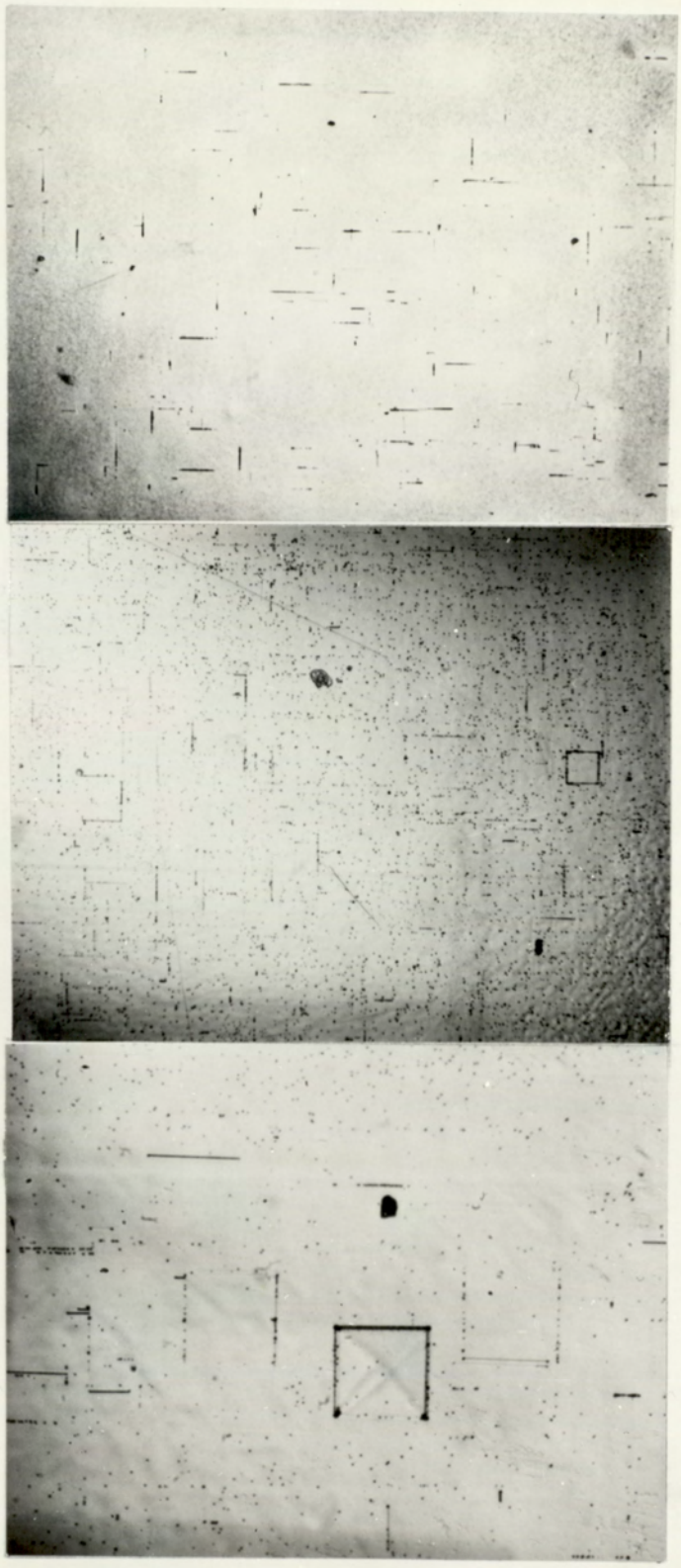


Fig. 5.21 Line etch figures on the epitaxial layer surface grown on (100) orientated substrate

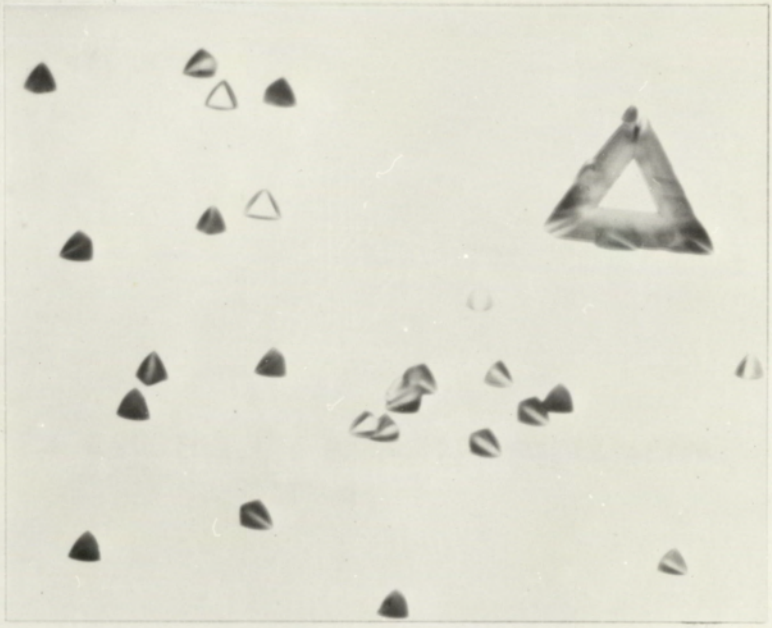


Fig. 5.22 Etch pits at the epitaxial layer surface

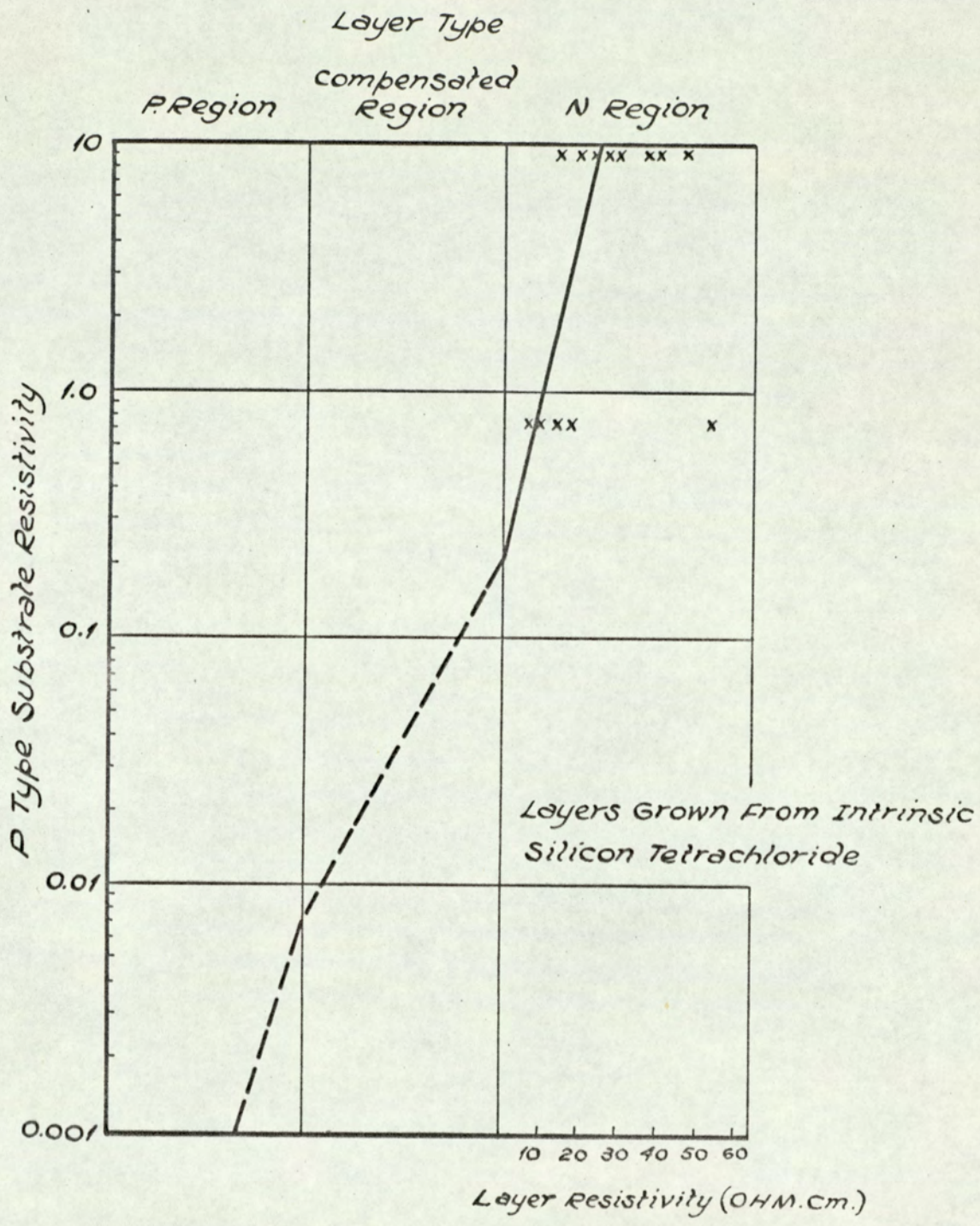


FIG. 5.23 EFFECT OF P TYPE SUBSTRATE RESISTIVITY ON THE LAYER TYPE & RESISTIVITY GROWN FROM INTRINSIC SILICON TETRACHLORIDE.

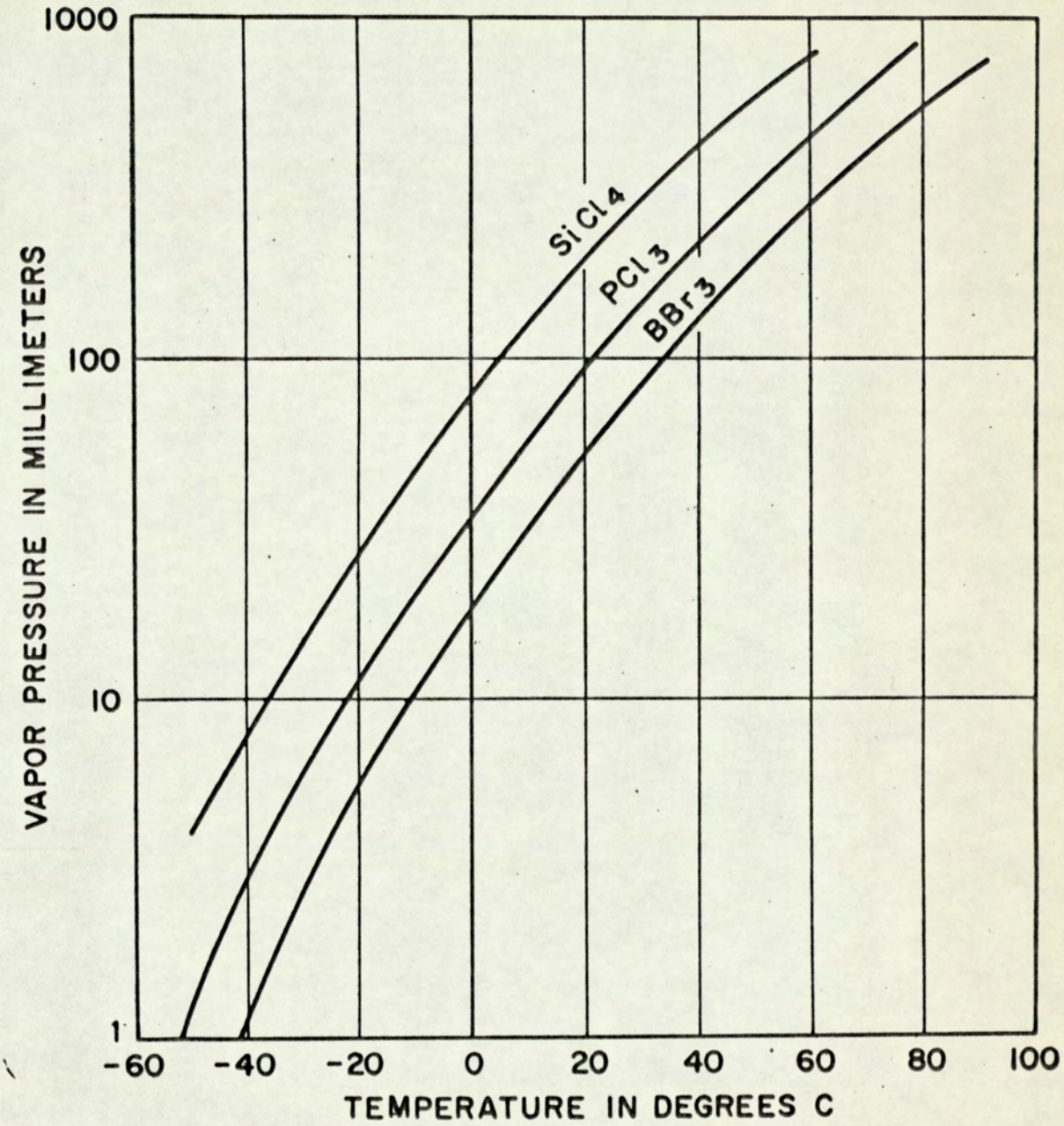
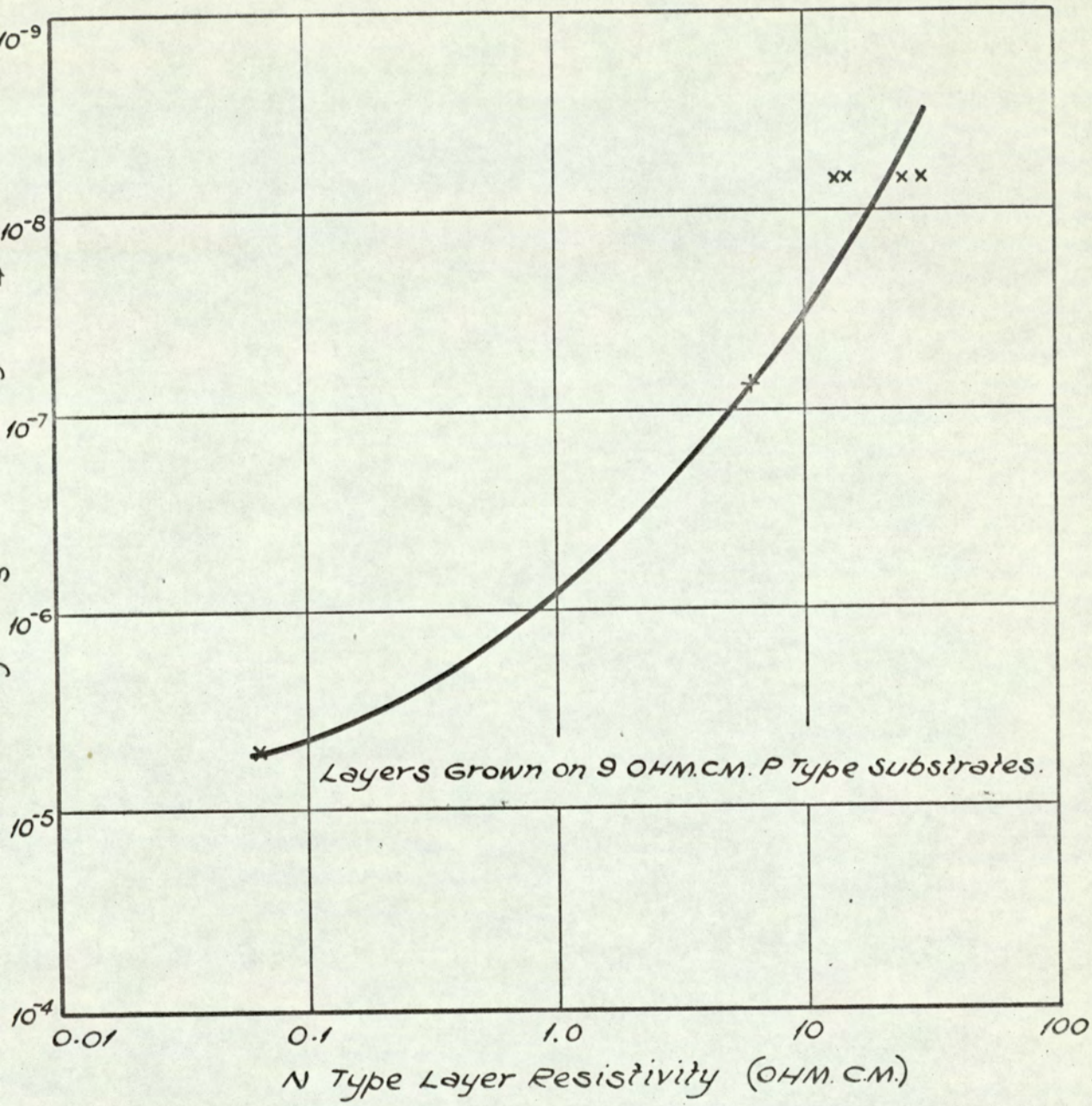


Fig. 5.24 Vapour pressure curves for $SiCl_4$; PCl_3 and BBr_3.



5.5.25. RELATIONSHIP OF THE CONCENTRATION OF PCl_3 IN $SiCl_4$ TO THE N TYPE LAYER RESISTIVITY.

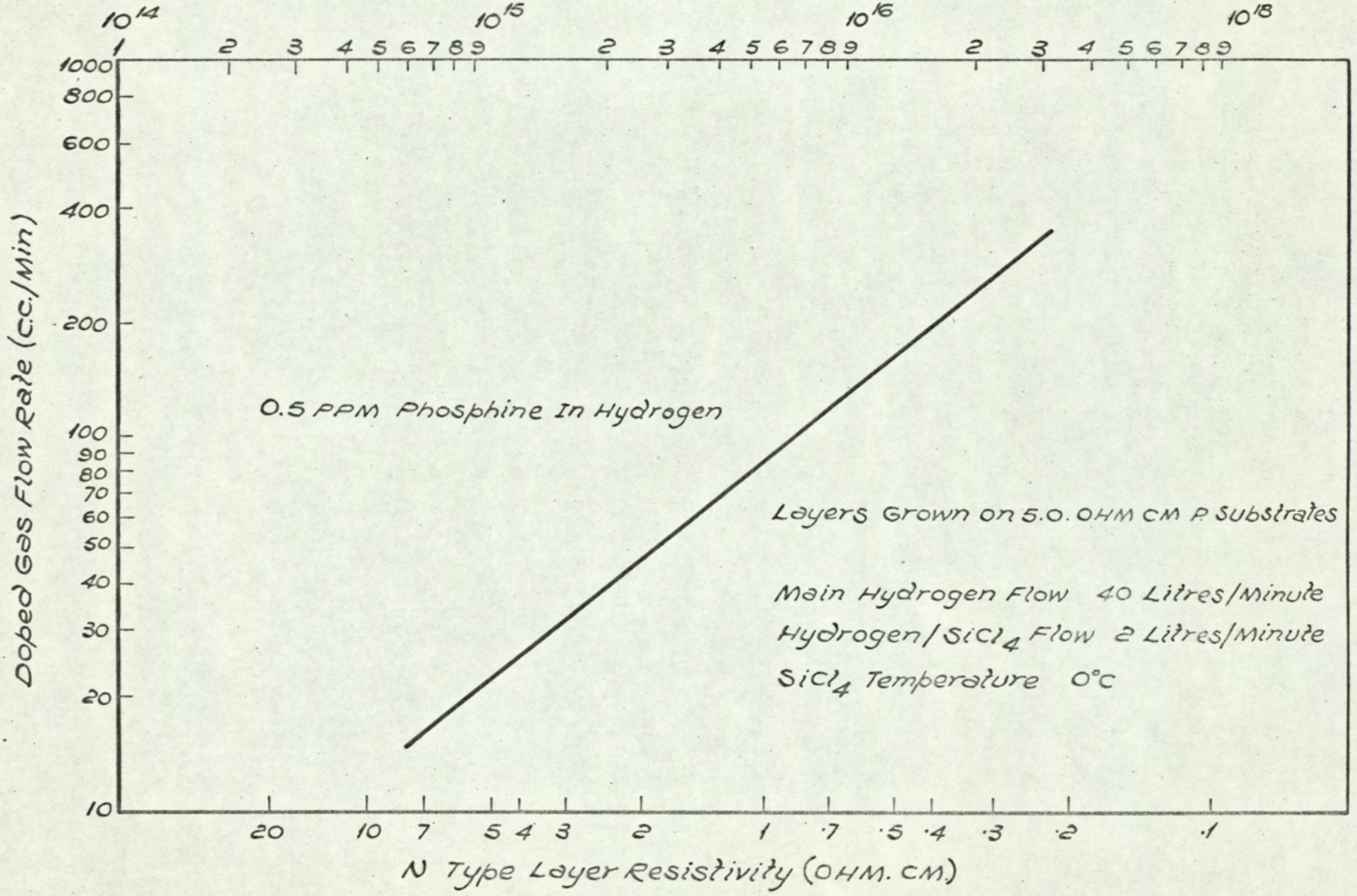


FIG. 5.26 RELATIONSHIP BETWEEN THE N TYPE LAYER RESISTIVITY AND PHOSPHINE/HYDROGEN DOPED GAS FLOW

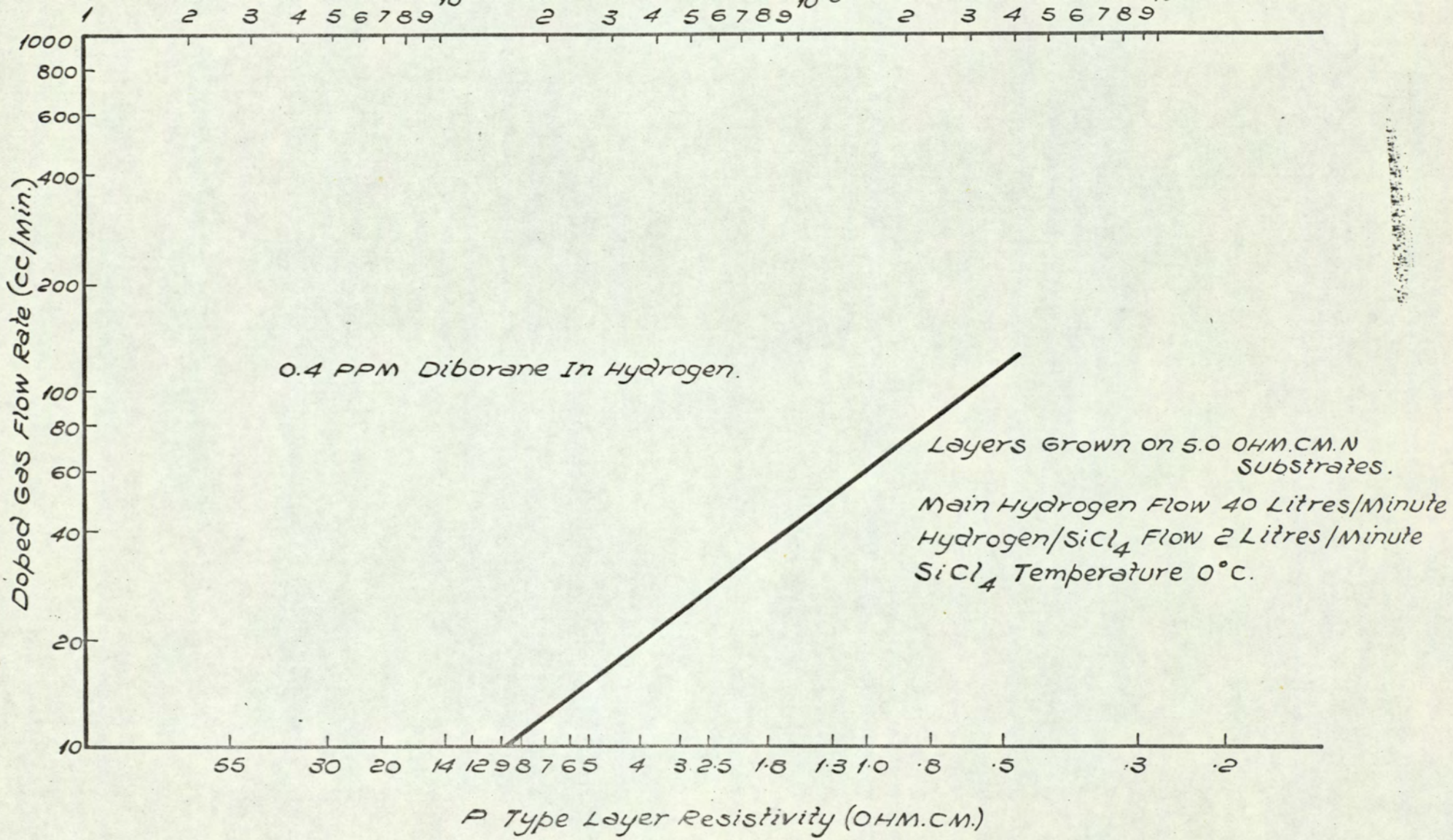


FIG. 5.27 RELATIONSHIP BETWEEN THE P TYPE LAYER RESISTIVITY AND DIBORANE/HYDROGEN DOPED GAS FLOW.

6. EXPERIMENTAL RESULTS

6.1 Comparison of the Methods of Measuring Layer Thickness

The results are shown in Table 6.1 of the four methods (1) Increase in weight (2) Angle lapping (3) Infra red and (4) Stacking fault, for measuring layer thicknesses of N type layers grown from intrinsic silicon tetrachloride on 0.01N ohm cm antimony doped substrates. Comparisons of these results indicate that the angle lapping, infra-red and stacking fault methods are in good agreement, but the increase in weight method is not consistent with the other methods.

6.2 Comparison of the Methods for Measuring Layer Resistivity

To compare the methods of measuring layer resistivity the structure of 10 ohm cm N layer on a 1.0 ohm cm P boron doped substrate was produced in the vertical deposition apparatus. The resistivity of the N layer was measured by the four point probe method and layer thickness by angle lapping and staining. An abrupt PN junction was formed in the N type epitaxial layer by diffusion and diodes fabricated as described in Section 4.3. The breakdown voltage and capacitance of the junction formed between the epitaxial N and diffused P regions were measured and related to the layer resistivity. The results are shown in Table 6.2 and the capacitance method indicates a variation in the layer resistivity while the resistivity obtained from the breakdown voltage does not correlate with that obtained by the other two methods.

6.3 Surface Protruding Imperfections

Small protruding imperfections with a general pyramidal form have been observed on some epitaxial layers grown in the initial deposition apparatus. The number of defects on the surface varied but were generally between 7 and 15 per sq cm and for layers grown on (111) orientated substrates the defects had a triangular base Figure 6.1 and on (100) orientated substrates a square base, Figure 6.2. These defects were found to exist through the layer to the substrate and in some cases were

associated with line etch figures.

6.4 Effect of Oxygen Impurities in the Gas System

To confirm that oxygen contamination in the gas system will produce lattice defects, a few ppm of nitric oxide were leaked into the gas system during the time interval between the hydrogen chloride polishing and silicon deposition. Etching of the layer surface in Sirtl etch revealed that it was completely covered with line etch figures, Figure 6.3, while under normal operating conditions in the system very few line etch figures are observed in the layer. This result confirms that oxygen in the gas system will result in lattice imperfections in the epitaxial layer.

6.5 Confirmation of the Epitaxial Growth of the Layer with the Substrate

To confirm that the layer was epitaxial with the substrate Back Reflection Laue X Ray Photographs were obtained from the layer and substrate and are reproduced in Figure 6.4. The Laue pattern consists of a set of diffracted spots on the X-Ray film and the position of these spots depend on the orientation of the crystal. Comparison of the patterns obtained from the substrate and the epitaxial layer indicate that the lattice orientations are identical.

6.6 The influence of the Epitaxial System and Intrinsic Silicon tetrachloride on layer type and resistivity

To investigate the effect of the epitaxial system and intrinsic silicon tetrachloride on the layer type and resistivity epitaxial layers were grown on (A) 1,000 ohm cm N and (B) 1,000 ohm cm P substrates. Material of this resistivity has a low impurity concentration and should have minimum effect on layer resistivity. The type of layers grown on these substrates was not defined by the thermo-electric probe method and measurement of layer resistivity was not possible with the four point probe method. The results indicate that the epitaxial system and intrinsic silicon tetrachloride do not have any effect on the layer type and resistivity and hence do not contribute significant electrically

active impurities to the layer.

6.7 Chemical Analysis of the Epitaxial Layers with Mass Spectrometer

Table 6.3 shows the mass spectrometer analysis of 0.01 ohm cm N type antimony doped substrate material used for the growth of epitaxial layers required for device processing, together with analysis of layers grown on this type of substrate. Sample C.532 produced in the multi-deposition apparatus with the PTFE manifold system contained quantities of impurities while samples produced after changing the manifold system to quartz, indicate that the concentration of impurities has been reduced. The measurement of the lifetime, Section 6.9.4, from devices with the same base width and resistivities produced from similar materials indicate that the lower lifetime is associated with the higher concentration of impurities present in the layer.

6.8 The Interaction of Doping Impurities from the Gas Stream and Substrate on the Layer Type and Resistivity

To investigate the interaction of doping impurities from the gas stream and the substrate on the layer resistivity the following epitaxial depositions were made. (A) Two deposition runs, with the same concentration of diborane and silicon tetrachloride in the gas stream, to grow P type layers on approximately (1) 1.0 ohm cm N and (2) 0.01 ohm cm N antimony doped substrates. (B) Two deposition runs, with the same concentration of phosphine and silicon tetrachloride in the gas stream to grow N type layers on approximately (1) 1.0 ohm cm P and (2) 0.01 ohm cm P boron doped substrates.

The silicon carbide coated susceptor was loaded with three substrates of the required specification together with an 0.01 ohm cm N antimony doped substrate positioned nearest the gas outlet, for thickness monitoring by the infra-red method. The resistivity of the layers were measured with the 4 probe method and the layer thickness determined by angle lapping and staining.

The results obtained for the effect of the N type substrate doping element on the P layer resistivity, Figure 6.5, show (a) the variation of layer resistivity on a single substrate and on the three substrates positioned on the susceptor, and (b) a comparison of the infra red and angle lapping film thickness measurements of these layers. Similar results for the effect of the P type substrate doping element on the N layer resistivity are shown in Figure 6.6.

For N type substrates the results indicate that P layers of higher resistivity are obtained on the lower resistivity substrates and for a deposition run there is a tendency for lower resistivity layers on the substrates positioned near the gas inlet.

For P type substrates the results indicate that N layers were obtained on the higher resistivity substrates and P type layers on the low resistivity substrates with the exception of a small N area in the centre of the substrate positioned nearest the gas inlet. For the higher resistivity substrates the junction depths measured by angle lapping and the infra red method are in close agreement and the resistivity variation for the different positioned substrates on the susceptor is no greater than the variation obtained on an individual substrate.

These results again confirm the significant influence that the substrate has on the layer resistivity and also show the variation in layer resistivity on a single substrate and on a series of substrates position on the susceptor. The thickness measurements also indicate that the metallurgically grown junction does not necessarily coincide with the PN junction.

6.9 Evaluation of Material from the Characteristics of Processed Devices

The object of growing silicon epitaxial material is to enable it to be used for the production of semiconductor devices. The characteristics of a device depend on its structure, geometry, method of processing and the material from which it is manufactured. Thus the evaluation of the characteristics of the device can provide information about the

device material.

The processing of a single substrate will yield a number of devices, depending on the device geometry and in practice can vary from thirty for the XTI transistor to over three hundred for the XP6 transistor. Because of the considerable effort required to individually complete all the devices and measure their characteristics it is accepted practice to take from the substrate a random sample of devices for final completion, i.e. dice mounted onto a heat sink and permanent electrical contacts made. The electrical characteristics of the devices are measured and their results assumed to be representative of all the devices from the substrate.

6.9.1 XTI High Voltage Medium Power Transistor

This device was initially chosen for material evaluation because at the time it was in production with the Physics Department Device Pilot lin and would allow direct comparison of the epitaxial material with the float zoned material normally processed. The device has an NPN structure and is manufactured according to the process reported by Lowe (39). N type epitaxial layers of various thicknesses were grown from intrinsic silicon tetrachloride on to various resistivity N type substrates doped with arsenic and antimony. A P type impurity is diffused into the epitaxial layer to form the base region and is followed by the diffusion of an N type impurity to form an N emitter region within the P base and the final structure shown in Figure 6.7. After the formation of this structure the substrates are diced, contacts made and the primary electrical characteristics of the device measured in accordance with the method reported by Taylor (40). 10 epitaxial substrates were processed and 77 devices completed. The epitaxial process variables are shown in Table 6.4 and the device characteristics in Tables 6.5A, B and C and 6.6A and B.

The comparison of the characteristics of these devices with those reported by Taylor (40) for devices of the same structure and size processed from 25 ohm cm N float zoned silicon under similar conditions

indicate that the epitaxial devices have similar electrical characteristics with two exceptions.

1. The epitaxial devices have a lower collector to base breakdown voltage BV_{CBO} with soft characteristics. When all other parameters are equal, the collector to base breakdown voltage is a function of the resistivity of the silicon at the base collector junction and increase in silicon resistivity will result in higher breakdown voltages, thus indicating that the epitaxial resistivity is lower than 25 ohm cm.
2. The epitaxial devices have improved collector to emitter saturation voltage V_{CE} resulting from the composite structure of the collector region in which the epitaxial part gives a high breakdown voltage and the low resistivity substrate results in almost zero collector resistance.

From a comparison of the characteristics of the devices fabricated from the epitaxial material grown on various resistivity, arsenic and antimony doped substrates, the following tentative conclusions can be made:-

1. Increase in the epitaxial layer thickness results in a decrease in the collector to emitter saturation voltage. Substrates 112V - 115V. The reason for this is that an increase in epitaxial layer thickness will result in an increase in the series ohmic collector resistance of the composite collector region.
2. Increase in substrate resistivity results in an increase in the collector to emitter saturation voltage. Substrates 114V, 131V and 132V. Again this can be explained because the composite collector region will have a higher series ohmic resistance due to the increase in resistivity of the substrate.

3. Increase in substrate resistivity results in a higher collector to base breakdown voltage, indicating that the epitaxial layers grown on higher resistivity substrates have higher resistivity, Substrates 114V, 131V, 132V. This is in agreement with the results obtained for the effect of N type antimony doped substrate impurity concentration on layer resistivity. Table 5.5, which shows that higher resistivity layers are obtained on higher resistivity substrates.

4. The collector to base breakdown voltage is lower for the epitaxial layers grown on the arsenic doped substrate compared with that for the antimony doped substrate, substrates 133V, 134V, indicating higher resistivity layer on the antimony doped substrate. This is in agreement with the results obtained for the effect of N type substrate doping element on layer resistivity. Table 5.4 which indicate that layers grown on antimony doped substrates, have higher resistivity than those grown on arsenic doped substrates of similar resistivity.

6.9.2 Epitaxial Diodes

Epitaxial structures were produced using the liquid doping process with (A) a composite junction of an epitaxial P layer on N^+ substrate and (B) a pure junction of an epitaxial P layer, on an epitaxial N layer on an N^+ substrate. These structures were fabricated into devices using a method similar to that described for producing PN junctions for capacitanc measurements, Section 4.3, and the characteristics of the junction measured. The structure of the devices are shown in Table 6.7 and their junction characteristics in Table 6.8 which indicate that the devices have leakage currents which rendered the measurement of the true breakdown voltage of the junction impossible.

6.9.3 XP6 Epitaxial Planar Transistor

The design of this device takes advantage of the planar process (41) in conjunction with the use of silicon epitaxial material. The process initially involves the thermal growth of a silicon dioxide layer on the surface of an N epitaxial layer grown on an N^+ substrate. The silicon dioxide is used as a mask against diffusant impurities and through which an aperture of selected size and shape is etched using photolithographic techniques. A P impurity is diffused into the aperture to form the base region and is followed by further etching of an aperture for diffusion of an N type impurity to form the emitter region. After the completion of the structure, Figure 6.8, the substrates are diced, assembled and contacts made for measurement of the characteristics which are reported in Table 6.9. Of significance in these measurements is the hard collector to base breakdown voltage BV_{CBO} and the collector to base leakage current I_{CB} which is of a lower magnitude to that for the previously reported devices.

6.9.4 XH6 Epitaxial Homogeneous Base Transistor

The design of this device requires a composite or pure epitaxial junction and has the advantage of silicon dioxide junction protection. The device structure is shown in Figure 6.9 and produced as follows:-

1. The epitaxial growth of (A) a P layer on N^+ substrate
   or (B) a P layer on N layer or N^+ substrate.
2. The formation of a P^+ layer by either
   (A) further epitaxial growth on the P layer
   or (B) diffusion into the P layer
3. The formation of a silicon dioxide layer on the P^+ layer by either (A) thermal oxidation of the layer
   or (B) deposition of silicon dioxide by "the epitaxial process". *

* The deposition of silicon dioxide produced by the introduction of gaseous carbon dioxide or nitric oxide into the silicon tetrachloride/hydrogen reaction.

4. The formation of the N emitter by diffusion through the P^+ layer into the P region.
5. The etching of the mesa to the N region.
6. Thermal oxidation to protect the exposed junctions.
7. Substrate diced and electrical contacts made for measuring the device characteristics.

Tables 6.10, 6.11 and 6.12 list the measured characteristics of these devices and they indicate that the epitaxially grown junction between the base and collector regions have hard characteristics and considerably lower leakage currents compared with those reported for the epitaxial diodes. Of further significance in these results is the difference in the gain h_{FE} characteristics of devices which were fabricated with exactly the same structure, geometric and processing conditions, Tables 6.11 and 6.12.

The measurement of the minority carrier lifetime of the epitaxial silicon forming the base region by the method reported by Wilson (42) indicates that the devices with higher gains are associated with material of higher lifetime, which in turn has been found to be connected with the lower impurity level of the silicon material.

6.9.5 Comments on the Epitaxial Material from Analysis of Device Characteristics

The epitaxial material used to produce the XT1 high voltage medium power transistor and epitaxial diode contain more than 750 line etch figures per sq. cm. while the material used for the XP6 epitaxial planar transistor and the XH6 epitaxial homogeneous base transistor contains less than 16 line etch figures per sq. cm. From the analysis of the measurements of the device characteristics it is concluded that:-

1. The quality of the epitaxial material is suitable for transistor action.
2. Devices produced from material containing large quantities of line etch figures have soft junction characteristics.

3. Epitaxially grown PN junctions in low quantity line etch figure material are compatible with diffused PN junctions.
4. The material contains electrically neutral impurity atoms.

6.10 Examination for Electrical Leakage at Line Etch Figures

The surface of a 25 micron thick N type epitaxial layer on an 8.0 ohm cm P substrate was etched to reveal the line etch figures and then made the cathode in an electrolytic copper plating cell. Section 4.5. After plating for a short interval the surface was examined for preferential deposition of copper at the line etch figure, but none was observed. This indicates that electrical leakage does not occur at the lattice defects forming the line etch figures.

6.11 Results of an Investigation for the Routine Production of Epitaxial Substrates for the XP6 Epitaxial Planar Transistor

Preliminary investigations to produce the XP6 epitaxial planar transistor indicated that a 15 micron N layer grown from intrinsic silicon tetrachloride on 0.01 ohm cm N type antimony doped substrate was required. This material was produced in the multideposition apparatus with the PTFE manifold system and silicon coated graphite susceptor. The temperature of the substrate was measured with an optical pyrometer before commencing growth while the deposition time was determined from previous runs.

The layer thickness was measured with the infra red method at the centre of each substrate and generally the resistivity of the layer monitored from the characteristics of the devices fabricated in the epitaxial material. Occasionally a 1.0 ohm cm P substrate was included in the resistivity of the N layer measured with the four probe technique and the layer thickness inferred from the layer thickness of the preceding substrate on the susceptor.

The general process details to produce this material are shown in Table 6.13 and the individual batch process details of substrate temperature and time with layer thickness results and layer resistivities for approximately 90 runs involving the processing of 175 substrates are shown in Table 6.14. The statistical analysis of these results are shown in Table 6.15.

TABLE 6.1

Comparison of results of methods for measuring epitaxial layer thickness

Substrate No.	Increase in weight Method (microns)	Angle Lapping Method (microns)	Infrared Method (microns)	Stacking Fault Method (microns)
192	12.8	8.9	9.8	9.0
193	9.04	6.7	7.5	6.2
219	39.4	39.1	41.1	40.1
227	56.4	38.6	41.1	40.8
228	91.2	89.2	90.7	94.5
230	42.4	24.4	25.4	24.2
231	58.4	58.9	63.0	61.5
232	125	130	132	128
233	35.6	36.1	39.6	37.3

TABLE 6.2

Comparison of methods of measuring epitaxial layer resistivity

Substrate No.	Four Point Probe Method	Capacitance Method		Breakdown Voltage Method
	Resistivity (ohm cm)			
1	8.3	15 13 12 3.4 2	Mean 9.1	0.44
2	5.6	3.6 3.6 8 8.5	Mean 5.9	2.3

TABLE 6.3

Mass spectrometer analysis of epitaxial layers and substrates

Parts per million weight for weight = $\frac{\text{Atomic parts per million x Atomic weight of element}}{\text{Atomic weight of silicon (28.09)}}$

Element	Isotopic Mass Number	Substrate		Epitaxial Layer				
		0.01 ohm cm N^+ Antimony Doped	Limit of Detection of Element in Substrate	Layer grown with P.T.F.E. manifold in the gas system: 15 micron 7 ohm cm P layer on 5 micron 2 ohm cm N layer on N^+ substrate		Layer grown with quartz manifold in the gas system: 30 micron 0.6 ohm cm P layer on N^+ substrate	30 micron 0.6 ohm cm N layer on N^+ substrate	Limit of Detection of element in layer
				Sample R.165	Sample C.532	Sample R.480	Sample R.482	
		Atomic Parts Per Million				nd = not detected		
Sb	121	52.5	0.05					
Sn	120				2			
Fe	$18^2/3$	nd	6.0		74	nd	nd	60
Mn	55				7			
Cr	52			24	20			
Cu	65	0.04	0.04	18	48	nd	nd	0.4
Ca	20	0.6	0.6	7	7			
K	$19\frac{1}{2}$				0.6			
Cl	35	0.4	0.4	24	1	12	4	4.0
S	$10^2/3$			60				
P	31	0.3	0.03	19.8	20			
Al	$13\frac{1}{2}$	0.3	0.3	12.2	6.8			
Na	$11\frac{1}{2}$			0.6				
F	19	0.09	0.03	6.0	14	0.9	2.7	0.3
B	11			0.8	0.8	1.3	nd	0.4

TABLE 6.4

XT1 High Voltage Medium Power Transistor - Epitaxial Layer and Substrate Details

Substrate Number	Substrate Resistivity ohm cm	Substrate Doping Element	Epitaxial Film Thickness (microns)	Pilot Line Batch Process Number	Number of Transistors Constructed	Transistor Reference Number	For T036 Mounting Vce(Sat) Ic = 200 ma Ib = 40 ma	For T036 Mounting Mean BV_{cbo}
48H	0.010-0.013	As	79	H.163	7	EA 1 - 7	-	-
49H	0.010-0.013	As	68.5	H.163	5	EA 8 - 12	-	-
112V	0.0075-0.0105	Sb	43.5	H.212	9	EA 13 - 18 E_1 1 - 3	0.06 - 0.08	370 S
113V	0.0075-0.0105	Sb	63.0	H.212	16	EA 19 - 31 E_2 1 - 3	0.08 - 0.1	320 S
114V	0.0075-0.0105	Sb	89.5	H.212	6	EA 32 - 34 E_3 1 - 3	0.10 - 0.12	240 S
115V	0.0075-0.0105	Sb	117	H.212	14	EA 35 - 45 E_4 1 - 3	0.12 - 0.17	490 S
130V	0.0075-0.0105	Sb	38	H.242	BV_{cbo}	0.5 to 5.0 volts Device structure has gone through the epitaxial layer into the substrate.		
131V	0.26 - 0.40	Sb	81.5	H.242	2	E1 4 - 5	0.14	>600
132V	0.26 - 0.40	Sb	89	H.242	2	E2 4 - 5	0.14	>600
133V	0.0075-0.0105	Sb	51	H.242	2	E5 1 - 2	0.08	375
134V	0.0095-0.019	As	51	H.242	2	E3 4 - 5	0.08	285

Although a number of dice were prepared from samples 131V - 134V only two dice from each batch were assembled.

	Ref No	BV_{cbo}	$V_{CE(sus)}$ 5ma.	V_{SB}	BV_{ebo}	I_{cbo} μA at 25°C	h_{FE} I_C=200ma V_C= 6V	h_{FE} I_C=50ma V_C= 6V	$V_{ce(sat)}$ I_C = 200 ma. I_B = 40 ma.	$V_{be(sat)}$	V_{ce} I_C = I_B =	V_{be}				
Substrate 48H	EA 1	160 (S)	95		8	100 / 160V	32	19	0.2	1.4						
	" 2	160 (S)	75		7.7	1ma / 160V	42	25	0.15	1.4						
	" 3	190 (S)	90		7	0.5ma / 190V	34	19	0.18	1.4						
	" 4	150 (80)	30 (S)		7.3	-	43	26	0.14	1.2						
	" 5	190 (S)	90		8.6	0.5ma / 190V	34	19	0.17	1.4						
	" 6	40 (S)	40 (S)		8.1	-	38	22	0.16	1.2						
	" 7	90 (VS)	70-80 (S)		8.6	100 / 80V	38	23	0.16	1.2						
Substrate 49H	" 8	10 (S)	-		8.3	5ma / 10V	36	21	0.18	1.1						
	" 9	200 (S)	105		8.6	250 / 200V	33	19	0.18	1.2						
	" 10	165 (S)	90		9.0	0.5ma / 165V	45	28	0.15	1.1						
	" 11	140 (S)	110		7.5	0.5ma / 140V	29	16.6	0.19	1.1						
	" 12	>200 (S)	110		9.9	50 / 200V	31	19	0.18	1.2						
		S = Soft.														

TABLE 6.5A Characteristics of XT1 High Voltage Medium Power Transistors mounted on TO5 Headers

	Ref No	BV_{cbo}	$V_{ce(sus)}$ 5ma.	V_{SB}	BV_{ebo}	I_{cb} μA.	h_{FE} I_C=50mA V_C=6V.	h_{FE} I_C=200mA V_C=6V	$V_{ce(sat)}$ I_C = 200 mA. I_B = 40 mA.	$V_{be(sat)}$	V_{ce} I_C = I_B =	V_{be}	$V_{be(sat)}$ I_C=50mA. V_C=6V.	$V_{be(sat)}$ I_C=200mA. V_C=6V.		
Substrate 112V	EA 13	100(s)	84(s)		6.2	-	25	37	0.12	0.78			0.68	0.76		
	" 14	350(s)	180		6.2	200/200V	25	40	0.12	0.78			0.68	0.76		
	" 15	350(s)	100(s)		6.2	750/200V	26.5	40	0.14	0.80			0.68	0.76		
	" 16	400(s)	190		6.2	600/200V	25	36.5	0.14	0.78			0.68	0.77		
	" 17	70(s)	60(s)		6.2	-	21	34.5	0.13	0.78			0.68	0.76		
	" 18	100(s)	30(s)		6.3	-	25	38.5	0.13	0.78			0.69	0.76		
Substrate 113V	" 19	10(s)	-		6.3	-	25	38.5	0.14	0.78			0.68	0.76		
	" 20	320(s)	-		6.5	70/200V	21	32	0.14	0.78			0.68	0.76		
	" 21	350(s)	230(s)		6.2	75/200V	25	40	0.14	0.78			0.68	0.76		
	" 22	160(s)	100(s)		6.2	-	28	41.5	0.14	0.78			0.68	0.75		
	" 23	300(s)	200(s)		6.4	20/200V	22	34.5	0.14	0.80			0.68	0.76		
	" 24	180(s)	100(s)		6.5	10/100V	23	34.5	0.15	0.80			0.69	0.75		
	" 25	320(s)	250(s)		6.5	70/200V	21	32.5	0.15	0.78			0.68	0.76		
	" 26	350(s)	280(s)		6.4	25/200V	19	32.5	0.15	0.80			0.68	0.76		
	" 27	350(s)	210(s)		6.4	130/200V	21	32.5	0.14	0.80			0.69	0.76		
	" 28	220(s)	200(s)		6.5	300/200V	20	33	0.15	0.80			0.68	0.74		
	" 29	400(s)	270(s)		6.4	25/200V	15.5	25	0.15	0.80			0.70	0.77		
	" 30	400(s)	280(s)		6.5	15/200V	21	33	0.14	0.80			0.70	0.76		
	" 31	350(s)	250(s)		6.2	300/200V	23	34.5	0.14	0.78			0.68	0.76		

TABLE 6.5B Characteristics of XT1 High Voltage Medium Power Transistors mounted on TO5 Headers

	Ref No	BV_{cbo}	$V_{CE(sus)}$ 5ma.	V_{SB}	BV_{ebo}	I_{cb} μA.	h_{FE} I_C=50mA V_C=6V	h_{FE} I_C=300mA V_C=6V	$V_{ce(sat)}$ I_C = 200 mA. I_B = 40 mA.	$V_{be(sat)}$	V_{ce} I_C = I_B =	V_{be}	$V_{be(Sat)}$ I_C=50mA V_C=6V	$V_{be(Sat)}$ I_C=200mA. V_C=6V.		
Substrate 114V	EA 32	210(s)	100(s)		6·3	850/200	26·5	39	0.17	0.80			0.68	0.76		
	" 33	170(s)	70(s)		6·4	300/200V	28	38·5	0.17	0.80			0.68	0.76		
	" 34	210(s)	100(s)		6·2	800/200V	28	38·5	0.18	0.80			0.68	0.76		
Substrate 115V	" 35	330(s)	190(s)		6·4	110/200V	28	38	0.18	0.80			0.68	0.76		
	" 36	400(s)	280(s)		6·5	15/200V	21	32·5	0.20	0.80			0.69	0.76		
	" 37	400(s)	280(s)		6·5	15/200V	22	32·5	0.20	0.80			0.68	0.76		
	" 38	280(s)	190(s)		6·5	400/200V	21	32·5	0.20	0.82			0.68	0.76		
	" 39	400	220(s)		6·2	60/200V	31	45·5	0.18	0.81			0.68	0.75		
	" 40	400	280(s)		6·4	13/200V	18	26	0.19	0.80			0.68	0.76		
	" 41	400(s)	300(s)		6·5	30/200V	20	32·5	0.20	0.82			0.69	0.76		
	" 42	400(s)	280(s)		6·5	20/200V	21	32·5	0.19	0.80			0.69	0.76		
	" 43	400(s)	290(s)		6·5	12/200V	20	32	0.19	0.80			0.69	0.76		
	" 44	180(s)	110(s)		6·4	-	21	33	0.19	0.81			0.68	0.76		
	" 45	300(s)	280(s)		5.0	20/200V	18	29	0.19	0.81			0.68	0.76		
		S=Soft.														

TABLE 6.5C Characteristics of XT1 High Voltage Medium Power Transistors mounted on T05 Headers

	Ref No	BV_{cbo}	$V_{CE(sus)}$ 5ma.	V_{SB}	BV_{ebo}	I_{cb} μA.	h_{FE} I_C=50 V_C=6V	h_{FE} I_C=200 V_C=6V	$V_{ce(sat)}$ I_C = 200 mA. I_B = 40 mA.	$V_{be(sat)}$	V_{ce} I_C = I_B =	V_{be}	$V_{BE(sat)}$ I_C=50mA V_C=6V	$V_{BE(sat)}$ I_C=200mA. V_C=6V		
Substrate 112V	E 1.1	380(s)	70		6.0	15 / 200V	28	41.5	0.06	0.76			0.66	0.74		
	„ 1.2	350(s)	200		6.0	20 / 200V	29.5	45.5	0.06	0.76			0.68	0.73		
	„ 1.3	390(s)	190		6.2	180 / 200V	26	40	0.08	0.76			0.68	0.72		
Substrate 113V	„ 2.1	170	170		6.4	3 / 100V	19	32	0.10	0.78			0.68	0.74		
	„ 2.2	470(s)	270		6.0	4.5 / 200V	25	38.5	0.08	0.76			0.68	0.74		
	„ 2.3	320(s)	270		6.2	85 / 200V	23	35	0.10	0.76			0.68	0.74		
Substrate 114V	„ 3.1	170(s)	80(s)		6.3	350 / 100V	25	37	0.11	0.78			0.68	0.74		
	„ 3.2	270(s)	120(s)		6.4	500 / 200V	26	42.5	0.10	0.76			0.67	0.72		
	„ 3.3	280(s)	130(s)		6.5	400 / 200V	26	40	0.12	0.78			0.68	0.72		
Substrate 115V	„ 4.1	440	280		6.3	3 / 200V	24	36	0.14	0.78			0.68	0.74		
	„ 4.2	500	270		6.2	2 / 200V	24	36	0.17	0.78			0.68	0.73		
	„ 4.3	520	280		5.5	0.8 / 200V	24	36.5	0.12	0.78			0.68	0.74		
		S=Soft.														

TABLE 6.6A Characteristics of XT1 High Voltage Medium Power Transistors mounted on TO36 Headers

	Ref No	BV_{cbo}	$V_{CE(sus)}$ [redacted] 5mA.	I_{CBO}. [redacted] 200V.	BV_{ebo}	I_{cb}	h_{FE} I_C=200mA V_C=6V	h_{FE} I_C=50mA V_C=6V	$V_{ce(sat)}$ I_C = 200mA. I_B = 40mA.	$V_{be(sat)}$	V_{ce} I_C = I_B =	V_{be}
Substrate 131V	E1.4	>600	350	120	6.8	0.8m	27.8	17.8	.14	.8		
	" 1.5	>600	420	4	6.6	150	29.4	20.0	.14	.78		
Substrate 132V	" 2.4	>600	450	0.07	6.5	10	23.2	15.6	.14	.8		
	" 2.5	>600	380	0.02	6.6	.15	22.5	14.3	.14	.8		
Substrate 134V	" 3.4	320	160	30	6.2	5/320	26.3	16.6	.1	.77		
	" 3.5	250	160	230	6.3	5/250	25.6	15.6	.1	.79		
Substrate 133V	" 5.1	370	210	3.8	6.6	5/370	30.7	18.5	0.08	.79		
	" 5.2	380	210	1.25	6.6	5/380	24.4	15.6	0.08	.78		

TABLE 6.6B Characteristics of XT1 High Voltage Medium Power Transistors mounted on T036 Headers

TABLE 6.7

Epitaxial Diodes - Epitaxial Layer and Substrate Details

Substrate Number	Substrate Resistivity and type ohm cm	Substrate Doping Element	1st Layer		2nd Layer	
			Resistivity and type ohm cm	Thickness microns	Resistivity and type ohm cm	Thickness microns
223	0.0I N	Sb	0.19 P	18		
222	0.0I N	Sb	1.5 N	11	0.28 P	18

TABLE 6.8

Characteristics of Epitaxial Diodes

Substrate Number	Device Number	V_R at 10 ma	V_f at 100 ma
223	1	18	3.75
	2	17.5	3.8
	3	15	3.5
	4	12	3.4
	5	22.5	3.75
	6	Short Circuit	
	7	15.5	3.75
	8	15.5	3.5
222	1	13	3.0
	2	18	3.25
	3	43	2.8
	4	2	3.4
	5	13	3.2
	6	11	3.1
	7	Short Circuit	
	8	24	3.7
	9	12	3.0
	10	18	3.4
	11	17	3.7
	12	36	3.5

	Ref No	BV_{cbo}	$V_{CE(sat)}$ [illegible]	V_{SB}	BV_{ebo}	nA I_{cb} 20V	I_B h_{FE} I_C=3A V_C=2V	I_B, h_{FE} I_C=4A V_C=2V	$V_{ce(sat)}$ I_C = 3A I_B = 70mA.	$V_{be(sat)}$	$V_{ce(sat)}$ I_C = 4A I_B = 70mA.	$V_{be(sat)}$	V_{CE} I_C=3A I_B=120mA	V_{BE} I_C=3A I_B=120mA	V_{CE} I_C=4A I_B=120mA	V_{BE} I_C=4A I_B=120mA
Substrate 228C	1	97.5	42.1		9.9	0.83			0.41	0.92	0.71	0.96	0.37	0.94	0.5	1.0
	2	95.5	47.5		·3	1.2			1.1	0.9	3.0	0.88	0.88	0.92	1.2	1.0
	3	96.7	42		9.8	1.1			0.57	0.9	0.98	0.94	0.5	0.92	0.62	0.9
	4	88.8	41.1		10.0	0.9			0.37	0.88	0.6	0.94	0.3	0.9	0.43	0.96
	5	95.0	41.6		9.8	1.15			0.5	0.88	0.88	0.92	0.46	0.92	0.58	0.96
	6	94.8	42.1		0.4	1.9			0.64	0.9	0.92	0.94	0.6	0.92	0.72	0.96
	7	54.4	37.8		10	20			0.42	0.9	0.64	0.92	0.39	0.9	0.5	0.96
	8	92.8	42.4		9.8	1.3			0.66	0.88	1.1	0.92	0.62	0.9	0.74	0.96
	9	47.2	41.2		9.9	2.3			0.58	0.88	0.94	0.92	0.54	0.9	0.65	0.96
	10	95.5	44.8		·3	1.3			0.62	0.9	1.2	0.92	0.56	0.92	0.68	0.96
	11	76.1	41.7		9.9	1.2			0.64	0.9	1.0	0.92	0.6	0.92	0.7	0.96
Substrate 230C/2	1	89.7	42.7		9.8	1.8	26	36	0.5	0.9	0.67	0.94	0.48	0.92	0.58	0.96
	2	49.4	42.5		9.9	7.5	26	36	0.48	0.9	0.64	0.94	0.46	0.92	0.56	0.97
	3	86.3	42.4		9.7	1.05	29	40	0.52	0.9	0.72	0.94	0.5	0.92	0.6	0.96
	4	56.1	43.1		9.6	1.35	27.5	38	0.4	0.9	0.56	0.94	0.36	0.92	0.47	0.96
	5	80.8	42.5		7.6	12	28	40	0.43	0.9	0.6	0.94	0.4	0.92	0.5	0.97
	6	91.7	42.5		9.9	0.81	25	36	0.54	0.9	0.7	0.94	0.5	0.92	0.62	0.96

TABLE 6.9 Characteristics of XP6 Epitaxial Planar Transistor

Ref No	BV_{cbo}	$V_{CE(sus)}$	V_{SB}	BV_{ebo}	nA I_{cb} 20V	h_{FE} I_C=3A V_C=2V	h_{FE} I_C=3A V_C=0.75	$V_{ce(sat)}$ I_C = 3A I_B = 75mA.	$V_{be(sat)}$	V_{ce} I_C = I_B =	V_{be}				
Substrate 22R															
1	95	25.2		8.5	0.47	55.5	52.5	0.52	1.1						
2	92	24.9		8.0	20.5	55.5	52	0.4	0.96						
3	78	25.1		7.5	0.36	58	54.5	0.47	0.97						
4	90	24.8		7.5	0.91	62.5	57.5	0.44	0.96						
5	93	25.0		9.2	1.5	48.5	45.5	0.53	0.94						
6	90	25.0		9.0	1.3	47.5	45	0.58	0.94						
7	91	25.2		5.9	1.4	43	40.5	0.66	0.94						
8	94	25.2		7.0	1.05	48.5	45.5	0.57	0.94						
9	92	24.8		7.3	1.05	52	48.5	0.58	0.94						
10	93	24.9		7.3	1.4	47.5	45.5	0.54	0.93						
11	95	25.0		9.2	4.5	68	64	0.54	0.95						
12	92	24.9		9.1	0.95	60	55.5	0.54	0.95						

TABLE 6.10 Characteristics of XH6 Epitaxial Homogeneous Transistor with N^+P Epitaxial Structure

Substrate 152R

Ref No	BV_{cbo}	$V_{(sus)CE}$ 1A	V_{SB}	BV_{ebo}	nA I_{cb} 20V	h_{FE} I_C=3A V_C=2V	h_{FE} I_C=3A V_C=0.5	$V_{ce(sat)}$ I_C = 3A I_B = 75mA.	$V_{be(sat)}$	$V_{ce(sat)}$ I_C = 2.5AMPS I_B = 100 ma.	$V_{be(sat)}$	h_{FE} I_C=2½A V_C=2V	h_{FE} I_C=2½A V_C=.7V		
1	140	70.5		8.8	0.8	60	48.5	0.42	0.94	0.25	0.92	69.5	57		
2	130	68.9		8.5	1.7	75	60	0.34	0.94						
3	110	68.7		8.7(s)	0.86	71.5	57.75	0.36	0.92	0.25	0.9	83.5	66		
4	100	66.5		8.5	1.1	77	62.5	0.32	0.92	0.24	0.9	89	69.5		
5	115	67.4		8.0	1.6	75	62	0.33	0.93	0.24	0.9	89	69.5		
6	120	67.8		7.9	1.0	75	61	0.34	0.92	0.22	0.89	83.5	66		
7	140	70.8		8.8	0.98	57.75	47.5	0.44	0.92						
8	110	69.3		6.5	0.86	66.5	55.5	0.36	0.92	0.23	0.9	78	62.5		
9	100	66.4		8.5	0.6	83.5	68	0.3	0.9	0.22	0.88	96	78		
10	105	69.3		8.6	4.5	62.5	51.75	0.4	0.92						
11	115	68.1		8.6	0.9	77	63	0.31	0.92	0.22	0.9	89	73.5		
12	115	68.8		8.5	1.7	68	57.75	0.34	0.92	0.22	0.9	82	66		
13	91	69.4		8.4	4.2	66.5	55	0.35	0.92						
14	120	68.7		8.6	0.56	75	62.5	0.3	0.92	0.22	0.9	89	71.5		
15	120	68.3		8.3	0.65	68	56.5	0.35	0.92	0.22	0.9	78	64		
16	105	66.5		8.5	0.78	75	60.5	0.34	0.92	0.24	0.9	89	71.5		
17	105	67.1		7.8	0.74	75	61	0.32	0.92	0.24	0.9	89	71.5		
18	120	68.7		8.5	0.74	65.5	53.5	0.4	0.92	0.24	0.9	73.5	62		
19	120	69.3		8.5	0.77	64	52.5	0.4	0.92	0.23	0.9	73.5	59.5		
20	120	68.7		8.3	0.95	70	57.75	0.35	0.92	0.24	0.9	81	66		

TABLE 6.11 Characteristics of XH6 Epitaxial Homogeneous Base Transistor with N^+NP Epitaxial Structure and P Base Region of 4-5 Micro Seconds Lifetime

Ref No	BV_{cbo}	$V_{(SUS)}$ 1A.	V_{SB}	BV_{ebo}	nA I_{cb} 20V	h_{FE} I_C=3A V_C=2V	h_{FE} I_C=3A V_C=0.7V	V_{ce} I_C = I_B =	V_{be}	V_{ce} I_C = I_B =	V_{be}				
Substrate 149R C 1	150	70.9		9.2	1.1	38.4	32.6								
2	158	70		9.2	0.74	39	33.4								
3	160	70.6		9.2	0.56	39.4	33.4								
4	92	70.7		9.1	3.2	39.4	32.6								
5	63	72.1		9.2	4.4	38	31								
D 1	170	71.1		9.1	0.53	48.5	39.4								
2	150	70.5		9.3	6.3	44	37.5								
3	150	71.4		9.0	0.65	43	36.2								
4	86	70.5		9.1	0.68	43	36.6								

TABLE 6.12 Characteristics of XH6 Epitaxial Homogeneous Base Transistor with N^+NP Epitaxial Structure and P Base Region of 1-2 Micro Second Lifetime

TABLE 6.13

Process Details for Producing Epitaxial Substrates for the XP6 Epitaxial Planar Transistor

Main Hydrogen Flow	40 litres/minute
Hydrogen chloride polishing	1.0 litres/minute for 5 minutes
Silicon tetrachloride/hydrogen flow	2.0 litres/minute
Automatic Temperature control setting	1300°C
Silicon tetrachloride temperature	0°C

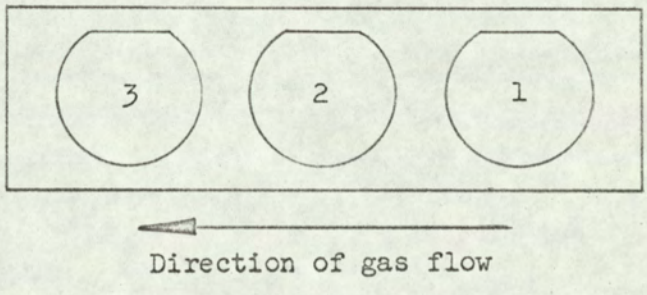
Silicon coated graphite susceptor

"Wacker" intrinsic silicon tetrachloride

N type substrate 0.01 ohm cm antimony doped, pulled crystal

P type substrate 1.0 ohm cm boron doped, pulled crystal

Position of substrates on susceptor



Approximate growth rate 1.4 microns per minute

Average stacking fault density <15 per sq. cm.

TABLE 6.14

Batch Process Details for Epitaxial Substrates for XP6 Epitaxial Planar Transistor

Run No.	Process Details: Substrate No. L. Series Position 3	Position 2	Position 1	Substrate Temperature °C Position 3	Position 2	Position 1	Deposition time Minutes	Layer Details: Layer Thickness (Microns) or P Substrate and Layer Resistivity Position 3	Position 2	Position 1	Remarks
11	28	27	26	1120	1115	1116	12	15.3	14.2	13.9	
12	31	30	29	1125	1122	1100	12.75	14.6	15.1	14.8	
13	34	33	32				12.75	13.9	14.7	15.3	
14	37	36	35	1168	1138	1160	12.75	12.0	10.6	12.4	
17	46	45	44				12.75	17.1	17.0	17.0	Evaporator refilled
18	49	48	47				11.25	14.3	14.8	15.5	
19	52	51	50	1160	1124	1169	11.25	18.1	14.7	17.4	New susceptor support
20	55	54	53	1180	1143	1140	11.25	17.0	16.5	18.8	
21	58	57	56	1130	1130	1118	9.75		12.3	14.0	
22	61	60	59	1130	1136	1136	11.25		14.2	17.0	
24	67	66	65				11.25	14.5	15.0	17.6	
25	70	69	68	1138	1140	1142	11.25	12.4	12.8	14.8	
26	73	72	71	1148	1142	1130	12.5	15.0	15.4	17.8	
27	76	75	74	1135	1136	1132	12.5	13.0	14.2	16.1	
28	79	78	77	1129	1132	1105	12.5	P(1.7)	14.3	15.3	
29	82	81	80	1162	1128	1152	12.5	P	14.5	15.9	
30	85	84	83				12.5	P	14.7	15.4	
31	88	87	86				12.5	P	14.5	17.0	
32	91	90	89	1152	1138	1128	12.5	P	14.5	16.2	
33	94	93	92	1140	1137	1132	12.5	P	13.8	15.4	
34	97	96	95	1112	1139	1139	11.75	P	15.3	16.3	
35	100	99	98	1178	1150	1182	10.75	P	15.3	17.8	

TABLE 6.14 (CONTINUED)

Run No.	Process Details: Substrate No. L. Series Position 3	Position 2	Position 1	Substrate Temperature °C Position 3	Position 2	Position 1	Deposition time Minutes	Layer Details: Layer Thickness (Microns) or P Substrate and Layer Resistivity Position 3	Position 2	Position 1	Remarks
36	103	102	101	1108	1130	1118	10.75	P	13.9	15.1	
37	106	105	104	1118	1136	1120	12.50	P	14.6	15.3	
41	115	114	113	1120	1118	1123	10.75	P(2.3)	14.3	15.6	Evaporator refilled
42	118	117	116	1115	1133	1139	10.75	P(1.9)	13.9	15.5	
43	121	120	119	1130	1127	1122	10.75	P	14.4	15.8	
44	124	123	122	1137	1137	1137	10.75	P	14.0	15.5	
45	127	126	125	1135	1140	1122	10.75	P	14.2	15.5	
46	130	129	128	1131	1131	1137	10.75	P	14.3	15.3	
47	133	132	131	1151	1150	1138	10.75	P	14.9	16.2	
48	136	135	134	1130	1133	1152	10.75	P	13.3	15.0	
52	148	147	146	1110	1130	1133	10.75	P(3.8)	14.6	15.8	Evaporator refilled
56	160	159	158	1150	1142	1148	10.75	P	15.0	16.3	
57	163	162	161	1130	1140	1136	10.75	P	14.8	16.1	
58	166	165	164	1160	1158	1130	10.75	P	14.8	16.3	
59	169	168	167	1140	1140	1143	10.75	P	14.8	16.1	
60	172	171	170	1135	1137	1113	10.75	P	14.6	15.4	
61	175	174	173	1128	1140	1140	10.75	14.7	15.0	15.6	
62	178	177	176	1135	1134	1119	10.75	15.5	15.1	15.9	
63	181	180	179	1132	1138	1130	10.75	15.4	14.4	15.5	
64	184	183	182	1140	1140	1141	10.75	15.0	14.4	15.4	
65	187	186	185	1132	1142	1150	10.75	16.0	15.6	17.2	
66	190	189	188	1130	1141	1142	10.75	14.2	14.2	15.9	
67	193	192	191	1132	1142	1142	10.75	14.5	14.1	15.7	
71	199	198	197	1122	1160	1128	9.5	14.4	15.3	15.0	Evaporator refilled

TABLE 6.14 (CONTINUED)

Run No.	Process Details: Substrate No. L. Series Position 3	Position 2	Position 1	Substrate Temperature °C Position 3	Position 2	Position 1	Deposition time Minutes	Layer Details: Layer Thickness (Microns) or P Substrate and Layer Resistivity Position 3	Position 2	Position 1	Remarks
72	202	201	200	1188	1150	1142	9.5	14.5	P	P(5.6)	
73	205	204	203	1118	1154	1140	9.5	P	15.3	16.4	
74	208	207	206	1155	1165	1160	9.5	P	15.9	17.7	
75	211	210	209	1130	1146	1132	9.5	P	15.1	15.9	
76	214	213	212	1138	1152	1140	9.5	P(3.2)	15.1	16.1	
77	217	216	215	1140	1150	1150	9.5	P(4.5)	14.7	16.4	
78	220	219	218	1130	1150	1140	9.5	P(3.7)	19.8	20.7	Deposition time suspected
79	223	222	221	1140	1142	1150	9.5	13.8	13.5	15.5	
80	226	225	224	1137	1140	1160	9.5	15.2	14.8	16.2	Evaporator refilled
83	234	233	232	1152	1140	1160	9.5	P(1.8)	15.1	17.7	Gaseous doping with PH_3
84	237	236	235	1130	1138	1162	9.5	P(7.2)	15.1	17.0	Gaseous doping with PH_3
85	240	239	238	1175	1160	1140	9.5	P(8.5)	15.8	17.5	Gaseous doping with PH_3
86	243	242	241	1145	1135	1094	9.5	P(0.7)	14.5	14.0	Gaseous doping with PH_3 Evaporator refilled
87	246	245	244	1151	1138	1072	9.5	P(2.81)	15.1	14.7	Gaseous doping with PH_3
88	249	248	247	1155	1132	1088	9.5	P(1.14)	14.1	14.2	Gaseous doping with PH_3
89	252	251	250	1155	1140	1085	9.5	P(22.8)	14.3	13.9	Gaseous doping with PH_3
90	255	254	253	1152	1136	1075	9.5	P(7.3)	13.2	13.0	Gaseous doping with PH_3
91		257	256		1137	1060	9.5		P(9.8)	13.0	
92	260	259	258	1140	1136	1095	9.5	P(0.5)	12.9	13.3	Gaseous doping with PH_3
93			261			1120	10.0			15.4	
94	264	263	262	1245	1238	1185	10.0	P(20.5)	15.4	16.5	Gaseous doping with PH_3
95		266	265		1190	1120	10.0		P(0.94)	15.2	
96		268	267		1182	1148	10.0		P(0.85)	13.9	
97		270	269		1179	1112	18.0		P(0.71)	18.2	

TABLE 6.15

Statistical Analysis of the Batch Process Details
for Epitaxial Substrates for XP6 Epitaxial Planar Transistor

Statistical Analysis	For all Substrates on the Susceptor	For Substrates in Pos.3 on the Susceptor	For Substrates in Pos.2 on the Susceptor	For Substrates in Pos.1 on the Susceptor
Mean Deposition Temperature ^{o}C (Optical Pyrometer)	1135	1131	1137	1142
Mean Layer Thickness (Microns)	15.2	15.8	14.4	14.8
Upper and Lower Limits for the Range of Thickness for 95% Confidence (Microns)	12.4-18.0	13.0-18.6	12.5-16.3	11.8-17.8

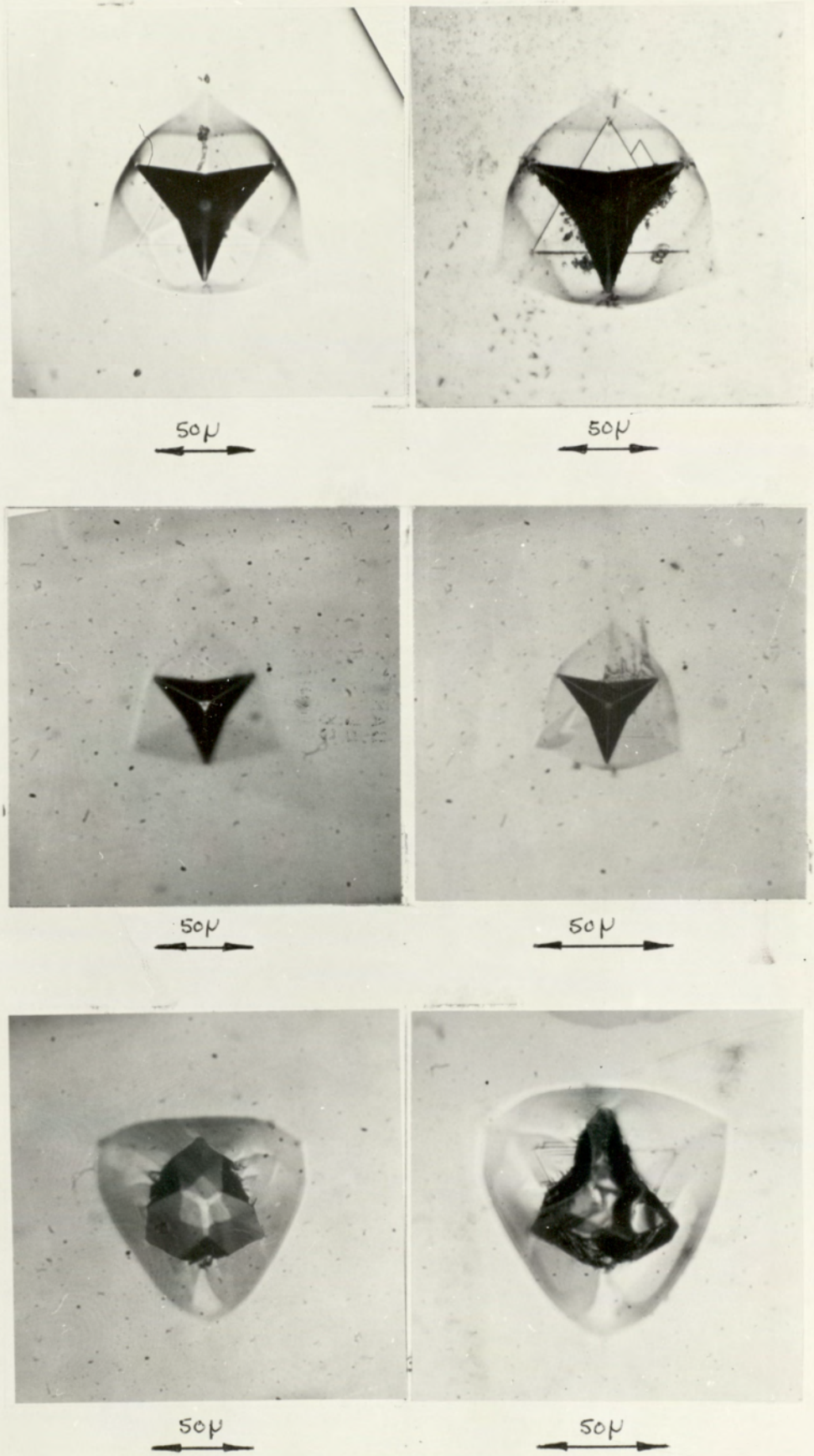


Fig. 6.1 Surface protruding imperfections on (111) orientated substrates

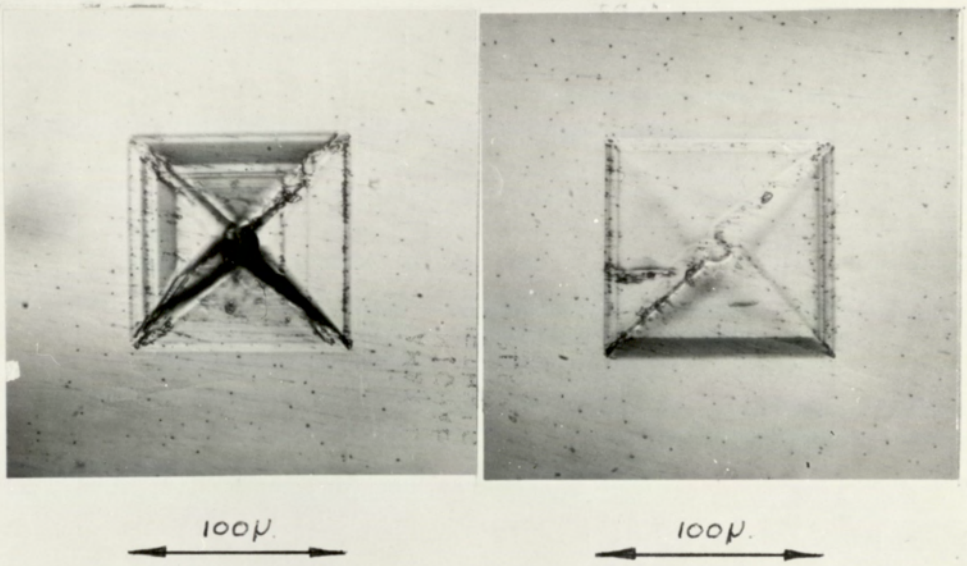
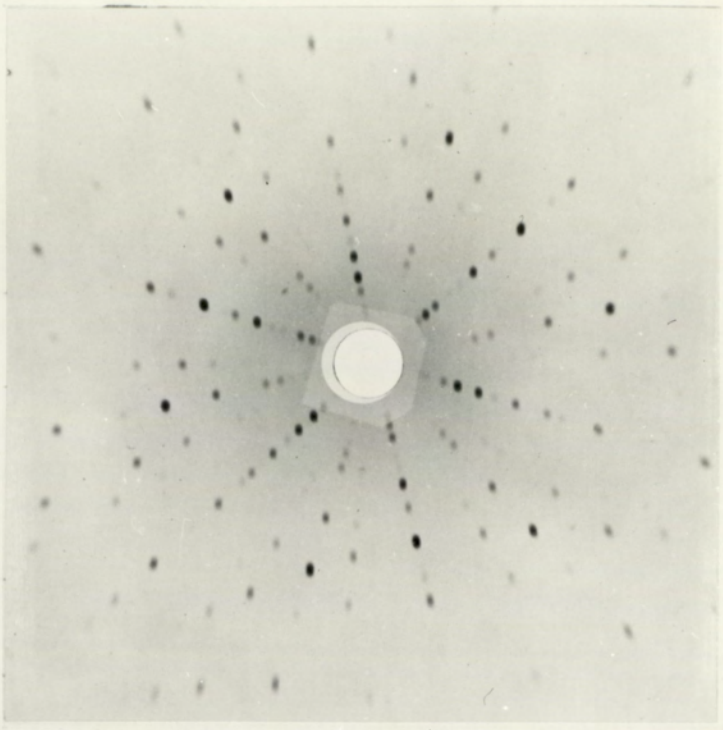


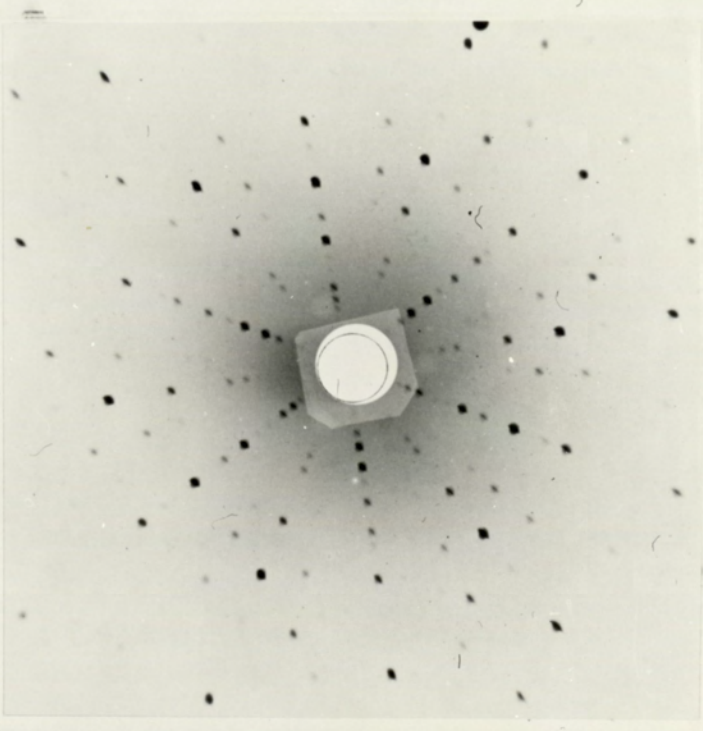
Fig. 6.2 Surface protruding imperfections on (100) orientated substrates

x300

Fig. 6.3 Line etch figures resulting from the leakage of nitric oxide into the gas system before silicon deposition



Substrate



Epitaxial Layer

Silver radiation Surface to film distance 3 cm

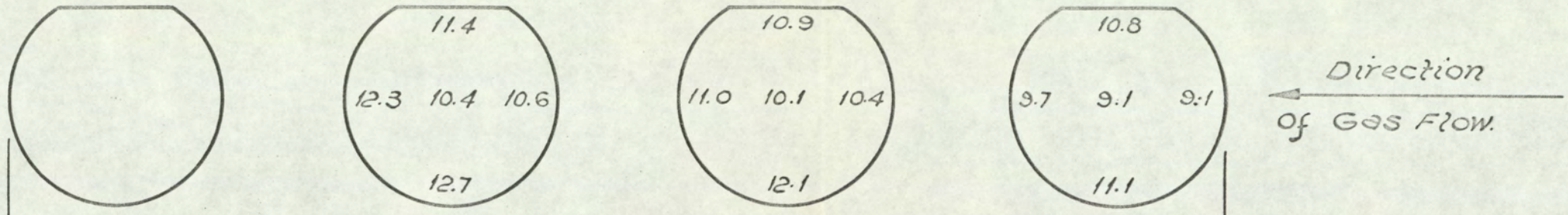
Fig. 6.4 Laue back reflection X-ray photograph of epitaxial layer and substrate

er Thickness

Infra Red 14·8 Microns.
Stacking Fault 13·9 Microns.

Angle Lap 12·0 Microns
Stacking Fault 12·2 Microns

er Resistivity



er Type

P Type

strate Resistivity 0.01N OHN CM N Sb

1.1 - 1.7 OHM CM. N Antimony Doped

e and Doping
Element.

Gas Flow Details.

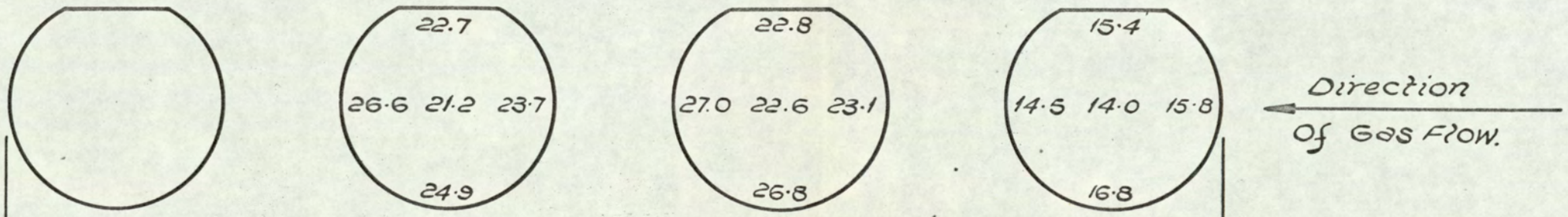
Doped Gas 20 cc/Min
0.4 PPM Diborane In
Hydrogen.
Main Hydrogen.
40 Litres/Min.
$SiCl_4/H_2$ 2 Litres/Min
$SiCl_4$ Temperature 0°C.

er Thickness

Infra Red 13·2 Microns.
Stacking Fault 15·5 Microns.

Angle Lap 9.6 Microns
Stacking Fault 14·3 Microns

er Resistivity



er Type

P Type

strate Resistivity
& Doping
ments.

0.01 OHM CM N Antimony Doped

Layer Resistivity Measured By Four Probe Method

FIG. 6.5. THE EFFECT OF THE INTERACTION OF GAS STREAM & SUBSTRATE DOPING ELEMENTS ON LAYER RESISTIVITY. — N SUBSTRATE P DOPANT IN GAS STREAM.

r Thickness

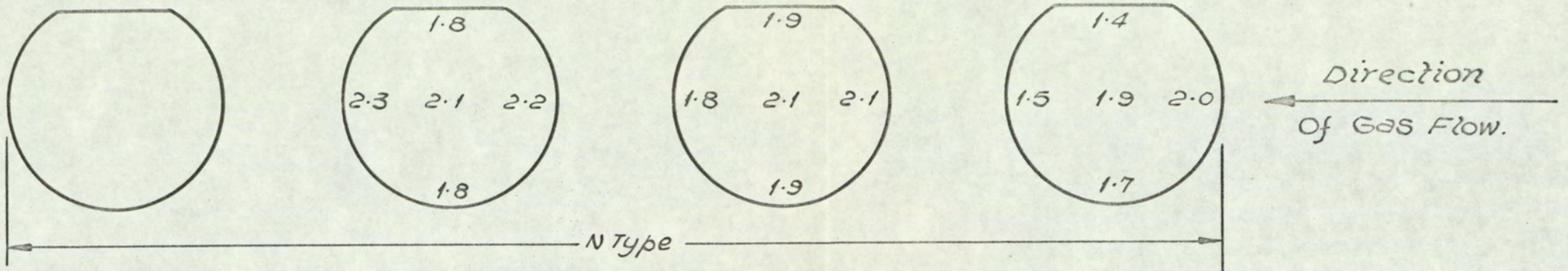
Infra Red 13.0 Microns

Stacking Fault 13.9 Microns

Angle Lap 12.0 Microns

Stacking Fault 12.2 Microns

r Resistivity



er Type

strate Resistivity 0.01N OHM CM N Sb

0.66 - 1.33 OHM CM P Boron Doped

and Doping
ment.

Gas Flow Details

Doped Gas 500 cc/Min
0·065 PPM. Phosphine
In Hydrogen.

Main Hydrogen 40 Litres/Min

Si Cl4/H2 2 Litres/Min.

Si Cl4/ Temperature 0°C.

r Thickness

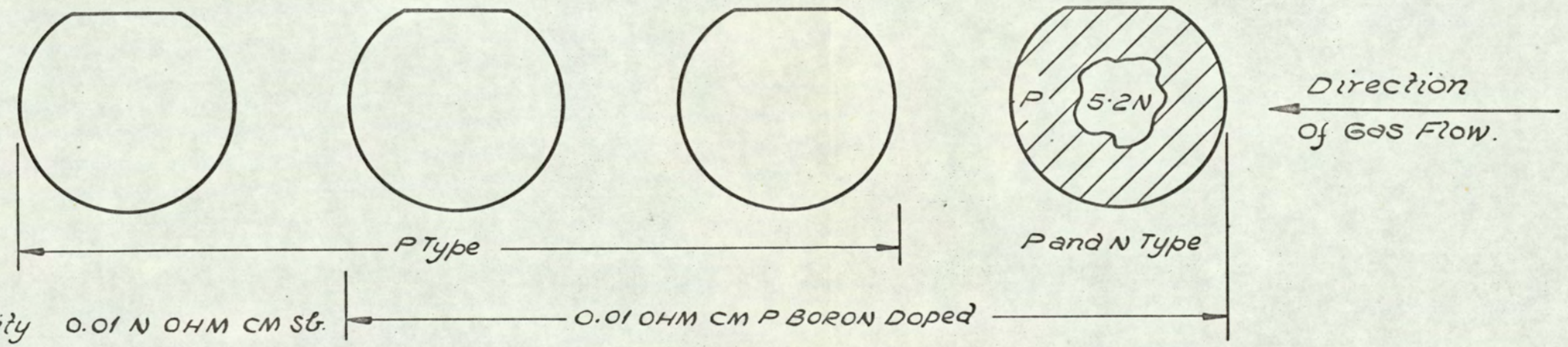
Infra Red 13·7 Microns

Stacking Fault 13·9 Microns

Angle Lap 3.2 Microns

Stacking Fault 13·2 Microns

er Resistivity



er Type

strate Resistivity 0.01 N OHM CM Sb.

0.01 OHM CM P BORON Doped

e and Doping
ment.

Layer Resistivity Measured By Four Probe Method.

FIG. 6.6. THE EFFECT OF THE INTERACTION OF GAS STREAM & SUBSTRATE DOPING ELEMENTS ON LAYER RESISTIVITY — P SUBSTRATE N DOPANT IN GAS STREAM.

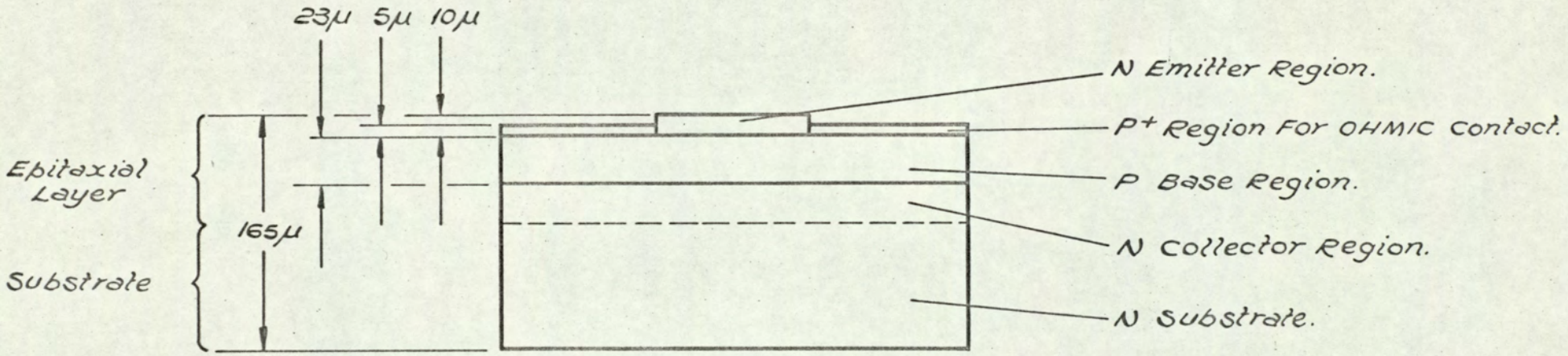


FIG. 6.7. STRUCTURE OF XT1. HIGH VOLTAGE MEDIUM POWER TRANSISTOR.

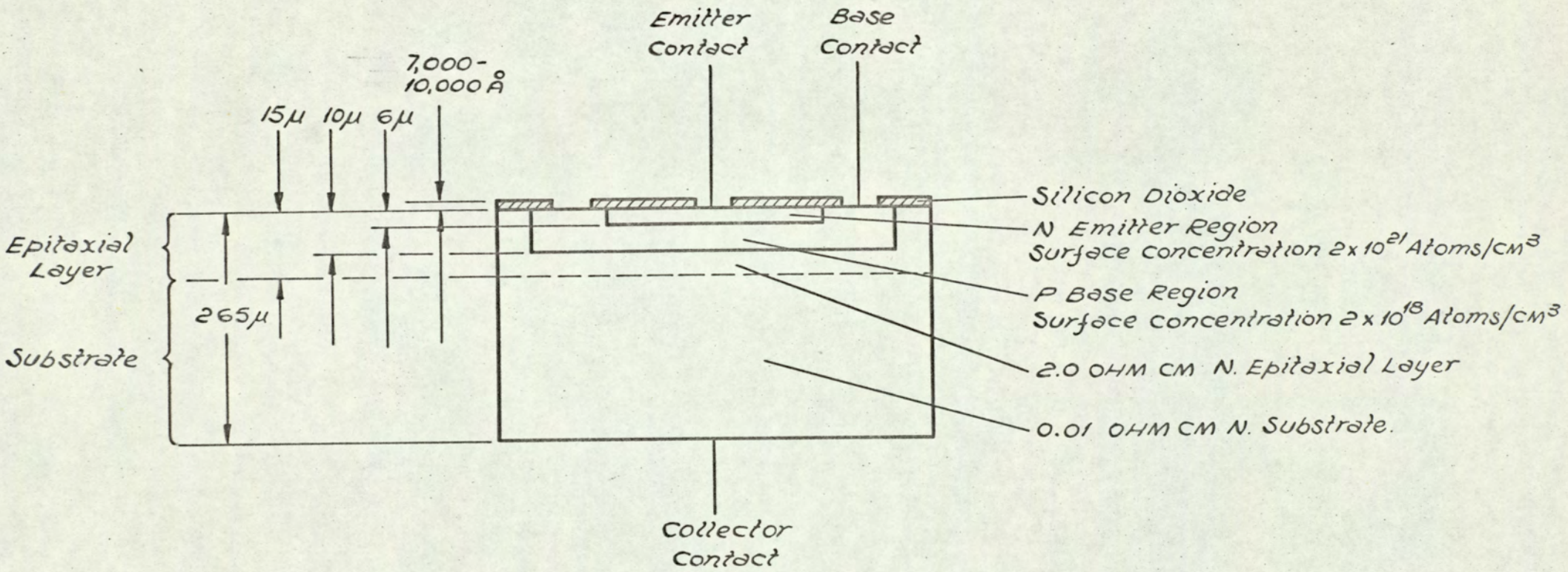


FIG. 6.8 STRUCTURE OF XP6 EPITAXIAL PLANAR TRANSISTOR.

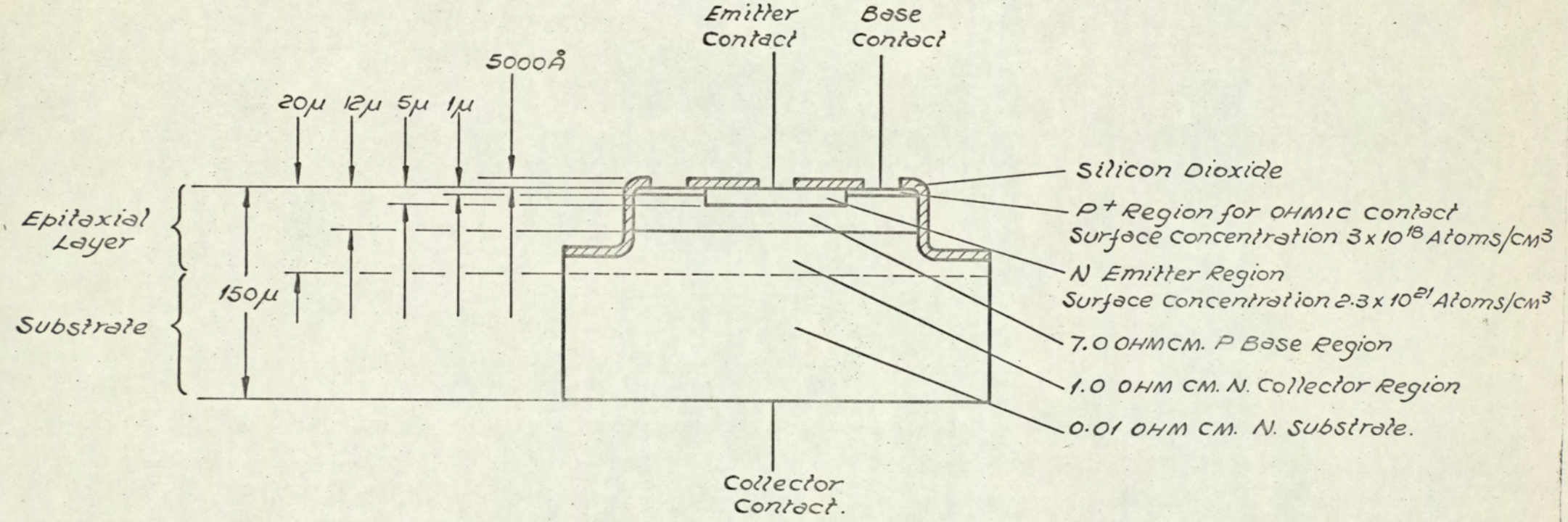


FIG. 6.9. STRUCTURE OF XH6 EPITAXIAL HOMOGENEOUS BASE TRANSISTOR

7. DISCUSSION

7.1 Apparatus

The first decision that had to be made in connection with the design of the apparatus was the method of heating the substrate in the form of a disc $\frac{7}{8}$ to 1 inch diameter and 0.010 inch thick sited in a reaction tube to the required temperature. The following methods of heating were considered: (1) external radiation heating with a resistance or glow bar type furnace and (2) internal radiation and conduction from a susceptor heated by (A) resistance or (B) induction.

With the silicon tetrachloride-hydrogen process the silicon produced is required at the substrate which should thus be at the highest temperature in the system. External radiation heating will result in the reaction tube walls being at a higher temperature than the substrate and thus in the preferential deposition of silicon at the surface of the reaction tube. Heating from within the reaction tube can concentrate the heated zone around the substrate.

In practice silicon deposition and hence the gas flow is required over only one surface of the substrate and thus the other surface can lie directly on a flat susceptor surface heated by radiation and conduction. Resistance heating of the susceptor would require water cooled electrical contacts to the susceptor making it inflexible with the great possibility of impurity contamination of the system. On the other hand with induction heating no direct contact is made to the susceptor and the induction heating coil can be placed outside the reaction tube resulting in a system with the following advantages, (A) the heat is produced at the substrate (B) the reduction of impurity contamination in the reaction tube and (C) a susceptor which can easily be withdrawn from the tube for loading and cleaning.

In this work the heating of the substrate by radiation and convection from a susceptor coupled to an induction heating coil has proved to be completely satisfactory. The coupling between the coil and

the susceptor is of high impedence and the generators made available for this investigation were not designed specifically for this type of coupling and efficient power from the generators for heating was not obtained.

The two constituents of the deposition chemical reaction, hydrogen and silicon tetrachloride are required in the gaseous state and of controlled composition at the substrate surface. However at room temperature silicon tetrachloride is in the liquid state and thus the apparatus was designed to make use of hydrogen as a carrier gas to transport silicon tetrachloride vapour from its liquid source and the gas composition controlled by the hydrogen flow rate and silicon tetrachloride temperature.

The use of epitaxial material for the processing of devices or for experimental investigation requires quantities of substrates with layers of consistent and uniform thickness.

With the vertical reaction tube of the initial deposition apparatus it was only possible to grow a layer on a single substrate in one operation cycle and the size of the susceptor could not be increased to accommodate more substrates because the diameter of the reaction tube was limited by the power available for heating from the induction generator. In order to develop the process the reaction tube was changed to a horizontal position resulting in the heating of a number of substrates for simultaneous deposition of layers. In order to obtain uniform thickness of the layers, different configurations of reaction tube geometry to produce horizontal and vertical gas flow over the substrates were investigated and the results reported in Section 5.5. The results indicate that with the experimental conditions used, it was not possible to obtain layers of uniform thickness as measured across two diameters on an individual substrate or on a number of substrates with simulatneously grown layers. However the statistical analysis of the variance of the thickness measurements indicate that in the configuration of reaction tube geometry with horizontal gas flow, only the substrate diameter and

not its position on the susceptor influences the thickness uniformity of the layer while in the other configurations the substrate position and its diameter influence the layer thickness uniformity.

This analysis indicated that the horizontal reaction tube with horizontal gas flow offered the best possibility for development to produce layers of uniform thickness on a number of substrates. With this system the thickest layer is obtained on the substrate nearest the gas inlet and the thinnest on the substrate near the outlet. This is probably due to depletion of silicon from the reactive gases as they flow over the substrate. It should be possible to reduce this rate of depletion of silicon from the reaction gases by increasing the velocity of gas flowing over the substrates and thus reducing the layer thickness variation along the substrates.

The velocity of gas flow can be increased by (1) reducing the cross section area of the reaction tube or (2) increasing the gas flow rate. The cross sectional area of the tube can be reduced by (A) decreasing the diameter or (B) altering its cross section shape. The reduction of the tube diameter would be a retrograde step in the development of the process, because it would result in the use of smaller diameter substrates (while at the time of this development quartz tubes of rectangular cross section were not readily available). Thus the only method available was to increase the rate of gas flow into the reaction tube.

This requirement of the higher gas flow was one of the reasons for the design and development of the multideposition apparatus. In this apparatus a small hydrogen flow is used to transport the silicon tetrachloride and is mixed with a high hydrogen flow (increased by a factor of 12 from the previous apparatus) to increase the velocity of the gas flow above the substrate. This has resulted in a considerable improvement in the uniformity of layer thickness on substrates along the susceptor. Further improvement was obtained (1) by tilting the susceptor 5° to 10° to the direction of gas flow, which results in each substrate

receiving a fresh supply of non-depleted reactive gases and (2) by a temperature gradient of approximately 20°C along the susceptor with the lowest temperature near the gas inlet. The progressive development of the process has resulted in the growth of layers of uniform thickness on individual substrates and on a series of substrates with simultaneously grown layers as reported in Section 5.6.

7.2 The Control of the Layer Resistivity and Type from the Gaseous Phase

The overall control of the layer type and its resistivity can be obtained by the addition of dopants to the gas stream which decompose or undergo chemical reduction in the hot zone to produce impurity atoms which are incorporated into the growing lattice.

In the liquid doping method, which is a two component system the rate of evaporation of the silicon tetrachloride and dopant will depend on their relative vapour pressures and will result in a change of concentration of the dopant solution in the silicon tetrachloride. This has been observed in this work with the phosphorus trichloride doping of the silicon tetrachloride. Theuerer (43) and Nuttal (44) reported that in this system there is a large change in the ratio of $PCl_3/SiCl_4$ vapour with continuous evaporation and that in order to keep a reasonable tolerance on the resistivity of the layer only 20-30% of the doped silico tetrachloride can be used before more silicon tetrachloride is added to the evaporator.

The effects of the preferential evaporation can be overcome by the use of a compensating evaporator containing undoped silicon tetrachloride before and in series with the doped evaporator. This is set at a predetermined temperature and compensates for the relative loss of silicon tetrachloride from the doped evaporator. This technique can provide a steady $PCl_3/SiCl_4$ vapour concentration and extend the effectiv use of the doped silicon tetrachloride in the evaporator.

With the liquid doping method a different solution which is usually obtained by a series of solution dilutions has to be prepared

for each doping level and this lack of flexibility has resulted in the solution method being replaced by the gaseous doping technique.

In this method the doping gases diborane, arsine or phosphine are diluted in hydrogen by the manufacturer and used in this investigation in the concentration range 0.05 to 25 ppm. The doped gas is introduced into the reaction system with accurate measurement and control of the gas flow and thermally decomposes in the reaction zone. This method has proved to be simple, accurate and flexible for the control of layer type and resistivity, but the following problems have been encountered with the supply of doped gas. (1) The manufacturer does not appear to be able to supply the doped gas to an accurate specified concentration and (2) the concentration of diborane and arsine in the hydrogen decreases over a period of time, due to their chemical instability and require regular calibration.

The results reported for layer resistivities in Section 6.8 for the interaction of doping impurities from the gas phase and substrate indicate slightly less doping of the P layers near the gas outlet (Figure 6.5) and this probably results from the depletion of the doping gas from the main gas stream as it flows over the substrates.

In these methods of doping, the layer resistivity is empirically calibrated against the concentration of liquid dopant in the silicon tetrachloride or the doped gas flow. This calibration is specific for the process conditions of hydrogen and silicon tetrachloride gas flows and the substrate type, resistivity and doping element, used to produce the layer because of the significant influence that the substrate can have on the layer.

7.3 Deposition Temperature

The effect of temperature on the deposition of silicon influences (A) the growth rate of the deposition process and (B) the morphology of the layer on the substrate and is reported in Section 5.2.

Figure 5.7 shows the effect of temperature on the layer growth rate which increases at a relatively low temperature and levels out at high temperature. If these results are considered in terms of a heterogeneous reaction, Section 2.1, the slope of the curve may be a measure of the activation energy for the process limited by the absorption rates of the reactants which are surface controlled, while the flattening out of the curve could be due to the predominance of the mass transfer (diffusion) control of the reactants at the higher temperature.

The morphology of the layer obtained on the substrate surface at different temperatures can be divided into three sections, viz, (1) for temperatures up to approximately 1050°C incomplete layers of fine crystallite, Figure 5.1, (2) for temperatures between 1050°C and 1200°C a complete layer with rough surface of definite triangular geometry, Figure 5.4, and (3) for temperatures above 1200°C a smooth mirror surface. It is assumed that the growth of the layer takes place by the addition of silicon atoms to steps and that these steps are formed mainly by two dimensional nucleation - Section 2.1. At high temperatures the rate of two dimensional nucleation R_n is large (equation 2.1) and results in many steps available for growth and a smooth surface following the substrate contours is formed. However, as the temperature is lowered the nucleation rate R_n is reduced and insufficient steps are available and layer growth occurs preferentially away from the surface and accounts for the rough regular surfaces observed.

In practice the requirement for device fabrication of a layer with a smooth surface and a high degree of lattice perfection results in the layers being grown at temperatures above 1200°C.

7.4 Structural Defects in the Layer

Three types of lattice defect:- etch pits, surface protruding imperfections and stacking faults, have been observed in the layers.

7.4.1 Etch Pits

The most common type of defect in single crystal silicon is the edge dislocation which is caused by an imperfect array of atoms in localised regions in a crystal. The point of emergence of the edge dislocation at the surface produces a well defined "etch pit" when the surface is subjected to a suitable etch. Etch pits have been observed at the surface of the layer and their concentration measured for layers grown on substrates prepared from float zoned and pulled crystal with different substrate preparations - Table 5.3. The results of these counts indicate that the method of substrate surface preparation has limited effect on the concentration of etch pits in the layer. However, the type of substrate material does appear to have some influence. Larger concentrations of etch pits were observed on layers grown on float zoned substrate material which initially contains more dislocations compared with pulled substrate material.

The dislocations are always present in normal single crystal silicon and may act as nuclei for the precipitation of foreign atoms or impurities that may be present in the silicon lattice. These impurities migrate to dislocations to relieve part of the lattice strain present at the dislocation site and the heterogeneous regions created can impart poor electrical characteristics to devices containing them (45).

These results indicate that the number of etch pits in the growing layer is related and similar to that of the substrate and in practice by using low etch pit density substrate material, the degrading effects of dislocations can be minimised.

7.4.2 Surface Protruding Imperfections

These defects have been observed on only a few layers produced in the initial deposition apparatus at an early stage in the development of the process. The defects appear as starlike hillocks on the epitaxial layer and have a single high point surrounded by well defined crystallographic planes or polycrystalline high points surrounded by

ill-defined crystallographic planes. On (111) orientated substrates the defects have triangular bases and on (100) orientated substrates square bases. The defects appear to originate at the interface between the substrate and layer. On (111) substrates some of the defects were associated with triangular or partial triangular stacking faults which were concentric in their configuration but related 60° to each other. Miller (46) and Chu (47) have reported that the tripyramid is in twin orientation with respect to the surrounding material, which explains the development of facets alternative to those usually observed on (111) surfaces, while the appearance of the tripyramid after etching suggests that each pyramid is a separate twin, the twin plane being the plane of the substrate.

Miller (46) and Nielson (48) attribute the origin of the tripyramid to carbon present on the substrate surface in the form of silicon carbide and the twin lamellæ are caused by the silicon layer overgrowth of the carbide. In this work, it is probable that silicon carbide was formed at the deposition temperature as a result of (A) the residue contamination left on the surface of the substrate after final cleaning in organic solvents or (B) the transport of carbon from the susceptor to the substrate, from a reaction between the hydrogen and an uncoated part of the graphite susceptor.

7.4.3 Line Etch Figures (Stacking Faults)

The surfaces of the epitaxial layers revealed on etching, line etch figures, that on (111) surfaces generally had the shape of equilateral triangles and on the (100) surfaces the form of squares or parts of squares.

This investigation indicated that generally:-

1. The defects observed in layers grown on mechanically polished substrates were often orientated in approximately straight lines as a result of nucleation at the scratches on the substrate surface, while defects in layers grown on

etched substrates were randomly distributed and fewer in number. This observation indicates that the surface damage of the substrate as a result of polishing effects the line etch figure nucleation.

2. The introduction of a few ppm of combined oxygen into the gas stream just prior to deposition to form an oxide at the surface results in line etch figures in the material - Section 6.4. Figure 6.3.
3. With certain process conditions, the stacking fault method of measuring layer thickness is in agreement with the other methods of layer thickness measurements - Section 6.1.

The foregoing observations indicate that the defects originate at the interface between the substrate and epitaxial layer as a result of surface damage or surface contamination of the substrate.

The poor characteristics of devices associated with layers containing these defects, Section 6.9, necessitated further investigations to eliminate the defects from the material. These investigations followed two paths: (1) the design and development of the multideposition apparatus described in Section 3.1 which would reduce the possibility of oxygen contamination of the gas system and (2) methods of improved substrate surface preparation.

The removal of mechanical substrate surface damage by aqueous polishing resulted in a marginal reduction of the concentration of line defects in the epitaxial material (Table 5.2) but the substrate surface after polishing was often uneven and quenching in deionised water could result in an adherent film of hydrated silica. A non-mechanical method for the controlled surface removal and polishing of the substrate was required and investigations of electropolishing and gaseous chemical polishing with anhydrous hydrogen chloride processes were made. A method for the preparation of flat surfaces of silicon by electropolishing has been reported by Baker (25) and apparatus was constructed to investigate

the preparation of substrate surfaces. With this process (Section 3.2) the rate of surface removal was not uniform and could result in wedge shaped substrates and a depression at the area on the surface, where the electrical contact was made to the rear of the substrate. This depression was overcome by nickel plating the rear surface of the substrate, which resulted in uniform current distribution and control of the process conditions produced substrates with flat mirror surfaces.

Once the substrate surface has been prepared by electropolishing or aqueous polishing there is a great possibility of surface damage and contamination during the subsequent processing operations preceding the epitaxial growth and thus simultaneously with the development of the electropolishing process a gaseous polishing process which can be operated in the apparatus was investigated. Because of the success of the gaseous polishing process further development of the electropolishing process was not considered.

The chemical reaction used to deposit silicon:-

$$SiCl_4 + 2H_2 \rightleftharpoons 4HCl + Si$$

is reversible and at the deposition temperature can proceed from right to left by the introduction of hydrogen chloride and use can be made of this reaction for the polishing of the substrate surface. Surface removal of the substrate is obtained by introducing anhydrous hydrogen chloride into the main hydrogen gas stream when the following reactions can occur

$$Si + HCl \rightleftharpoons Si(Cl_x H_Y) + H_2 \text{ for } x > y$$

$$Si(Cl_x H_Y) + Cl_2 \text{ for } x < y.$$

With this process the substrate surface free of mechanical damage and oxide is produced in situ immediately prior to the epitaxial deposition. The rate of removal of the silicon from the substrate can be accurately controlled by the gas concentration and polishing time and unlike the electropolishing method is not a function of the resistivity or conductivity type of the silicon (49).

In practice the use of hydrogen chloride polishing of mechanically polished substrates immediately prior to epitaxial deposition has resulted in almost complete elimination of line defects from the epitaxial layers - Table 5.2, provided no oxidising impurities are present in the gas system. The process is very simple to operate requiring only the controlled introduction of hydrogen chloride into the gas system as the substrates are already positioned and at the temperature for epitaxial deposition. However, the success of the process is dependent on the purity of the anhydrous hydrogen chloride gas and some supplies used in this investigation were not satisfactory because they contained small quantities of oxidising or carbon containing impurities.

7.4.3.1 Identification of Line Etch Figures

The line etch figures have been studied by Finch (50, 51) with the electron microscope and by Schwuttle (52, 53) using the Lang diffraction contrast topography technique who have reported that these defects arise from stacking faults.

A stacking fault in the diamond lattice is produced when an extra (111) plane is inserted into or removed from the crystal and is shown schematically in Figure 7.1. This changes the stacking sequence of the planes from say abcabcabc to abcbcabc, that is over the stacking fault region the symmetry is hexagonal. The lattice on either side of a stacking fault is of identical orientation. The stacking fault can also be considered as a pair of twins on adjacent planes with surface energy of twice that of a single twin boundary. However, it cannot be a single twin because the lattice orientation on either side of this type of boundary is not the same.

A stacking fault is always associated with partial dislocations. When these dislocations on intersecting $\{111\}$ slip planes meet as illustrated in Figure 7.2, the combination of the leading partial dislocation lying in the $(1\bar{1}1)$ plane with that which lies in the $(\bar{1}11)$ plane forms another type of partial dislocation at the junction of the

two stacking fault ribbons by the reaction.

$$\frac{1}{6}\ a\ [\bar{1}\bar{2}1] + \frac{1}{6}\ a\ [211] \rightarrow \frac{1}{6}\ a\ [1\bar{1}0]$$

and is known as a "stair rod" dislocation which is immobile.

The following observations about the defects when examined by thin film electron microscopy were reported:-

1. Diffraction contrast of the type observed is correct for this type of stacking fault.
2. Single faults have been observed to end at partial dislocations.
3. Stair rod dislocations have been observed at the intersection of two faults on different (111) planes.
4. The absence of extra spots on diffraction patterns indicate that multi-twins are not present.

These observations indicate that the faults are stacking faults and the dislocations associated with the stacking fault are defined by the magnitude and direction of slip movement associated with it which is called the Burgers Vector and has been reported (51) for these defects to be a/6 ⟨110⟩.

X-Ray analysis of the defects obtained from changes in diffraction contrast observed in topographs recorded by different Bragg reflections confirm (53) that the triangle faults are stacking faults with their rod dislocations at the corners of triangle with a Burgers Vector of a/6 ⟨110⟩.

7.4.3.2 Mechanism of Growth of the Stacking Faults

For describing the growth mechanism for the stacking faults observed in epitaxial layers, the simple stacking sequence of (111) layer in the face centred cubic lattice abcabc ... etc has been used rather than the more complex stacking sequence of the diamond lattice aa'bb'cc' aa'cc'cc' .... etc. The validity of such a procedure when dealing with

crystallographic imperfections in the diamond lattice has been demonstrated by Hornstra (54).

It is assumed that the vapour deposited epitaxial layers form by the nucleation and two dimensional growth process and growth occurs by the formation of a number of separate nucleation centres, atoms migrate to the centres causing them to spread laterally and the separate areas join up to form a layer. At some stage either before or after completion of the layer, fresh nucleation centres occur on top of the layer, and the process repeats.

Booker and Sticker (55) have suggested the following growth mechanism for stacking faults. To start with, it is assumed that the stacking sequence is such that the atoms in the surface of a (111) substrate (layer N = 0) are in a type "a" position. Then the atoms of the nucleation centres (layer N = 1) invariably go down in sequence in "b" positions and the whole layer joins in correct sequence. The atoms in the next layer go down in "c" positions and the process continues. Consequently, the resulting epitaxial layer is free from crystallographic imperfections. On the other hand, if one of the nucleation centres goes down in incorrect sequence as a result of surface damage or oxide patches on the surface, a stacking fault occurs on the (111) plane parallel to the substrate - layer interface, the regularity is disrupted, and a defect arises. Let it be supposed that the stacking fault initiating the defect is an intrinsic stacking fault.

In Figure 7.3(a) areas P, Q and R (layer N = 1) are in correct sequence with atoms in "b" positions, while area S (N = 1) is in incorrect sequence with atoms in "c" positions. Since we are dealing with lateral spreading of diamond lattice material over a (111) plane, growth occurs faster along the $[2\bar{1}\bar{1}]$ $[\bar{1}2\bar{1}]$ and $[\bar{1}\bar{1}2]$ directions than along other directions. This characteristic growth behaviour arises because of the particular arrangement of the atoms and bonds in the diamond lattice. Hence, areas P, Q and R spread as equilateral triangles with apexes oriented along $\langle 211 \rangle$ directions and sides orientated along $\langle 110 \rangle$

directions. In particular, one set of apexes point in the $[2\bar{1}\bar{1}]$ direction. On the other hand, the stacking sequence so far for area S is abcac. A consideration of atom models shows that the "c" layer added in this manner has its fast and slow directions reversed. Consequently, area S spreads as a triangle inverted with respect to triangles P, Q and R, i.e. one apex points in the $[\bar{2}11]$ direction. When the separate areas join up, the atoms of area S do not match the atoms of the surrounding areas and so area S is bound by a crystallographic imperfection. The shape of the mismatch boundary depends on the regularity of the growth, and on the positions of the surrounding nucleation centres.

If the boundary is a perfect equilateral triangle - Figure 7.3(b) orientated in the same manner as triangle S in Figure 7.3(a) and no further growth irregularities occur, then the atoms of the second layer (N = 2) take the position shown in Figure 7.3(c). The atoms outside the triangle are in "c" positions and those inside the triangle are in "a" positions. The third layer (N = 3) is shown in Figure 7.3(d). It can be seen that the defect propagates from layer to layer, retains its shape and increases in size. Analysis shows that the defect consists of stacking faults on the three inclined $\{111\}$ planes and a cross section through such a defect is shown in Figure 7.4.

This growth mechanism explains why the defects appear on the (111) epitaxial layer surface as triangles.

7.5 Soft PN Junction Characteristics

Softness of a PN junction means that before avalanche breakdown is reached, a comparatively large reverse current, i.e. in this investigation 1 mA., is flowing through the junction. The collector to base breakdown voltages of devices constructed in the epitaxial layers have shown soft characteristics - Section 6.9.

The soft reverse characteristics of PN junctions can be due to the following factors.

1. Incorrect concentration of impurity atoms in the junction.
2. Defects in the silicon.
3. Surface leakage of the junction.
4. Precipitation of impurities in the junction.

Simultaneously with the processing of the epitaxial material, normal silicon wafers were processed and devices constructed. The device fabricated from the normal material did not have soft collector to base breakdown voltage. This indicates that the concentration of impurity atoms at the base to collector junction was suitable to result in hard breakdown characteristics and that the processing technique does not result in surface leakage.

The cause of softness in the junction could thus be due to (a) defects in the silicon for example the stacking faults or (b) precipitation of impurities.

To detect the possibility of electrical leakage at the stacking fault the surface of the layer was made the cathode in an electrolytic plating cell and examined for preferential deposition of copper at the stacking fault, but none was observed and this observation indicates that electrical leakage does not necessarily occur at the lattice defect caused by the stacking fault (Section 6.10).

With the development of the process it became possible to produce silicon epitaxial material almost free of stacking faults and this was used to produce devices. Sections 6.9.3 and 6.9.4. Because of the different methods used to fabricate devices from material with and without stacking faults a direct comparison of the device characteristics cannot be made. However devices produced in material without stacking faults do not exhibit soft junction characteristics.

These results indicate that the presence of stacking faults in the material results in soft junction characteristics, however no electrica leakage has been detected at an unprocessed stacking fault.

Queisser (56) has investigated the effect of coherent (111) twin boundaries and second order (211) twin boundaries which have a high surface energy similar to that of a stacking fault on the junction characteristics of mesa diodes. The diodes were produced by phosphorus diffusion into the P type substrates and mesa diodes containing the boundaries produced. Diodes produced from the regular material and diodes containing (111) boundaries had hard reverse characteristics, while a high percentage of diodes containing (211) boundaries had soft characteristics. However when this experiment was performed using the gettering conditions of a glass oxide hard reverse characteristics of diodes containing (111) and (211) boundaries were obtained. These results indicate that the softness of the junction is not caused by the structure of the (211) boundary, but could arise from the presence of concentration of impurities at the boundary. The examination of these boundaries by copper decoration and infrared microscope techniques indicated that no decoration was found on the (111) boundary, but there was a tendency for preferential precipitation along the (221) boundaries. Thus this difference in the precipitation at the (111) and (221) boundaries could account for the difference in susceptibility of softness of the PN junctions containing the boundaries.

From these results it is concluded that the stacking faults have an indirect effect, resulting from preferential impurity precipitation at the defects, on device characteristics. Thus in order to avoid devices with soft junction characteristics it is important that material used for device fabrication contains no stacking fault.

7.6 Layer Resistivity

The layer resistivity is a measure of the excess donor or acceptor impurity atoms within the silicon epitaxial layer and these electrically active impurities can arise as follows:-

$$N_{TOTAL} = N_{SYSTEM} + N_{SiCl_4} + N_{SUBSTRATE} + N_{GAS\ PHASE\ DOPING}$$

Where N_{TOTAL} are the total number of impurities in the layer; N_{SYSTEM} the impurities arising from the apparatus, hydrogen carrier gas and susceptor: N_{SiCl_4} impurities from the silicon tetrachloride; $N_{SUBSTRATE}$ impurities arising from the substrate and $N_{GAS\ PHASE\ DOPING}$ impurities deliberately introduced into the gas phase.

In this investigation the contribution of $N_{SYSTEM} + N_{SiCl_4}$ to N_{TOTAL} was estimated by growing layers on 1,000 ohm cm P and N substrates from intrinsic silicon tetrachloride (Section 6.6) and the results indicate that these variables do not contribute significant active impurities to the layer.

The contribution of impurities from the substrate is more significant and results from layers grown on substrates of both conductivity type with different resistivities and various doping elements - Section 5.7 - indicate that (A) the substrate has increasing effect on the layer resistivity and type as the substrate resistivity decreases (see Table 5.5 and Figure 5.23) and (B) the layer resistivity is effected by the N type doping element in the substrate and that the elements have decreasing effect in the order phosphorus, arsenic and antimony - Table 5.4.

The combined effect $N_{SUBSTRATE} + N_{GAS\ PHASE\ DOPING}$ is shown in Figures 6.5 and 6.6. These results indicate that the impurities in the substrate can contribute significantly to the total impurities in the layer and suggests that the impurities are transferred to the growing layer.

Grove (57) has made a theoretical investigation of the effect of diffusion, which is inherent in the process because of the high temperature of the deposition reaction, on the impurity distribution within the layer. Using a theoretical model of regular solid state diffusion and a constant diffusion coefficient the calculations indicate that with high layer growth rates the epitaxial layer will always be infinitely thick in comparison to the extent of the region effected by solid state diffusion. The theoretical result using the commonly accepted

diffusion coefficients have been compared with experimental results of the impurity profile near the substrate - layer interface obtained with the differential capacitance method and were found to be in agreement, indicating that the impurity distribution follows the predictions of simple diffusion theory.

Diffusion can account for the difference between the metallurgical and PN junctions observed for P layers on 1.0 and 0.01 ohm cm N substrates and N layer grown on 1.0 ohm cm P substrates (Figures 6.5 and 6.6) but does not account for the following observations made in this investigation

A. almost the complete absence of N layers grown on 0.01 ohm cm P substrates - Figure 6.6,

B. the quantity and type of impurities contained in the thick layers over 20 microns produced in this work to observe the influence of the substrate on the layer,

C. the reduction in transfer of impurities from a highly doped substrate to the layer by sealing the back side of the substrate with silicon dioxide or a film of lower doping material,

and D. the effect that substrates positioned near the gas inlet can have on layers grown on substrates positioned near the gas outlet in a multideposition system.

A further process known as autodoping which involves the reverse of the deposition reaction, i.e. the reaction used for substrate polishing could account for these observations. In this process it is assumed that:-

1. Silicon and dopant impurities are removed from the solid at a rate proportional to their concentration at the solid surface as a result of chemical species associated with etching characteristics in the overall deposition reaction and that no preferential etching of silicon or dopant occur.

2. The gas phase composition during the reaction is modified by mixing with the incoming gases of hydrogen, silicon tetrachloride and dopant impurities.
3. Silicon and dopant atoms are then deposited in proportion to their concentration in the modified gas phase and corrected as necessary for differences in dopant efficiencies.

Thomas (58) has proposed a theoretical model of this process and the results are in reasonable agreement with experimental data. This process can account for the following:-

A. the variation of resistivity of layers grown on different resistivity substrates (Table 5.5) arises because of the difference in number of impurity atoms etched from the deposition surface and available for redeposition,

B. the variation in layer resistivity on substrates of the same resistivity, but doped with different elements (Table 5.4). This arises because the redistribution of dopant impurities is dependent on their deposition efficiency and has been reported by Nuttal (44) for PCl_3 and $SbCl_3$ to be in the ratio of 1 to 0.03 and this is in agreement with the observations that auto doping is less pronounced on antimony doped substrates,

and C. The doping concentration is found to decrease with distance from the substrate as indicated by increasing breakdown voltages of devices produced from layers of increasing thickness (Table 6.4).

From these investigations it is concluded that the combination of the two processes, diffusion and autodoping, results in the transfer of impurities from the substrate to the layer. The effects of diffusion in

the final layer will be more predominant at the layer/substrate interface and autodoping will be more predominant away from the interface. The transfer of impurities by these processes will be greater for lightly doped layers grown on substrates of high doping concentrations. The processes will also have an effect on the impurity profile of the grown junction ranging from abrupt step junctions to graded junctions, but no detailed investigation of junction profiles has been made in this work.

In theory the process of diffusion and autodoping can be minimised by (A) lowering the deposition temperature, (B) increasing the growth rate, (C) using dopant impurity elements in the substrate with low diffusion coefficients and low deposition efficiencies and (D) by the use of a non-reversible chemical reaction to produce silicon.

In practice reducing the deposition temperature will lower the nucleation rate R_N which will result in layers with a rough regular surface and thus growth is made at the lowest temperature consistent with growth of the crystal lattice with a high degree of perfection. Similarly the growth of the layer is made at the maximum rate which results in a flat defect free surface.

The use of substrates containing impurity doping elements with low diffusion coefficients is limited practically because of the limited doping elements available (see Table 7.1) and the problems associated with producing single crystal with impurities of low segregation coefficient and the inability to easily grow single crystal from the melt containing the required quantities of dopant impurities. For N type material it is possible to use antimony which has one of the lowest diffusion coefficients and a low deposition efficiency, but single crystals cannot be grown from the melt containing more than 2% of impurities, thus preventing antimony doped substrates containing impurity concentrations greater than 10^{19} atoms per c.c. For P type material only boron with a relatively high diffusion coefficient is available. Indium and thallium have lower diffusion coefficients while indium has

a very low segregation coefficient and hence indium doped silicon single crystals cannot be produced from the melt. No details of the segregation coefficient of thallium has been published.

It should also be possible to eliminate autodoping by using a non-reversible silicon deposition reaction such as the pyrolytic decomposition of silane - Section 2.2. With this process the temperature of deposition is again limited by the nucleation rate and found to be similar to that of silicon tetrachloride (61, 62) and it has been reported (63) that some interaction occurs although to a lesser degree between the substrate and the layer.

7.7 Impurities in the System

Impurities in the gas system can be classified into two groups (A) Macro impurities which are associated with the nucleation and growth of the layer and (B) Micro impurities which are incorporated into the growing crystal lattice and associated with the electrical properties of the layer.

The most important Macro impurities in the gas system are those containing molecular or combined oxygen and result in the formation of oxide at the silicon surface. Thin oxide layers produce steps, the height of which may not be equal to an integral multiple of the lattice spacing and result in the layer growing round the oxide inclusion and maintaining its coherence by the formation of stacking faults (51) - Figure 6.3. Thicker oxide layers reduce the number of steps available for nucleation and result in the nucleation and growth of polycrystalline films. Carbon is another impurity which has been detected in the gas system and has been found to result in the formation of protruding imperfections - Section 6.3.

The micro impurity atoms - boron as an acceptor and phosphorus, arsenic and antimony as donors are deliberately incorporated into the growing layer via the gas phase or by solid state diffusion or autodoping to control the conductivity of the layer.

However other impurities which have a detrimental effect on the layer electrical properties have been detected. The comparison of the gain characteristics of transistors (Section 6.9.4) indicate that some transistors have low gain characteristics which were associated with low life time material which is due to a higher level of electrically inactive impurities. Mass spectrometer analysis - Table 6.3 - indicated the presence of transition elements in the layers but not in the substrate. Further investigation revealed that these impurities were arising at the PTFE manifold (Figure 3.11) which is the terminal for the stainless steel and quartz gas lines. Examination indicated that the hydrogen chloride gas and silicon tetrachloride gas flowing through the PTFE manifold were absorbed by the PTFE and during the long periods of no gas flow through the manifold, the absorbed gases diffused around the manifold and reacted with the stainless steel gas lines forming the chloridesof the transition elements which were eventually transferred to the reaction zone, chemically reduced and incorporated in the growing lattice.

By replacing the PTFE manifold with a quartz manifold and changing the gas flow to produce a continuous nitrogen or hydrogen purge it has been possible to reduce the concentration of transition impurities in the layer - Table 6.3 - resulting in an improvement in the lifetime of the material and the associated gain characteristics of the devices.

It is also possible that other impurities which have not been detected are incorporated into the growing lattice. The gases in particular can be sources of impurities. The main hydrogen gas is only purified to 1 ppm level for oxygen and water vapour, while it is not possible to purify the doped gases. The main hydrogen and hydrogen doped gas are from the same supply and known to contain small quantities of carbon dioxide, carbon monoxide, nitrogen, oxygen and water vapour. Although their concentration at the substrate surface is insufficient to effect the nucleation carbon, oxygen or nitrogen could be incorporated in the growing layer.

7.8 Processing of Material over a Limited Period of Time

The analysis of the results - Table 6.15 - to produce epitaxial substrates over a period of time indicated a variation in layer thickness of ±18.5%. Such a large variation in layer thickness may be tolerable for producing XP6 epitaxial planar transistor type structures where the device is fabricated within the high resistivity layer and the low resistivity substrate acts as a support for the layer. For a device of the XH6 Epitaxial Homogeneous Base Transistor type, where the epitaxial layers form part of the device structure, the layer thicknesses are critical for the device characteristics and variations of ±18.5% are not acceptable in order to produce devices with consistent characteristics.

TABLE 7.1

Silicon Doping Elements, Diffusion Coefficients and Segregation Coefficients

Group	Doping Elements	Type	Diffusion Coefficient CM^2 per sec (59)	Segregation Coefficient (60)
3B	Boron B	P	7×10^{-12}	8.0×10^{-1}
3B	Aluminium Al	P	3.8×10^{-11}	2.0×10^{-3}
3B	Gallium Ga	P	1×10^{-11}	8.0×10^{-3}
3B	Indium In	P	2.5×10^{-12}	4.0×10^{-4}
3B	Thallium Tl	P	2.5×10^{-12}	-
5B	Phosphorus P	N	7×10^{-12}	3.5×10^{-1}
5B	Arsenic As	N	7×10^{-13}	3.0×10^{-1}
5B	Antimony Sb	N	5.5×10^{-13}	2.3×10^{-2}
5B	Bismuth Bi	N	6.0×10^{-13}	7×10^{-4}

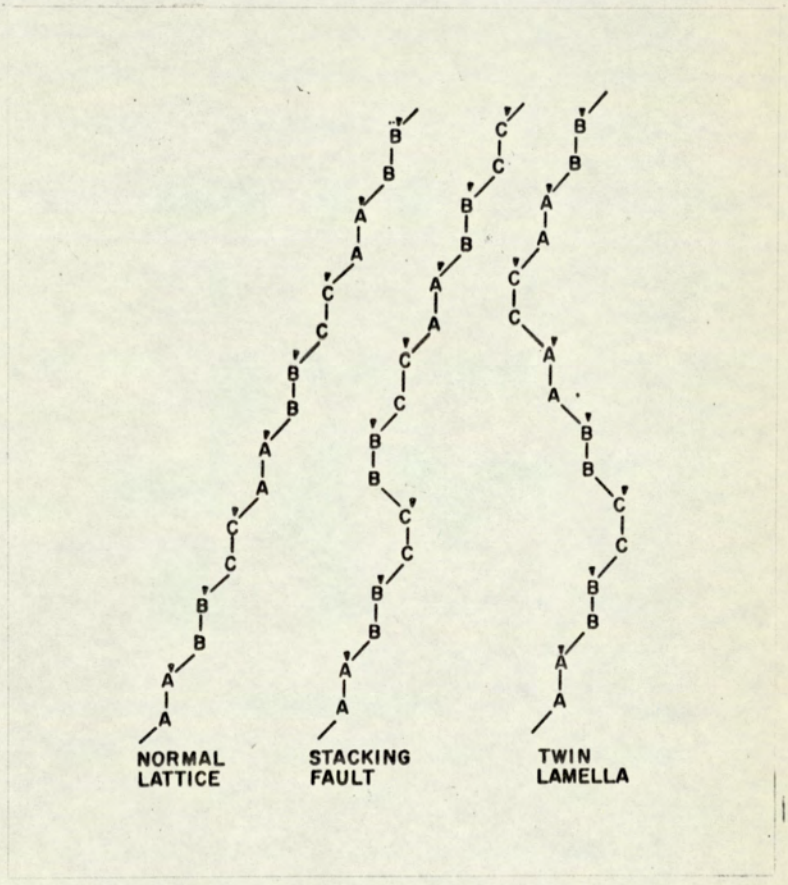


Fig. 7.1 Defects in the diamond lattice

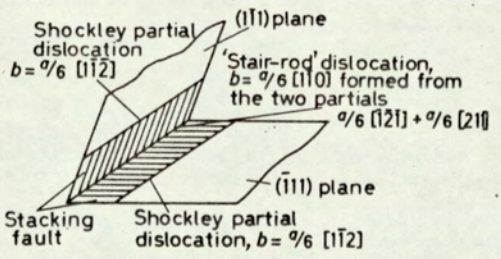
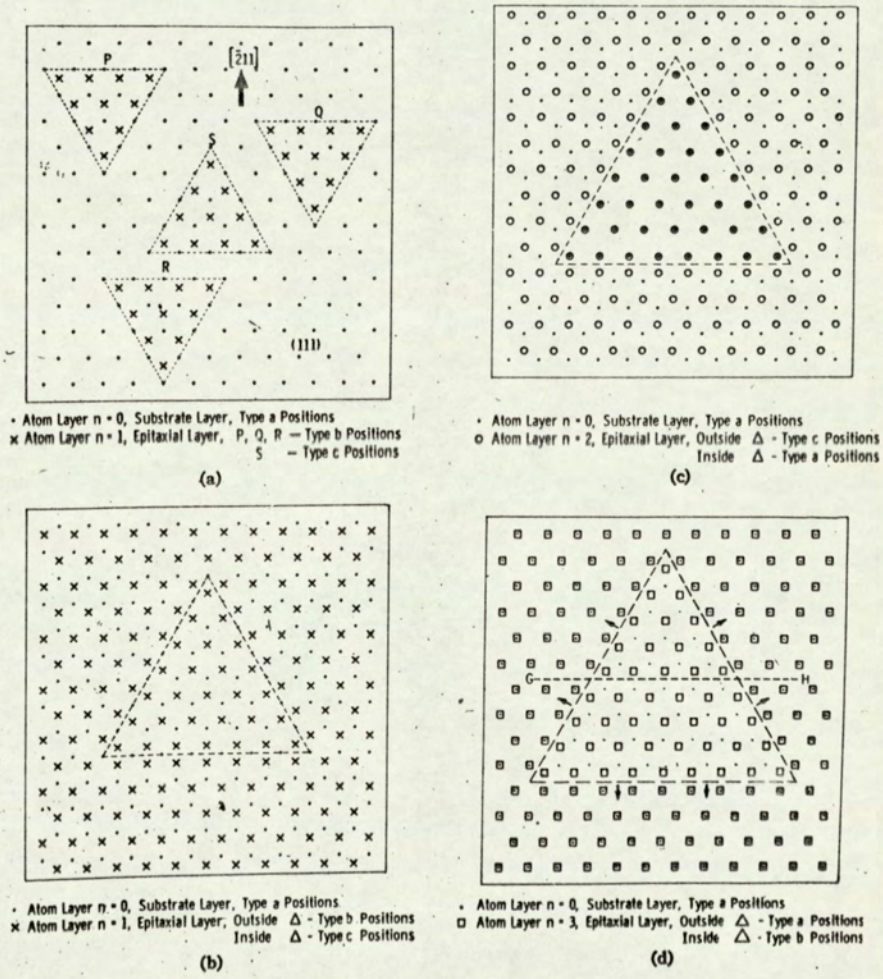


Fig. 7.2 Formation of a stair rod dislocation



Schematic diagrams showing successive stages in the formation of a triangle defect. (a) Nucleation centers go down at P, Q, and R in correct sequence, and at S in incorrect sequence. (b) Completion of first layer. It is assumed that the mismatch boundary takes the form of a perfect equilateral traingle. (c) Completion of second layer. The mismatch boundary has moved outwards on all three sides. (d) Completion of third layer. The movement continues.

Fig. 7.3 Schematic diagrams showing successive stages in the formation of a triangle defect

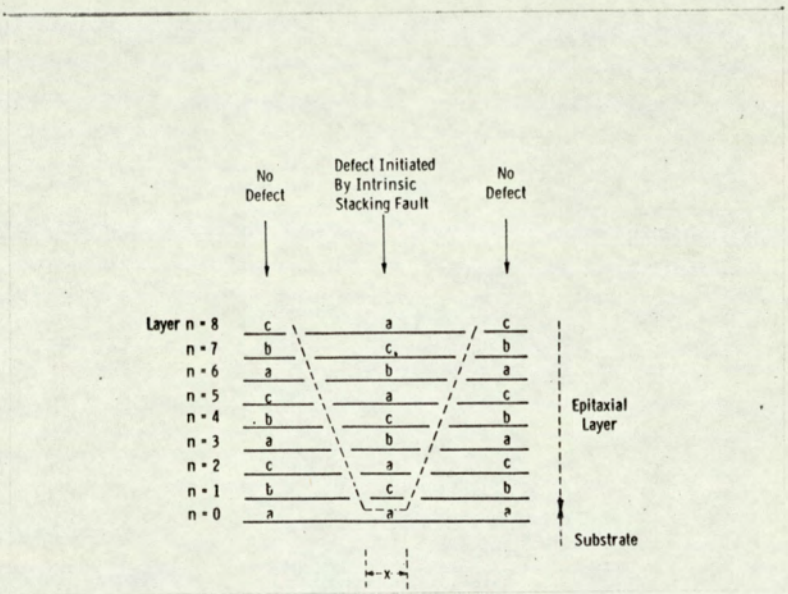


Fig. 7.4 Cross section through the defect of Fig. 7.3(d) corresponding to the line GH. The defect is initiated by a stacking fault on the (111) plane parallel to the substrate, and then propagates as stacking faults on the three inclined {111} planes. The defect has the form of a regular tetrahedron.

8. CONCLUSIONS

8.1 Silicon Layers

Single crystal silicon layers of a quality suitable for transistor fabrication can be grown by nucleating silicon, produced by the hydrogen reduction of gaseous silicon tetrachloride, onto substrates at approximately 150°C below the silicon melting temperature.

8.2 Layer Thickness

The layer thickness is a function of the growing time, while the layer uniformity is dependent on the gas flow velocity, composition, and the reaction system geometry. By using a high velocity gas flow almost parallel with the substrate surface and slightly tilting the substrate into the gas flow, simultaneously grown layers of uniform thickness can be produced on a number of substrates. For a series of deposition runs the reproducibility is $\pm 18.5\%$ and this degree of control over a period of time can be satisfactory for devices of the type that have the complete transistor structure fabricated within the layer; however, when the transistor base and collector regions are epitaxially fabricated, a wide variation in transistor characteristics will be expected.

8.3 Layer Resistivity and Conductivity Type

The layer conductivity type and resistivity are a function of the deliberately introduced impurity atoms from the gas phase and the contribution of impurities from the substrate resulting from diffusion and autodoping. By the selection of a substrate containing a low concentration of impurities i.e. high resistivity or impurities with low diffusion coefficients and low deposition efficiencies, the impurities from the gas phase become the predominant factor controlling the layer type and resistivity.

8.4 Crystal Perfection

The nucleation and growth of the layer is dependent on the

deposition temperature. For layers of high lattice perfection, the deposition temperature should be as high as possible while the opposite is required to minimise the transfer of doping impurities from the substrate to the layer. In practice, a deposition temperature of approximately 1250°C is used which is the minimum temperature to produce an epitaxial layer with a flat mirror surface.

Two important types of lattice defects have been observed in the epitaxial layer (a) edge dislocations as delineated by etch pits and (b) stacking faults. The concentration of etch pits in the layer is related to the concentration originally in the substrate and can be minimised in the epitaxial layer by use of low etch pit substrate material. Stacking faults generally originate at the substrate layer interface as the result of surface damage or the presence of oxide impurities on the substrate surface. The stacking faults result in a soft collector to base breakdown voltage of devices produced in layers containing them. However, by (a) ensuring that oxidation of the substrate surface cannot occur during processing, by eliminating oxidising impurities from the system, and (b) gaseous etching the substrate surface with anhydrous hydrogen chloride immediately prior to epitaxial deposition it is possible to practically completely eliminate stacking faults from the layer.

8.5 Measurement of Layer Thickness

Two types of layer thickness can be measured: (a) the thickness as measured from the metallurgical interface between the substrate and layer, and (b) the thickness as measured from a boundary between different types of impurities or concentration of impurities. The former can be measured by the stacking fault method and the latter by angle lapping and delineation of the boundary or with the infrared interference method. In practice it has been found that when layers are grown on 0.01 ohm cm antimony doped substrates from intrinsic silicon tetrachloride, the metallurgical and impurity boundaries are

very similar and use is made of this agreement for the calibration of the growth rate in the apparatus by measuring the layer thickness with the non-destructive infrared method.

8.6 Measurement of Layer Resistivity

The resistivity of layers of opposite type to that of the substrate can be measured by the four point probe method, because of the effective isolation of the junction. However, for device fabrication a high resistivity layer on a low resistivity substrate of the same type is required. The resistivity of these layers can be measured within certain conditions non-destructively by the three point probe method. Nevertheless, this method is only satisfactory if the layer thickness is greater than the depletion layer width at the breakdown voltage of the point contact diode. Destructively the layer resistivity can be obtained from capacitance measurements of a shallow PN junction, formed in the layer, while this method can also determine the impurity concentration profile through the layer section.

In order to monitor the resistivity of layers grown on substrates of the same type, a monitoring substrate of opposite type to the layer and containing the minimum of impurities to effect the layer is processed simultaneously, and from which the layer resistivity can be obtained by the four point probe method. This does not give an absolute measure of the layer resistivity but does provide a method for monitoring or changing the layer resistivity.

8.7 Impurities in the Layer

Impurities in the layer can be of two types: (a) Macro impurities effecting nucleation such as oxidising impurities which result in the formation of stacking faults or inhibit epitaxial nucleation and carbon which can initiate the growth of surface protruding imperfection, and (b) Micro impurities which are incorporated into the growing crystal lattice. Certain impurities are deliberately introduced to control the layer type and resistivity. Other impurities of the transition elements

have been detected in the layers and were found to originate from within the apparatus and to effect the lifetime of the layer and hence the gain characteristics of the transistor.

8.8 Procedure for Producing Epitaxial Layers

In practice substrates are prepared from a single crystal pulled from the melt because of its lower dislocation density and doped with antimony for N type material and boron for P type material. Each deposition system has its own peculiarities and the process is empirically calibrated. The layer growth rate is calibrated against time for the main hydrogen gas flow together with the silicon tetrachloride temperature and hydrogen flow, and the doped gas flow rates are calibrated for layer resistivity. These calibrations are specific for the process conditions of gas flows and substrate properties which are used to produce the layer, and any change in a process parameter will require recalibration of the system.

High resistivity 1-20 ohm cm N layers have been grown on low resistivity 0.01 ohm cm N substrates. By introducing impurities of different type or concentration into the gas stream consecutive layers of different type or impurity concentration can be grown which result in the formation of PN junctions.

8.9 Suggested Future Work

The following have not been investigated in this work:-

1. the impurity profiles of layers and PN junctions,
2. the degree of variation of layer resistivity over a period of time,
3. the effect on the device characteristics of eliminating gaseous impurities present in the hydrogen by the use of a hydrogen palladium diffusion unit.

These problems offer scope for further investigations of the

process together with further development to produce layers of uniform thickness over a period of time.

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