NUMERICAL MODELLING OF MULTILAYER SEMICONDUCTOR DEVICES:

An investigation into reverse recovery voltage snap-off in snubber diodes

BY

Peter Thomas HOBAN
Master of Philosophy

THE UNIVERSITY OF ASTON IN BIRMINGHAM

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1. SUMMARY

The classic paper by Somos has shown how abrupt recovery occurred in alloyed semiconductor diodes, but had postulated that the commutation of diffused diodes may differ dramatically. This was confirmed by other workers. Diffused soft recovery diodes are now in general use. My investigations have shown that diodes can change their recovery characteristics and produce snap-off phenomena. Diode snap-off can be dangerous as it may lead to the destruction of the device and thus to circuit failures. Previously soft-recovery diodes were thought to be immune from this effect.

Prior to this thesis the only method of determining if a diode would be prone to snap-off was by extensive experimental investigations. Such investigations have provided the information required to construct a simple model that will predict the operating conditions under which snap-off will occur.

The experimental data indicated that the shape of the carrier density profile during commutation influenced the recovery characteristic. Existing analytical models of diode carrier profile and junction capacitance were therefore used to explain the diode behaviour. Calculations of diode capacitance during switching and a simple derivation describing capacitance variations, indicated that the propagation of the depletion layer could explain this snap-off effect. Because the diode capacitance and space charge region can be represented by Poissons equation, it was thought that the solution of this equation coupled with the carrier continuity equations would provide a method of predicting when snap-off would occur. The suitability of the finite element method as a solution strategy was investigated and various iterative methods, matrix ordering techniques and convergence considerations were studied. In addition the previous work of Benda and Spenke, plus Schunemann and Muller was used to identify which physical parameters were dominant during switching. This work showed that no easy simplifications could be made and therefore this increased the required complexity of the prospective FEM model. The conclusion derived was that a FEM model was more suited to investigating and analysing the diode snap-off mechanism, and less suited for circuit simulations and predictions. A SPICE model was therefore used (in collaboration with other workers) to predict the effects of diode snap-off in a GTO circuit. A diode snap-off model based on empirically derived equations is suggested as a method of determining when snap-off will occur. At the time of writing the author knows of no other prediction technique suitable for simulating voltage snap-off in high power, high voltage snubber diodes used in practical GTO inverters.

KEY WORDS

1. High Voltage snubber diodes
2. Diode reverse recovery snap-off
3. Numerical modelling
4. Circuit simulations
5. Transient analysis

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2. INTRODUCTION

2.1 Foreword

The classic paper by Somos [5] has shown how abrupt reverse recovery in alloyed semiconductor diodes could produce voltage spikes. Such spikes can be dangerous as they may lead to the destruction of the device and thus to a circuit failure [6]. It was postulated by Somos that the recovery of diffused diodes [66] may differ dramatically from that of alloyed devices [93, 98]. This assertion has been confirmed by other workers [44, 90, 93]. Diffused diodes are now designed with a soft recovery characteristic. This type of recovery is essential in modern day high stress switching circuits.

The rapid development in semiconductor technology has produced a dramatic increase in the voltage, current and power handling capability of individual devices. Device/circuit interactions have now become so complex that traditional circuit and device descriptive equations may, under certain circumstances, no-longer adequately describe the high speed transient behaviour of the total device/circuit system. My research has identified conditions under which diffused soft recovery diodes can change their recovery characteristic and produce dangerous voltage spikes associated with a discontinuity in the current waveform known as current chop-off. Such discontinuities in the current waveform have been reported in alloyed [5], P-i-N [88] and Gold doped [96] devices. However, modern diffused soft recovery diodes were previously thought to be immune from this effect.

This thesis will demonstrate that soft-recovery diodes may be operated in either a safe or an unsafe mode. The mode of operation is determined by a combination of environmental conditions, device structure, operation parameters and external circuit component values.

The design of many present day GTO circuits has not taken into account the presence of a safe performance envelope [45,129] for snubber diodes. Consequently such circuits may run the risk of in-service failure.

Prior to this thesis the only method of determining if a diode operating under high stress conditions in a complex circuit would be prone to generate excessive voltage excursions was by extensive experimental investigations. To ensure safe operation of devices in service and yet avoid the costly and time consuming experimental programme that this would require, the possibility of establishing computer based numerical models which could then be used to simulate in-service conditions was therefore investigated.

My experimental studies have provided the information required to construct a simple model to predict the operating conditions under which snap-off will occur. These results and the new methods of experimental analysis that were pioneered to catalogue this effect have been published [45].

The experimental data indicated the shape of the carrier density profile during commutation was responsible for snap-off. Existing analytical models of diode carrier profile and junction capacitance were used to explain the diode behaviour. Calculations of diode capacitance during switching and a simple derivation describing capacitive variations, indicated that the propagation of the depletion layer [50,93,94] could explain the current chop-off [88] effect. Because the diode capacitance and space charge region can be represented by Poisson's equation, it was thought that solution of that equation [38, 57, 115, 132] coupled with the carrier continuity equations would provide a method of predicting when snap-off would occur. The suitability of the finite element method [84, 87, 151] as a solution strategy and various iterative methods, matrix ordering techniques and convergence considerations were studied. In addition the previous work of Benda and Spenke [50] plus Schunemann and Muller [95] was used to identify which physical parameters were dominant during switching. This work showed that no easy simplifications could be made and therefore this increased the required complexity of the prospective FEM model. The task of writing computer code to adequately describe the 3-D problem, coupled to an external circuit, time discretised and temperature sensitive proved to be extremely arduous. The conclusion derived was that a FEM model was more suited to investigating and analysing the diode snap-off mechanism and less suited for circuit simulations and predictions.

A SPICE model was therefore used (in collaboration with other workers [46]) to predict the effects of diode snap-off in a GTO circuit. A diode snap-off model based on empirically derived equations is suggested as a method of determining when snap-off will occur. This method uses a curve fitting technique to produce descriptive equations of device performance.

Substitution of an operating parameter into a general equation provides a test that can be made on the operating condition of the device. At the point when the diode 'snaps-off' the current waveform can be predicted using a constant charge relationship. By assuming the diode to be a current generator the L.dI/dt overvoltage can then be calculated. At the time of writing the author knows of no other prediction technique suitable for simulating voltage snap-off of high power, high voltage snubber diodes used in practical GTO inverters.

Some of the results of this study have been published and were instrumental in assisting the development of a new generation of megawatt inverters [46].

It is intended that this thesis will be of interest to readers from a number of disciplines, such as Mathematics, Physics and Engineering. The purpose of this section is therefore to acquaint the reader with some background information on the mathematical modelling process, on device theory and on the practical circuits that will be simulated. A knowledge of the systematic approach I have employed will assist the reader in understanding the structure of this thesis. The introductory material on devices and circuits should give the reader some knowledge of the reason for, and operating environment of, snubber diodes. In addition the reader will also note that the background information on devices is presented as a series of device descriptions, starting with a simple diode and progressing to a GTO. This step by step progression from simple to complicated devices is mirrored in the structure of the SPICE model (to be described in Section 5). In such a SPICE model complicated devices can be represented by a combination of simple devices and circuit components to produce an equivalent circuit [69] of the device to be modelled.

2.2 The mathematical modelling process

Throughout this project a systematic approach to modelling was implemented. A mathematical modelling process was used which described the physical problem in terms of mathematical formulae which were then used to make predictions. This procedure was divided into a number of sequential steps. These were:-

(a) Problem identification.

(b) Formulation of the problem into mathematical terms.

(c) Formulation of a solution strategy applicable to the mathematical formulae produced in (b).

(d) Implementation of the preferred solution technique.

(e) Interpretation of the solution.

(f) Implementation of the verified model to make predictions and simulate device/circuit performance.

In this case the modelling process commenced with some unusual experimental data. Thus the starting point of the model was a set of empirical results that were not fully understood. In this real situation the problem was therefore undefined which precluded a clear statement of what was happening. Consequently although stages (e) and (f) were important for an engineering solution, the most time consuming portion was stage (a) which involved skills unrelated to mathematics. The rationale for this being, it is difficult to simulate an unexplained phenomenon. Thus a large portion of this thesis is devoted to experimental investigations (see section 3). At this stage the essential problem features were separated from those that were irrelevant. Thus engineering and scientific skills along with a relevant literature search were important features of this modelling exercise.

One aspect that was considered was that of the model purpose.
It is unlikely that any one model type can adequately fulfil both an analytical and simulation role and therefore choices must be made as to the preferred model type. In this project the primary aim was to simulate the device/circuit

system and to predict the occurrence of dangerous voltage excursions. Consequently the model type and solution method was chosen to fulfil this goal.

The constructed model was then validated and its results interpreted. Validation of the model was achieved in two parts. Firstly the mathematics used was as far as possible self consistent. Secondly the results were made to duplicate performance in the real world. Thus when experimental and predicted results were not in adequate agreement a modification to the model was initiated and the modelling process repeated.

Implementation was the final part of the model development. In computer modelling this essentially consists of developing a software package.

The relative importance of steps a, b, c, d, and e, showed that there is a considerable amount of 'art' involved in mathematical modelling which rendered experience more important as the complexity of the model increased.

2.3 An overview of the device/circuit problem

The rapid development in semiconductor technologies and novel gate structures has produced a dramatic increase in the voltage, current, power handling and frequency capability of individual devices [128]. Use of such devices at their improved rating produces high stress conditions within the device/circuit system. These high stress conditions invariably produce problems not associated with the operation of generically similar but lower rated devices. The complexity of such device/circuit equations has now reached the stage where, under certain circumstances traditional circuit and device equations may no-longer adequately describe the high speed transient behaviour of the total device/circuit system.

Since analytical prediction techniques have in the past proved inadequate, potentially dangerous voltage excursions (such as those in GTO circuits) must be investigated by experimental techniques that have become increasingly difficult to apply, expensive and time consuming. It has become obvious

therefore that this urgent need for cost reducing prediction techniques could be satisfied if a better understanding of the transient behaviour of even the most simple semiconductor devices (such as P^+. N and P.i.N diodes) was obtained. This urgent need could be achieved by using the type of sophisticated numerical simulation that has proved so cost effective and reliable in low power, large scale integration (LSI) applications. However, since the solution of the non linear partial differential equations describing the intrinsic behaviour of these power devices requires a different approach to that of the low power device structures in LSI, considerable software development is required to gain the cost benefits of such a simulation approach. Such software development has been mentioned in many papers in the form of results gained from computer programmes. However, the commercial value of such programmes has prohibited the availability of detailed code listings. Such work may however, be categorised as either specific or general.

The nature of specific models dealing with leading edge technology renders them difficult to apply to devices for which they were not originally written and general purpose codes are almost certainly too simple for in depth analysis of complex device behaviour. In addition most published software suffers from the disadvantage of being based upon equations that describe processes adequately under steady state conditions but inadequately under high stress transient conditions. The arduous task of applying such models to alternative problems is therefore so great as to necessitate some software development.

2.4 Background information on devices and circuits

2.4.1 Semiconductor devices

Semiconductors are materials which at room temperature have a resistivity (10^{-4} to 10^{7} ohm.m) between that of conductors (10^{-8} ohm.m) and insulators (10^{12} to 10^{20} ohm.m). The resistivity of the majority of metals can be explained by the free electron theory of conductivity [227] in which certain electrons are free to move through the lattice structure under the influence of an electric field. This theory can not be applied to semiconductors because the

presence of two types of charge carriers [52] has a significant effect on semiconductor resistivity. These two carrier types are electrons (-ve) and holes (+ve). In intrinsic semiconductors, electrons can be thermally excited into the conduction [226] band leaving an equal number of vacancies (or holes) in the valence band. In very pure semiconductor material (known as intrinsic material [54]) the number of holes is equal to the number of electrons. Since the number of charge carriers in intrinsic material decreases with decreasing temperature, at low temperatures there are few thermally generated carriers. This results in a high resistance at low temperatures. In contrast metals show a reduction in resistance at low temperatures since the number of charge carriers is not reduced but their motion is impeded less by a reduction in lattice vibrations.

The introduction of dopant impurities into an intrinsic semiconductor can result in either a p-type (excess of holes) or n-type (excess of electrons) semiconductor. The interface that is formed between a P-type and an N-type semiconductor is known as a PN junction [1] (see figure 1 (a)). The current-voltage relationship of a PN junction under forward bias conditions obeys a theoretical equation known as the Shockley equation [64].

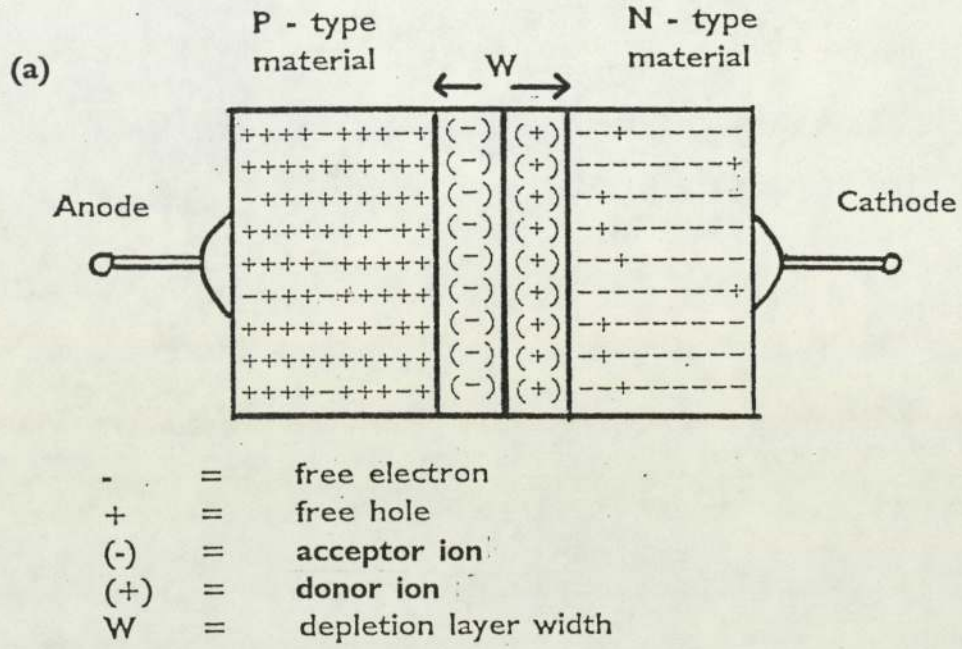
$I_d = I_o . \{\exp (e.V/k.T) - 1\}$ ..... Shockley equation -(E1)

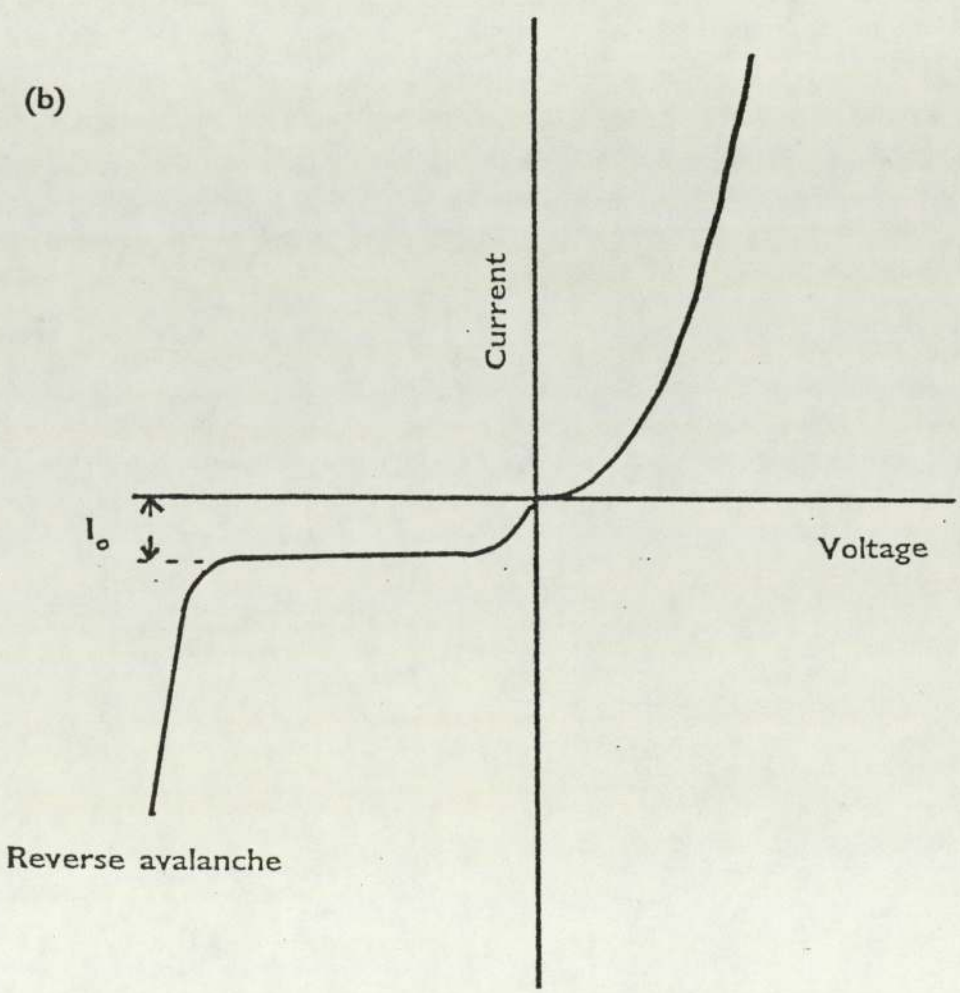
where e = Electronic charge
V = Applied voltage
k = Boltzmann constant
T = Absolute Temperature (degrees Kelvin)
I_o = Reverse saturation current
I_d = Diode current

The characteristic curve shown in figure 1 (b), shows that the PN junction has an asymmetric current carrying characteristic that will allow significant current to flow in one direction only. The physical basis of this empirical formula can be seen by reference to the band theory of solids [226, 227, 228].

FIGURE 1

(a) Diagram of a PN Junction
(b) Plot of the V-I Characteristic of an ideal PN Junction





This feature of allowing the flow of significant current in one direction only is very useful, causing the majority of diodes to be used in rectification processes where ac is converted to dc. Hence diodes are sometimes known as rectifiers.

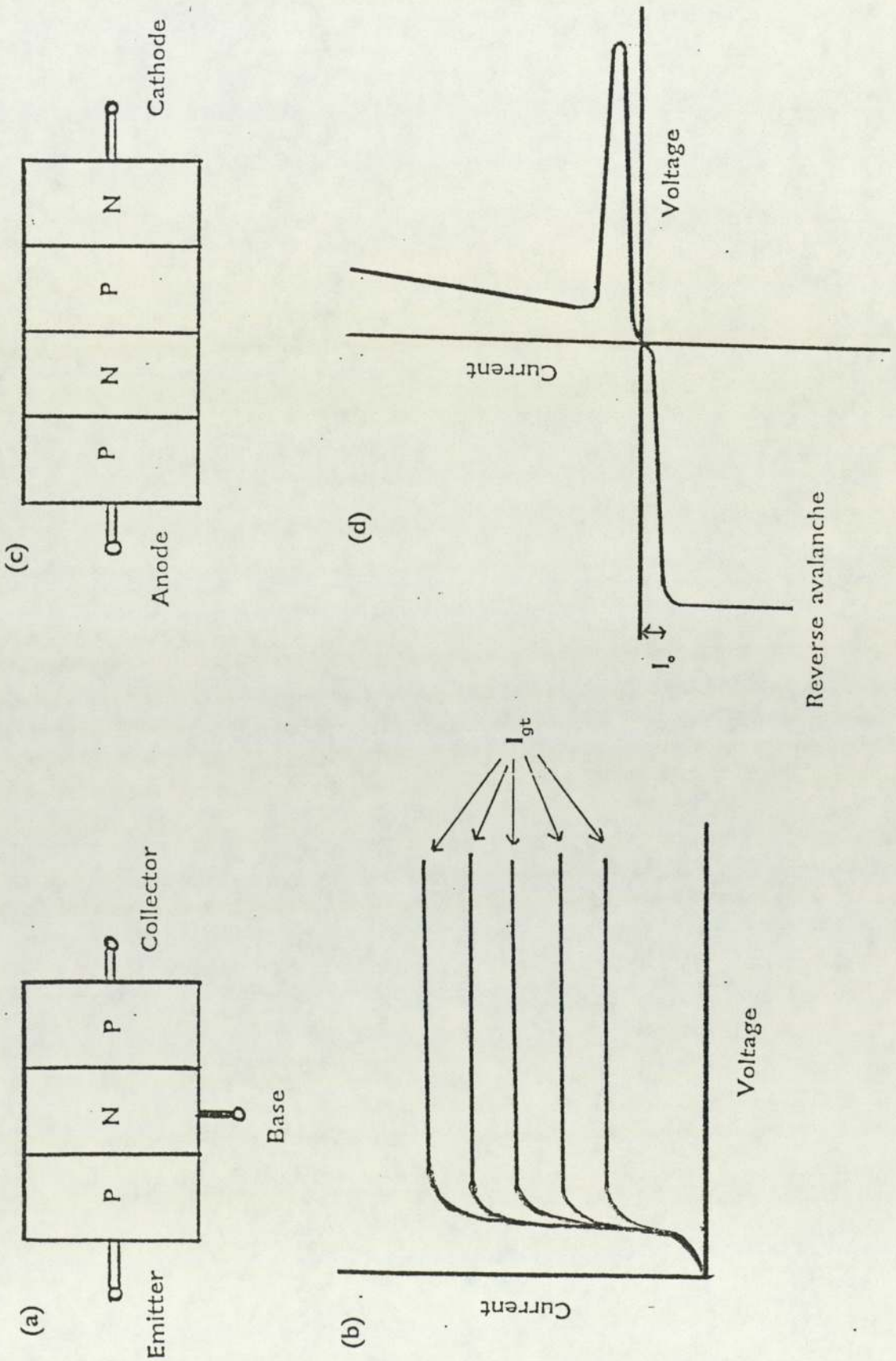
2.4.2 **Semiconductor switches**

The addition of a third layer of doped semiconductor material to a PN junction produces either a PNP or a NPN structure. These three layer devices are known as bipolar junction transistors [1]. Each transistor consists of one PN and one NP junction in close proximity. They are three terminal devices as shown in figure 2(a). The electrodes (terminals) are called the base, the collector and the emitter. If a voltage is applied across the transistor, one junction becomes forward biased the other becomes reverse biased. Current flows across the forward biased junction and into the base region where the charge carriers then diffuse over the reverse biased junction. Once they enter the depletion layer associated with this junction they are swept across into the collector region. The application of a suitable voltage to the base region ensures the forward biased junction remains forward biased and allows current to continue to flow across the device. The removal of a bias to the base region allows the carrier concentration in the base region to fall reducing the forward bias across the forward biased junction and eventually prevents significant current flow. Thus the three terminal device can be used as an on/off switch. Figure 2(b) shows the I-V characteristic of this device.

A four layer device (e.g PNPN) has a total of three junctions. A diagram of this construction is shown in figure 2 (c). Such a PNPN device is called a dynistor, a switching diode or a Shockley diode [229,236]. Its switching function is controlled by the anode Voltage V_a. Increasing the externally applied anode voltage, forward biases the two PN junctions and reverse biases the NP junction causing the NP junction to hold off all of the potential drop across the device. If V_a exceeds the break over voltage, V_{bo}, determined by the NP junction, the diode is turned on since the NP junction becomes driven into a reverse avalanche conduction mode. Once such a four layer diode has been turned on it will remain conducting until the forward current falls below a

FIGURE 2

(a) Diagram of a **PNP** device.
(b) Plot of V-I characteristic of a **PNP** device.
(c) Diagram of a **PNPN** diode.
(d) Plot of V-I characteristic of a **PNPN** diode.



holding current value at which time the diode turns off. The I-V characteristic of this device is shown in figure 2(d).

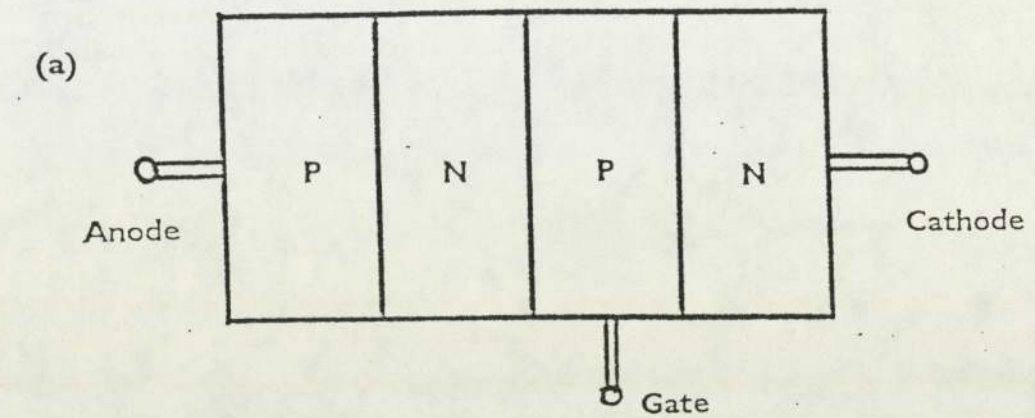
If the PNPN device has an external contact or gate attached to the second P layer then the device is known as a silicon controlled rectifier (SCR) or solid state thyristor [77] (see figure 3 (a)). It can be turned on at a voltage level substantially below V_{bo} by an electrical pulse applied to the gate. The I-V characteristic of this device is shown in figure 3(b). The operation of the device can be described by considering the thyristor as a combination of two three layer devices as shown in figure 4 (a). Therefore the thyristor consists of two bipolar transistors with common electrodes (see figure 4(b)). The gate electrode forms the collector of the PNP transistor and the base of the NPN transistor.

A voltage applied across the device between the anode and cathodes biases the device, but will not turn the device on. A positive reverse bias applied to the N-type cathode causes a very small reverse leakage current to flow but the device remains off. This is the reverse blocking state of the device. Likewise a positive forward bias applied to the P-type anode will not turn the device on. In this case the NPN transistor will not conduct unless a bias is applied to its base via the gate connection. In addition the PNP will not conduct since the bias applied to its base is supplied via the NPN transistor. This is the forward blocking state of the device.

If a positive current is applied to the gate, the NPN transistor turns on and draws current from the base of the PNP transistor, which then also turns on. When the transistors are both turned on, then the thyristor current flows from anode to cathode if the device is forward biased. Thus the two transistors provide a positive current feedback loop for each other and the device remains on even after the gate potential has been removed. This latching feature is an advantage over the bipolar junction transistor which remains in the on state only as long as the gate bias is applied. Thus use of a thyristor offers the opportunity to control thousands of volts and thousands of amps with a gate pulse of tens of volts and amps i.e. a considerable gain in the control level is

FIGURE 3

(a) Diagram of a PNPN thyristor
(b) Plot of V-I characteristic of a PNPN thyristor



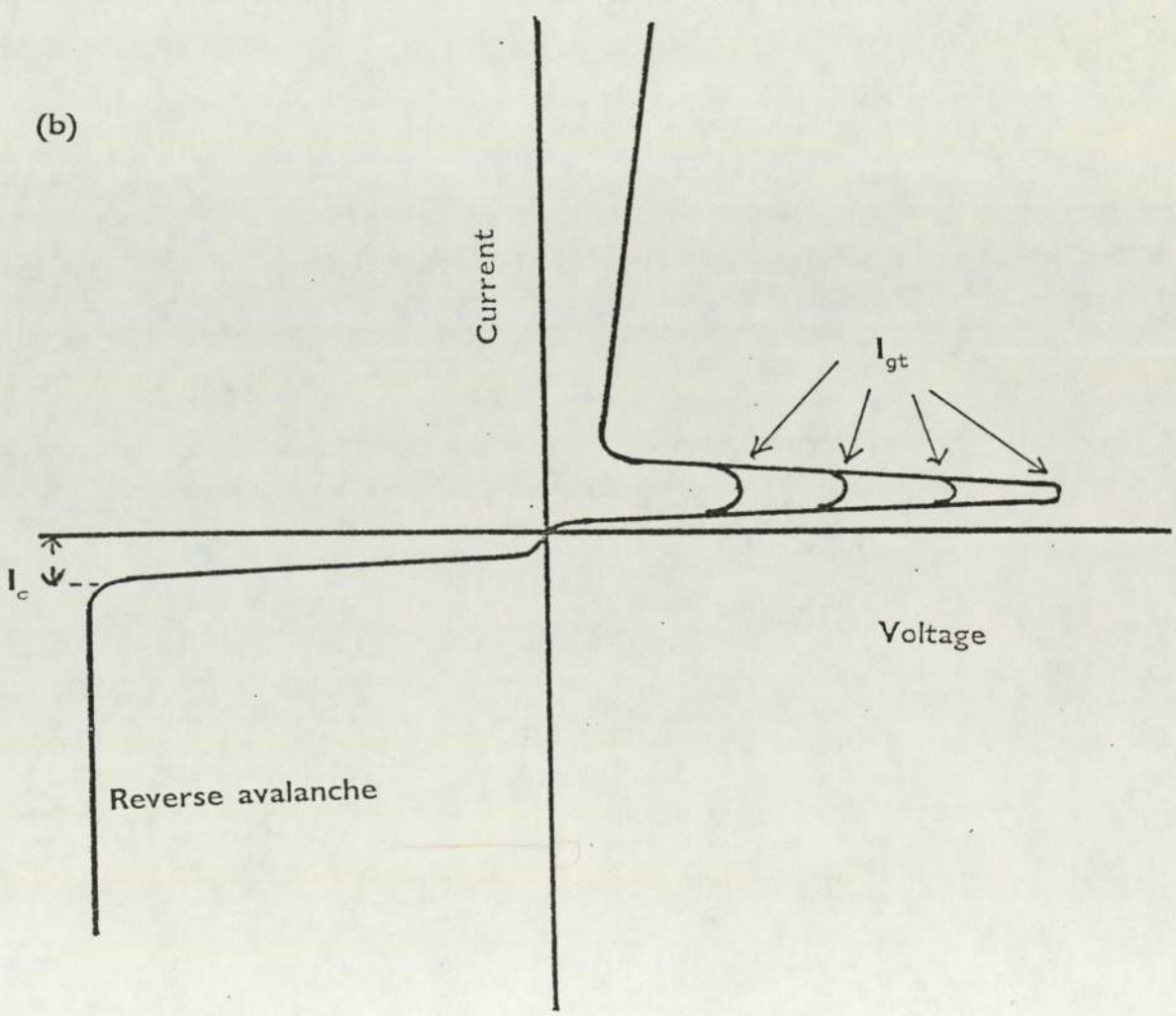
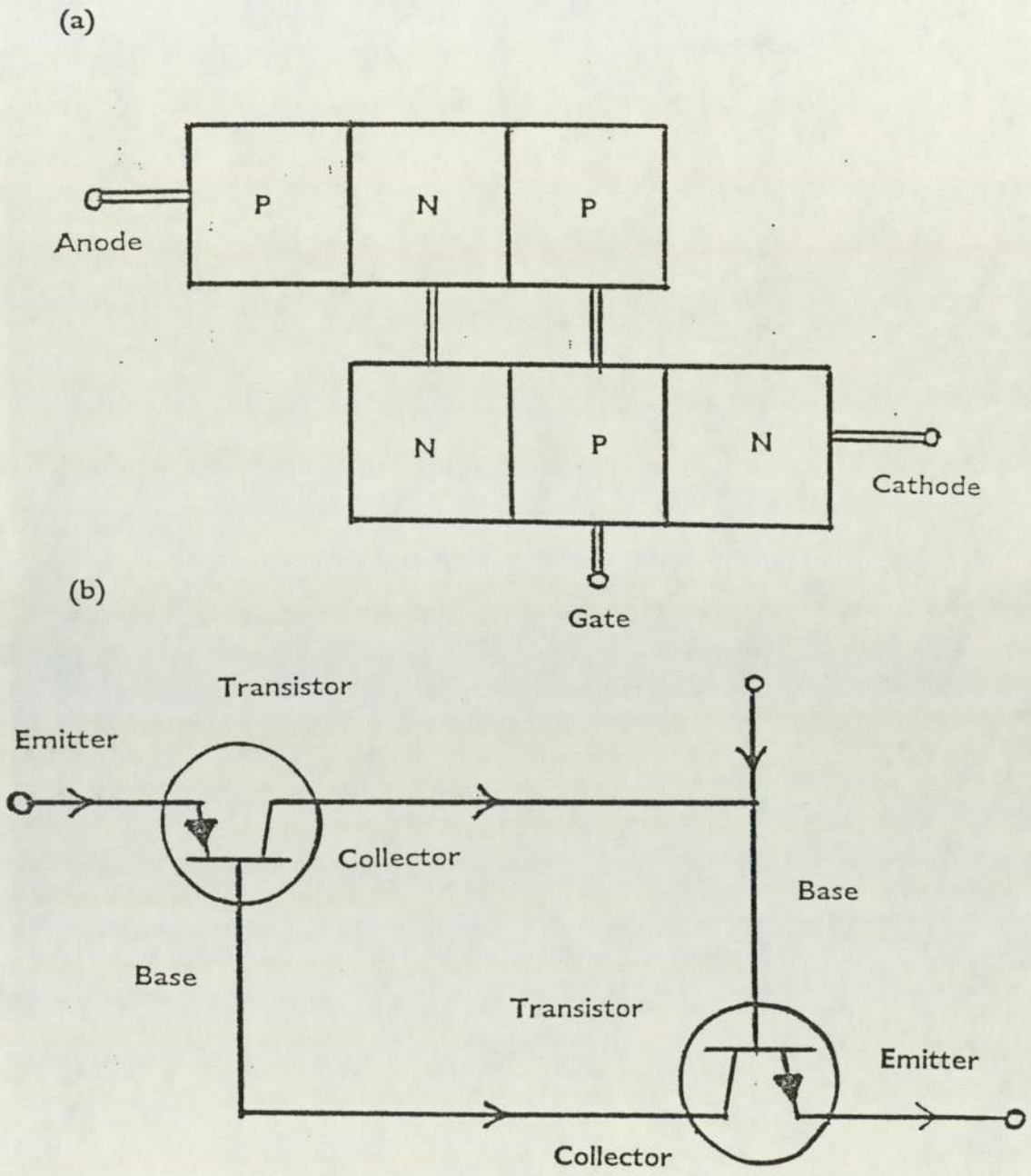


FIGURE 4

(a) Diagram of two, three layer devices
(b) Diagram of two transistor representation of the solid state thyristor



achieved. Such semiconductor switches can be used to construct static inverters. Standby power supplies, vibrator power supplies, variable speed AC motor drives and battery vehicle drives all make use of static inverter technology. The generic term inverter may be used to cover choppers, inverters and several forms of converters [237].

A converter is a unit for transforming one type of AC to a different type of AC or one type of DC, to a different type of DC.

An inverter transforms DC to AC (the inverse operation being rectification performed by a rectifier).

In electrical circuits a chopper (cf vibrator) is a piece of equipment that produces alternating current by periodically interrupting or reversing a continuous steady current from a direct-current source. It is effectively a single ended inverter for transforming DC to DC or DC to AC.

The normal thyristor used in such circuits can only return to the off-state when the forward current falls below a certain device dependent value known as the holding current. Thus to turn a thyristor off [60], the forward current must be reduced to below this value by some external current control or the external voltage bias across the device must be reversed (this would drive the current density below the holding current value). This process known as commutation is achieved by the action of the external circuit [76].

In AC supplied circuits the current reverses every half cycle turning off the device. In DC supplied circuits, thyristor turn-off can be achieved by a process known as forced commutation. This essentially consists of an auxiliary thyristor that is used to divert current away from the main thyristor thus reducing the forward current to below the holding current. Once the current in the thyristor has fallen below the holding current the positive feedback loop in the two transistor model becomes unstable and the device turns off.

If a semiconductor switching device could be devised that could be turned off

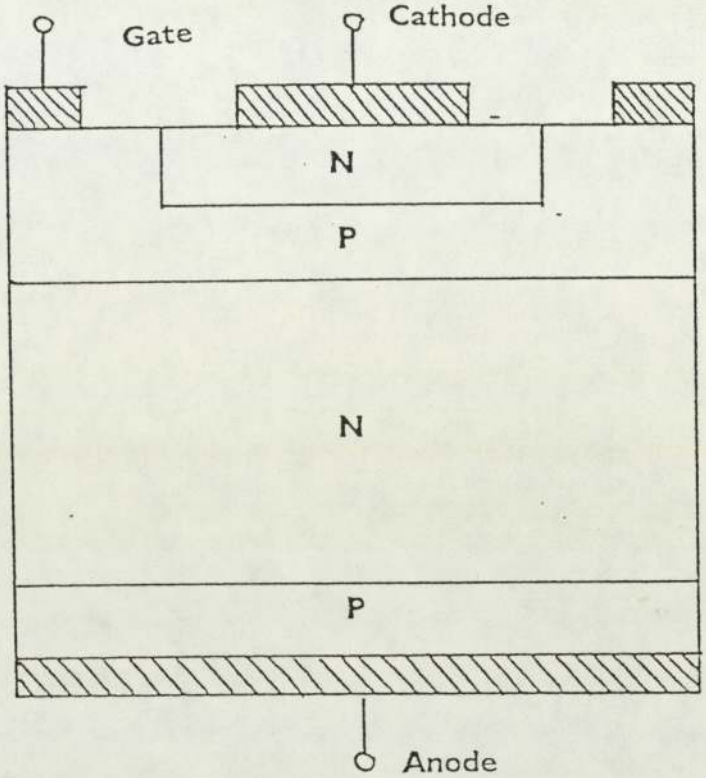
by a gate pulse then these auxiliary circuits would no longer be required. Figure 5(a) shows a schematic diagram of a gate turn off thyristor. In a GTO (gate turn off thyristor) it is not necessary to reverse the polarity of the main terminals to achieve turn-off and control is achieved by the use of one gate electrode only [29]. The turn-on process in this device is similar to that of the conventional thyristor described above. The positive gate current forward biases the cathode P-type material (the base). This results in electron emission from the cathode N-type material. These electrons travel to the anode where they induce hole injection by the anode emitter. The charge multiplication effect then brings the GTO into conduction. To turn-off this device a reverse gate current and potential is applied. This extracts charge (holes) from the P-base. The difference between this device and the gate assisted turn-off thyristor is in the control gate structure. The gate consists of a number of finely divided 'fingers' (see figure 5(b)). Therefore the extraction area is large, reducing the time required for turn-off to occur. As hole extraction reduces the excess carrier concentration, carrier multiplication gradually ceases, turning the device off by squeezing the conduction area down to zero. Therefore the replacement of a normal thyristor by a GTO renders the forced commutation components unnecessary. By using a GTO in the simple circuit shown in figure 6(a) the inductor, capacitor and auxiliary thyristors are no longer necessary. The cost advantage is obvious and in addition as shown in figure 6(b) a far simpler circuit that is smaller, lighter more efficient and possibly more reliable is produced [30].

The use of GTO's in inverter circuits reduces the component count compared to conventional thyristors but as with other semiconductor switches it does require the installation of a snubber circuit [39,75,63,62] to limit the rate of rise of reapplied voltage. The demand for higher power and greater switching frequency has increased the operating stress on GTO's so that efficient snubber design and effective snubber components have become increasingly important. The savings in component count and relatively simple gate drive more than offset any difficulties that the design of an efficient snubber circuit may present. Thus until a practical 'snubberless' GTO is developed, increases in circuit performance must be won by improved efficiency of the snubber circuit. Thus

FIGURE 5

(a) Schematic diagram of the Gate Turn Off thyristor.
(b) Diagram of GTO slice showing cathode fingers.

(a)



(b)

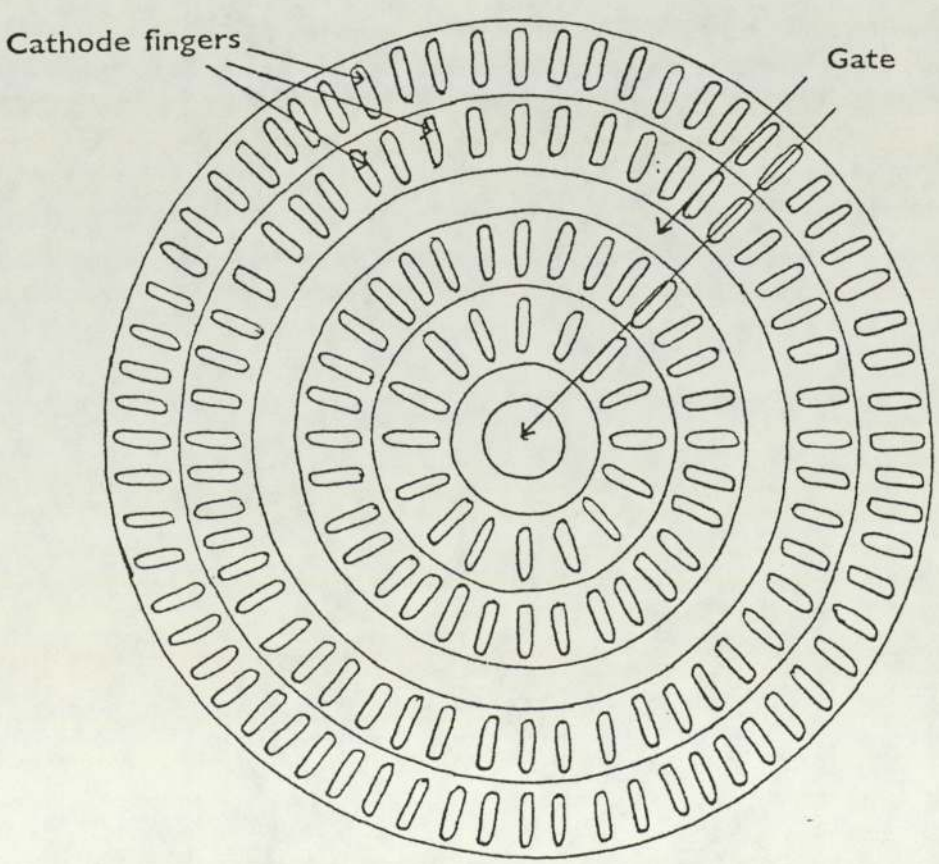
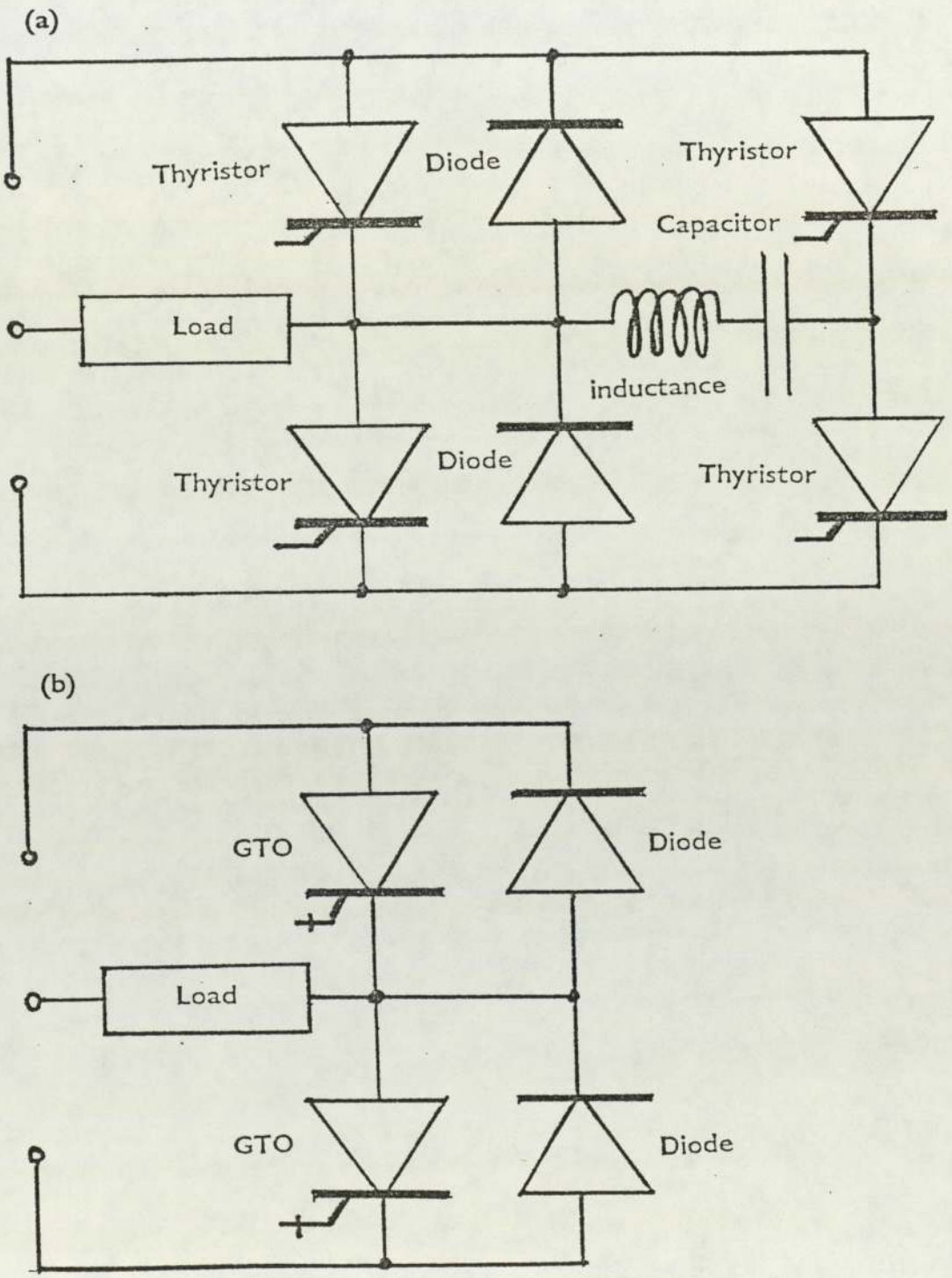


FIGURE 6

(a) Diagram of simple inverter circuit using normal thyristors as switching elements.

(b) Diagram of simple inverter circuit using GTO's as switching elements.



this project is concerned with improving the predictability of high stress snubber diode performance.

2.4.3 **The snubber circuit**

Each semiconductor device has some capacitance associated with its construction [18]. Consider a simple parallel plate capacitor as shown in figure 7(a). Capacitive current flow through the device is then described by the equation:

$$i_c = C_o dV/dt \qquad \text{- (E2)}$$

where i_c = current flow through the capacitor

C_o = Capacitance

V = Voltage across the capacitor

Thus the application of a time varying voltage across the anode/cathode terminals will produce a corresponding current flow in the device. Such current flow through a PNPN device can turn the device on due to the current amplifying nature of the two transistor model; see figure 7 (b). In small devices operating at low frequency, both C_o and dV/dt are small and therefore do not constitute a turn-on hazard. However in large devices, capacitance can be of the order of nanofarads and dV/dt's of kilovolts per microsecond. Thus capacitive current can reach the level of Amps, which is high enough to turn a device on. This is known as the dV/dt effect [2]. Because of this phenomenon, the rate of rise of the reapplied voltage on a GTO must be limited to avoid a refire during turn-off.

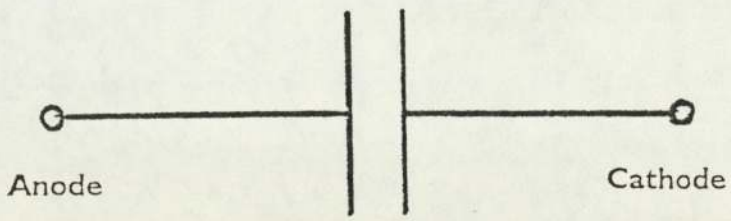
Such ungated turn on events are undesirable not only in terms or circuit current regulation but also because turn-on by a weak gate pulse can result in reduced device dI/dt capability and thus device failure. From equation (E2) it can be seen that limiting the dV/dt limits the capacitive current and thus could prevent a non-gated turn-on.

In practical circuits the limitation of reapplied voltage is achieved by connecting

FIGURE 7

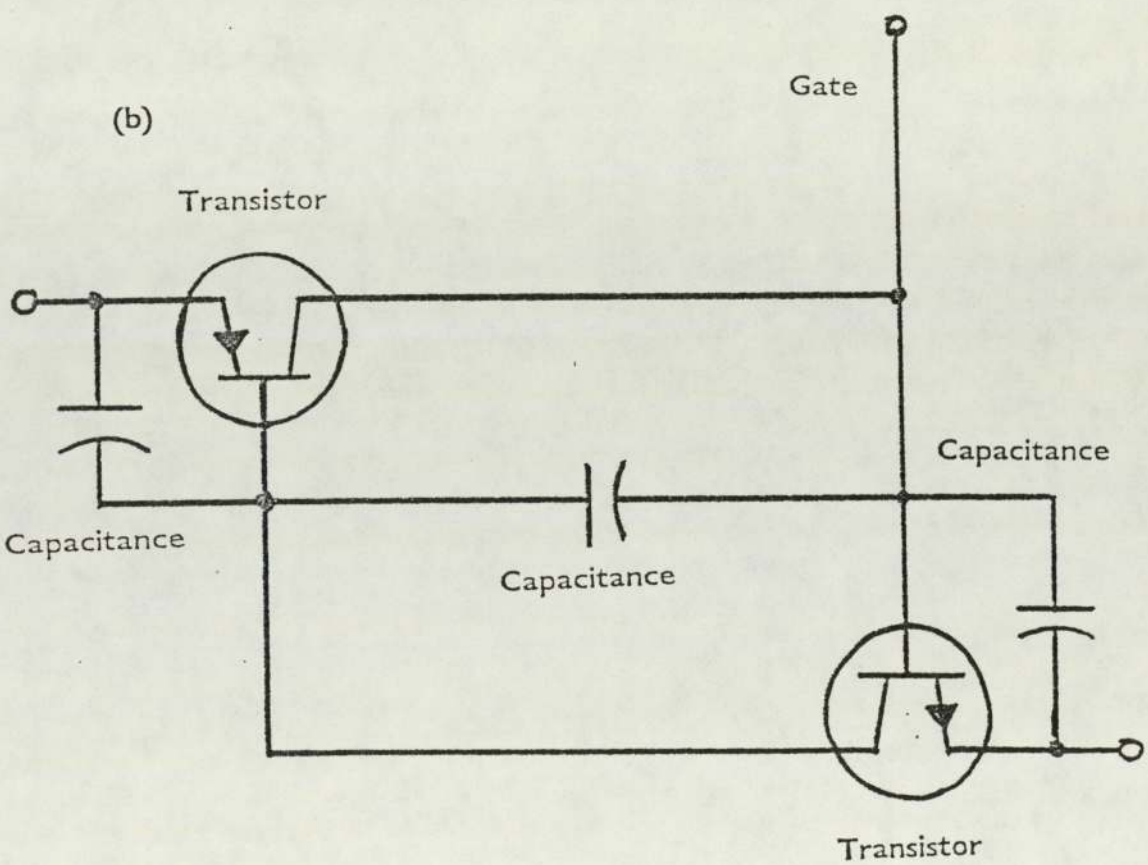
(a) Diagram of parallel capacitance.
(b) Diagram showing equivalent two transistor thyristor circuit including **PN** junction capacitance.

(a)



$$I = C.\frac{dV}{dt}$$

(b)



a snubber capacitor in parallel with the GTO (see figure 8 (a)). During turn-off this capacitor charges up while limiting the dV/dt. When the device next turns on the charged capacitor will discharge through the GTO increasing the turn-on duty by both dumping its stored energy into the device and increasing the initial dI/dt. To limit this current inrush, a resistor is placed in series with the capacitor (see figure 8 (b)). This resistor then dissipates the stored energy of the capacitor during GTO turn-on. The RC time constant of the snubber network then inhibits the ability of the capacitor to limit the turn-off dV/dt and therefore a diode is placed across the snubber resistor to make the snubber network polarised. Hence a GTO snubber network consists of a resistor, a capacitor and a diode as shown in figure 8 (c) [34]. It should be noted that the alternative dV/dt protection strategy of shorting [35] dots as employed on conventional solid state thyristors [77] is not available to GTO's because of their structure.

Thus during normal GTO operation the snubber diode is subjected to successive reversals of applied external bias. During GTO turn-off the diode will be forward biased and a pulse of forward current will flow through the diode to charge up the snubber capacitor. During GTO turn-on the capacitor will discharge through the snubber resistor producing a reverse bias across the diode equal to the ohmic voltage drop over the resistor. The reversal of bias changes the conduction state of the diode from on to off. Ideally the diode should therefore have a 'perfect switch' characteristic with no intermediate state between on and off.

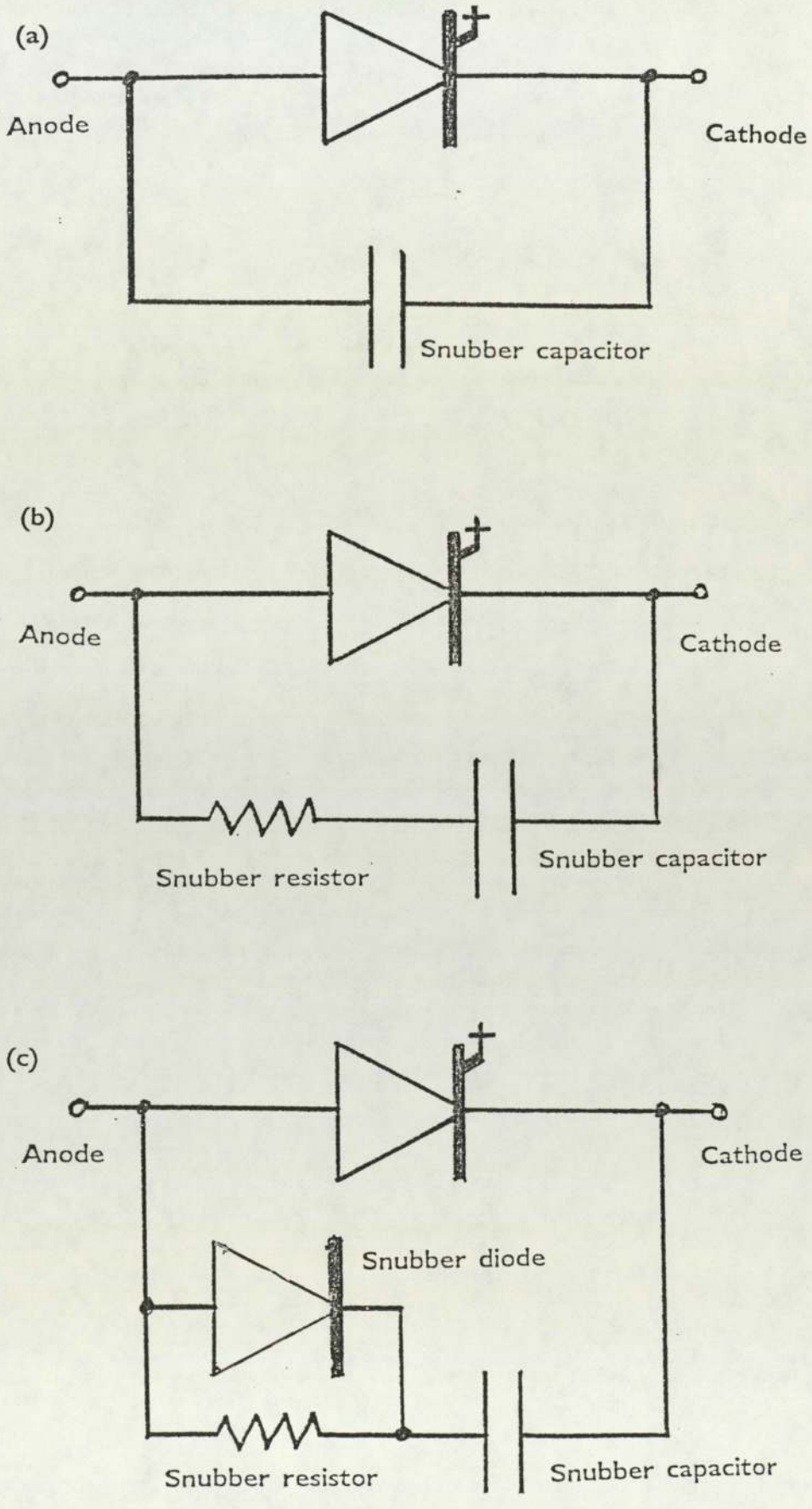
2.4.4 **Diode reverse recovery**

Because the 'perfect switch' characteristics that are desirable in all diodes is not realised in practical devices the target characteristics for a snubber diode are:

1) small transient forward voltage drop [131]
2) small stored charge [159, 165]
3) fast recovery time [158, 159]
4) a soft reverse recovery characteristic.

FIGURE 8

(a) Capacitive snubber.
(b) Resistive/capacitive snubber.
(c) GTO polarised snubber circuit.



It has long been known that the diode is not a perfect switch [6] in that a finite time is required after a reverse bias has been applied for the device to become reverse blocking. This finite recovery time has been shown to be due to the minority carrier storage effect [8,10]. This occurs in PN junctions when a reverse bias is applied. A semiconductor with a relatively long bulk lifetime has an excess of minority carriers being injected across the PN junction. This excess of minority carriers remains near the junction as a net charge. When a reverse bias is then applied to the PN junction the carriers stored near this junction are extracted and produce a transiently high reverse current. The time interval between the application of the reverse bias and the recovery of the junction (i.e. volts start to build up across the device) is known as the storage time of the diode [9]. Thus diode commutation during GTO switching results in reverse current being drawn as the stored charge accumulated during the on-state is extracted. The current reaches a peak (which is substantially higher than the normal reverse saturation current) and then diminishes as the free charge carrier density decays and a reverse bias depletion layer is formed.

The type of recovery waveform a diode possesses is of interest to the circuit designer because it is responsible for the size of the peak reverse recovery voltage generated by diode commutation in an inductive circuit. Figure 9 (a) shows a sketch of the current and voltage waveforms of a snubber diode under a simulated snubber duty. The forward current loop generates excess charge carriers within the diode that are extracted as reverse current when the applied bias is reversed. As these carriers are used up the diode impedance increases producing a voltage overshoot which then collapses to a steady state level as the diode turns off. This steady state level, V_r, is approximately equal and opposite to the initial capacitor charging voltage, V_{ch}, in a LC circuit. This type of reverse recovery waveform is typical of what is known as normal diode recovery.

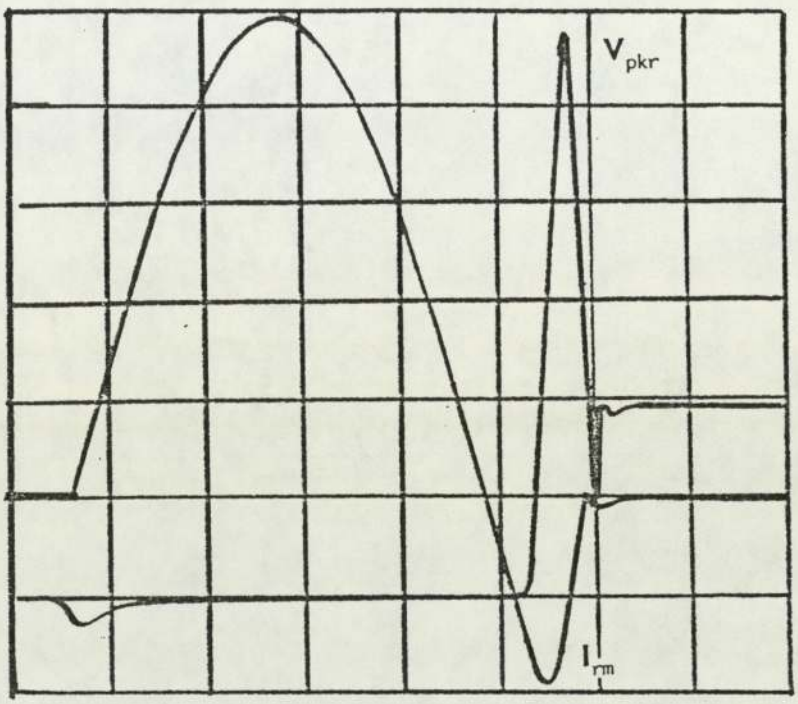
From simple circuit theory the over voltage V_L is equal to the product of circuit inductance and the recovery dI_r/dt as shown in figure 9(b). These idealised curves are straight line approximations to the practical recovery

FIGURE 9

(a) Sketch of oscillogram showing diode forward current loop and reverse recovery behaviour.

(b) Diagram of idealised diode reverse recovery voltage and current curves.

(a)



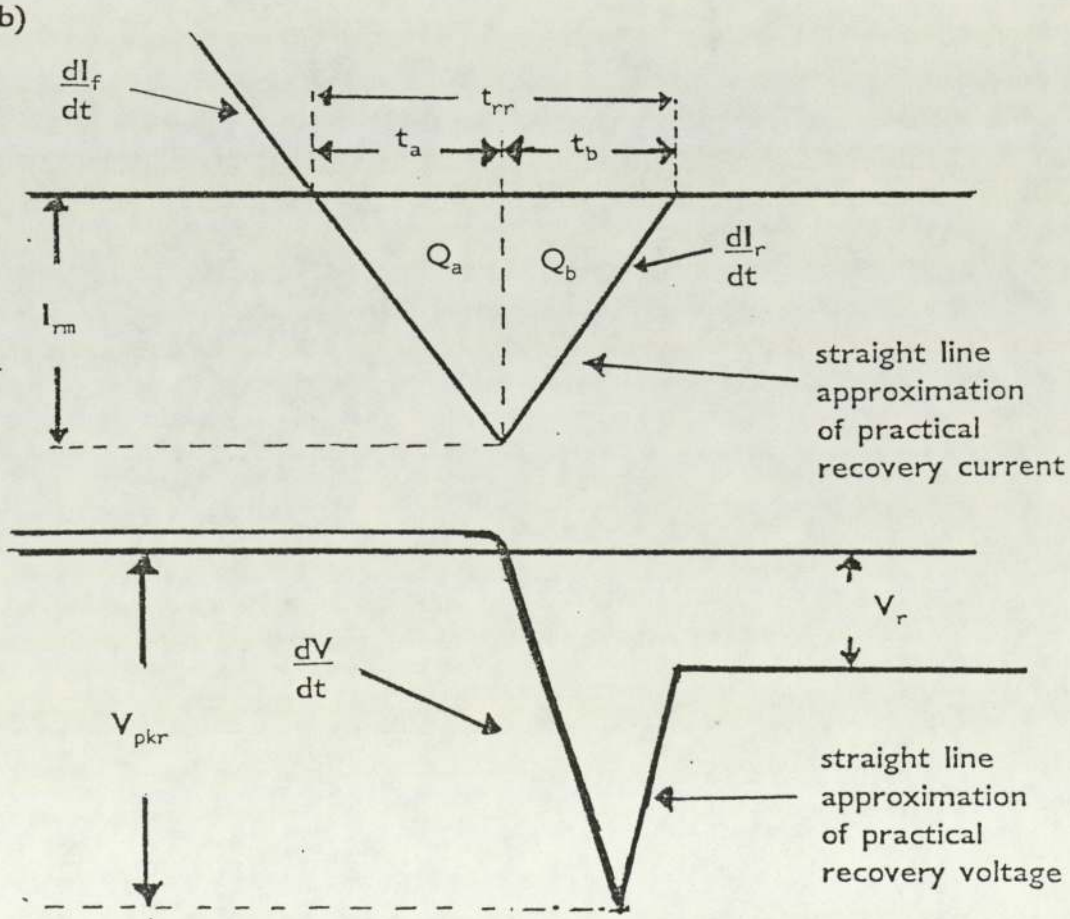
V = 50V/Div

I = 20A/Div

t = 2μs/Div

inverted voltage trace

(b)



waveform shown in figure 9 (a). The dV/dt to the peak reverse recovery voltage V_{pkr} is governed by the diode capacitance in its equivalent circuit model. Since $V_{pkr} = V_r + V_L$ and V is proportional to dI_r/dt then as dI_r/dt increases so V_L and thus V_{pkr} also increases. The size of the overvoltage generated determines the softness or snappiness of the diode. These two terms are loosely defined and are used synonymously.

Soft recovery is usually described as one in which the recovery dI/dt and thus the overvoltage is small as shown in figure 10 (a). Some diodes produce relatively small overshoot voltages but are oscillatory as shown in figure 10(b).

Snappiness is associated with an abrupt recovery waveform in which the high recovery dI/dt generates a recovery voltage that is many time larger than V_r as shown in figure 10(c). The high dI/dt produces a voltage step. In such cases the large dV/dt generated can shock excite the circuit into producing parasitic LC oscillations.

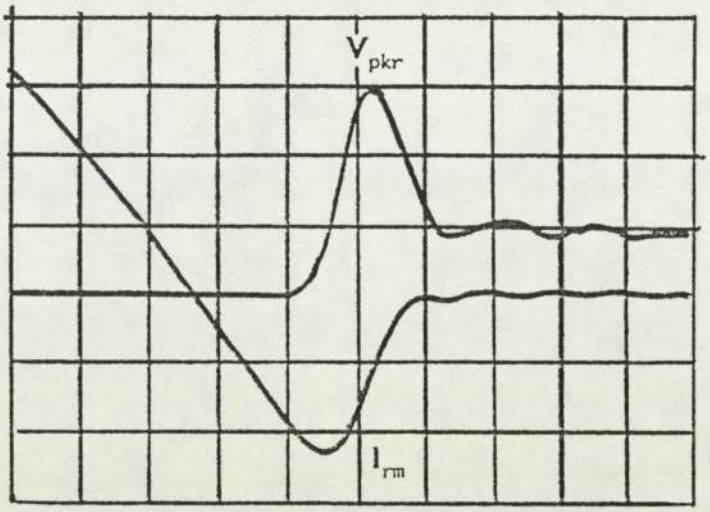
The step recovery diode, [40] also known as a snap-off diode, [4] a snap back diode or a boff diode, has a particularly abrupt reverse recovery waveform. The diode is designed so that most of the stored charge is close to the junction and as such is available for immediate extraction when a reverse bias is applied. When the diode switches from forward bias to reverse bias the stored charge is rapidly extracted producing a relatively large peak reverse current (if charge is extracted rapidly, recombination processes do not significantly reduce the magnitude of stored charge). The reverse current is then abruptly cut off since all of the stored carriers have been extracted. The diode thus remains in a low impedance state until cut off occurs and hence a large recovery dI/dt is produced. The reverse voltage generated by the dI_r/dt builds up very rapidly since current cut off occurs over a time period of a few picoseconds. The fast rising waveform produced is rich in harmonics and thus snap off diodes are sometimes used as harmonic generators [35].

A fast recovery diode [169,160,161] is a device in which very little charge storage occurs. In low power devices fast recovery can be achieved by using a

FIGURE 10

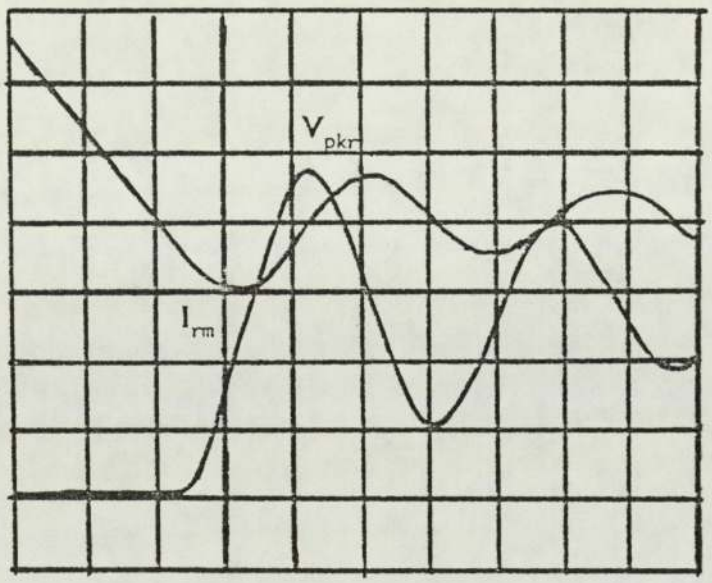
(a) Sketch of oscillogram of diode normal reverse recovery.
(b) Sketch of oscillogram of diode oscillatory reverse recovery.
(c) Sketch of oscillogram showing diode reverse recovery snap off.

(a)



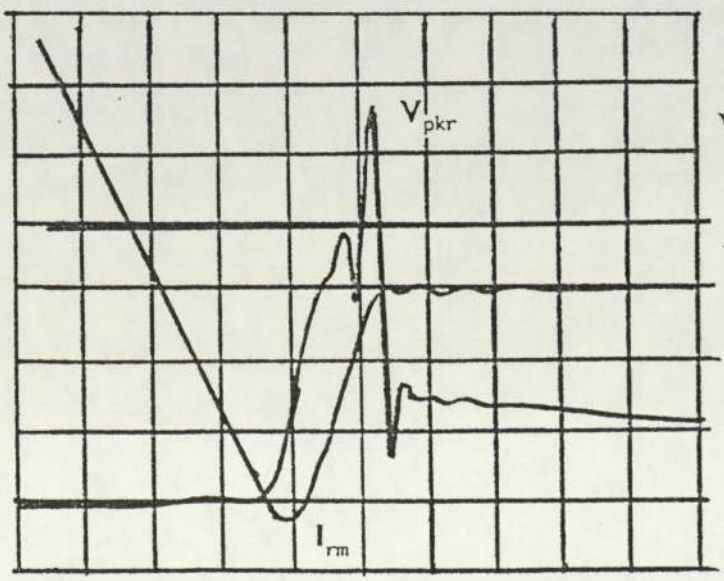
V = 500V/Div
I = 20A/Div
t = 0.5μs/Div
inverted voltage trace

(b)



V = 200V/Div
I = 50A/Div
t = 0.2μs/Div
inverted voltage trace

(c)



V = 500V/Div
I = 20A/Div
t = 0.5μs/Div
inverted voltage trace

novel structure such as a Schottky diode [129] or by using a direct gap semiconductor such as gallium arsenide (in which minority carrier lifetimes are very much shorter than in silicon). In high power fast recovery diodes this is usually achieved by decreasing the carrier lifetime at the expense of forward conduction losses.

A description of the soft-recovery diode used in high power circuits is given in section 3.3.5.

The above text has described different diode types. As previously stated the type of diode used in a circuit will determine the inductive recovery overvoltage. In an ideal world the circuit designer would choose the appropriate diode type and excessive overvoltages would not be produced. Unfortunately the real world is far from ideal. My research will demonstrate that soft-recovery diodes can exhibit abrupt recovery. Since diodes can show a dual behaviour characteristic, it is important that the reader understands the difference between such diode and recovery types. This understanding will provide an insight into how and why a diode changes its recovery characteristic.

2.5 Aims of the Project

In this particular project the aim was to create a mathematical model of a semiconductor device that could be used to simulate performance and predict dangerous voltage excursions. The device chosen for this study was the high voltage, high power snubber diode. As a prerequisite to the modelling process an amount of experimental data was obtained. These experimental results were so unexpected as to warrant further investigations. One course of action to explain these results would have been by a brute force solution of the semiconductor device equations in three dimensions with time discretization and modified by the external circuit. Even a superficial analysis of this problem revealed that such an approach would certainly take longer than the lifetime of this project. In order to make some progress on this issue it was therefore necessary to try and explain these results in analytical terms. Once this had

been achieved then the numerical modelling process would be considerably easier and a suitable solution strategy could be employed.

The aims of the project can be split into three parts:

1) Experimental work (Section 3)

   a) To identify and categorise the effect of circuit parameters, operating conditions and diode design on the type of reverse recovery a diode exhibits.

2) Device modelling (Section 4)

   a) To explain the diode snap-off phenomenon in terms of an analytical model/models.
   b) To apply the findings of the analytical modelling process to a numerical modelling strategy.

3) Device/circuit simulation (Section 5)

   a) To implement the preferred solution strategy and simulate the in-service performance of the high power, high voltage snubber diode.
   b) To make predictions of the in-service diode performance under operating conditions not previously met in practical circuits.

This thesis therefore is presented with the above structure and sub-structure as outlined in Section 2.1.

3. THE EXPERIMENTAL INVESTIGATION

3.1 Foreword

The experimental data had significant impact on both (a) and (f) of the defined modelling process as outlined in Section 2.1. The device chosen for this study was a high voltage, high power snubber diode. To obtain the required experimental information a synthetic test circuit was constructed to represent in-service duty. This duty is described in the following section.

3.2 The design of a synthetic test circuit

3.2.1 The diode commutating current pulse

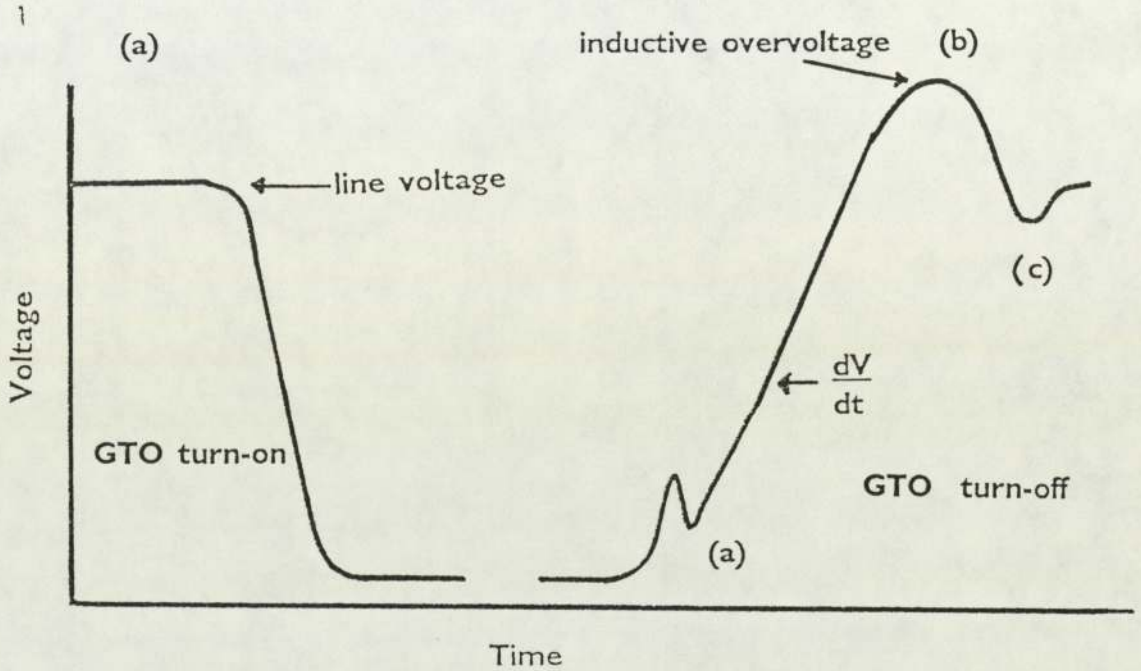
Consider the GTO turn-on and turn-off waveforms shown in figure 11 [44]. During turn-off the snubber diode is forward biased and therefore shorts out the snubber resistor. The snubber capacitor is therefore effectively in parallel with the GTO. The capacitive current flowing through the snubber capacitor is described by equation (E2).

At points (a), (b) and (c) on the voltage waveform in figure 11 (a), this capacitive current is equal to zero. Between points (a) and (b) the dV/dt and thus the capacitive current is positive (i.e. forward current). Between points (b) and (c) the dV/dt is negative and therefore the capacitive current is negative. The dV/dt over a large section is approximately constant therefore producing the type of current waveform shown in figure 12(a). The falling current at the end of the current pulse can be approximated by the sine wave formula. When the frequency of the GTO switching is increased, the pulse becomes short and as shown in figure 12(b) appears as a slightly asymmetric half sine wave. This high frequency switching condition represents a high stress condition under which diode snap-off is likely to occur.

Therefore an ideal test circuit for GTO snubber diodes would be one in which a half sine wave of forward current was followed by a reverse bias to extract

FIGURE 11

(a) GTO turn-on and turn-off voltage waveforms.
(b) GTO turn-on and turn-off current waveforms.



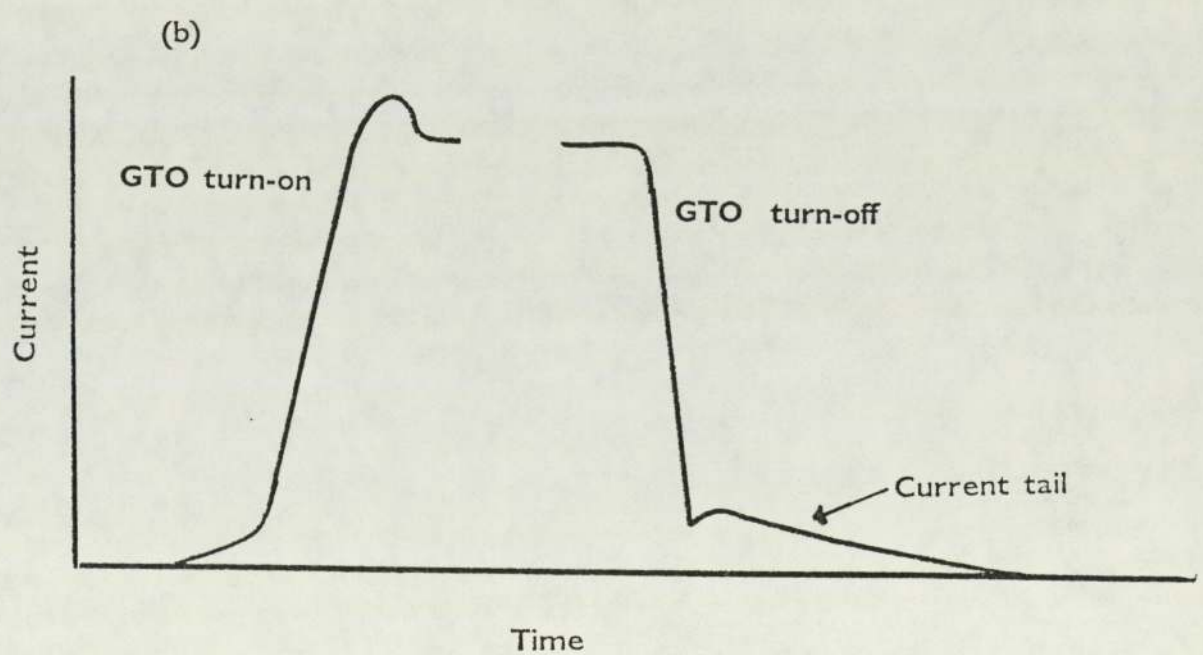
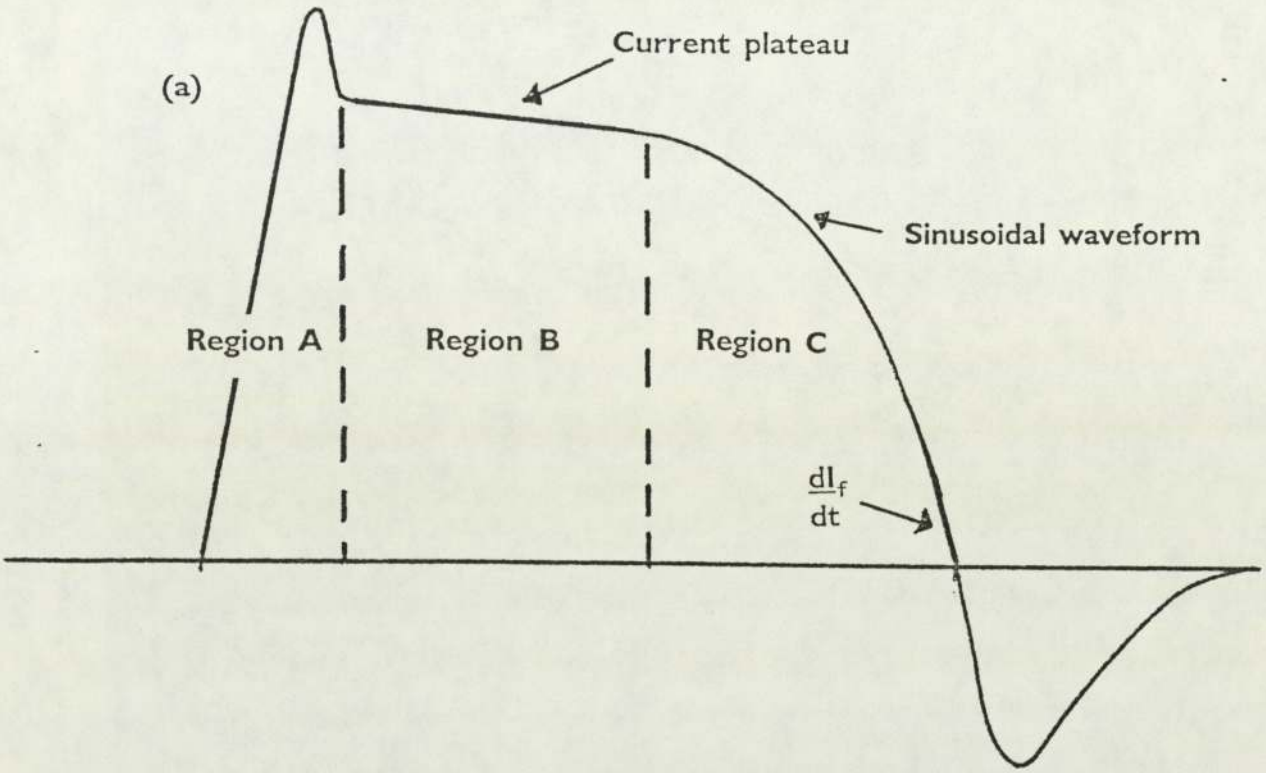
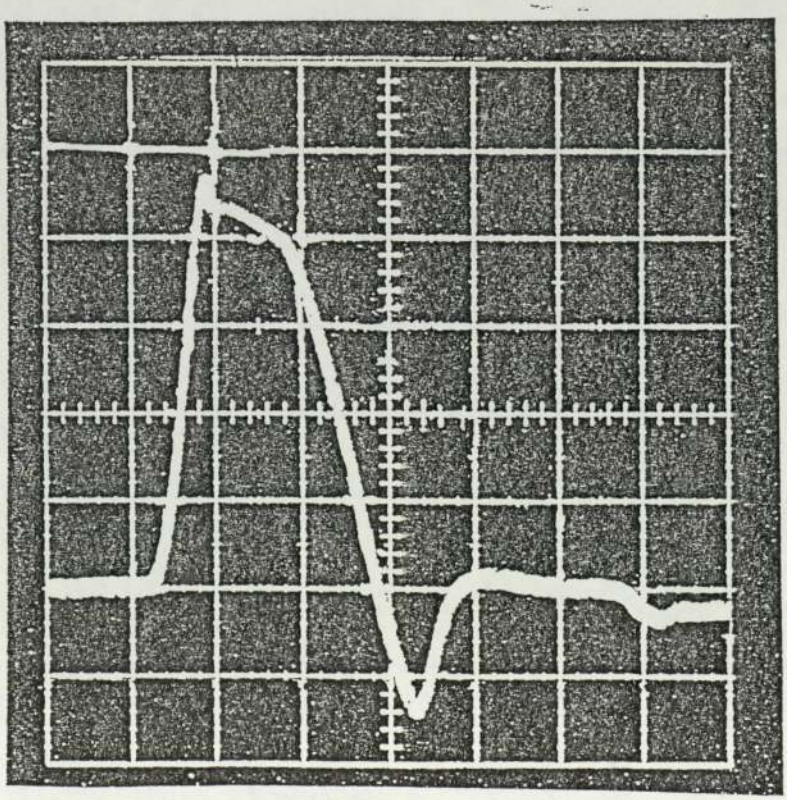


FIGURE 12

(a) Diagram of idealised snubber diode current waveforms.
(b) Oscillogram of in-service snubber diode current.



(b)



the stored charge and thus turn the diode off by commutation.

3.2.2 **The synthetic test circuit**

In an LCR circuit the discharge of a capacitor C through a known inductance L_c and a known resistance R causes a periodic reversal of circuit potential and current. Alternate loops of forward and reverse current flow through the resistance which damps the oscillation causing it to decay away. A simple LCR circuit was therefore used to apply a forward current pulse followed by a reverse voltage to the test diode. Failure of the test diode during an investigation sequence would not result in the failure of the conventional thyristor switch due to a protective anti-parallel diode being included in the circuit design.

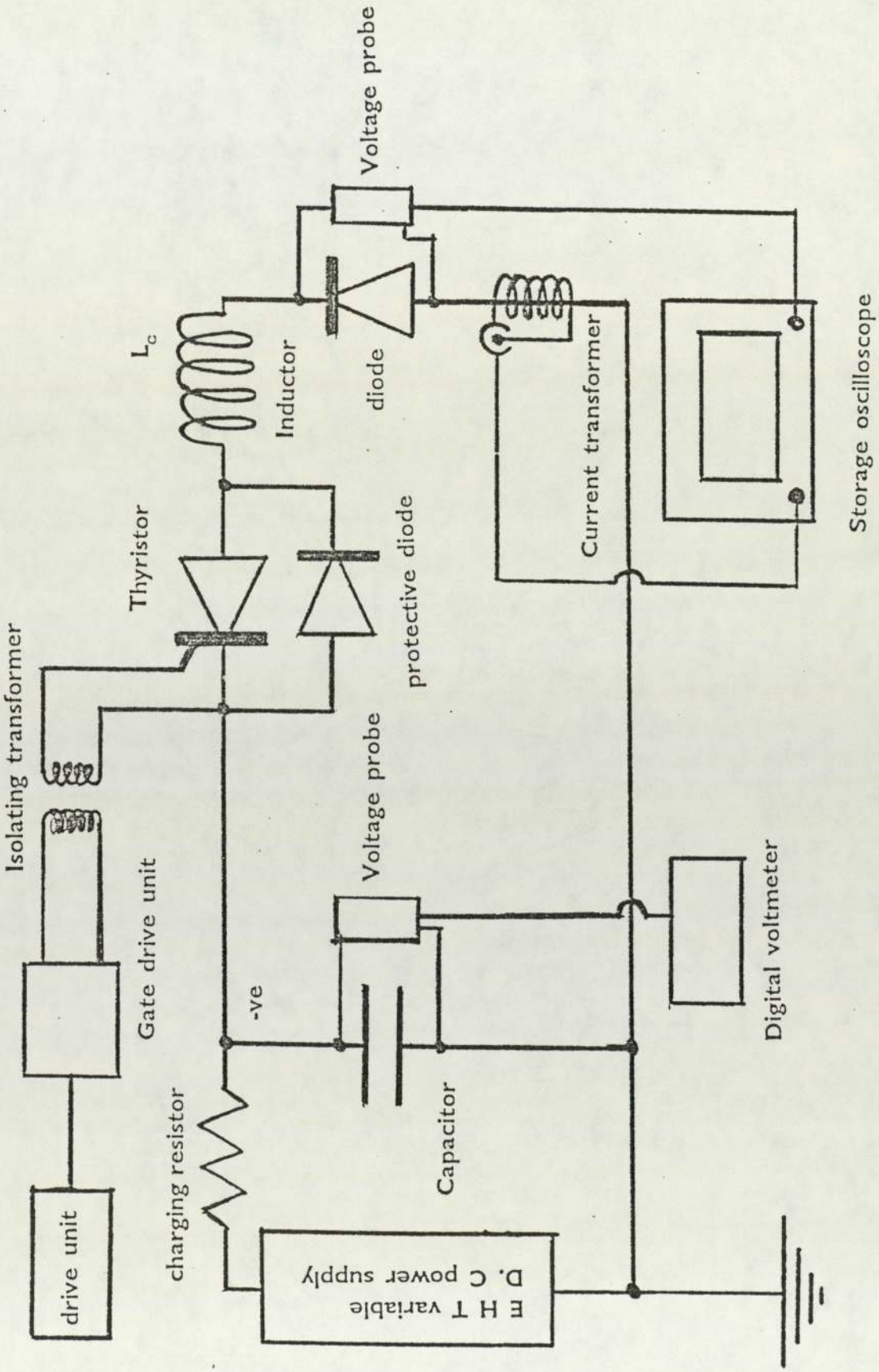
Figure 13 shows such a circuit in which the discrete resistor has been replaced by the diode under test. A variable power supply can be used to charge up the circuit capacitor C. The potential of the capacitor can be measured using a voltage probe and digital voltmeter combination. Manual operation of a gate pulse unit triggers the circuit thyristor into conduction and allows the capacitor to discharge through the inductor and the diode. Voltage signals of current flow through the diode and potential drop across it, can be displayed on a dual channel storage oscilloscope via a current transformer and a voltage probe. Use of a current transformer to measure the current signal rather than a current shunt (sometimes known as a current viewing resistor) has the advantage of not introducing two earths on the measuring system.

Using a test circuit similar to that shown in figure 13 and described above, various diodes were subjected to a series of tests. By altering the capacitor charging voltage the peak forward current could be varied. In a low resistance circuit the steady state recovery voltage, V_r, is very nearly equal to the initial charging voltage, V_{ch}, on the main circuit capacitor. Thus:

$$I_{pkf} = V_r.(L_c/C)^{-1/2} \qquad \text{- (E3)}$$

FIGURE 13

The synthetic test circuit



The frequency of the oscillation during the capacitor discharge is dependent on the circuit inductance and circuit capacitance. Since both of these parameters are constant during the voltage decay the initial forward current pulse width is also constant and independent of the capacitor charging voltage. Hence, for a current pulse of constant width the commutating dI/dt (i.e. dI_f/dt) increases as the peak forward current is increased by use of the charging voltage.

3.3 Identifying the Problem

3.3.1 The effect of commutating dI/dt on recovery voltage.

Using the test circuit shown in figure 13 and described in section 3.2.2 the commutating dI/dt was varied by adjusting the charging voltage applied to the circuit capacitor. Thus during each test sequence the diode under test was subjected to a series of current pulses of increasing commutating dI/dt. Photographic records of each test were obtained and from these the commutating dI/dt and the peak reverse recovery voltage V_{pkr} were measured. A series of such measurements could then be used to plot a curve of commutating dI/dt against peak reverse voltage as shown in figure 14. The curve obtained can be divided into three regions [45]:

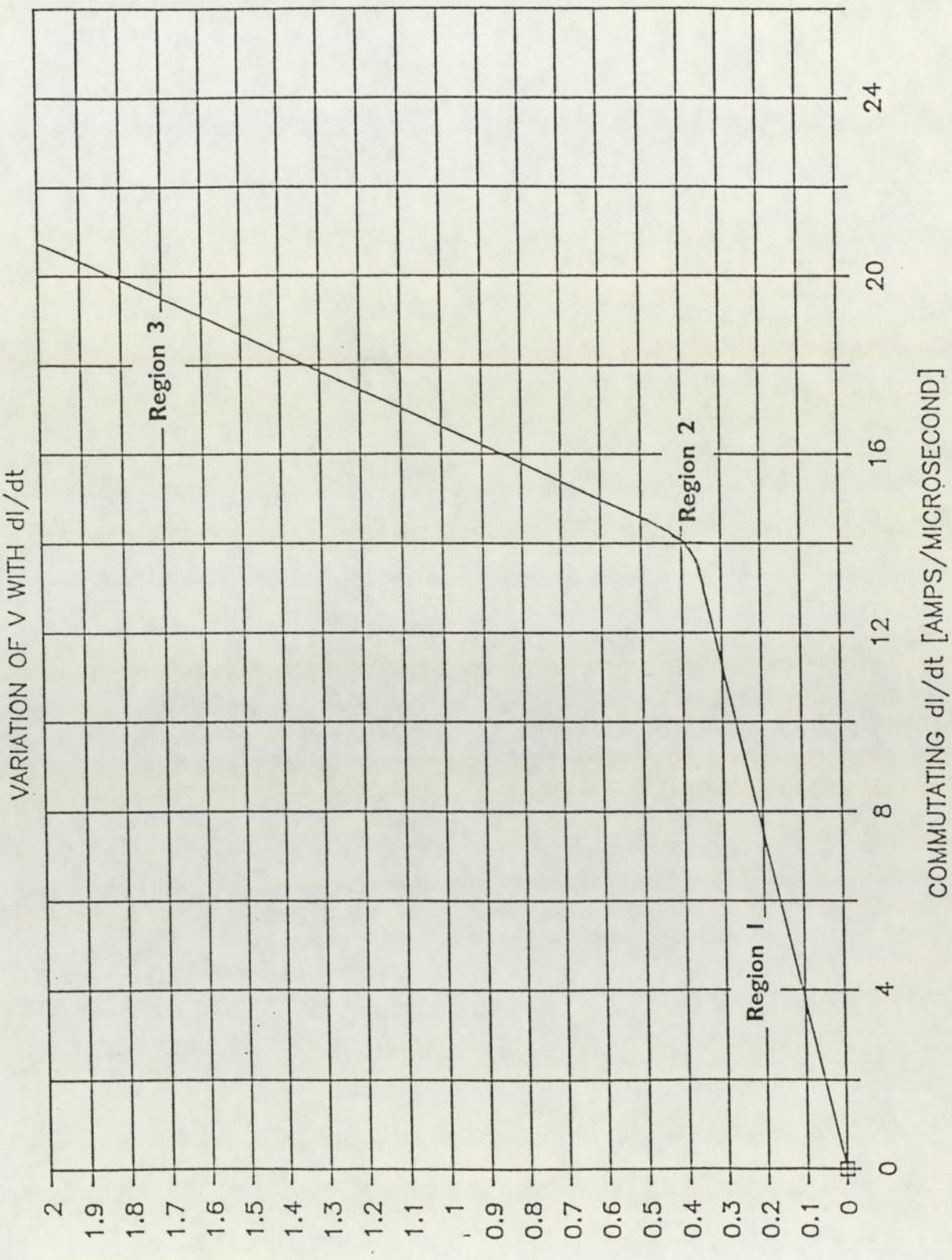
1. A region where the recovery voltage is approximately linearly proportional to the commutating dI/dt and the recovery waveform can be classified as a normal or soft recovery type.

2. A transition region between normal and snappy recovery.

3. A region where the recovery voltage is approximately linearly proportional to the commutating dI/dt and the recovery waveform can be classified as a snappy or an abrupt recovery type. In this region the proportionality constant between V_{pkr} and dI_f/dt is much greater than in region 1.

FIGURE 14

Graph showing the variation of peak reverse recovery voltage with commutating dI/dt.



For the results obtained, the gradient of the curve in region 1 is dependent upon the circuit inductance according to the relationship:

$$V_{pkr} = (\text{constant}_1 \times L_c) \cdot dI_f/dt \qquad \text{- (E4)}$$

The voltage in region 3 appears to be largely proportional to the commutating dI_f/dt. Thus the peak reverse recovery voltage in region 3 may be dependent upon circuit inductance but with a different proportionality constant to that present in region 1.

$$\text{Thus:} \quad V_{pkr} = (\text{constant}_2 \times L_c) \cdot dI_f/dt + \text{constant}_3 \qquad \text{- (E5)}$$

where constant_3 is negative.

In region 2 the recovery voltage varies non linearly with the commutating dI/dt and can be considered as the knee of the curve.

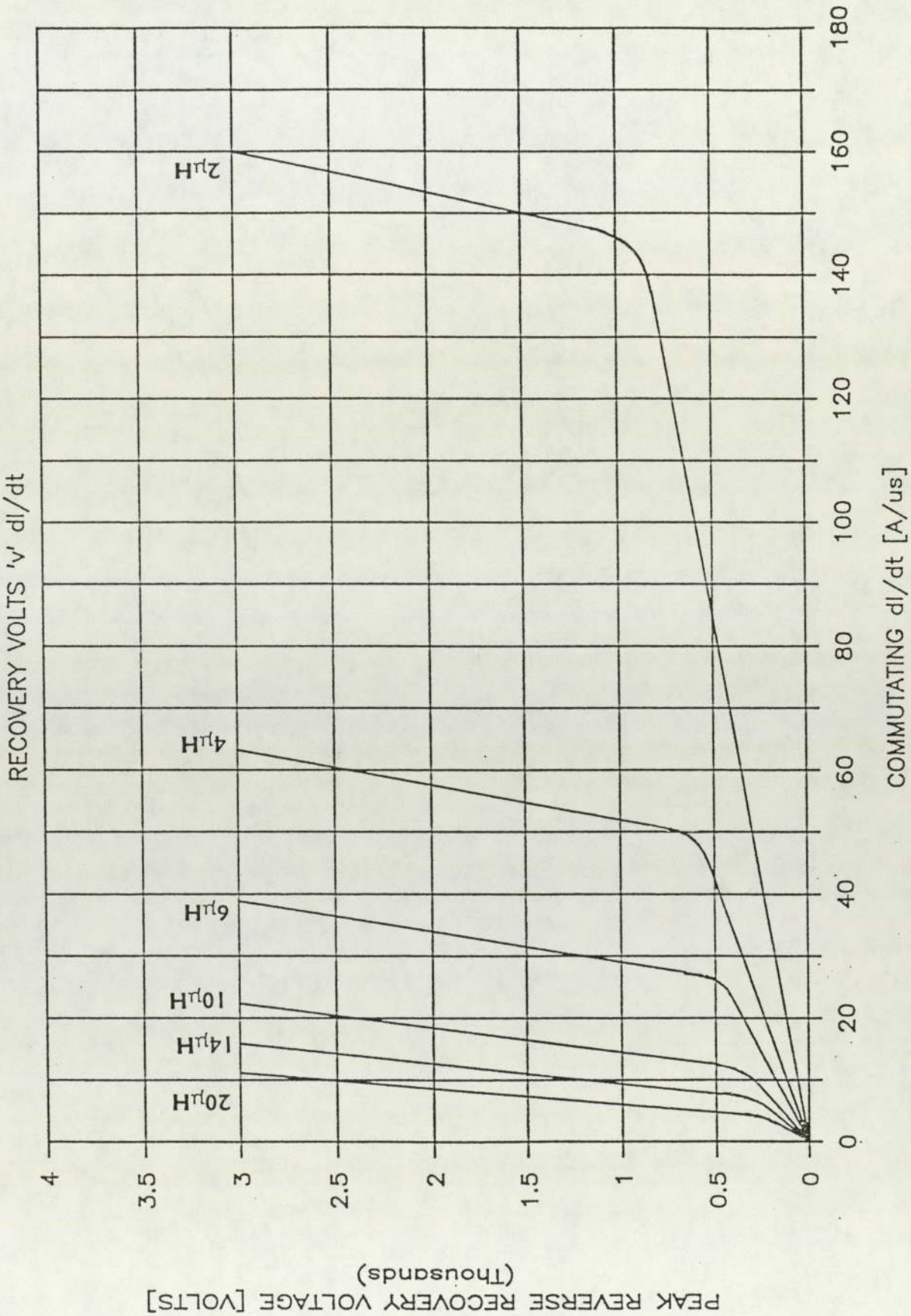
The three region form of the curve described above was unexpected. Prior to this experimental investigation it was assumed that there would be a simple straight line relationship between V_{pkr} and dI_f/dt. Thus previously extrapolation of the V_{pkr} against dI_f/dt curve up to the diode voltage rating was thought to be a satisfactory prediction technique. After these experimental results, however it became apparent that such extrapolations were not valid in all circumstances.

3.3.2 The effect of main circuit series inductance on recovery voltage

Using the test circuit described in section 3.2.2 a series of measurements of the reverse recovery voltage were made for different values of circuit inductance L_c. The resulting curves of peak reverse recovery voltage against commutating dI/dt are shown in figure 15. Each curve shows the three region behaviour identified in section 3.3.1. Generally for a given dI/dt the peak recovery voltage increases with circuit inductance. It can also be seen that the dI/dt at which snap-off occurs (the critical dI/dt) increases with decreasing circuit

FIGURE 15

Graph showing variation of peak reverse recovery voltage with commutating dI/dt for various values of main circuit series inductance.



inductance.

The gradient of each curve produced in figure 15 is equal to the quotient, $V_{pkr}/(dI_f/dt)$, since each curve up to the critical dI/dt is described by the straight line equation:

$$V_{pkr} = m_o . \frac{dI_f}{dt} + c_o \qquad \text{- (E6)}$$

where m_o = the gradient of the curve

c_o = a constant

Prior to critical dI/dt, c_o is equal to zero because of the L.C discharge circuit used, that is, when the charging potential of the circuit capacitor is zero the commutating dI/dt is zero.

Thus:

$$m_o = V_{pkr}/(dI_f/dt) \qquad \text{- (E7)}$$

In an L.C discharge circuit

$$dI_f/dt = V_r/L_c \qquad \text{- (E8)}$$

where dI_f/dt = commutating dI/dt

L_c = main circuit series inductance

V_r = final recovery voltage

Note that in a non-resistive circuit $V_r = V_{ch}$. - (E9)

$$\text{therefore } m_o = V_{pkr}.L_c/V_r = L_c.V_{pkr}/V_r = L_c.Ç \qquad \text{- (E10)}$$

where Ç = the softness factor $= V_{pkr} / V_r$ - (E11)

From equation (E10) it can be seen that the gradient of the experimental

curves prior to the critical dI/dt is equal to the product of circuit inductance and softness factor 'Ç'. The curves produced in figure 15 can then be replotted as the variation of the softness factor Ç with the commutating dI/dt (see figure 16). Figure 16 shows that prior to snap-off the value of Ç is independent of both circuit inductance and commutating dI/dt. The curves produced have a much sharper transition from normal to snappy recovery and therefore exhibit a two region behaviour.

Construction of a line through the data points defined as the knee of each curve in figure 16 yields data points for the variation of critical dI/dt (dI_{crit}/dt) with circuit inductance. This information is presented as a graph in figure 17. It indicates that there may be a dI/dt above which the diode will always be snappy and a dI/dt below which it will never be snappy, regardless of circuit inductance.

This curve can be approximated using the simple power relationship:

$$\frac{dI_{crit}}{dt} = A.L_c^{B} \qquad \text{- (E12)}$$

where A and B are constants.

3.3.3 The effect of forward current on recovery voltage

Figure 18 shows that by firing a short pulse during which the diode does not fully turn on, diode snap-off can be generated even in very low inductance circuits [45]. The pulse width is controlled by the size of the discrete circuit capacitance and circuit inductance. In addition the capacitance also controls the peak forward current (see section 3.2.2). Using the test circuit shown in figure 13 and the test method as described in section 3.2.2 the effect of peak forward current on the reverse recovery characteristic of the diode under test was investigated. The procedure described in section 3.3.2 was repeated with the exception that the circuit capacitance was varied.

FIGURE 16

Graph showing the variation of the ratio V_{pkr}/V_r with commutating dI/dt for various values of main circuit inductance.

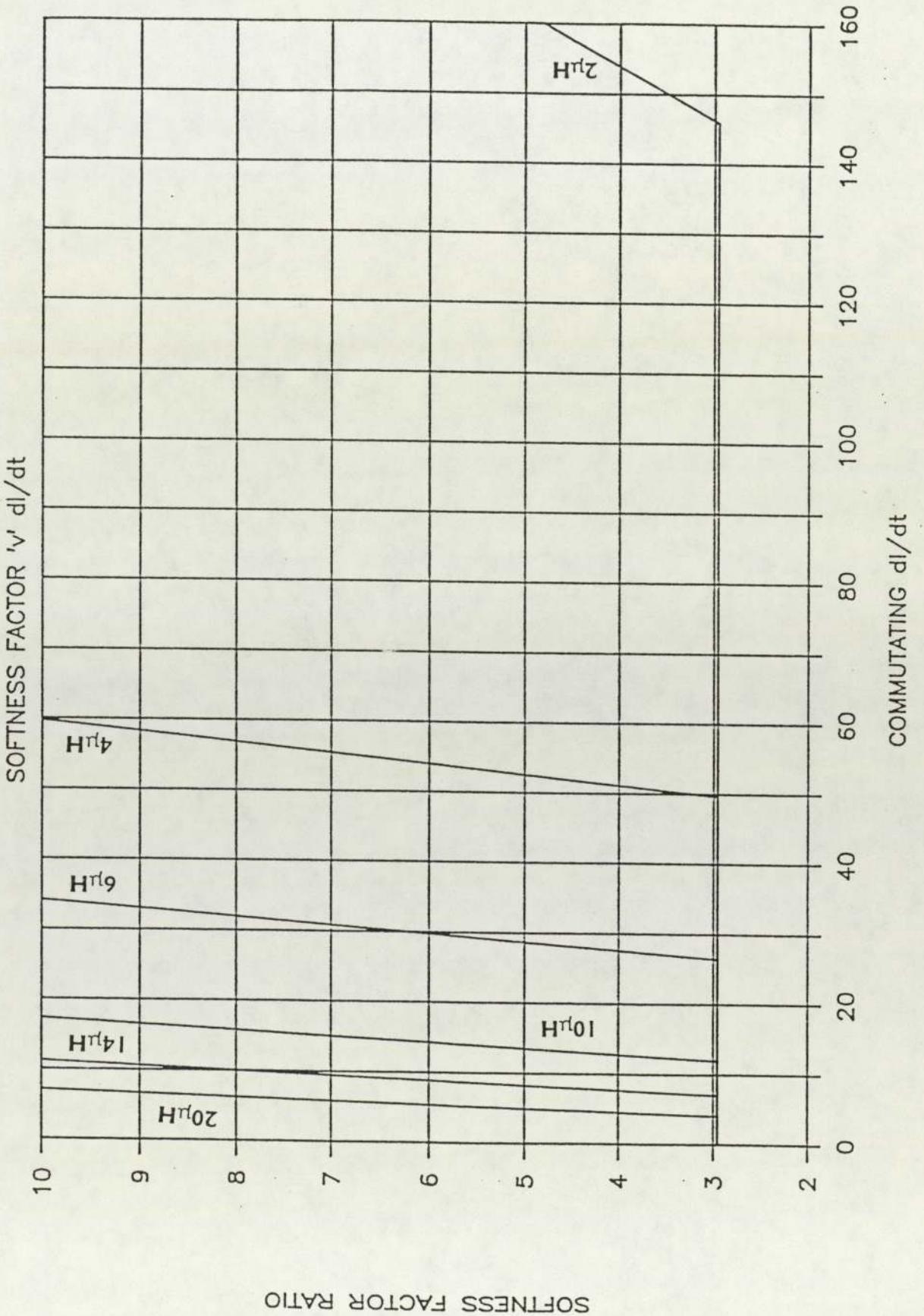


FIGURE 17

Graph showing the variation of critical dI/dt with main circuit series inductance.

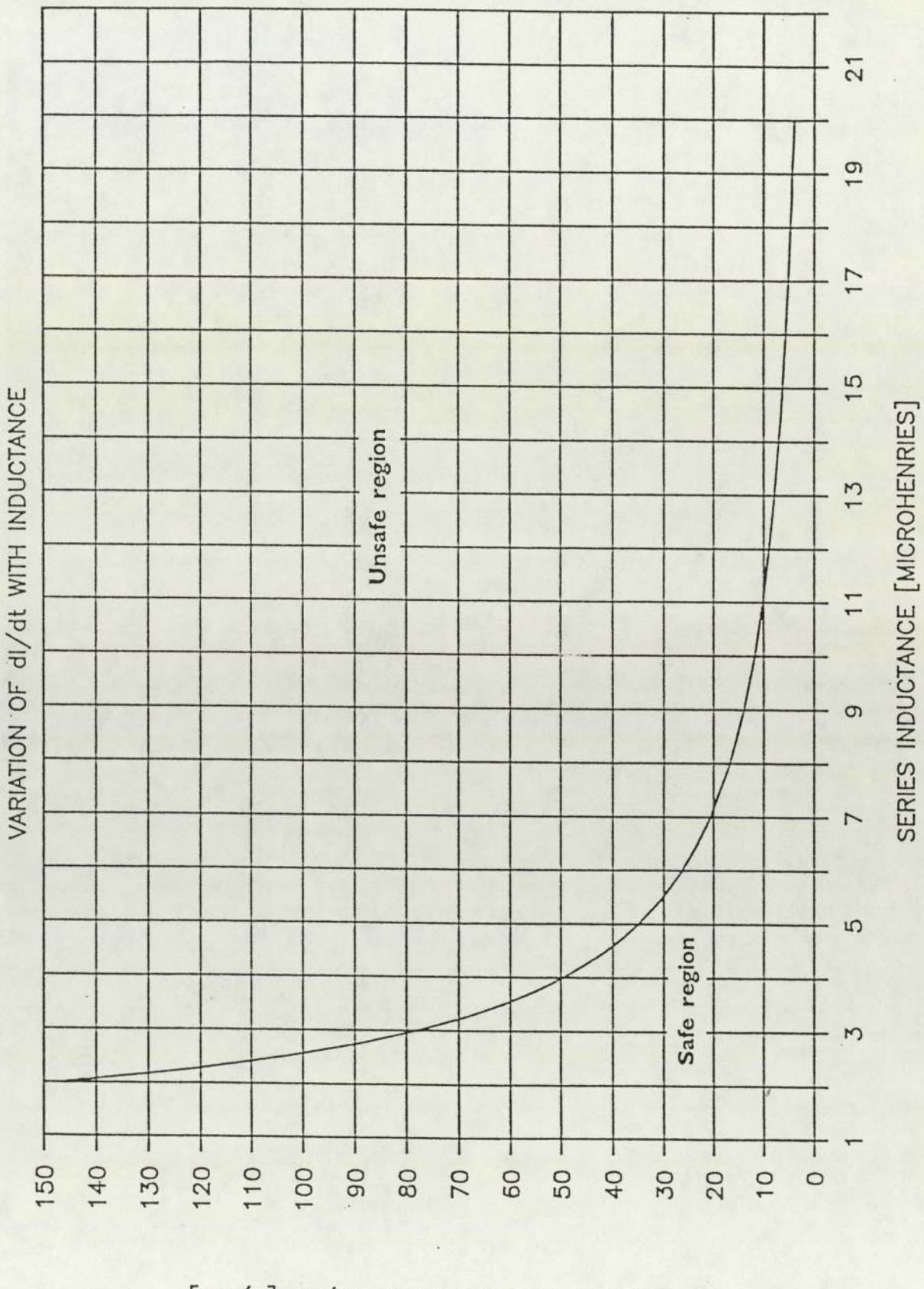
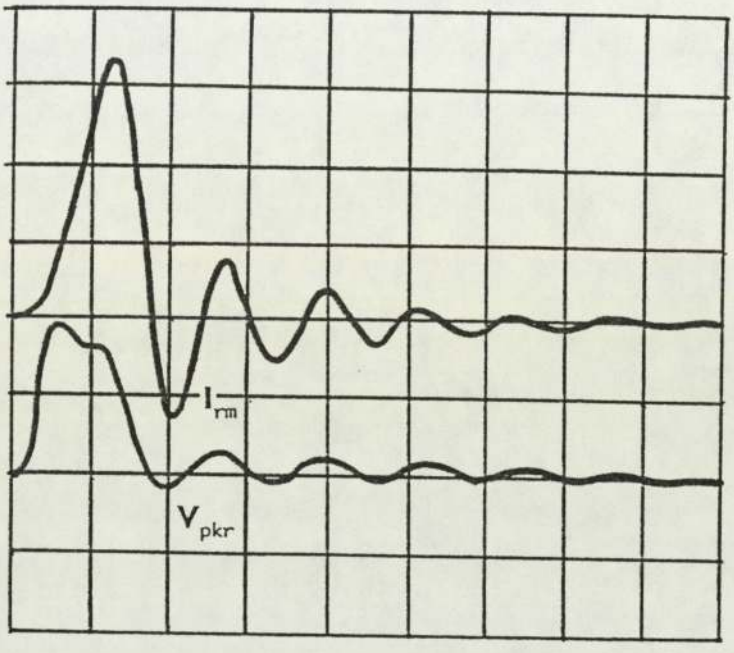


FIGURE 18

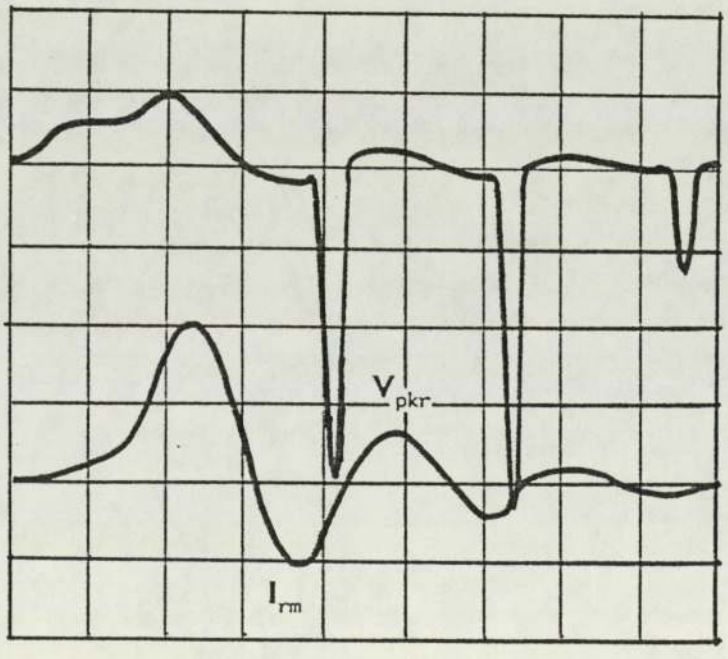
(a) Sketch of oscillogram showing oscillatory behaviour.
(b) Sketch of oscillogram showing voltage spike generation during oscillations.

(a)



V = 5V/Div
I = 10A/Div
t = 2us/Div
L_c = 0.8uH
C = 1uF

(b)



V = 20V/Div
I = 50A/Div
t = 1us/Div
L_c = 0.8uH
C = 0.5uF

Tests were thus performed with different values of circuit capacitance. From the results, curves of peak reverse recovery voltage against commutating dI/dt were constructed for each test circuit: as shown in figure 19.

Each curve obtained with a known value of capacitance produced the three region behaviour as previously described in section 3.3.1. As circuit capacitance is increased the dI/dt at which snap-off commences increases. The gradient of the curve prior to this critical dI/dt increases with increasing circuit capacitance. Thus for the same circuit inductance the commutating dI/dt at which snap-off occurs can be increased or lowered by increasing or lowering the forward current density just prior to current zero.

In the test circuit used to obtain the above results the peak forward current is governed by the circuit inductance, the circuit capacitance and the capacitor charging voltage. Thus:

$$I_{pkf} = (L_c.C)^{½} \cdot dI_f/dt \qquad \text{- (E13)}$$

where I_{pkf} = peak forward current

For the graph shown in figure 19; L_c, C and dI_f/dt are known, so therefore I_{pkf} may be calculated. Using figure 19 as the information basis, the critical dI/dt for each value of capacitance was calculated and then the peak forward current produced under that condition calculated. This calculated data was then used to construct a graph showing the variation of critical dI/dt with peak forward current (see figure 20). As the peak forward current is increased the critical dI/dt also increases.

Thus the worst case for diode snap-off will be a low forward current followed by a high commutating dI/dt.

There are two types of diode commutation [5]:

1) AC - DC commutation as shown in figure 21(a). Here the forward

FIGURE 19

Graph showing the variation of peak reverse recovery voltage with commutating dI/dt for various values of main circuit series capacitance.

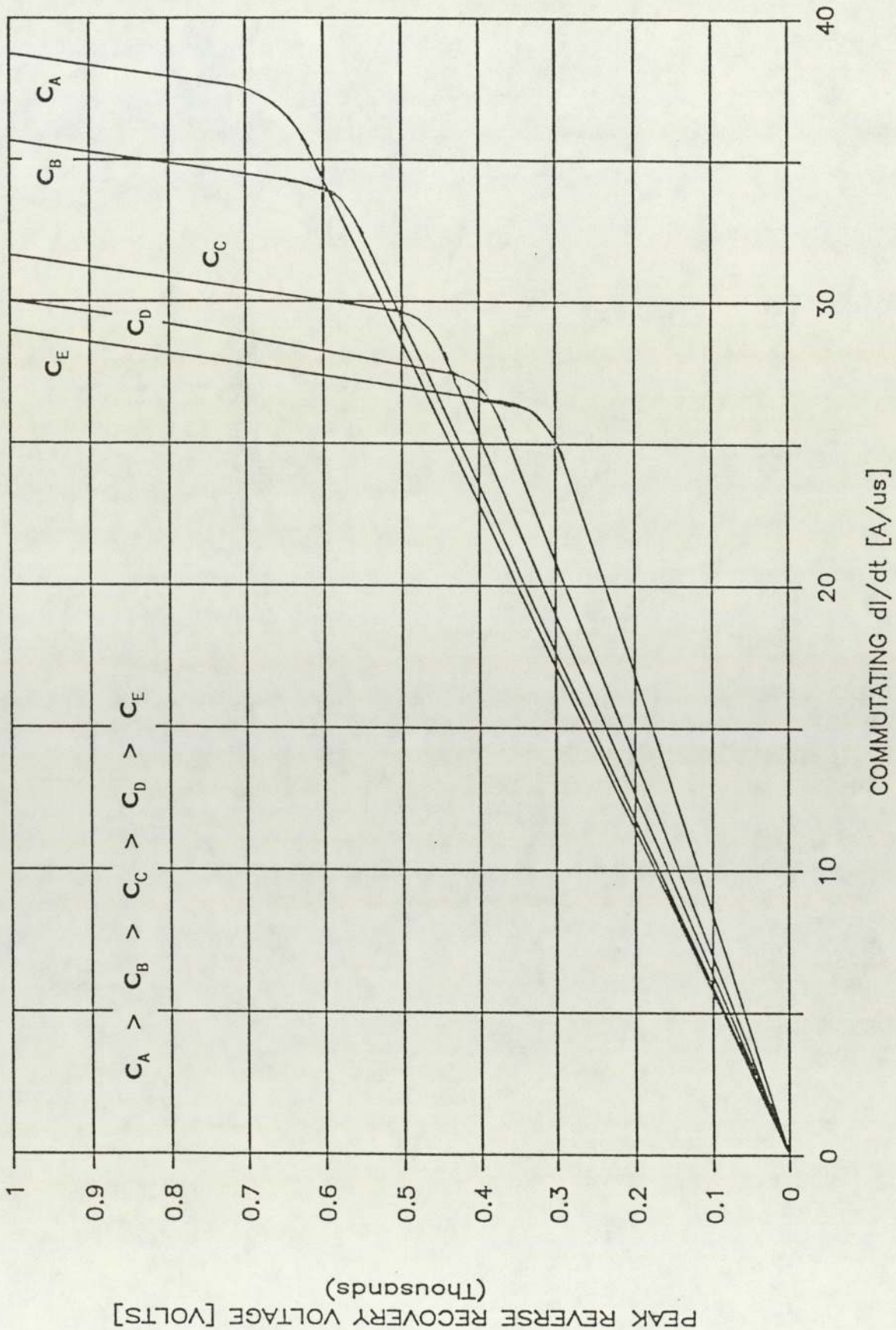


FIGURE 20

Graph showing the variation of peak forward current with critical commutating dI/dt.

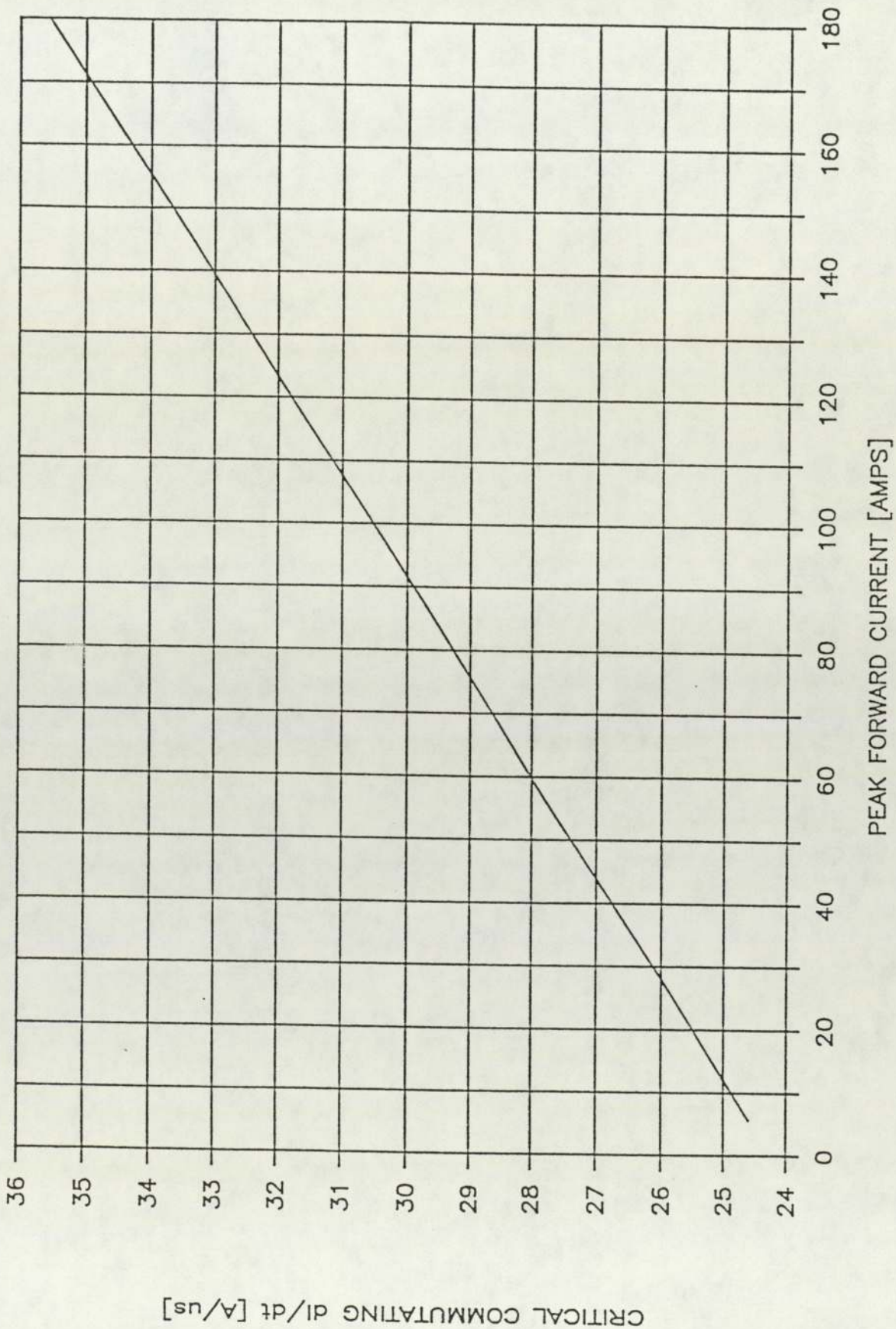
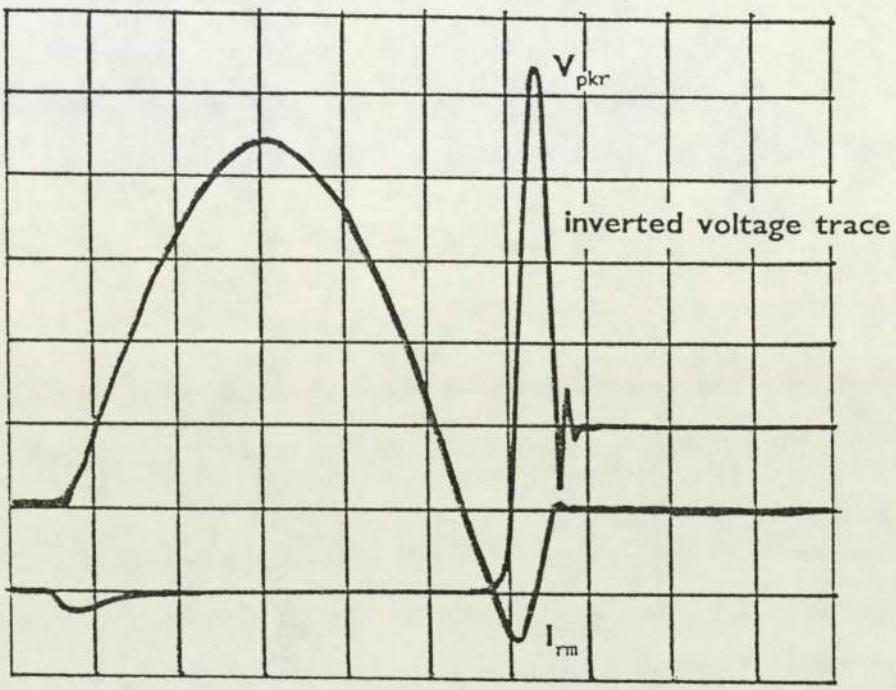


FIGURE 21

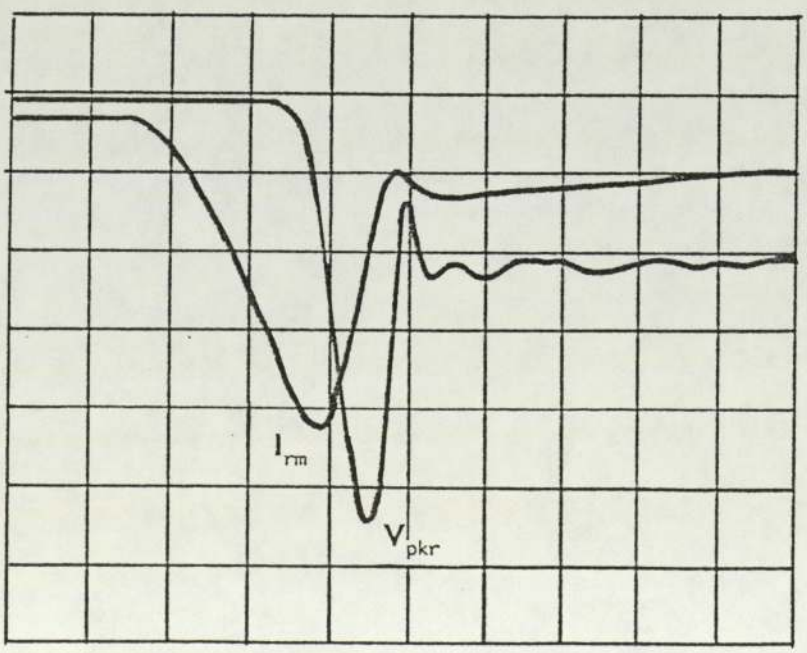
(a) Sketch of oscillogram showing normal diode recovery waveform with a sinusoidal current pulse.

(b) Sketch of oscillogram showing normal diode recovery waveform with a trapezoidal current pulse.

(a)



(b)



current pulse width represents a long time compared with the charge carrier lifetime.

2) DC commutation where a steady state current flows prior to current reversal as shown in figure 21(b).

By referring to figures 12(a) and 12(b) it can be seen that as the width of region B is varied both types of commutation can be found in GTO circuits.

In the case of AC - DC commutation, to achieve a high dI/dt a high peak forward current is required which in turn increases the stored charge of the diode. In the DC case the stored charge is proportional to the forward current but the commutation dI/dt may be varied independently. Thus a diode may be tested with a low I_f (forward current) and a high dI_f/dt.

Figure 22 shows a number of curves representing the variation of diode recovery current against time for various values of forward current. As the forward current is reduced the recovery characteristic of the diode changes from being soft to snappy - as illustrated by the oscillations on the current waveforms. The overvoltage produced by such oscillations would be equal to the product of circuit inductance and dI_r/dt.

The early work reported by Somos [5] was performed at relatively low dI/dt's (32 $A.\mu s^{-1}$) over a small forward current range (0 to 3A) and on alloyed diodes of small voltage rating. Modern day devices are however made with diffused junctions and operate at a high dI/dt's (100 to 1000 $A.\mu s^{-1}$) with large forward currents (up to 1000 A). Thus there was a need to investigate the transient behaviour of modern devices.

The circuit used in figure 13 to investigate the effect of forward current on snap-off was subject to the drawback of a linked forward current and commutating dI/dt. This effect can be calculated and allowed for as shown in figure 20 . However to decouple the commutating dI/dt from the peak forward current as Somos had done in previous work, the circuit shown in

FIGURE 22

Sketches of diode reverse current characteristic.

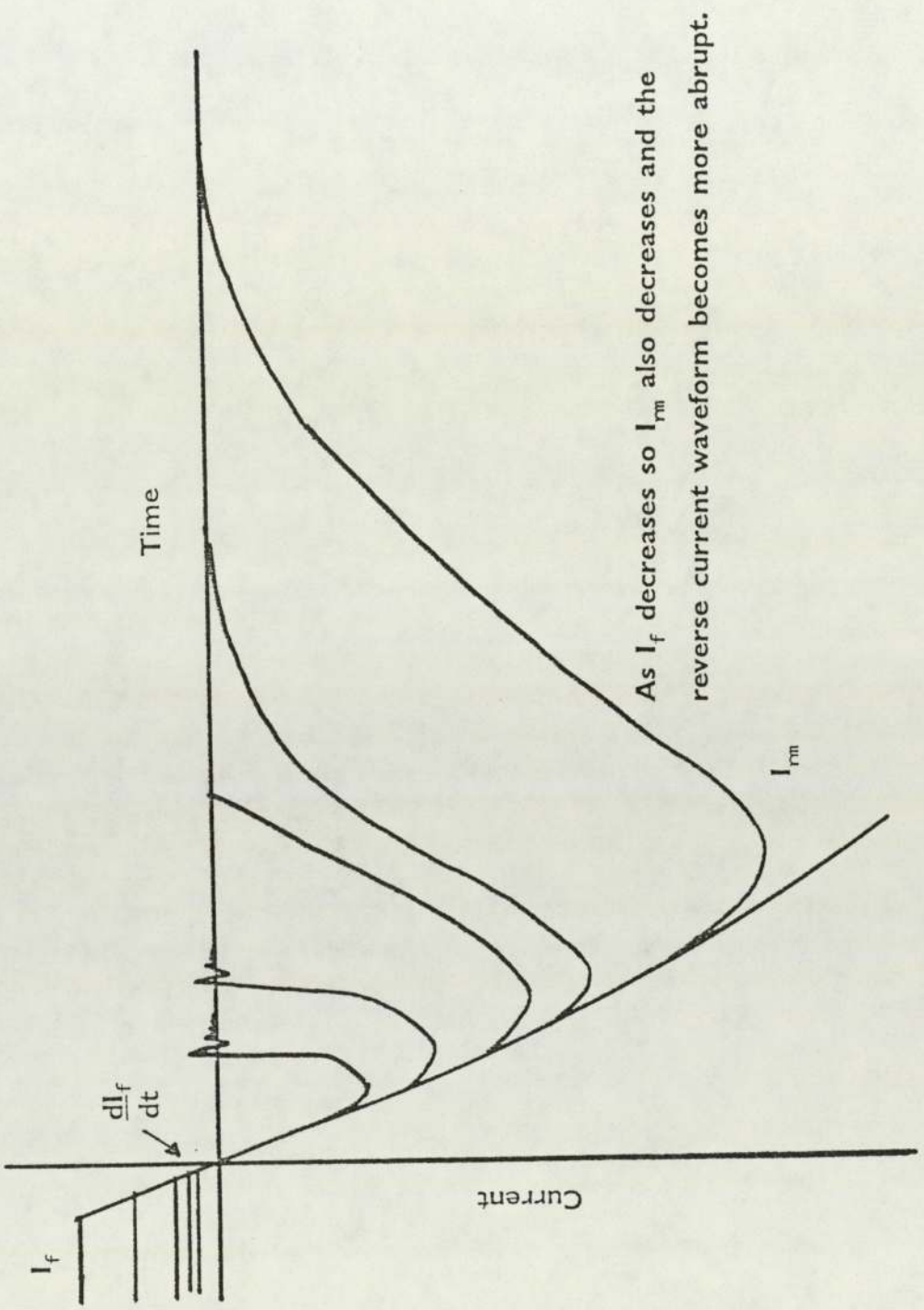


figure 23 was constructed. This differed from the Somos circuit but was used to determine if this previous work was valid for modern devices.

Using the circuit shown in figure 23 the reverse current waveform was closely monitored. The recovery times t_a (current zero to peak reverse current) and t_b (peak reverse current to second current zero) were measured for different values of peak forward current and commutating dI/dt. This data was used to calculate the snappiness factor S, (equal to the ratio t_b/t_a). A graph was then plotted (figure 24) showing the variation of S_n with commutating dI/dt for various values of forward current. The value S_n is equal to the ratio S/S_o. The quantity S_o is calculated by plotting a graph of S against dI/dt and extrapolating back to the point when dI/dt = 0 i.e. $S_o = S$ at dI/dt = 0. These curves show that as the commutating dI/dt is increased the recovery waveform become more abrupt. The change in abruptness becomes more rapid after a critical value of dI/dt is reached.

The experimental data can be replotted as curves showing the variation of S_n with forward current; as shown in figure 25. As the forward current prior to the commutating dI/dt is increased the recovery current waveform becomes softer. This work thus indicates similar conclusions can be drawn for diffused diodes undergoing snap-off to those postulated by Somos about alloyed rectifiers showing abrupt recovery.

3.3.4 **The effect of junction temperature on recovery voltage**

Chu et al [153, 154, 155] have investigated the variation of the t_a/t_b ratio with commutating dI/dt. The sequence of measurements were performed at two temperatures. From this information it can be inferred that the diode reverse recovery characteristic becomes softer as operating temperature increases. The work of Chu differs from this study in that at the experimental dI/dt's studied and in the low voltage diodes used, the snap-off effect was not observed.

All of the previous tests reported in this thesis were performed at room

FIGURE 23

Diagram of trapezoidal current pulse test circuit.

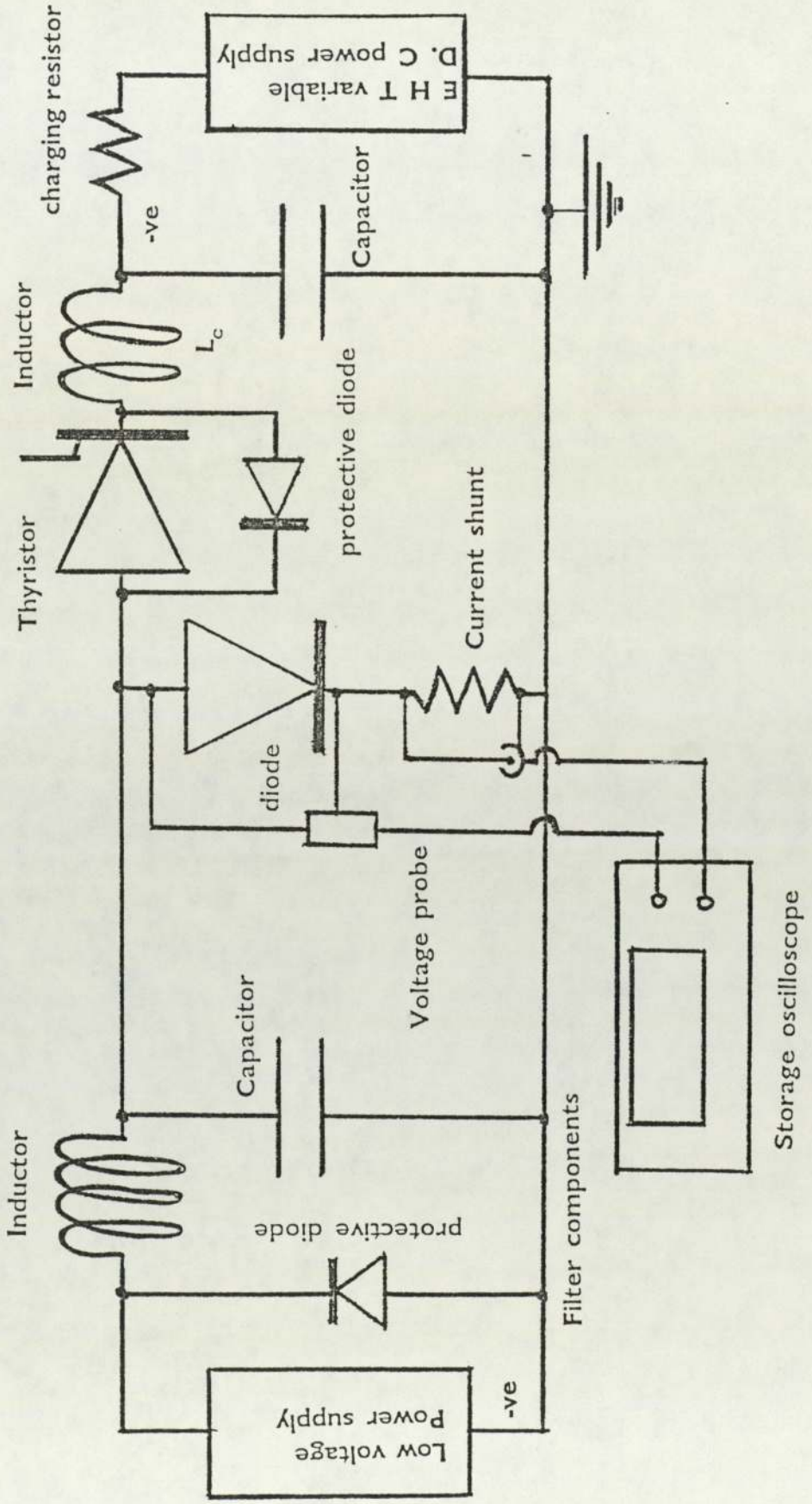


FIGURE 24

Graph showing variation of normalised snappiness factor S_n with commutating dI/dt for various values of constant forward current.

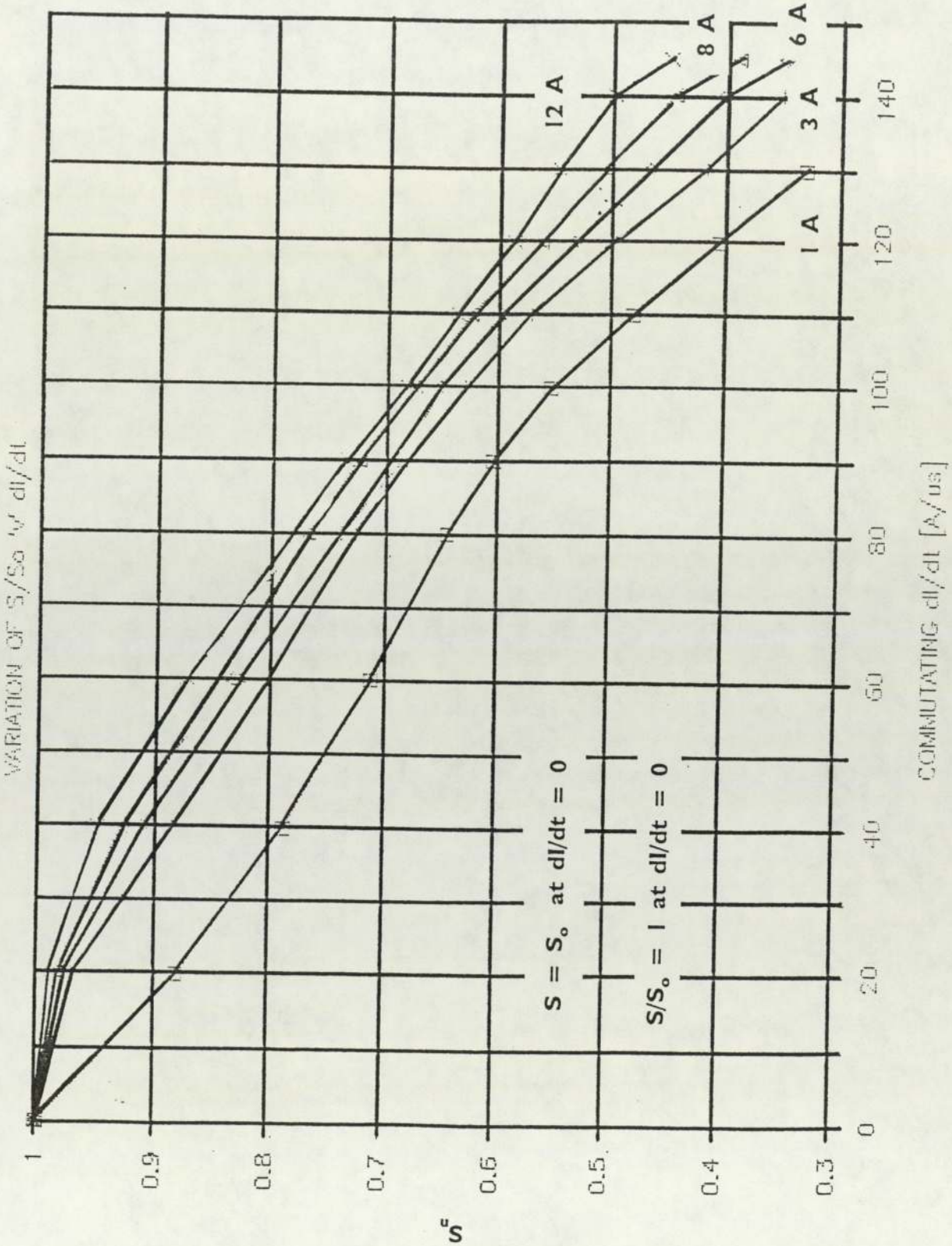
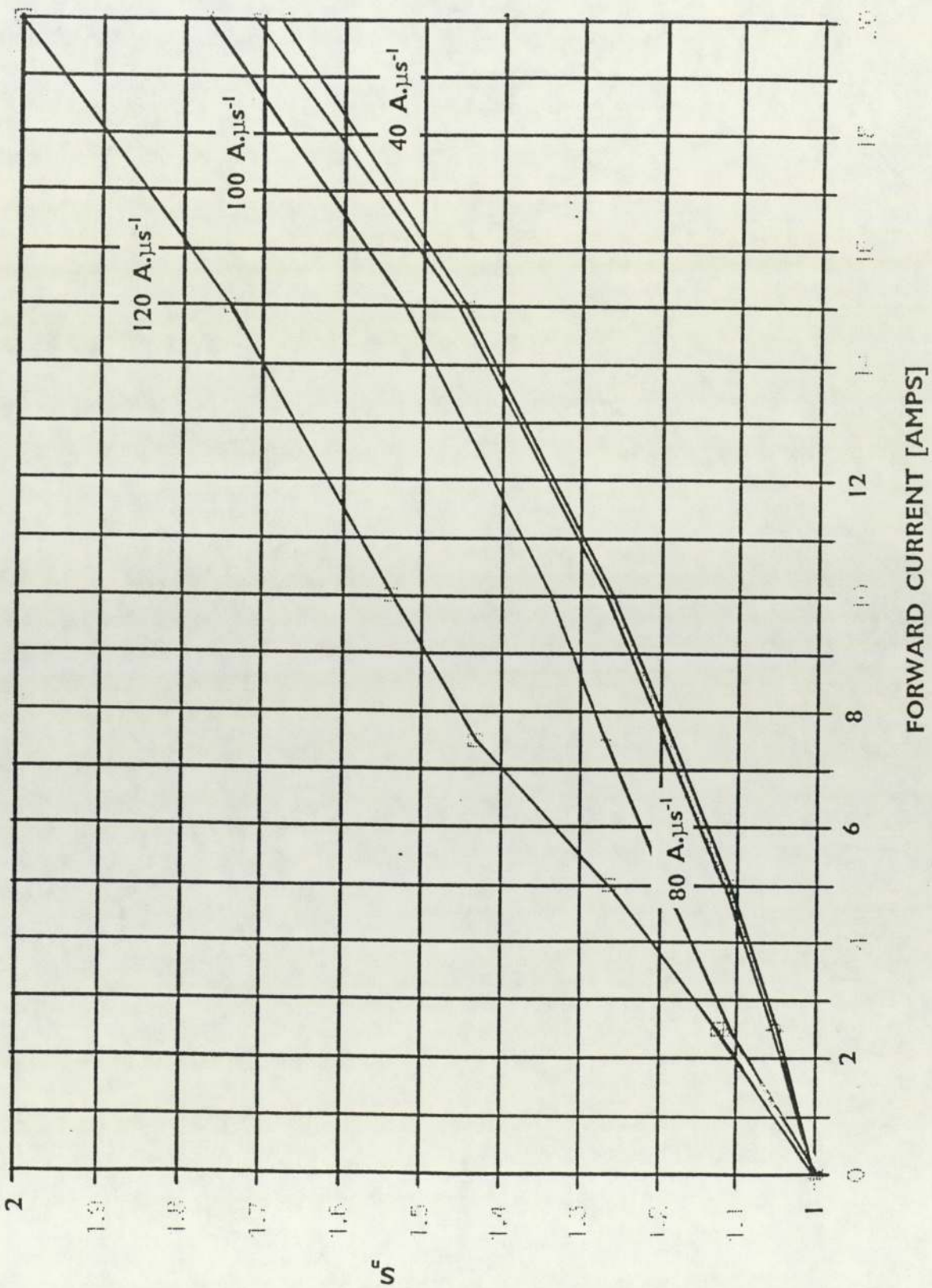


FIGURE 25

Graph showing variation of normalised snappiness factor S_n with forward current for various values of constant commutating dI/dt.



temperature (20 °C). Chu's work demonstrated the snappiness ratio has a temperature dependence (see also [126]). A test circuit that can be used to investigate this effect is shown in figure 26 . The pulse generating circuit and measuring instruments can thus be kept at room temperature during a series of tests, while the test diode can be placed inside an environmental chamber. The extension lead connecting the diode and circuit electronics consists of a high voltage co-axial cable to minimise increased circuit inductance. Since the increase in circuit inductance is negligible the data obtained could then be compared to previous results. Figure 27 indicates how the diode recovery characteristic varies with temperature.

Generally snap-off is worst at low temperatures and the critical dI/dt as which snap-off occurs increases with temperature. It is interesting to note that as device stored charge increases so does the critical dI/dt at which snap-off occurs. The stored charge can be increased by either increasing the forward current or by increasing the carrier lifetime. Both of these measures increase the number of carriers prior to commutation. Increasing the temperature of a device increases the number of thermally generated carriers. Thus it can be inferred that snap-off occurs in devices with shallow carrier concentration gradients across the base width of the diode.

3.3.5 **The design of high voltage, high power, soft recovery snubber diodes**

The work described in sections 3.3.1 to 3.3.4 inclusive show how the device operating conditions influence the transient diode performance. These operating conditions are imposed upon the device either by the external circuit or surrounding environment and are thus independent of the diode construction. The work described in the following sections demonstrates how the transient diode performance is dependent upon the device construction. Prior to this text, the following section gives an overview of high voltage, high power design trade-offs [153,155,156,162,163,164,165,192,210], as this will aid the reader in the understanding of sections 3.3.6 to 3.3.9 inclusive.

High power semiconductor devices use the same basic physical effects as low

FIGURE 26

Diagram showing synthetic test circuit to investigate the effect of temperature.

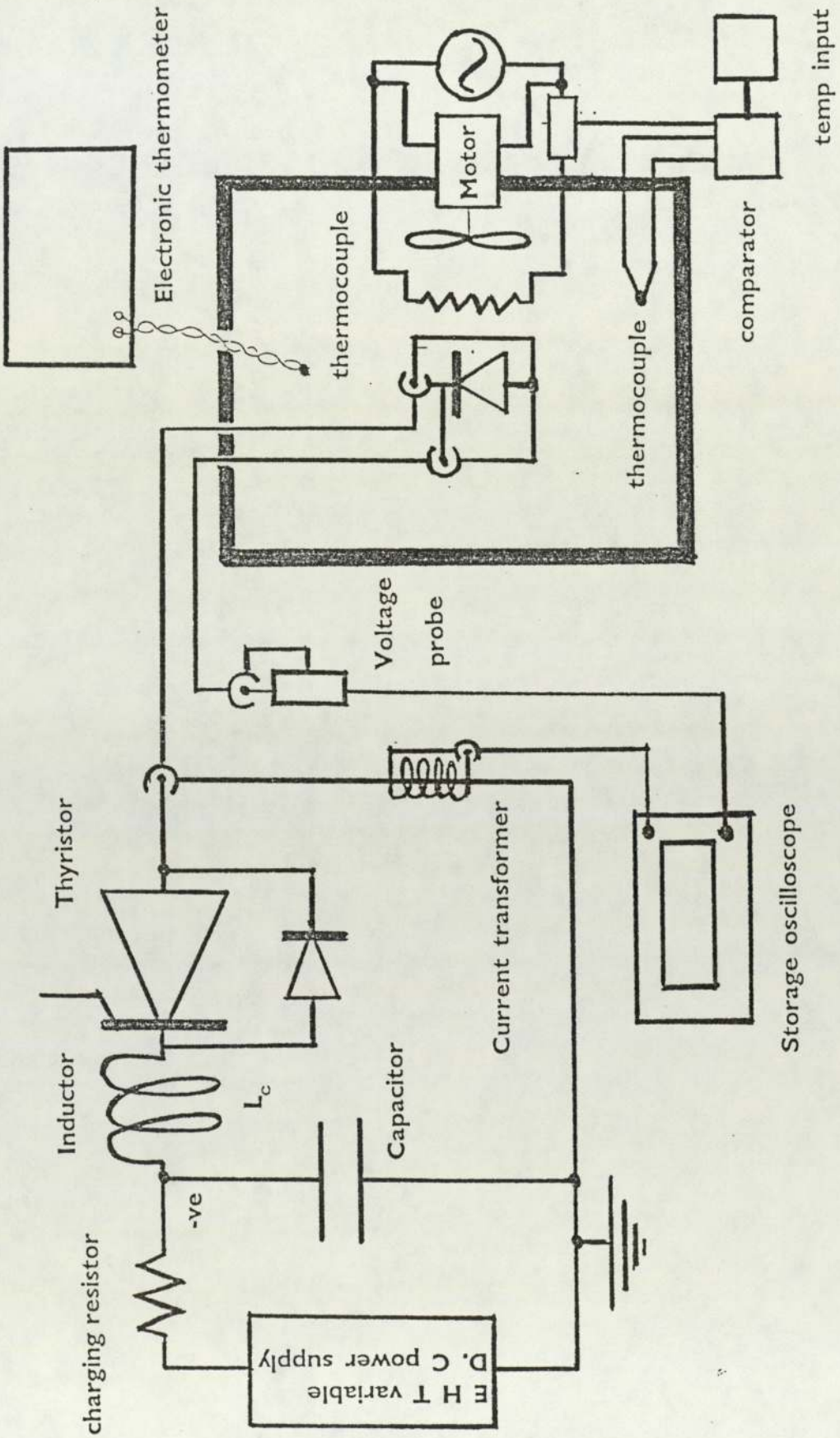
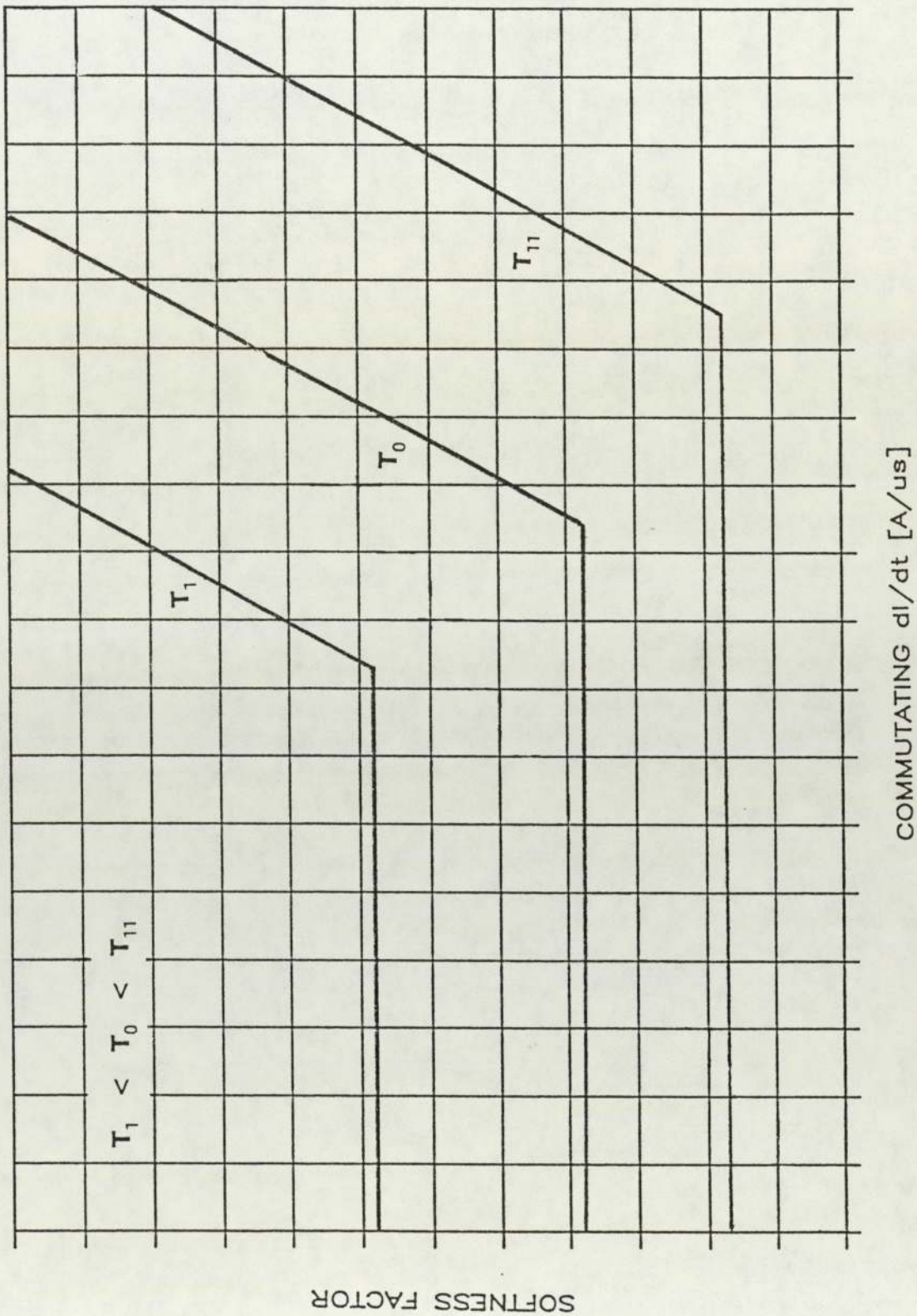


FIGURE 27

Graph showing the variation of the ratio V_{pkr}/V_r with commutating dI/dt for different values of temperature.



power devices, yet in terms of construction these two types of device have very little in common. Low power devices are primarily intended for use in a signal processing role, while high power devices are intended to have a control application.

The requirements of power handling forces the adoption of many novel structures to overcome the problems associated with the electrical characteristic of a simple PN junction.

As the power handling capability of individual devices has increased, it has done so in terms of voltage rating, current rating and frequency rating. Thus to achieve a high voltage blocking capability, the structure must involve a wide and a lightly doped base region. A lightly doped region has a high resistance which if conductivity modulation were not present would impede current flow. Thus in power structures minority carrier devices are more widely used than majority carrier devices such as field effect transistors or Schottky diodes [129]. The presence of a wide conductivity region in a power device with a long carrier transit time introduces some drawbacks associated with the minority carrier storage effect [3]. Thus the stored charge of a power device limits the frequency at which it can be used. To gain an increase in the operating frequency, the stored charge must be limited by lifetime killing techniques [16] which reduce the excess carrier lifetime.[36]

As the area of the device is increased (usually to increase the device current rating), the frequency problem becomes more acute. An increase in junction area may reduce the ohmic volt drop but it also increases junction capacitance and increases the stored charge. Both of these changes have serious detrimental effects on the frequency performance of the diode. As operating frequency increases the switching losses far exceed the conduction losses. Thus scaling up of a device in geometrical terms will not necessarily increase the power handling capability by a proportional amount.

The impurity concentration profile of most high power diodes is not that of the well documented simple PN structure. High power diodes tend to have a

multilayer structure of which the most common is that shown in figure 28(a). In this configuration the diode is formed from a wide, weakly doped base region which is situated between a heavily doped P region and a heavily doped N region. The base region is sufficiently large to accommodate the reverse bias space charge region and the N^+ layer (or the P^+ layer in the case of a P base diode) provide a low resistance contact at the silicon to metal interface.

These $P^+.N.N^+$ and $P^+.P.N^+$ behave very differently in terms of reverse recovery performance to the classic PN structure [40,43]. At low frequencies the P.i.N structure behaves very similarly to a PN junction but at high frequencies it exhibits a variable resistance [41].

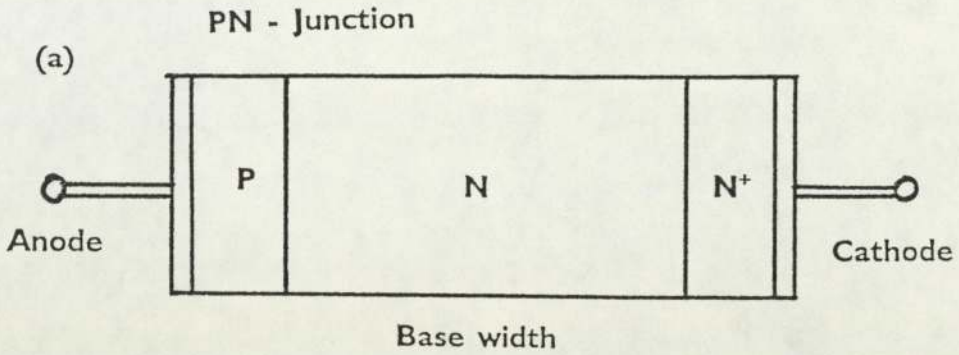
Various methods are available to produce the soft recovery characteristic that is desirable in high power circuits. Each method has the common approach of causing the diode junction to recover as quickly as possible and then to have a reservoir of charge away from the junction that may be extracted over a longer time period to produce the soft recovery current tail. This strategy may be contrasted with the boff diode [4] described in section 2.3.4.

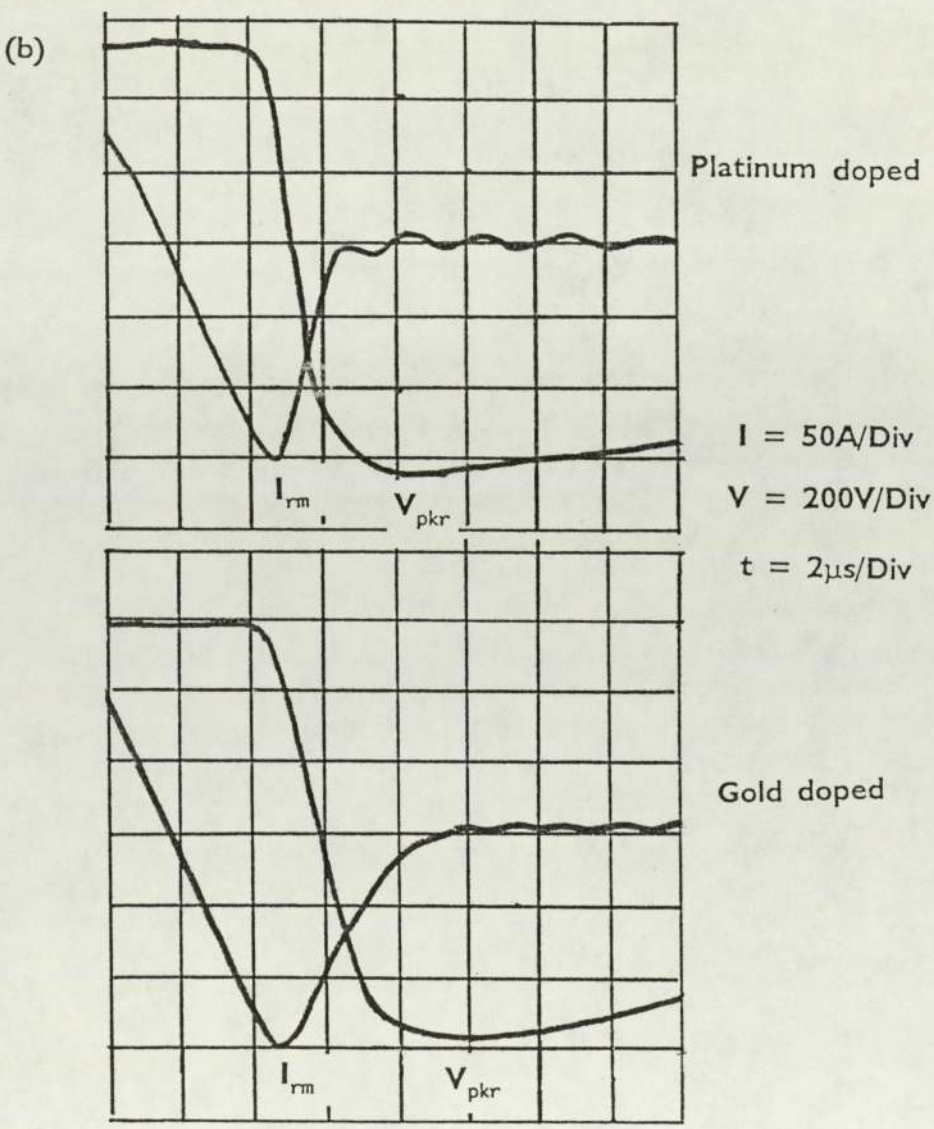
The use of a wide base region increases the post junction recovery carrier storage effect. Thus use of a high resistivity starting material enables the extraction of stored charge after the junction recovery to occur at a slower rate producing a soft recovery current tail. The introduction of a lifetime gradient in the diode base region also enhances the production of a soft recovery characteristic if the high life-time region is away from the junction. Over the past few years this technique has proved successful in providing industry with high power soft recovery diodes. Unfortunately it has been identified [45] that this soft recovery characteristic is not present under high stress conditions. In such circumstances diode snap-off occurs generating severe voltage transients.

Another theoretical method to achieve a soft recovery characteristic is to produce a built in electric field within the junction. However, this is not practical for high power devices since the doping gradient required to produce

FIGURE 28

(a) Diagram of the multilayer structure of a diode.
(b) Sketches showing diode recovery for Gold doped and Platinum doped diodes.





such a field would prevent the device from achieving a high voltage rating. A high voltage blocking capability is essential for high power rectifier operation.

3.3.6 **The effect of diode base width on recovery voltage**

It has been shown that certain physical parameters influence the reverse recovery waveform of a diode [5]. To investigate the effect of base width a series of diodes of different base widths were tested by Somos. The base width of the diode is responsible for the voltage withstand rating of the diode [164] as governed by equation (E14).

$$V_m = d^2.q.N_n / 2.\varepsilon \qquad \text{- (E14)}$$

where V_m = Maximum reverse voltage withstand
d = Base width
q = Electronic charge
N_n = Density of donor atoms
ε = Dielectric constant of Silicon

The base width is either the width of the P region in a N^+P junction or the width of the N region in a P^+N junction. The dI/dt was kept constant during the tests and in each case the same peak reverse recovery current was reached. Differences in the recovery current only appeared after peak current - this is the point at which the recovery current ceases to be determined by the external circuit and is predominantly dependent on the diode. In these tests the recovered charge was found to increase with the base width. In addition increasing the base width effectively increases the bulk recovery time and modifies the abrupt recovery waveform to a soft recovery waveform in which the current falls smoothly to zero.

The diodes tested by Somos were of a low voltage alloyed type in a low (25 $A.\mu s^{-1}$) commutating dI/dt circuit. The diodes used to-day are generally of the diffused type and used in high (100 to 1000 $A.\mu s^{-1}$) commutating dI/dt circuits. Such high power rectifiers are usually designed using high resistivity N-type

silicon as the starting material. As in alloyed diodes the voltage rating is governed by the base width of silicon. Thus to achieve a high voltage rating the diode must either have a very wide region or a high resistivity starting material (in practice both are used).

Chu et al [153,154,155] have published details of a series of experiments on P.I.N structures. By varying the diffusion profiles and junction depths different values of base thicknesses were obtained. By testing this set of diodes in the JEDEC [264] circuit Chu was able to produce a graph showing the variation of the t_a/t_b ratio against base width. In this graph the recovery waveform appears to become softer as the base width is increased.

In my experience as the voltage rating of a diode generic type increases, the recovery waveform at low dI/dt's (i.e low stress conditions) becomes progressively softer. Again this is due to the manufacturers practice of increasing the device voltage rating by increasing the device base width.

3.3.7 **The effect of lifetime killing techniques on the recovery voltage**

The amount of charge stored in a diode during the on state is proportional to the volume of silicon in the diode. As the base width of the diode is increased to attain the desired voltage rating so the volume of diode silicon increases and thus the stored charge also increases. To reduce the stored charge in high voltage diodes, so called 'lifetime killing' techniques are employed [14, 17, 20, 23, 26]. Such methods depend on the relationship between stored charge and carrier life time, [70] which is:

$$Q_s = I_f \cdot \tau \qquad \text{- (E15)}$$

where Q_s = stored charge

I_f = steady state forward current

τ = carrier lifetime

Thus by reducing the carrier lifetime, the stored charge for a known forward

current can be reduced. As the carrier lifetime is reduced so the forward voltage drop of the diode is increased and thus the power dissipation of the diode also increases. Thus in $P^+.N.N^+$ structures there is a trade off between base width, resistivity and carrier lifetime. It seems though that the balance between these parameters will need to be altered if future diodes are to be optimized [30] for a snapless performance characteristic.

The conventional technique for lifetime control is gold diffusion [15]. The gold atoms diffused through the silicon lattice deform the structure and introduce free carrier traps (see section 4.6.1). An alternative dopant is Platinum [22,24,25] which increases the maximum operating junction temperature relative to gold and is therefore being increasingly used in place of Gold. In both cases the carrier lifetime is controlled by the diffusion process, i.e. temperature of diffusion, length of time of 'drive' and concentration of dopant at the silicon surface. A third technique is that of electron irradiation [18,19,21]. Irradiation introduces lattice damage and thus carrier traps into the silicon lattice. The carrier lifetime is controlled by the radiation dose and by annealing [29,32] the lattice structure after irradiation.

Houston et al [206, 209] have shown that each technique alters the snappiness of the device in a different way. Thus diodes that have been treated in different ways to produce the same recovery time show different reverse recovery characteristics. Houston has published data showing some recovery characteristics of four physically similar diodes that have been treated by different lifetime killing techniques. Each technique drastically reduces the recovery time, the peak reverse current and the stored charge. The snappiness ratio also improves with lifetime killing. A superficial analysis of these results indicates that lifetime killing improves the recovery characteristics of the diode. This is true for the peak reverse recovery current and for recovery time but may not be true of the softness of the recovery waveform. It is known that current 'chop-off' and oscillation effects have been found in certain Gold doped diodes [96].

Vitins et al [165] have compared the effect of Gold and Platinum diffusion on

the recovery characteristics of diodes. Figure 28(b) shows sketches of Gold and Platinum doped diodes undergoing reverse recovery. Although both lifetime killing techniques result in the same junction recovery time, the recovery voltage generated by the platinum doped diode is very much softer. This effect is due to the absolute carrier lifetime and also to a carrier lifetime gradient (or rather lack of it to produce abrupt recovery) across the diode base width. This effect is dealt with in section 3.3.9.

3.3.8 **The effect of device fabrication material on recovery voltage**

Assalit et al [162] have studied the production of a soft recovery characteristic in electron irradiated diodes by using various combinations of low resistivity starting material and wide base widths. Instead of using the t_a/t_b ratio as a measure of snappiness a set of four classes of recovery were suggested in their paper and the test diodes were classified in these groups for different base widths and silicon resistivity. These results indicated that for a certain resistivity the softness of the diode increased as the base width was increased. In addition for a constant base width the softness of the diode recovery was enhanced as the resistivity of the silicon was decreased.

3.3.9 **The effect of doping profile on recovery voltage**

Diffused dopant lifetime killing techniques have the advantage of not only reducing the recovery time but also promote a soft recovery characteristic [60,61].

The reasons for achieving an abrupt recovery characteristic have previously been outlined in section 2.3.4. Diffused dopants effectively introduce a carrier lifetime gradient throughout the diode [11, 28, 97] and thus produce the opposite effect to that of the carrier profile in a snap diode. Specifically, the high lifetime region is furthest away from the junction. Consequently a proportion of the stored charge is unavailable for immediate extraction when a reverse bias is applied. The reverse current therefore gradually taper off in the form of the characteristic soft recovery current tail.

Electron irradiation produces a carrier lifetime profile that is constant over the base width of the diode. This inevitably produces a more abrupt recovery waveform than a diode with the same t_a (junction recovery time) that has been produced by a diffused lifetime technique.

Although diffused dopant lifetime killing techniques improve the soft recovery characteristic of the device, they are detrimental to the on-state losses. One possible method of achieving a low on-state loss and a soft recovery characteristic could be by employing a step carrier density profile introduced by proton irradiation [13,14]. By reducing the carrier lifetime in a targeted segment of the diode base width, the diode recovery time may be reduced at the same time as minimising the increase in on-state losses. Therefore if the proton irradiation is applied close to the blocking junction then the peak reverse current will be reduced since initially few carriers will be available for extractions. The recovery current after peak reverse current will be 'boosted' by carrier diffusion from the high lifetime region. Thus the diode recovery will have a soft recovery current tail. A soft recovery characteristic obtained in this manner will also have a lower forward drop than a diode whose recovery characteristic has been engineered by conventional techniques.

3.4 Experimental Conclusions

It is likely that given an unfavourable combination of circumstances, all soft recovery diodes can be made to produce excessive voltage spikes due to a snap-off or current chop-off phenomenon. The point on a diode performance curve at which snap-off will occur is determined by: a) the circuit arrangement, b) the operating conditions, c) the diode design.

a) The circuit arrangment

1) As the main circuit series inductance is increased so the peak reverse recovery voltage increases.

2) As the main circuit series inductance is increased so the critical commutating dI/dt at which diode snap-off occures decreases.

3) As the value of parallel capacitance is increased so the magnitude of the initial voltage spike decreases (see section 5.3.2).

4) The critical commutating dI/dt is independent of the value of parallel capacitance (see section 5.3.2).

5) As the value of parallel resistance is decreased so the peak reverse recovery voltage decreases (see section 5.3.4).

6) As the value of parallel resistance is decreased so critical commutating dI/dt increases (see section 5.3.4).

7) As the value of parallel connected inductance increases so the value of critical commutating dI/dt decreases (see section 5.3.5).

8) The peak reverse recovery voltage is an complex function of parallel circuit inductance (see section 5.3.5).

9) The effect of series connected devices and inductive, resistive, capacitive snubbers on both the peak reverse recovery voltage and critical commutating dI/dt is a complex function governed by the above rules (see section 5.3.6).

b) The operating conditions

1) As the magnitude of the peak forward current increases so the critical commutating dI/dt increases.

2) As the pulse width of the forward current decreases so the critical commutating dI/dt decreases.

3) As the junction temperature increases so the critical commutating dI/dt increases.

4) As the commutating dI/dt is increased so the peak reverse recovery voltage increases proportionally until a critical dI/dt is reached after which diode snap-off occurs.

c) The diode design

1) As the base width (voltage rating of the diode) is increased so the soft recovery characteristic is enhanced.

2) As the junction area of the diode is increased so the soft recovery characteristic is enhanced.

3) As the resistivity of the diode silicon is decreased so the soft recovery characteristic is enhanced.

4) As the carrier lifetime is increased so the soft recovery characteristic is enhanced.

5) As the carrier lifetime profile becomes more 'flat' across the base width of the diode so the recovery characteristic becomes more abrupt.

4. DEVICE MODELLING

4.1 Numerical measures of diode snappiness

To be consistent with the declared mathematical modelling strategy described in section 2.1 a method of presenting results in an easily understandable form was sought. In parallel with the experimental investigations and modelling process the question of the validity of snappiness measures was considered. Thus by adopting a suitable measure of diode snappiness, the experimental and simulation results could be more readily compared and their significance easily digested.

Figure 9(b) shows how the reverse current waveform can be split into a region t_a (the time from current zero to peak reverse current) and a region t_b (the time from peak reverse current to second current zero). It should be noted that the time t_a is not the same as the time t_s (although in many cases they are numerically similar). In addition the recovery time t_{rr} is larger than t_s, since t_s is measured to the point of junction recovery and t_{rr} is measured to the cessation of the transient reverse recovery current. Thus t_{rr} is equal to the sum of t_a and t_b.

A numerical measure of diode snappiness can be achieved by taking the ratio of these two time periods. Various authors use this method but define the ratio differently. Thus Vitins et al [165] and Ramsbottom [160] have used the ratio of $K=t_a/t_b$. The alternative ratio of $S = t_b/t_a$ has been used by Chu et al [155], Eriksson et al [168] and Houston et al [206, 209] (see also [231]).

These ratios are referred to as the t_a/t_b or t_b/t_a ratios or they may be called the as softness ratio, softness factor, snappiness ratio, snappiness factor, wave shape factor or recovery factor [153].

For diodes undergoing normal reverse recovery in a simple LCR circuit these ratios can be used to both compare snappiness in different diodes and to predict the level of peak recovery voltage.

Figure 9(b) shows that:

$$\frac{dI_f}{dt} = \frac{I_{rm}}{t_a} \quad \text{- (E16)}$$

and

$$\frac{dI_r}{dt} = \frac{I_{rm}}{t_b} \quad \text{- (E17)}$$

$$\text{Defining } S = t_b/t_a \quad \text{- (E18)}$$

then from (E16) and (E17)

$$S = \left[\frac{dI_f}{dt}\right] \cdot \left[\frac{dI_r}{dt}\right]^{-1} \quad \text{- (E19)}$$

$$\text{Now } V_{pkr} = V_L + V_r \quad \text{- (E20)}$$

$$\text{and } V_L = L_c \cdot \frac{dI_r}{dt} \quad \text{- (E21)}$$

$$\text{therefore } V_{pkr} = L_c \cdot \frac{dI_r}{dt} + V_r \quad \text{- (E22)}$$

By assuming a small circuit resistance, a substitution for L_c may be made into (E22) by using equations (E8) and (E9) to produce:

$$V_{pkr} = V_r \cdot [\, 1 + (dI_r/dt) / (dI_f/dt) \,] \quad \text{- (E23)}$$

From equation (E19), equation (E23) becomes:

$$V_{pkr} = V_r \cdot (1 + S^{-1}) \quad \text{- (E24)}$$

In theory these equations could be used by the circuit designer to predict the voltage overshoot. However, in practice the situation is much more complex.

Figure 29(a) shows a diagram of an inverter [74]. During GTO turn-off, the diode commutation can be represented by the equivalent circuit shown in figure 29(b). The maximum circuit commutating dI/dt is governed by the stray circuit inductance and the level of forward current.

Since $V_r = I_{pkf} \cdot (L_c/C)^{½}$ - (E25)

and $V_r = L_c.dI_f/dt$ - (E26)

then by combining (E25) and (E26) to eliminate V_r, the following equation is produced:

$dI_f/dt = I_{pkf} \cdot (L_c.C)^{-½}$ - (E27)

Equation (E27) can therefore be used to calculate the commutating dI/dt for a known circuit inductance and operating forward current (assume circuit capacitance is constant and substitute the value of stray inductance for the circuit inductance in the above equation).

For a known circuit capacitance of 0.72μF and a 600A turn-off current, the variation of maximum circuit commutating dI/dt with stray circuit inductance can be calculated and used to construct the graph shown in figure 30(a).

Figure 30 (b) shows the variation of diode peak reverse recovery voltage for different values of stray circuit inductance. These curves were calculated assuming a snappiness ratio S equal to unity.

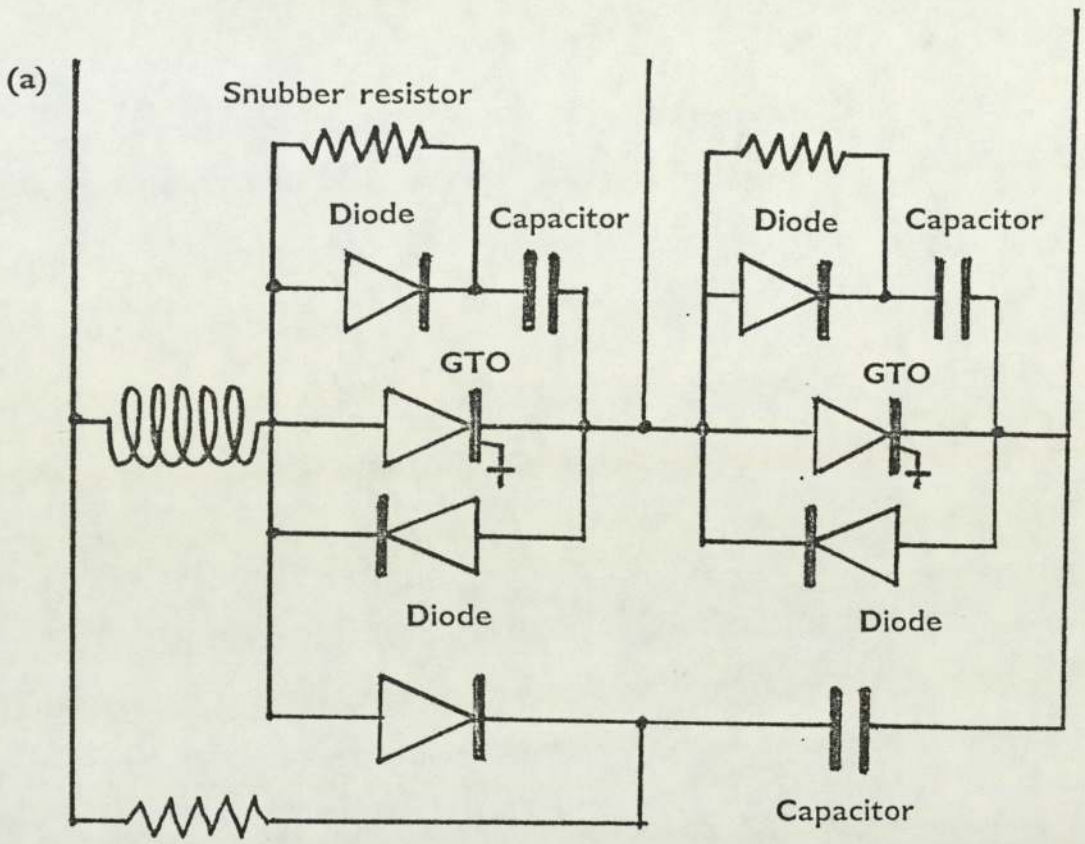
Thus in the case when S = 1 then $dI_f/dt = dI_r/dt$ and therefore

$V_{pkr} = L_s.dI_f/dt + V_r$ - (E28)

(where L_s = stray circuit inductance).

FIGURE 29

(a) Schematic circuit diagram of an inverter.
(b) Equivalent circuit during diode snubber duty.



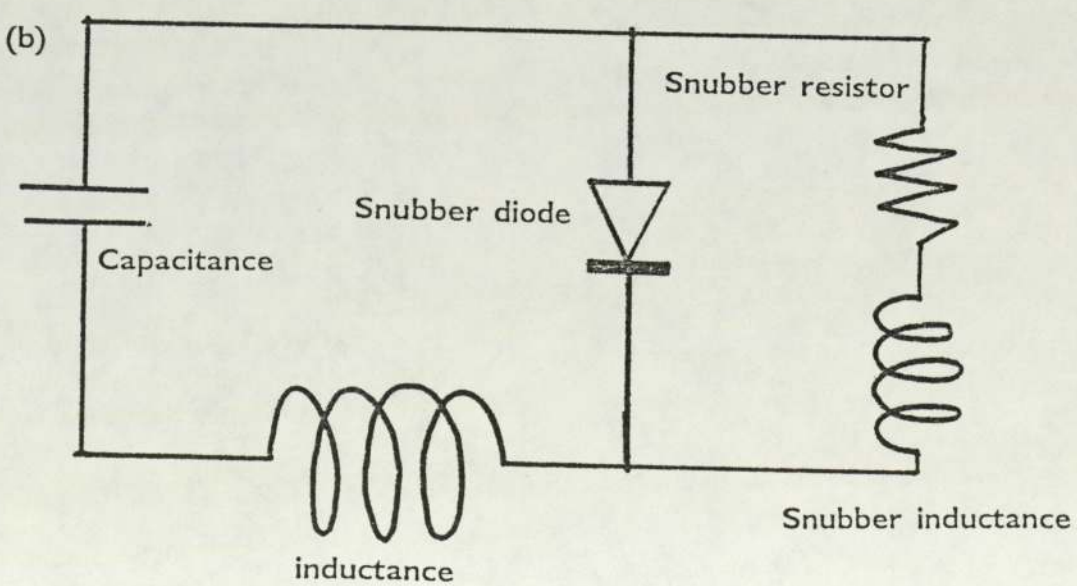
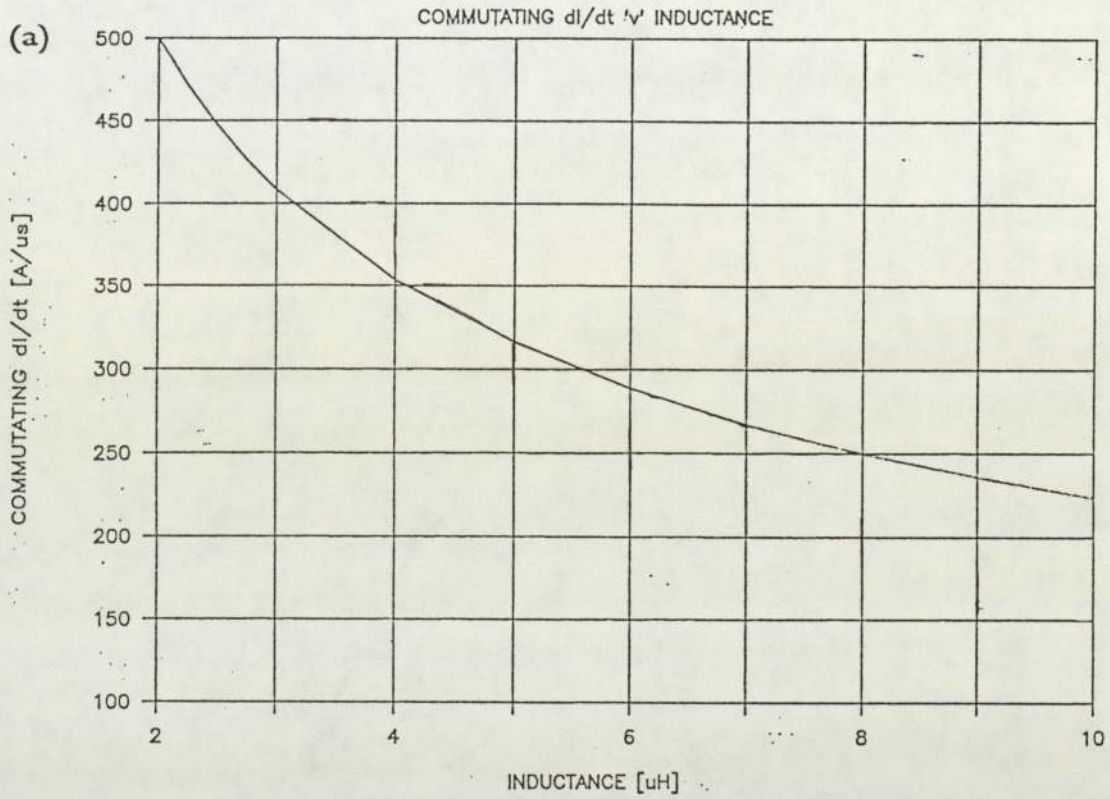


FIGURE 30

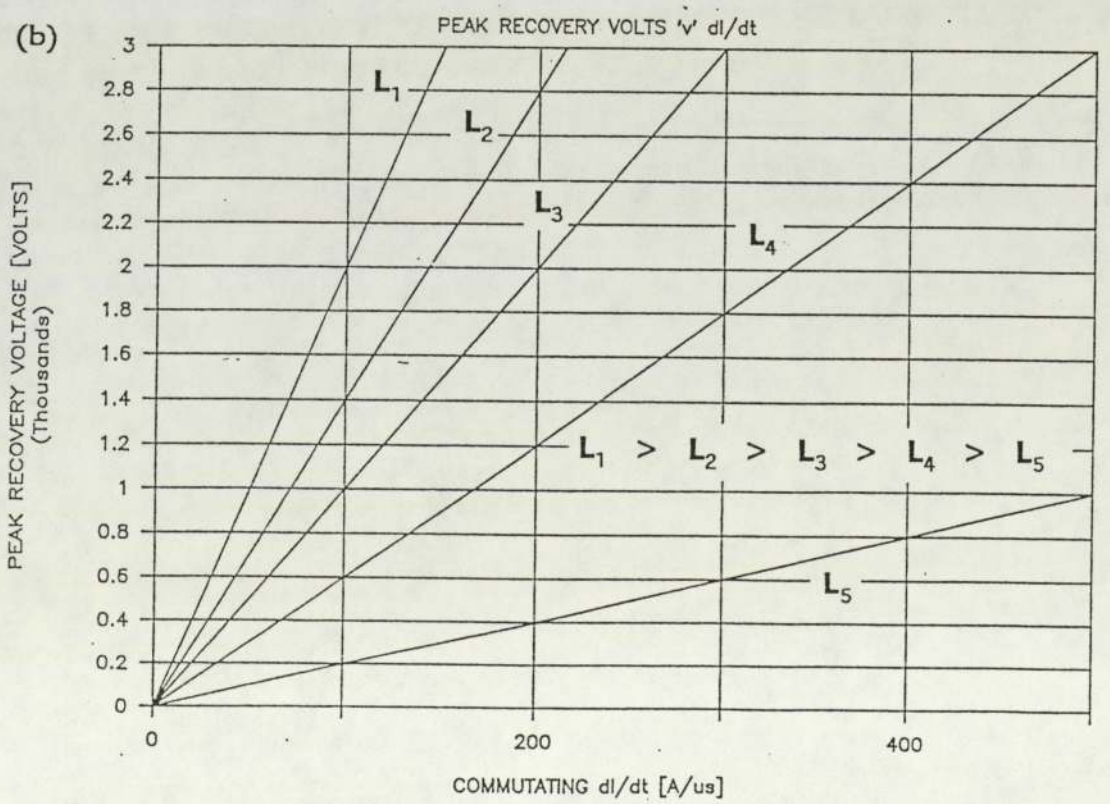
(a) Graph showing the variation of maximum commutating dI/dt with stray circuit inductance.

(b) Graph showing the variation of peak reverse recovery voltage with commutating dI/dt for different values of circuit inductance.

(a)



(b)



Since $V_r/L_s = dI_f/dt$ - (E29)

then $V_{pkr} = 2.L_s.(dI_f/dt)$ - (E30)

If a diode of voltage rating of 3.0kV is chosen then a 3.0kV line can be drawn on the graph shown in figure 30(b). The intersection of this line with one of the other curves represents the maximum safe dI/dt for that value of stray inductance.

Figure 30 provides information that can be replotted as a graph of maximum safe commutating dI/dt and maximum allowable circuit commutating dI/dt against stray inductance as shown in figure 31. The intersection of the two displayed curves defines two operating regions: safe and unsafe. Generally practical recovery waveforms will generate less volts because of additional circuit components, but this exercise serves to illustrate that the diode may be operated in an unsafe region depending on the value of circuit components and in this case principally circuit inductance.

The commutating dI/dt to which a diode is subjected is primarily circuit dependent but the recovery dI/dt is predominately device dependent. Thus diodes of different types will have different softness factors and generate different recovery voltages when the same commutating dI/dt is applied in the same inductive circuit. Figure 32 shows calculated curves of device peak reverse recovery voltage for different values of softness factor to a constant value of circuit inductance. From this graph the maximum safe dI/dt (the dI/dt at which the peak reverse recovery voltage equals the diode voltage rating) can be plotted against softness factor. Figure 33 shows just such a variation. As the softness of the diode increases so does it's maximum safe commutating dI/dt. As the recovery dI/dt increases relative to the commutating dI/dt so the waveform becomes abrupt and eventually it can shock excite the circuit to generate voltage spikes in excess of the normal inductive voltage overshoot.

A desirable diode characteristic is therefore a soft reverse recovery waveform. The cessation of the reverse current at a rate slower than the commuting dI/dt

FIGURE 31

Graph showing the variation of maximum circuit dI/dt and critical dI/dt with stray inductance.

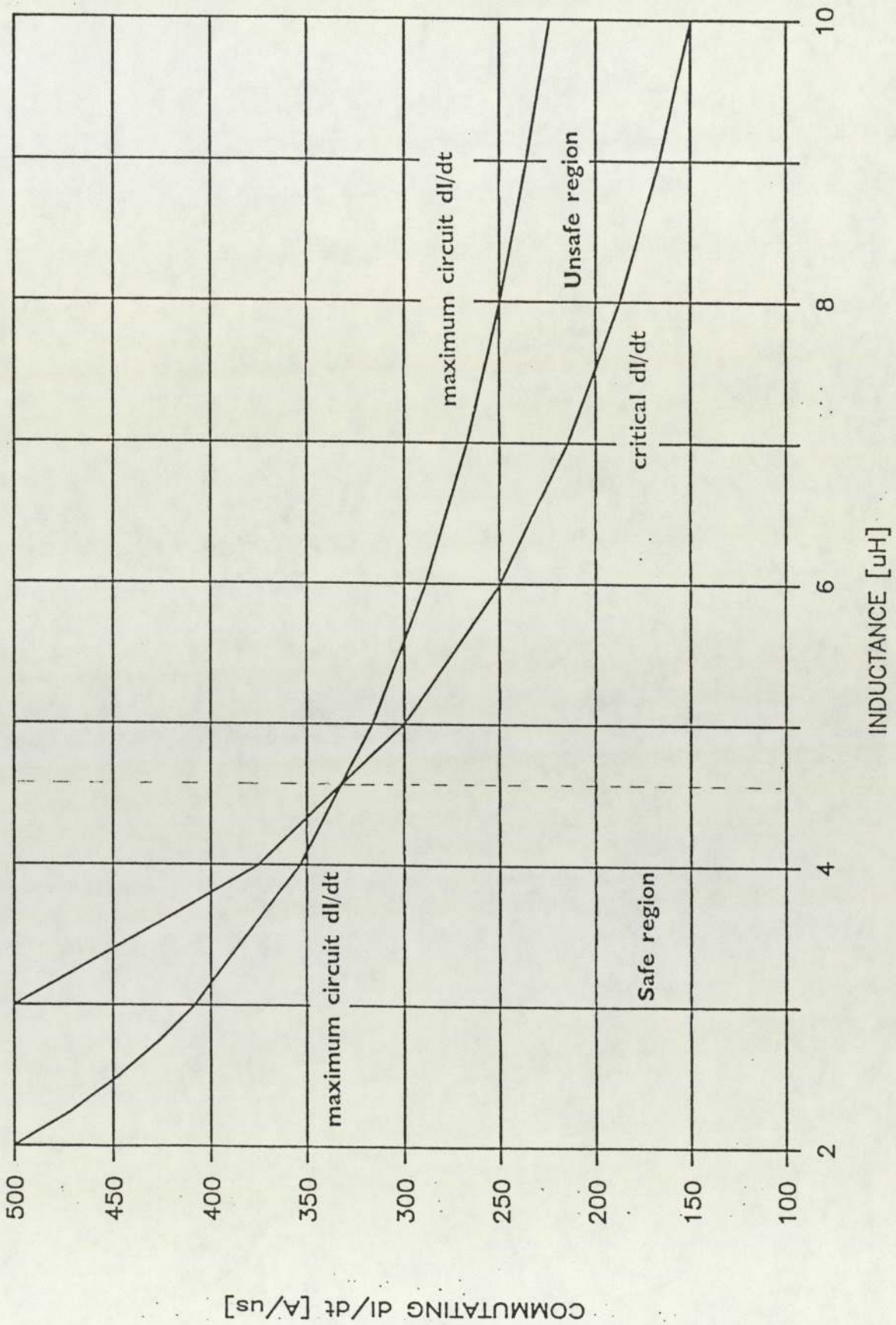


FIGURE 32

Graph showing the variation of peak reverse recovery voltage with commutating dI/dt for various values of diode softness factor.

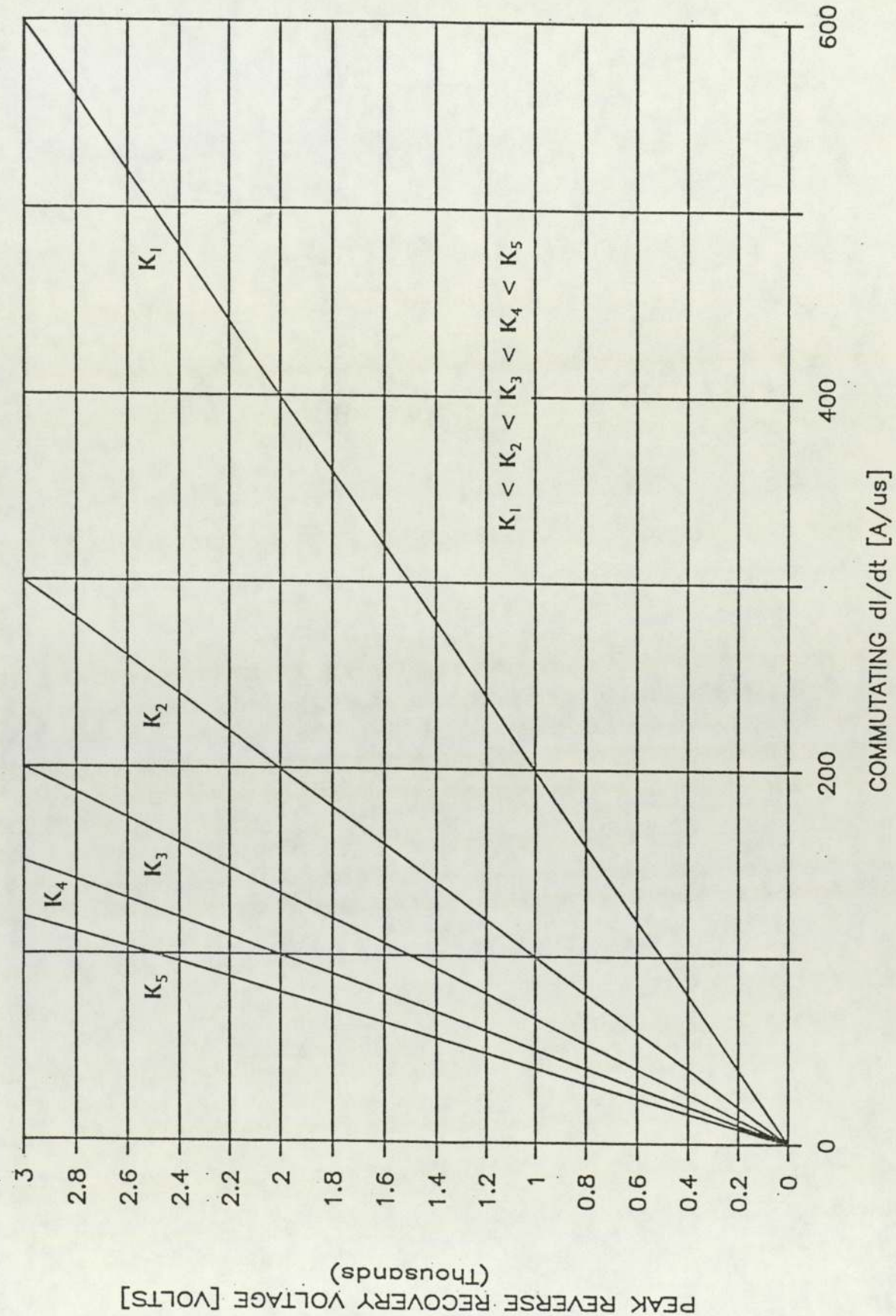
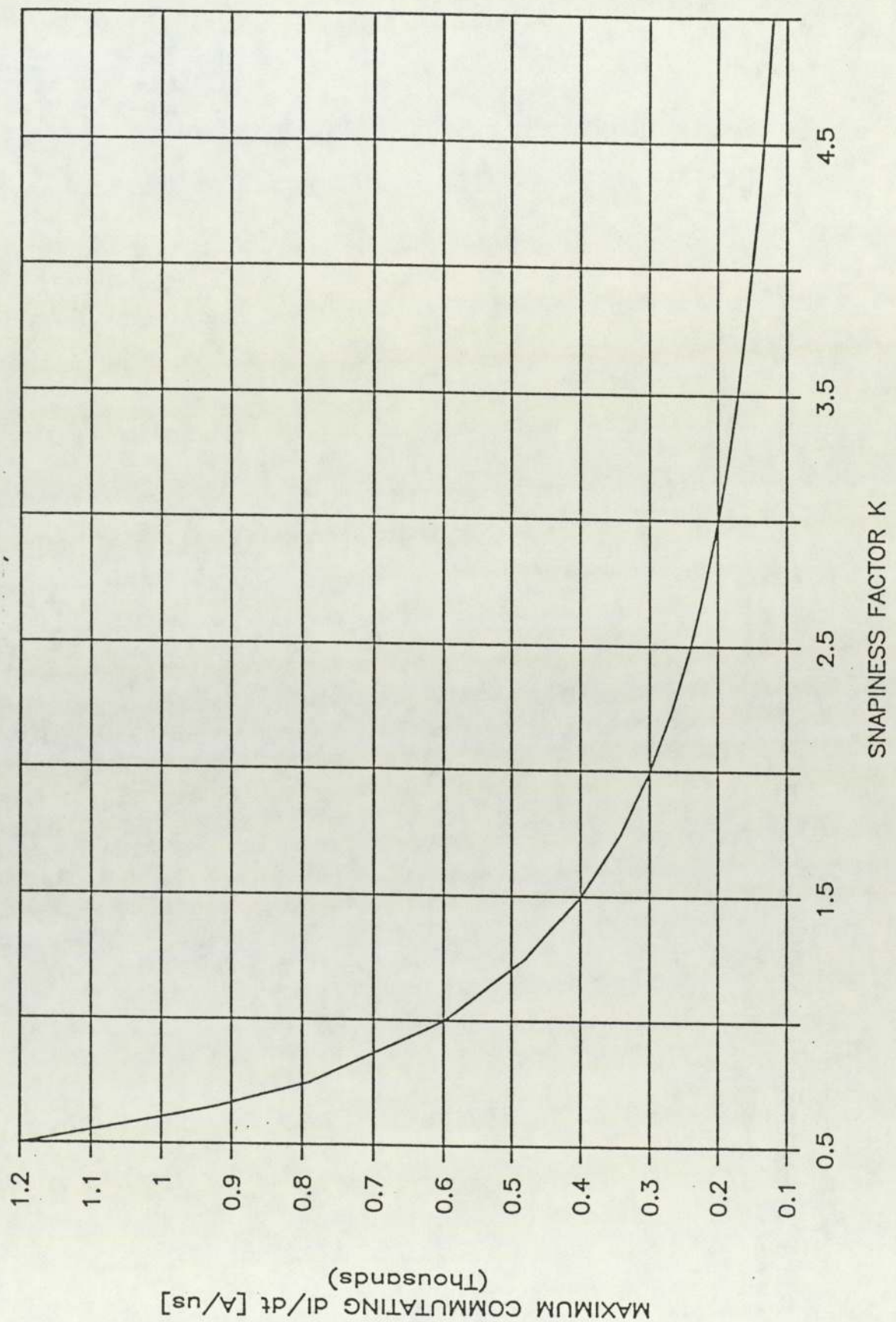


FIGURE 33

Graph showing the variation of safe maximum commutating dI/dt with softness factor.



produces a recovery current that is said to be soft. Many of today's high power fast switching diodes are designed to have a soft recovery characteristic in which the reverse current slowly tails off. Such a reverse current tail is advantageous, since the recovered charge is less than for a diode of the same softness factor S but with a linear dI_r/dt.

Figure 34(a) illustrates that measurements of the t_b/t_a ratio in a diode with a soft recovery tail would produce a higher value of S than is realistic. To improve the usefulness of S, authors such as Houston et al [206, 209] specify the dI_r/dt as being equal to the slope of a line from the peak reverse current I_{rm} to $0.25xI_{rm}$ (see figure 34(b)). This line is then extrapolated to the x-axis and t_b is measured to this point. However as the complexity of the diode design increases, the reverse recovery current tail becomes more convoluted and the $0.25xI_{rm}$ definition becomes less relevant to V_{pkr} as the maximum dI/dt occurs further away from the recovery current zero.

Alternative points such as $0.5xI_{rm}$ [209] and $0.75xI_{rm}$ [162] have been suggested. Figure 35(a) shows how these definitions produce different t_b times and thus different t_a/t_b ratios for the same diode. To try and resolve these drawbacks Balenovich et al [211] have used a definition of dI_r/dt based on the slope between I_{rm} ($dI/dt = 0$) and the inflection point of the reverse recovery curve i.e. $d^2I/dt^2 = 0$ - see figure 35(b). This definition gives a ratio of more significance in V_{pkr} calculations but could prove difficult to measure in practice as some waveforms are similar to that shown in figure 36(a), which has no inflection point to measure. For clarity a schematic diagram of this type of diode recovery is shown in figure 36(b).

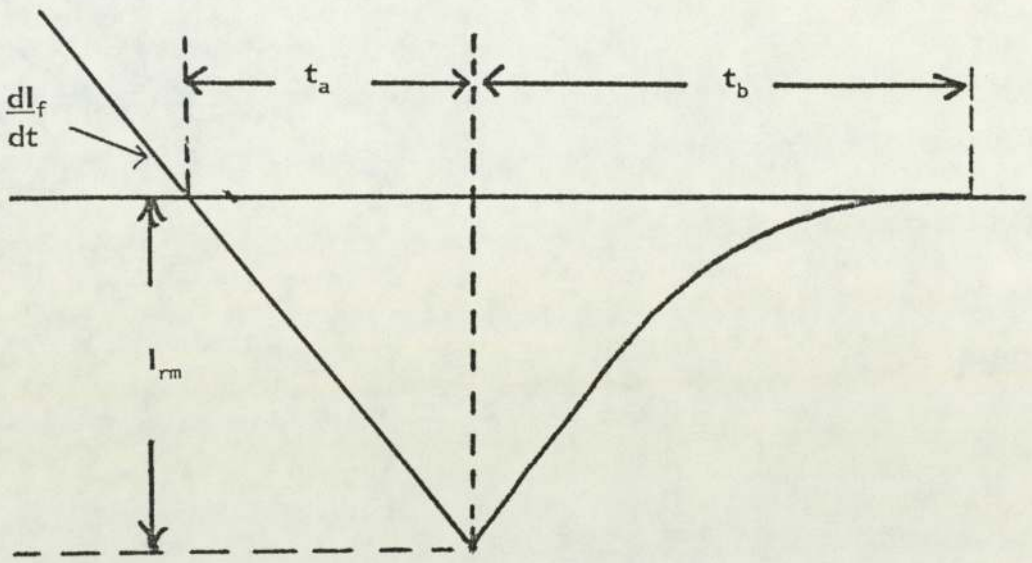
The parameter of primary importance in V_{pkr} generation is dI_r/dt. However direct accurate measurement of dI_r/dt can be difficult, which is why manufacturers have in the past used time ratios. In triangular waveforms these time ratios are related to dI_r/dt as follows:

$$dI_r/dt = (S^{-1}).dI_f/dt \qquad \text{- (E31)}$$

FIGURE 34

(a) Diagram of soft recovery waveform.
(b) Diagram showing derivation of softness factor.

(a)



(b)

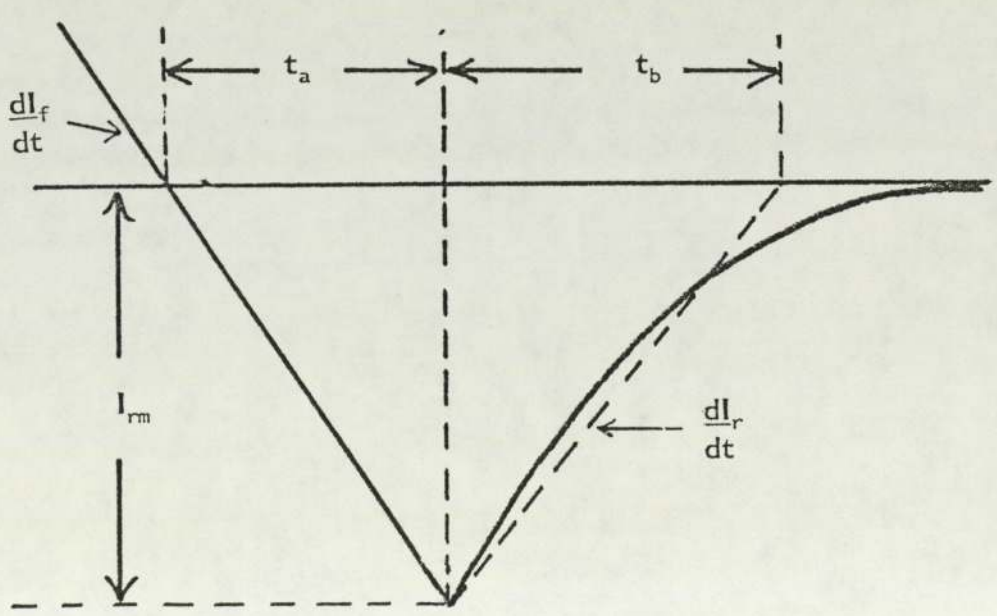


FIGURE 35

Diagrams showing alternative definitions of softness factor.

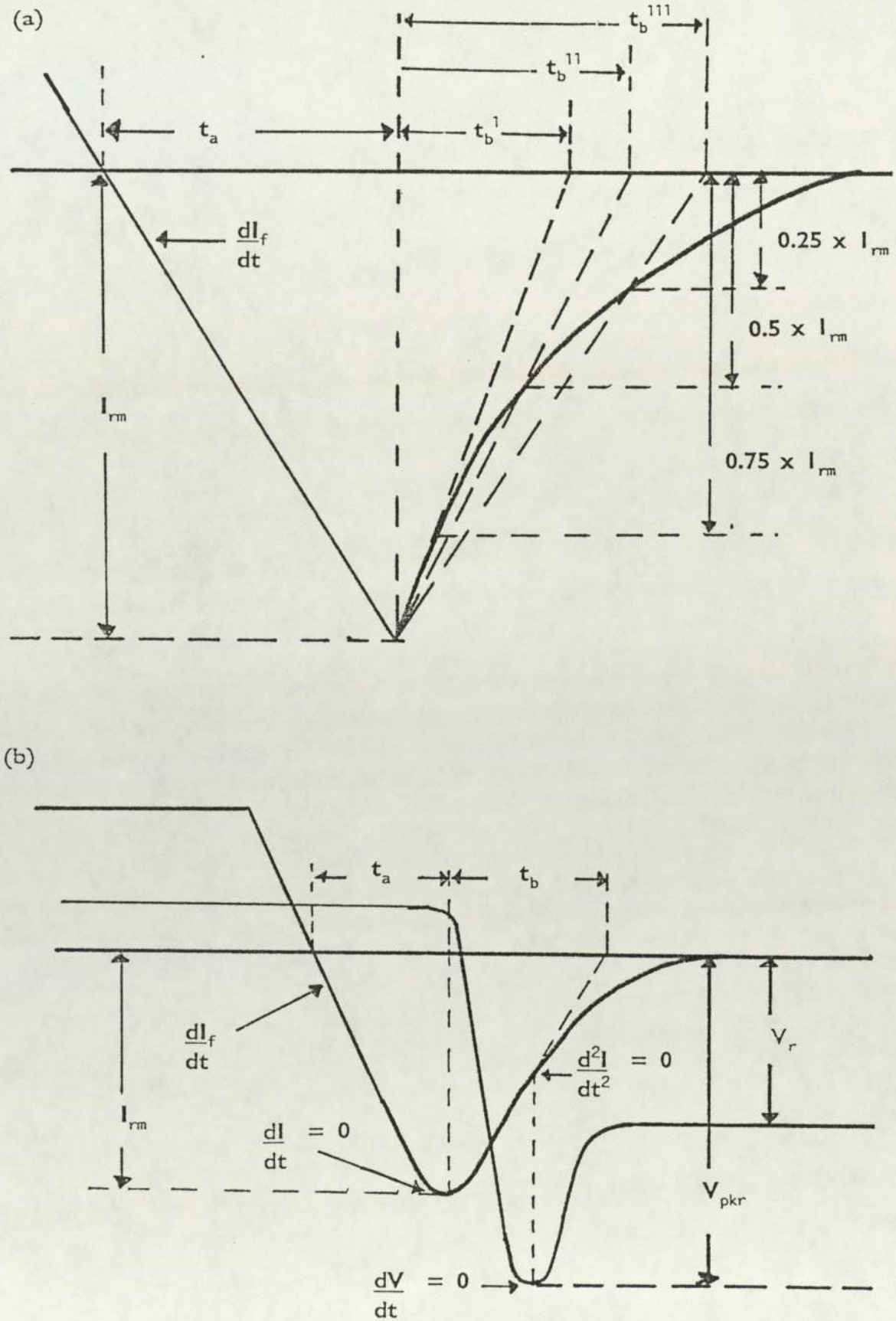
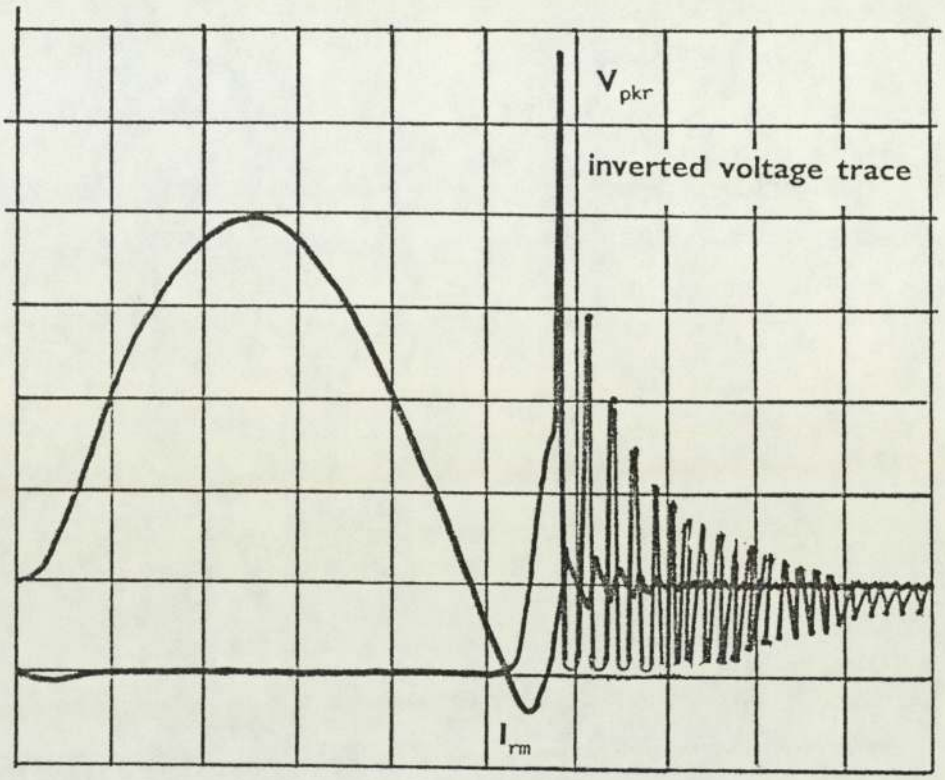


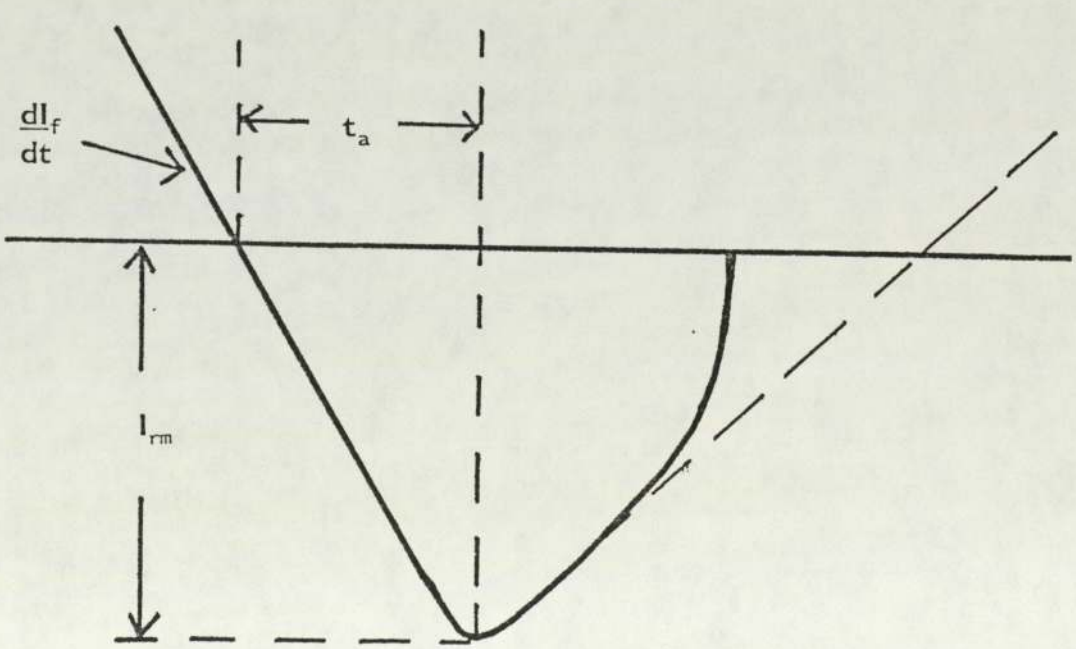
FIGURE 36

(a) Sketch of oscillogram showing diode snap-off.
(b) Diagram showing current waveform with no inflection point.

(a)



(b)



This relationship holds good for the simple waveform shown in figure 9(b) but not for many diodes in practical circuits where V_{pkr} is also dependent on device circuit interactions. The primary use of such a ratio would be to compare two devices and from the snappiness ratio predict which device would produce the higher V_{pkr}.

The disadvantage of time ratio definitions is that t_b is always defined in terms of an average dI_r/dt when V_{pkr} is dependent on the maximum dI_r/dt. For these waveforms equation (E24) is no longer valid and therefore such time ratio measures of snappiness are not very good indicators of the probable reverse recovery overvoltage under high stress conditions.

A method [232] of avoiding these problems is by specifying diodes in terms of a softness factor Ç equal to the ratio V_{pkr}/V_r. Thus referring to the idealised recovery waveform shown in figure 9(b):

$$Ç = V_{pkr}/V_r \qquad \text{- (E32)}$$

and

$$Ç = 1 + S^{-1} \qquad \text{- (E33)}$$

Unlike the K and S ratios the Ç ratio does not depend on the assumption that for an ideal triangular waveform:

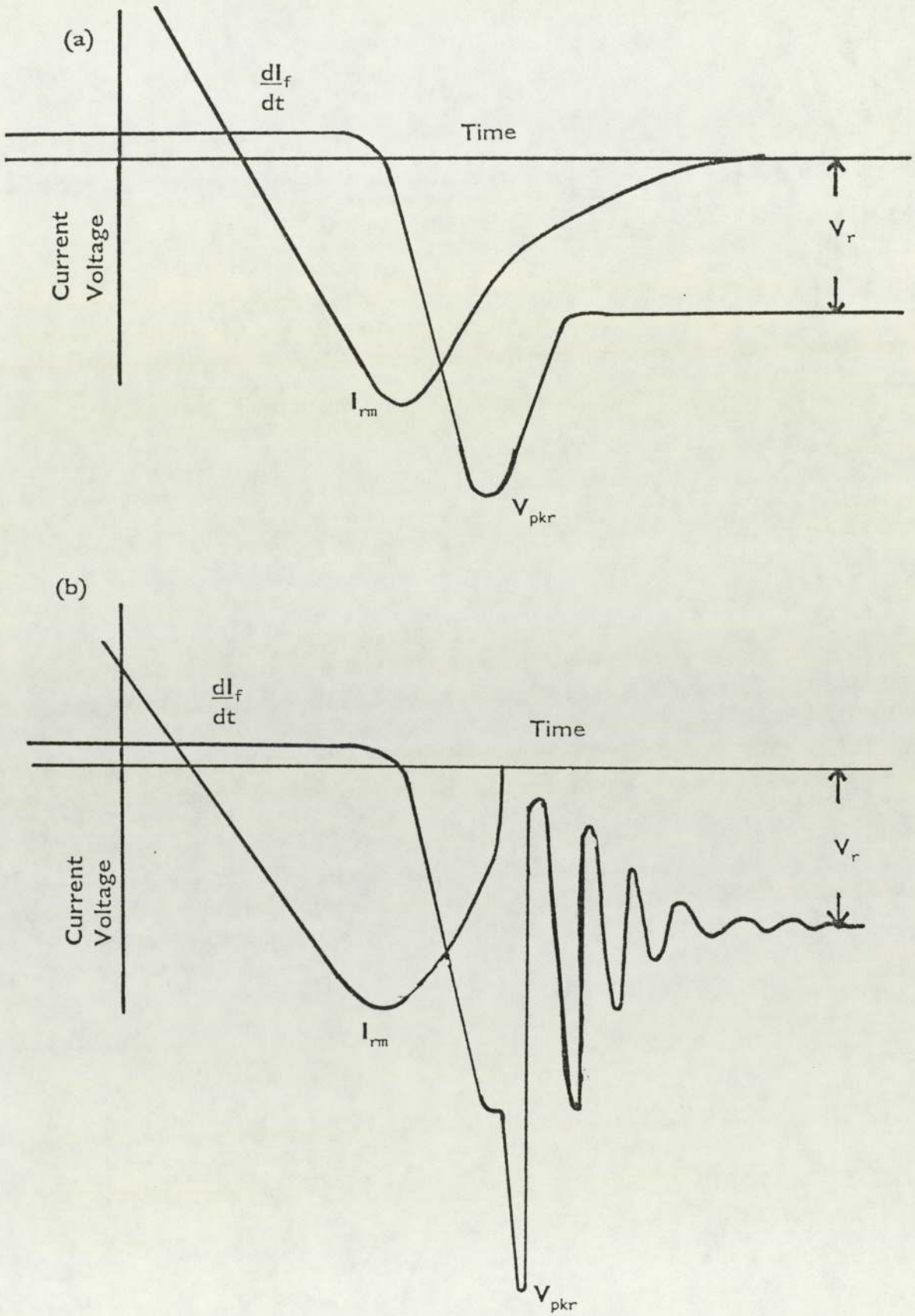
$$t_a/t_b = \{(dI_r/dt)/(dI_f/dt)\} \qquad \text{- (E34)}$$

Thus the ratio Ç can be applied to curves found in practice. As the waveforms become more complex difficulties in defining dI_r/dt are not reflected in the V_{pkr}/V_r ratio. In addition Ç is relatively easy to measure. The advantage of the Ç measure is shown in figures 37 (a) and (b). Each of these waveforms has the same t_a/t_b ratio and thus this measure would not detect the large voltage spike in figure 37 (b). However, the Ç ratio would have successfully identified the occurrence of a large voltage spike.

The general term, snappy recovery is used to describe the generation of

FIGURE 37

(a) Diagram of soft recovery.
(b) Diagram of snappy recovery.



voltage spikes, but it does not describe the mechanism by which they are produced. A voltage spike may be produced simply by applying a high enough commutating dI/dt to a device with a softness factor that would produce a recovery dI/dt sufficiently large to shock excite the circuit into generating such a spike. Alternatively a voltage spike may be caused by a sudden discontinuity in the recovery current waveform [5, 45, 88]. In such cases the reverse current suddenly chops or 'breaks away' [88] to zero. Such discontinuities are device dependent.

Figure 10(c) shows a sketch of an oscillogram of diode current and voltage waveforms that are produced during diode snap-off. In this case the voltage spike is produced by a large recovery dI/dt that is approximately linear. Figure 38(a) shows a linear recovery current that has produced oscillations on the recovery voltage. These oscillations are not similar to those shown in figure 10(c) but are a prelude to diode snap-off.

Figure 38(b) shows a sketch of an oscillogram of current and voltage waveforms in a diode that is undergoing reverse recovery snap-off. The forward current pulse and commutating dI/dt proceed as in the normal recovery case until what is the expected recovery voltage is reached at which point a voltage spike is produced. The resulting rapid dV/dt shock excites the circuit producing a number of subsequent spikes. Figure 38(c) shows the same event on an expanded time base. The voltage spike is associated with a rapid change in dI/dt. In this case the dI^2/dt^2 is always positive and no inflection point exists.

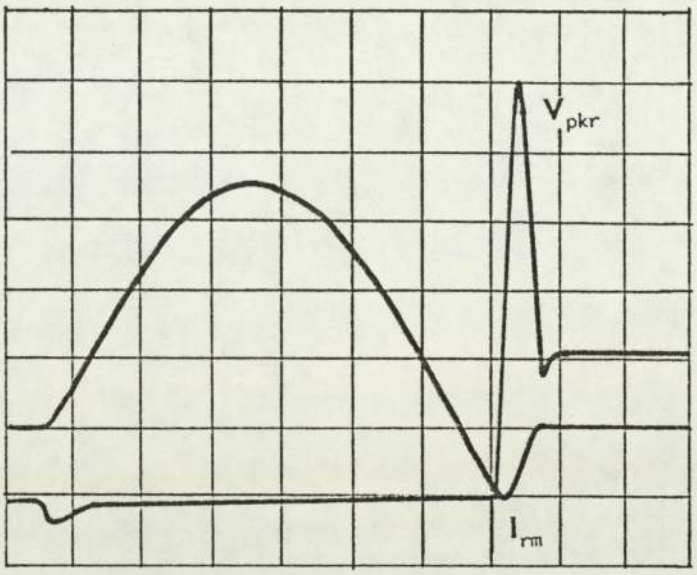
In figure 36(b) the maximum dI/dt occurs just before current zero and figures 38(b,c) show current chop-off where dI/dt max occurs after a soft recovery waveform. This current 'chop' effect after a soft recovery tail can be seen more clearly in figure 46(a). In such cases measurement of the S ratio would not indicate a problem (since the current step is so small). Use of the Ç ratio would, however, indicate this snappy behaviour of the diode.

The above defined measure of diode recovery characteristic (i.e. Ç) can thus

FIGURE 38

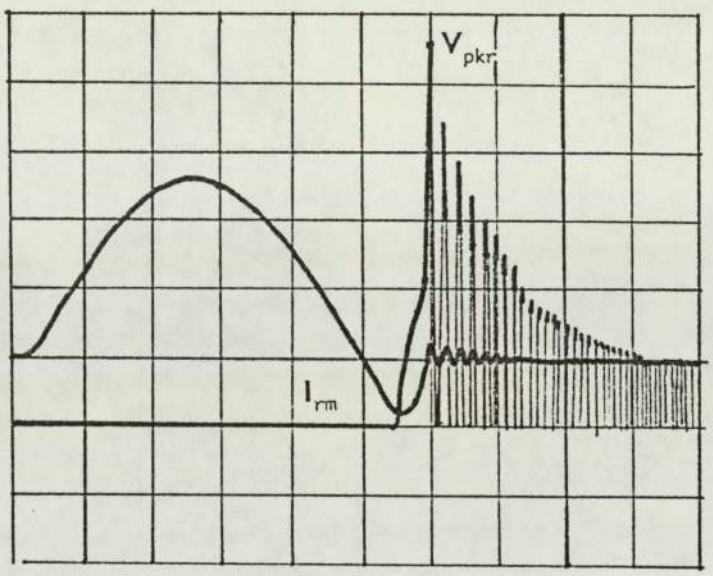
(a) Sketch of oscillogram showing normal recovery.
(b) Sketch of oscillogram showing snap-off recovery.
(c) Sketch of oscillogram showing current chop-off.

(a)



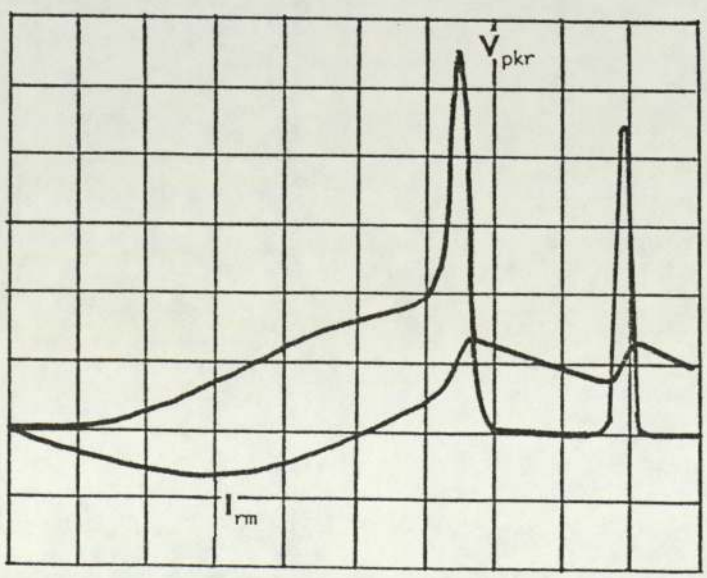
V = 50V/Div
I = 20A/Div
t = 2μs/Div
inverted voltage trace

(b)



V = 500V/Div
I = 100A/Div
t = 2μs/Div
inverted voltage trace

(c)



V = 500V/Div
I = 50A/Div
t = 0.2μs/Div
inverted voltage trace

be used to determine if a diode is exhibiting snap-off. As such, this exercise has fulfilled the stated aim (section 2.1) of interpreting the solution and expressing these conclusions in a readily understandable form.

4.2 Formation of the problem into mathematical terms

4.2.1 An overview of the reverse recovery process

The following standard derivation [224] is dependent upon a non-inductive, resistive external circuit and a step change in applied bias [12] (see figure 39).

Consider an N^+NP diode in a forward biased state. Thus a forward current I_f flows through the diode. At a time $t = 0$, this steady state condition is disturbed when a reverse voltage is applied to the diode to produce a reverse recovery event. Carriers moving by diffusion in the space charge neutral region are swept out of the diode in the reverse direction upon approaching the edge of the depletion layer. This reverse current is maintained until all of the stored charge is extracted from the base.

Figure 39 shows the excess minority carrier distributions in a wide base diode. From $t = 0$ until $t = t_s$, the slope $(dn_p/dx)_{x=o}$ is constant, corresponding to the rate of charge extraction that is limited by the external circuit. From $t = t_s$ to $t = t_\infty$ this slope, falls as the reverse current is device limited and the diode stored charge is used up. It should be noted that up until $t = t_s$ the diode junction, remains forward biased even though the diode current is negative. After $t = t_s$ the voltage becomes negative eventually equalling the applied reverse voltage.

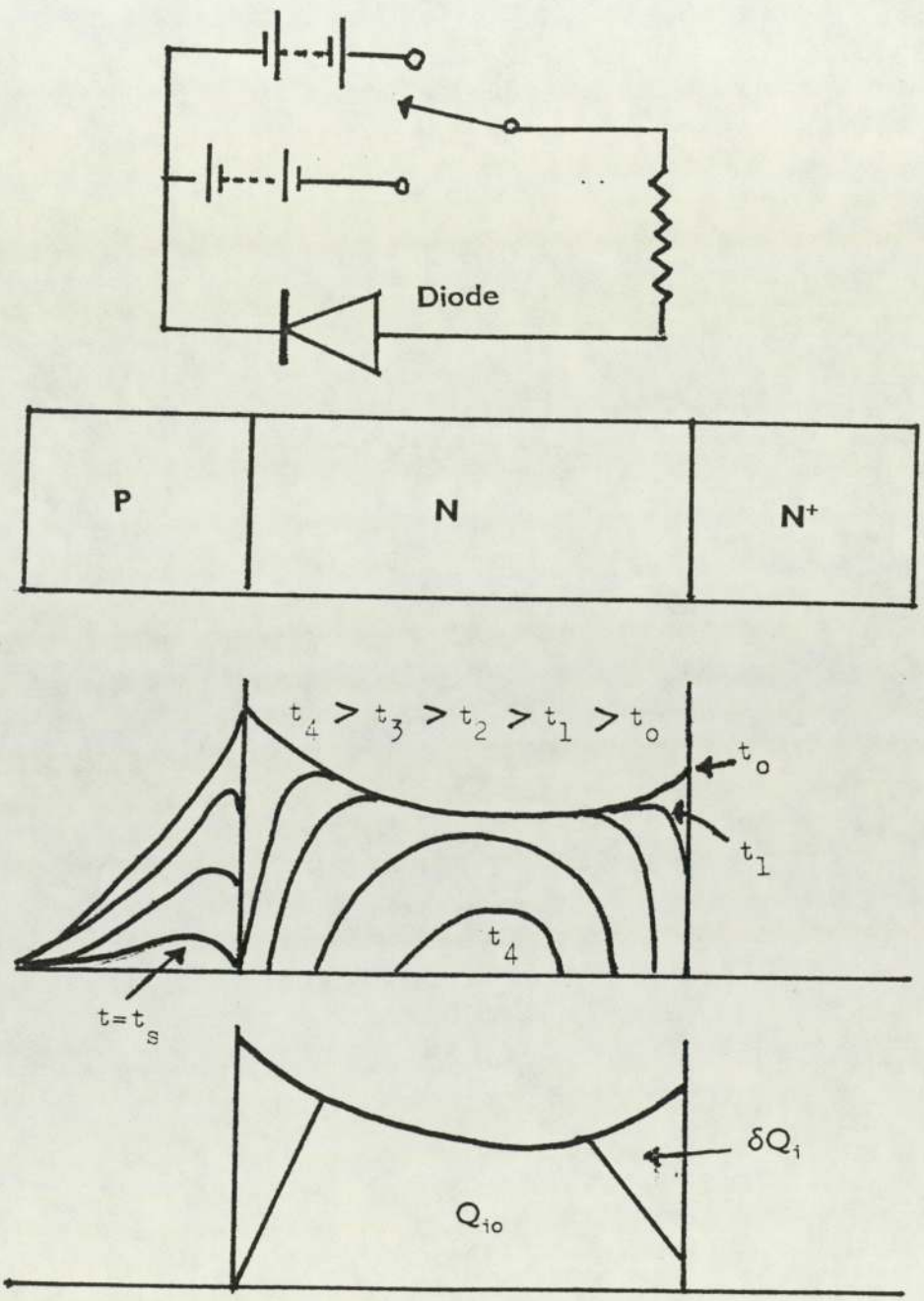
For a $N^+.P$ diode of unit cross-sectional area the continuity equation for electrons in the p-region can be written as:

$$\frac{d\,(n - n_o)}{dt} = \frac{n - n_o}{\tau_n} - \frac{1}{q} \cdot \frac{di_n(t)}{dx} \qquad \text{- (E35)}$$

where $i_n(t)$ is the current due to electron flow in the positive direction.

FIGURE 39

Diagram showing the carrier distribution in a wide base diode.



Multiplying by -q (the electronic charge) and integrating over the p-region yields the following equation.

$$\frac{d}{dt}\int_o^w -q\,(n - n_o)\,dx = \int_o^w \frac{di_n(t)}{dx}\,dx - \int_o^w \frac{-q}{\tau_n}\,(n - n_o)\,dx \qquad \text{- (E36)}$$

Defining Q(t) as the excess stored charge in the p-region reduces equation (E36) to

$$\frac{dQ(t)}{dt} + \frac{Q(t)}{\tau_n} - i_n(W,t) = -i_n(0,t) \qquad \text{- (E37)}$$

The quantity Q (t) is negative since it is associated with electrons. By defining an effective lifetime τ_f in the forward direction as:

$$\frac{Q(t)}{\tau_f} \equiv \frac{Q(t)}{\tau_n} - i_n(W,t) \qquad \text{- (E38)}$$

Then (E37) becomes (E39) by substitution of (E38).

$$\frac{dQ(t)}{dt} + \frac{Q(t)}{\tau_f} = -i_n(0,t) \qquad \text{- (E39)}$$

The total reverse current of an N^+.P diode consists of current due to electron flow plus current through the depletion layer capacitance. Defining the average depletion layer capacitance as C^*_t modifies the charge control equation (E39) to:

$$\frac{dQ(t)}{dt} + \frac{Q(t)}{\tau_f} - C^*_t \cdot \frac{dV(t)}{dt} = -i(t) \qquad \text{- (E40)}$$

where the value of C^*_t is given by:

$$C^*_t = \frac{1}{V_2 - V_1} \int_{v1}^{v2} C_t(V)\, dV \qquad \text{- (E41)}$$

The V_1 and V_2 are the limits over which the voltage across the diode varies. During the time interval that is circuit limited, the recovery dV/dt across the diode is small.

$$\text{Thus} \quad i_c = C^*_t \cdot \frac{dV}{dt} \rightarrow 0 \qquad \text{- (E42)}$$

$$\text{and} \quad \frac{dQ(t)}{dt} + \frac{Q(t)}{\tau_p} = I_r \qquad \text{- (E43)}$$

which can be solved to give $Q(t) = I_R.\tau_f - (I_R + I_f).\tau_f.\exp(-t/\tau_f)$ - (E44)

(see reference [224])

Assume that in figure 39 the carrier concentration in the p-region at $t > t_3$ is

$$n(x,t) = f(t)\, n(x) \qquad \text{- (E45)}$$

Then it follows that the stored charge is directly proportional to the reverse current.

$$\text{Thus} \quad Q(t) = -i(t) \cdot \tau_R \qquad \text{- (E46)}$$

Where τ_R is an effective reverse biased lifetime. The excess stored charge at $t=t_s$ is given by $-I_R\,\tau_R$. By substituting this relationship into (E43) and (E44) the following equation is produced.

$$t_s = \tau_f \cdot \left[\ln(1 + (I_F/I_R)) - \ln(1 + (\tau_R/\tau_f)) \right] \qquad \text{- (E47)}$$

By measuring t_s for two values of I_F/I_R the parameters τ_f and τ_R can be determined.

If during the time period t_3 (i.e $t=t_s$ to $t=t_\infty$) dV/dt is not small then the current flow through C^*_t cannot be neglected. If the diode circuit has an external resistance R then

$$dv(t) = - R\, di(t) \qquad \text{- (E48)}$$

Substituting this relationship into equation (E46) and (E40) yields

$$\frac{di(t)}{dt} \cdot \{(\tau_R + R.C^*_t + i(t).(1 + [\tau_R/\tau_f])\} = 0 \qquad \text{- (E49)}$$

at $t = t_s,\ i(t) = - I_R$

$$\text{hence} \quad i(t) = - I_R \cdot \exp\{-(t - t_s)/\tau\} \qquad \text{- (E50)}$$

$$\text{where} \quad \tau = \tau_R + \frac{R.C^*_t}{1+\tau_R/\tau_f} \qquad \text{- (E51)}$$

The fall time measured to 10% of the initial value of reverse current is written as:

$$t_f \approx 2.3\ \frac{(\tau_R + R.C^*_t)}{1 + \tau_R / \tau_f} \qquad \text{-(E52)}$$

Thus the recovery characteristics of a diode are determined by the minority carrier lifetime, the transit time, the forward current, the reverse current, and also the external circuit parameters. In addition the fabrication method determines τ_R and thus influences the diode performance.

In high power, high voltage snubber diodes diffused junctions are used. Thus the onset of recombination effects in the end regions are not as rapid as in alloyed devices. Diffused diodes therefore, tend to have a soft recovery characteristic under low stress conditions.

4.2.2 **A capacitive model of the diode**

The following derivation and discussion differs from the standard argument outlined in section 4.2.1 in that the commutation process is assumed to occur in a non-resistive, inductive circuit with a varying reverse bias (see figure 10).

Referring to the diode turn-on/turn-off waveform shown in figure 21(a), it can be seen to have a variable impedance. This non-linear impedance can be represented by the equivalent circuit shown in Figure 40 (a). Here the ohmic resistance is represented by a variable resistor and the stored charge is represented by a variable capacitor. In a diode the depletion layer can thus be physically represented as a parallel plate capacitor. Thus:

$$Q_s = C_d \cdot V_d \qquad \text{- (E53)}$$

where Q_s = Diode stored charge
C_d = Diode capacitance
V_d = Voltage across diode

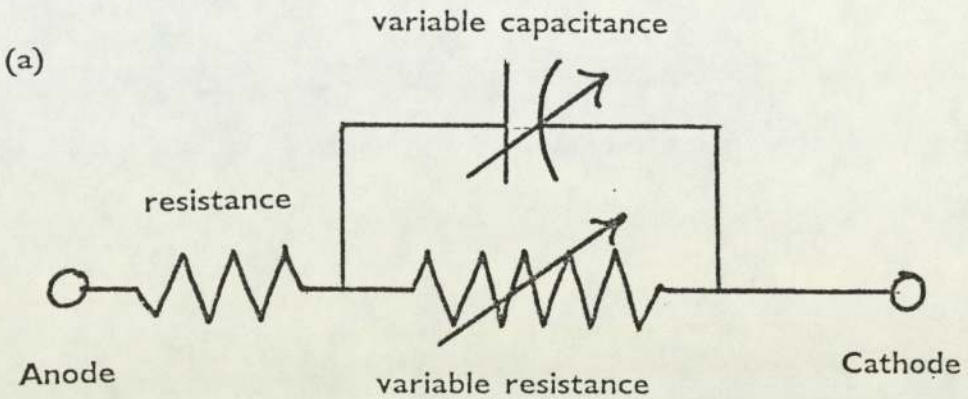
This basic equation can be used to relate the diode stored charge to the product of the voltage drop across the depletion layer and an equivalent capacitance. Differentiation of the above equation yields an expression for the diode current I_d.
Thus:

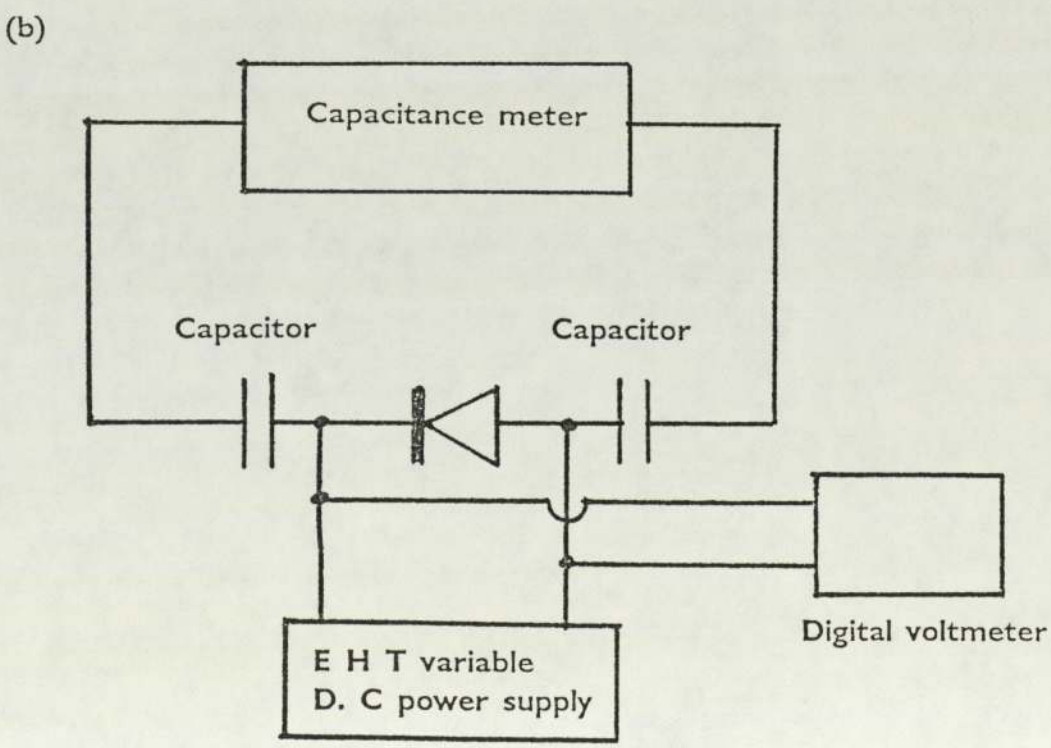
$$I_d = \frac{dQ_s}{dt} = C_d \cdot \frac{dV_d}{dt} + V_d \frac{dC_d}{dt} \qquad \text{- (E54)}$$

This equation expresses the fact that after the start of diode recovery there are two components of diode current. The first component is that of the well known C.dV/dt current. The second component is that due the variation of diode capacitance during switching.

FIGURE 40

(a) Diagram showing equivalent circuit of diode.
(b) Diagram of circuit to measure diode capacitance.





The need for a variable capacitance in the equivalent circuit was indicated by published work [166,167,173,187] and was confirmed by measurements made on a reverse biased diode using the circuit shown in figure 40(b). A commercially available electrical component tester capable of measuring, inductance, resistance and capacitance was used to measure the capacitance of two isolating capacitors connected in series with the diode under test. Since the values of discrete capacitance are combined reciprocally then when C_{Isol} is combined with C_{diode} the following equation holds true.

$$\frac{1}{C_{meas}} = \frac{1}{C_{Isol}} + \frac{1}{C_{diode}} + \frac{1}{C_{Isol}} \qquad \text{- (E55)}$$

where C_{meas} = Total measured capacitance

C_{Isol} = Isolating capacitance

C_{diode} = Diode capacitance

The above equation can be rearranged to form:

$$\frac{1}{C_{diode}} = \frac{1}{C_{meas}} - \frac{2}{C_{Isol}} \qquad \text{- (E56)}$$

If C_{Isol} is large (E56) then reduces to

$$\frac{1}{C_{diode}} \approx \frac{1}{C_{meas}} \qquad \text{- (E57)}$$

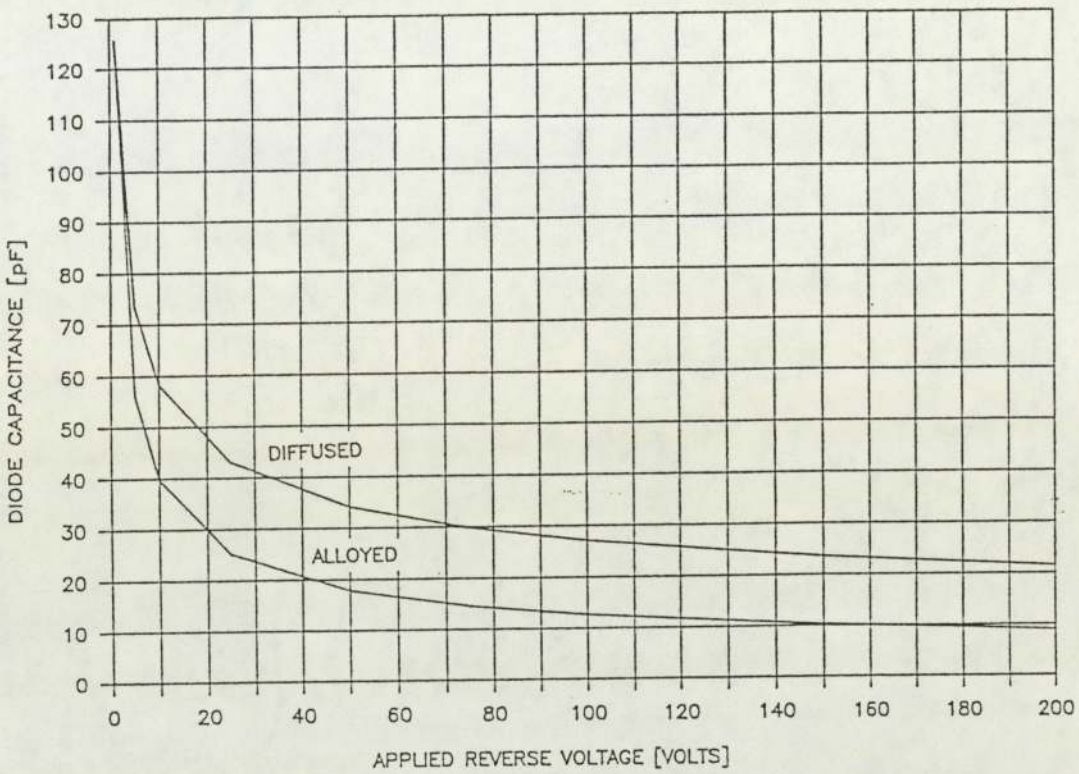
Because the value of C_{Isol} was chosen to be large (20μF) relative to C_{diode} these discrete capacitors presented a low impedance path to the ac test signal. Conversely these capacitors present no dc path. This isolates the capacitance measuring instrument from the high voltage bias applied across the diode. Thus as the reverse bias voltage was altered the diode capacitance could be measured.

It can be seen from the curves in figure 41 that the reverse bias capacitance of

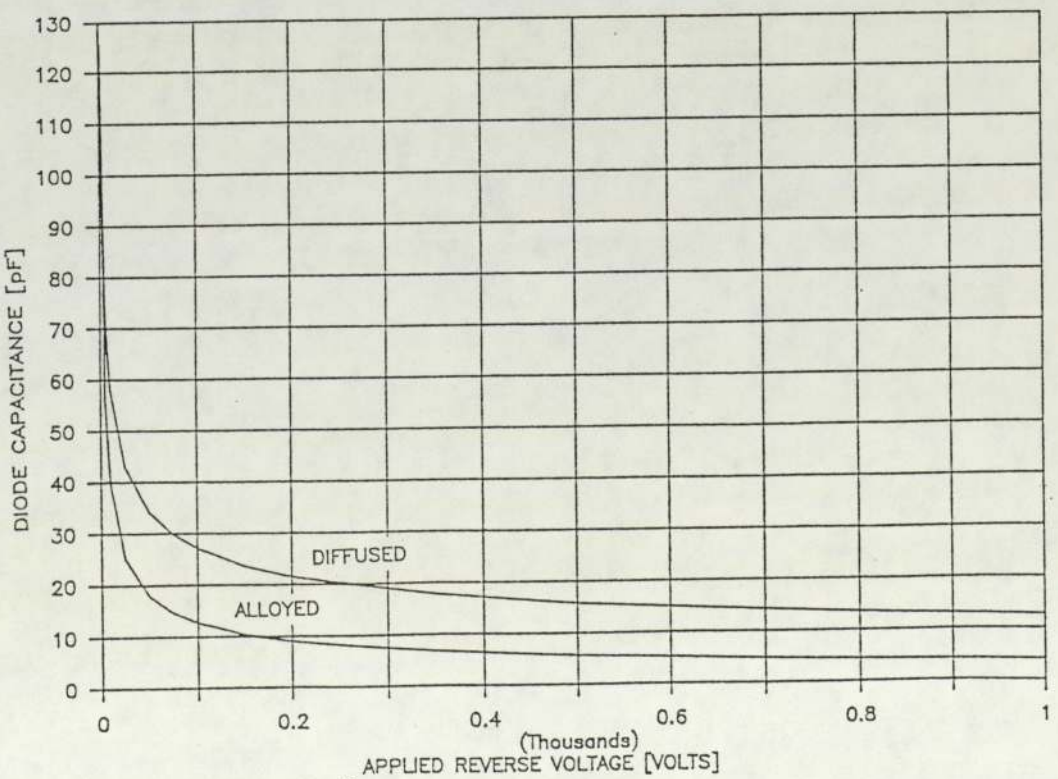
FIGURE 41

Graphs showing the variation of diode capacitance with applied voltage.

(a)



(b)



a diode varies with the magnitude of the reverse bias. Thus in equation (E54) the $V_d \cdot dC_d/dt$ current is produced because capacitance varies with voltage and voltage is varying with time. By using the substitution;

$$\frac{dC_d}{dt} = \frac{dC_d}{dV_d} \cdot \frac{dV_d}{dt} \qquad \text{- (E58)}$$

equation (E54) can be rewritten as

$$I_d = \frac{dV_d}{dt} \cdot \left[C_d + V_d \cdot \frac{dC_d}{dV_d} \right] \qquad \text{- (E59)}$$

The above equation is a clear statement of how the diode current is produced after junction recovery.

To investigate if the variation of capacitance was a 'real' effect, the variation of voltage and current with time was carefully measured for a diode undergoing reverse recovery. At each measurement point three items of data were recorded i.e. current I, voltage V and time t. Thus at point one, $V = V_1$, $I = I_1$, and $t = t_1$. Similarly at point three, $V = V_3$, $I = I_3$ and $t = t_3$. To determine the pseudo-capacitance of the diode at $t = t_2$ the rate of change of voltage was first calculated at that point. In this case:

$$\frac{dV_2}{dt} = \frac{V_1 - V_3}{t_1 - t_3} \qquad \text{- (E60)}$$

$$\text{Since} \quad C = I.\,(dV/dt)^{-1} \qquad \text{- (E61)}$$

$$\text{Then} \quad C_2 = \frac{I_2.(t_1 - t_3)}{V_1 - V_3} \qquad \text{- (E62)}$$

By suitable interchanging of the above subscripts the variation of diode pseudo-capacitance with time can be plotted. Equation E61 holds true for a simple capacitor. Figure 40(a) shows that as R becomes very large the diode can be considered as a simple R-C network. Thus measurement of the voltage V_d

includes the voltage drop due to contact resistance. Such a calculation also includes measurement errors and a distortion factor due to the phase shift between current and voltage signals. The term pseudo-capacitance is therefore introduced to differentiate between true diode capacitance and the ratio i_d:dV_d/dt. Thus graphs showing the variation of pseudo-capacitance with time are intended to indicate that capacitance variations occur and to illustrate the differences between diode recovery types.

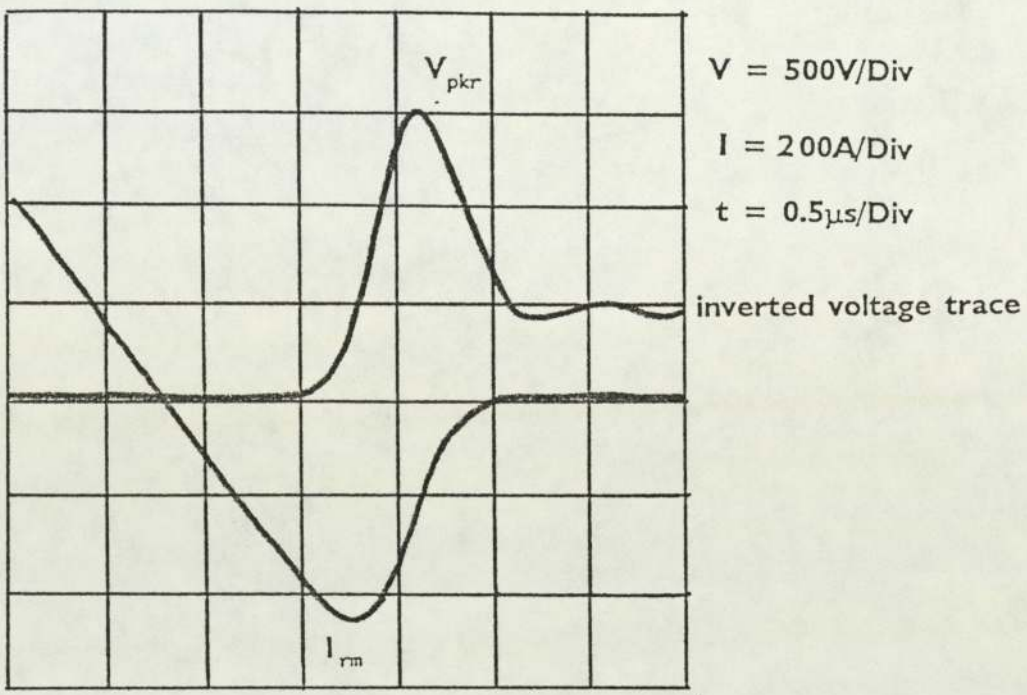
Figure 42(a) is a sketch of an oscillogram showing a diode undergoing normal (soft) reverse recovery. Using the method described above the variation of diode pseudo-capacitance with time was plotted. Figure 42(b) shows such a plot for a diode undergoing normal reverse recovery. The data points are highlighted by symbols to allow the accuracy of the calculation to be seen. By comparison with figure 42(a) the reader can see how close this approximation is to the actual current/voltage traces. The diode pseudo-capacitance is relatively constant (slightly reducing with time) during the circuit controlled phase of diode recovery. During the diode controlled phase of recovery, the pseudo-capacitance increases, reaching a maximum at the peak reverse recovery voltage. It is at this point where snap-off can occur. In this case the diode current does not rapidly fall to zero but rather slowly decays to zero. This soft recovery current tail can be explained in terms of the diode pseudo-capacitance. At the peak reverse recovery voltage the $C_p.dV/dt$ current is zero but the magnitude of the pseudo-capacitance is at a maximum. There is thus a $V.dC_p/dt$ current that prevents a current chop-off phenomenon. Referring to figure 43(a) the variation of pseudo-capacitance with time is replotted. Using this graph as a basis for calculation, a graph showing the variation of dC_p/dt with time can be constructed as shown in figure 43(b). Thus there is a rapid variation in pseudo-capacitance aiding the soft-recovery characteristic of the diode.

The variation in pseudo-capacitance during a normal diode recovery was then compared with the variation in pseudo-capacitance during snap-off recovery. Figure 44(a) is a sketch of an oscillogram showing a diode undergoing snap-off recovery. Figure 44(b) is graph showing the approximate recovery curves

FIGURE 42

(a) Sketch of oscillogram showing normal reverse recovery.
(b) Graph showing variation of voltage current and diode pseudo-capacitance with time for normal reverse recovery.

(a)



(b)

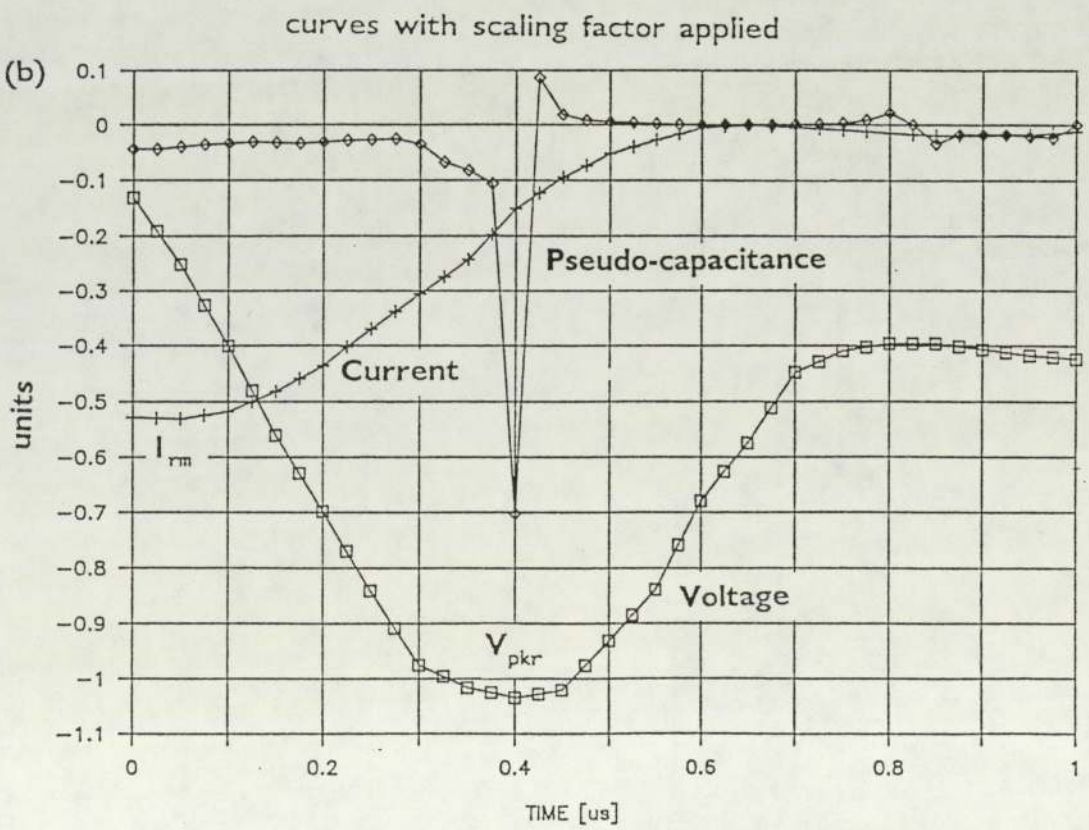
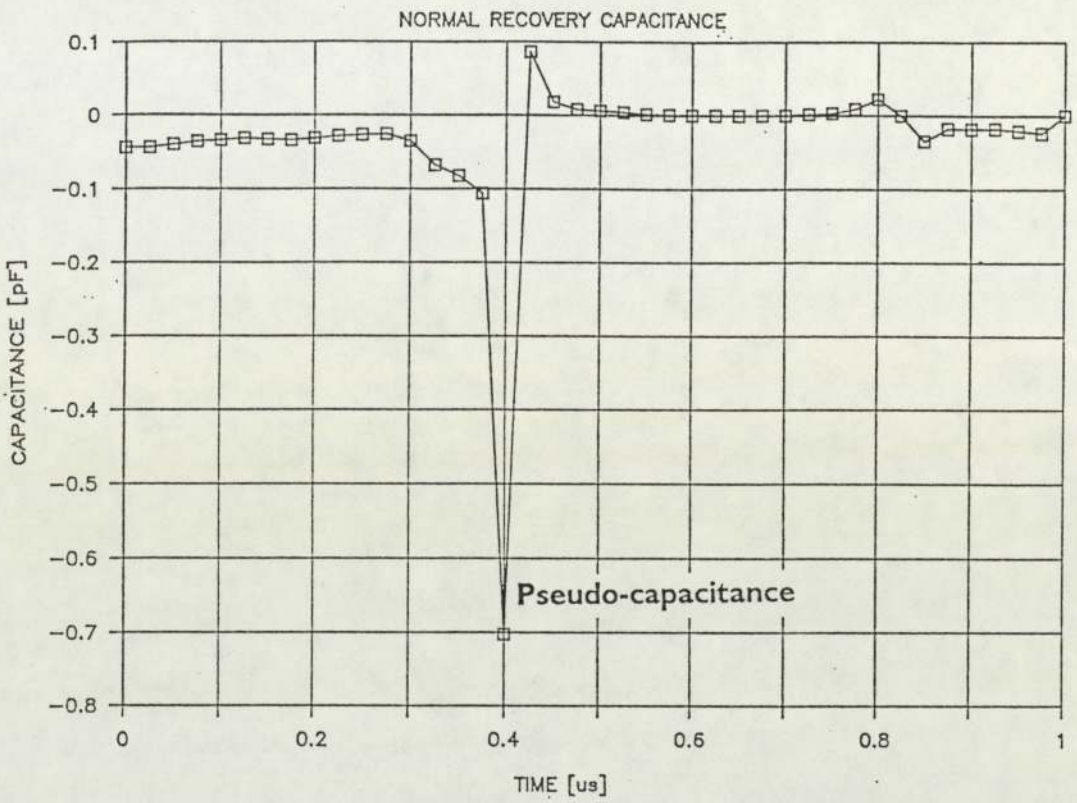


FIGURE 43

Graphs showing variation of diode pseudo-capacitance and dC_p/dt with time.

(a)



(b)

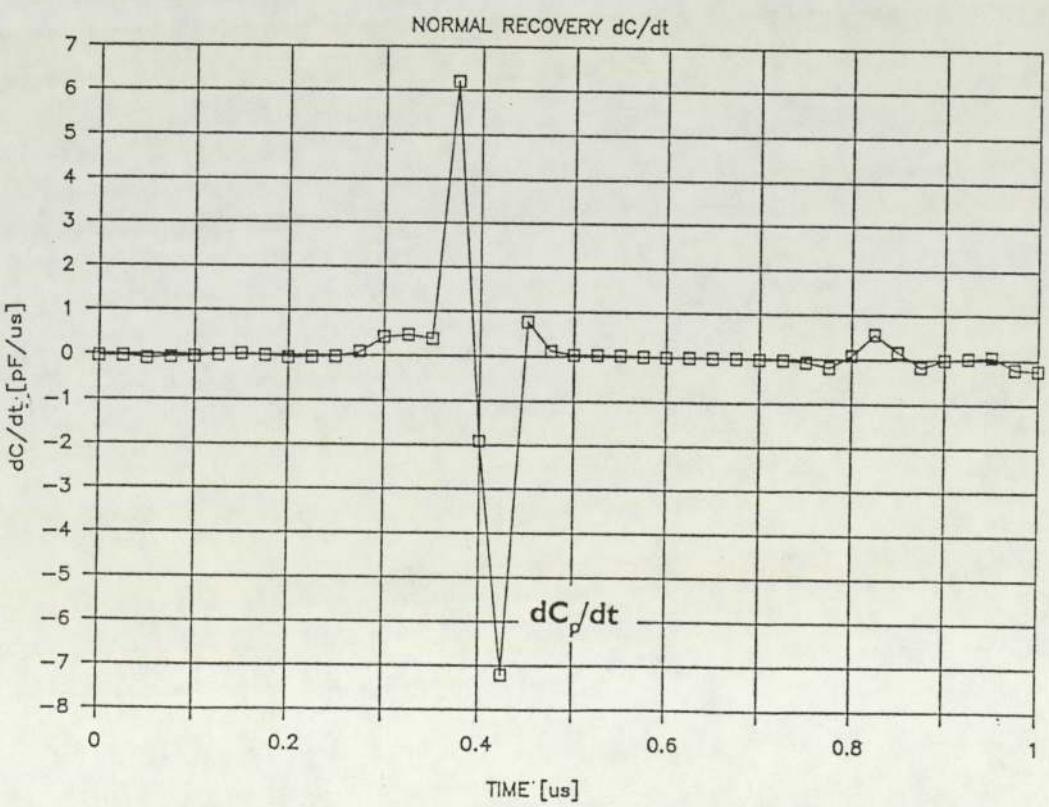
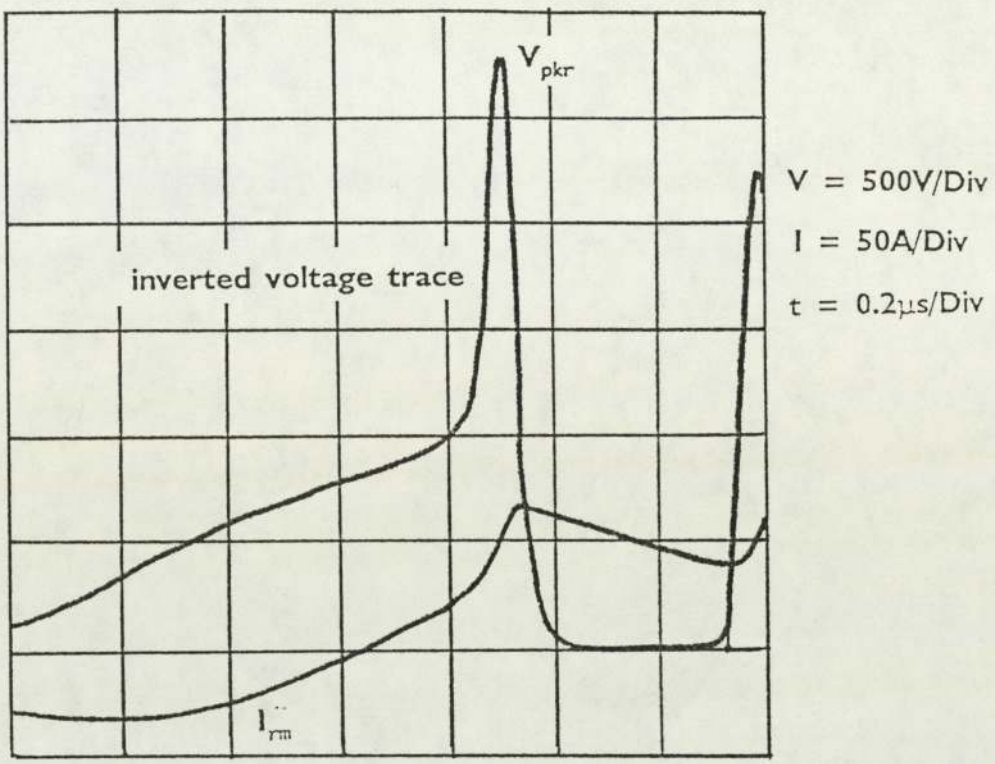


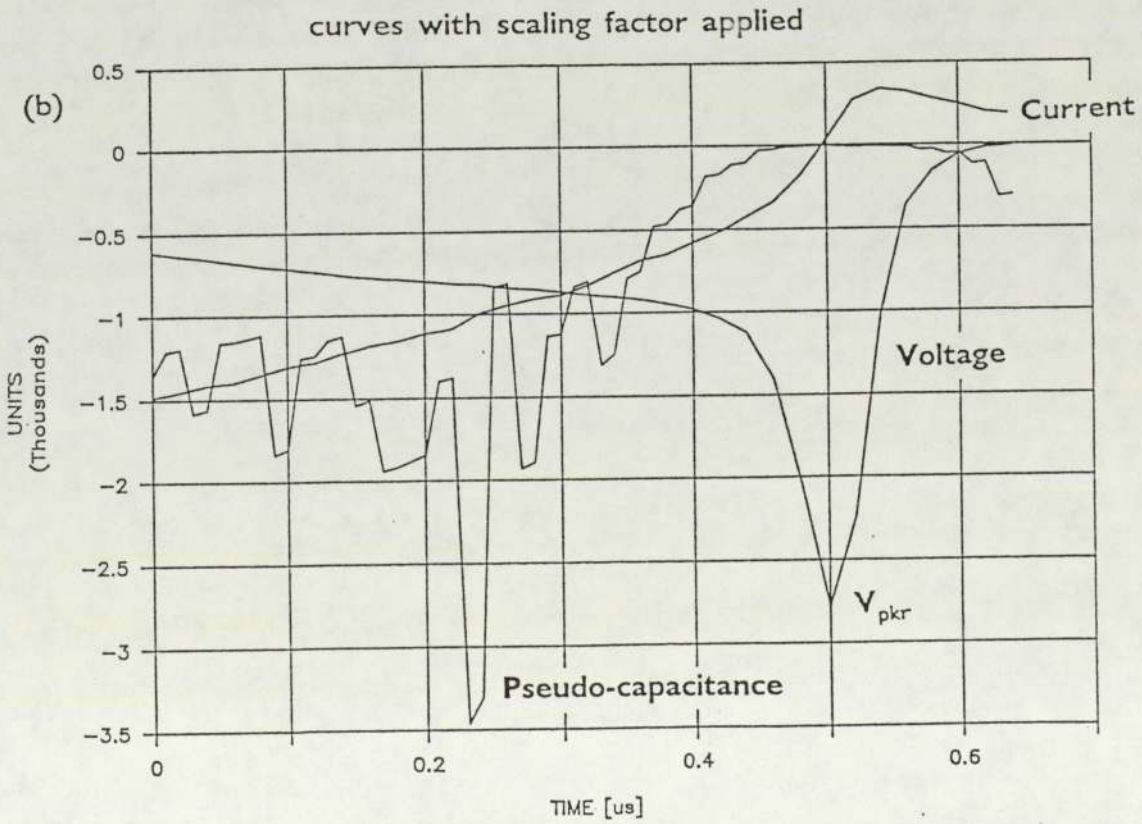
FIGURE 44

(a) Sketch of oscillogram showing diode snap-off.
(b) Graph showing variation of voltage, current and pseudo-capacitance with time.

(a)



(b)



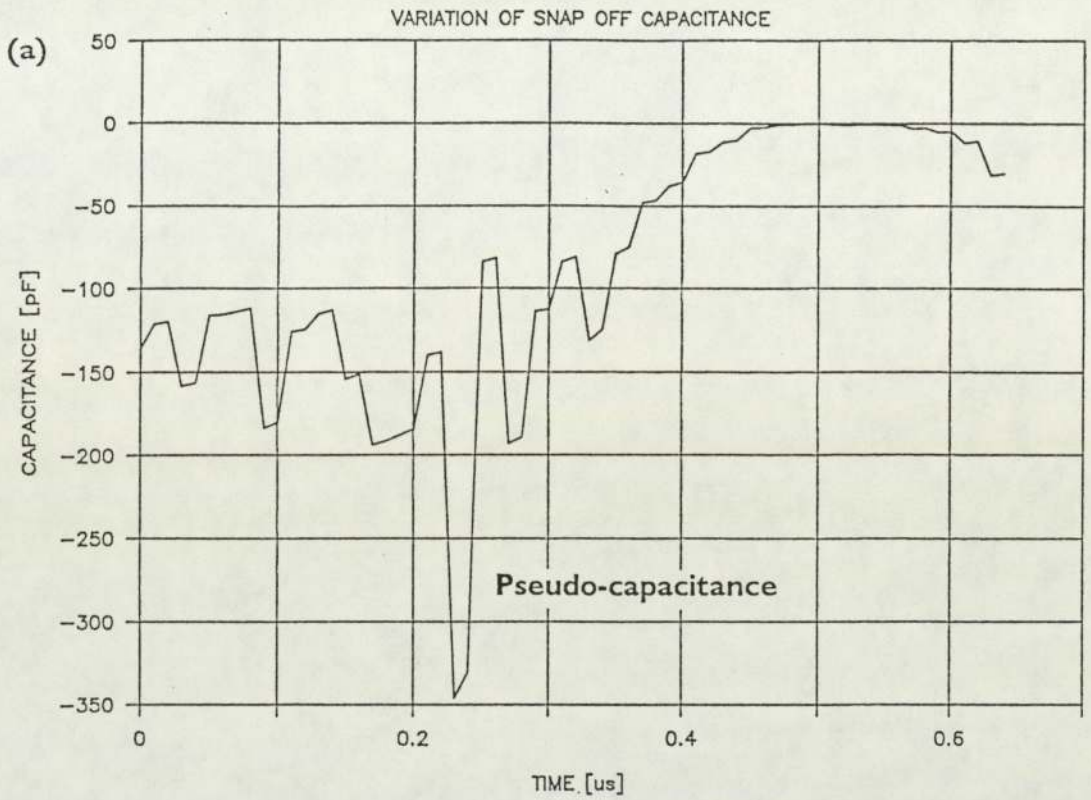
reconstructed from data points measured on figure 44(a). The shape of this curve is very different from that in figure 42(b). Here, oscillations are present on the calculated capacitance waveform, and at the peak reverse recovery voltage the diode pseudo-capacitance is at a minimum, not a maximum as in the normal recovery case. However, there are some similarities between figure 42(b) and 44(b). Both graphs show a peak in the diode pseudo-capacitance followed by a decay to zero capacitance. The difference between normal and snap-off recovery is that in the later this capacitive peak occurs before peak reverse voltage and then decays away to zero at V_{pkr}. Thus at time t = 0.45 μs, when the current waveform can either become abrupt or soft there is only a very small $C_p.dV/dt$ current and a very small $V.dC_p/dt$ current. With only a small capacitive current contribution, the reverse recovery current 'chops' suddenly to zero producing a large L.dI/dt overvoltage.

Referring to figure 45(a) the variation of snap-off pseudo-capacitance is replotted with time. Using this graph as a basis for calculation a graph showing the variation of dC_p/dt with time was constructed as shown in figure 45(b). Thus there are rapid oscillations in the dC_p/dt decaying away to zero at peak reverse recovery voltage.

The variation in pseudo-capacitance during snap-off recovery was then compared with the variation in pseudo-capacitance during snap-off recovery in the presence of a diode snubber network. Figure 46(a) is sketch of an oscillogram showing a diode undergoing snap-off recovery with a snubber network. Figure 46(b) is a graph showing the approximate recovery curves reconstructed from data points measured on figure 46(a). The shape of the pseudo-capacitive curve is similar to that of the normal recovery curve shown in figure 43(b). There is a peak pseudo-capacitance that then decays and switches sign from negative to positive. In addition there are reduced oscillations on the pseudo-capacitive trace prior to the capacitance peak. However there are also some similarities between figure 46(b) and 44(b). In both cases the capacitive peak occurs prior to the peak reverse recovery voltage. In figure 46(b) at time t = 0.45 μs the current waveform can either

FIGURE 45

Graphs showing variation of diode pseudo-capacitance and dC_p/dt with time for a diode undergoing snap-off recovery.



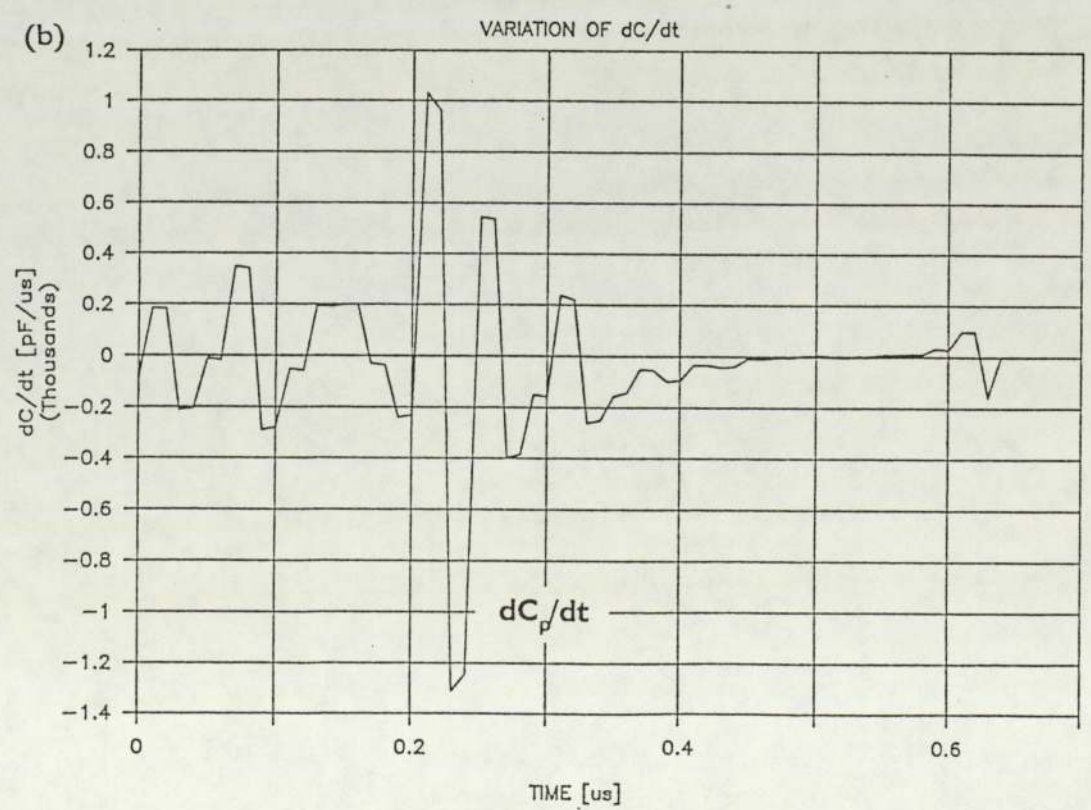
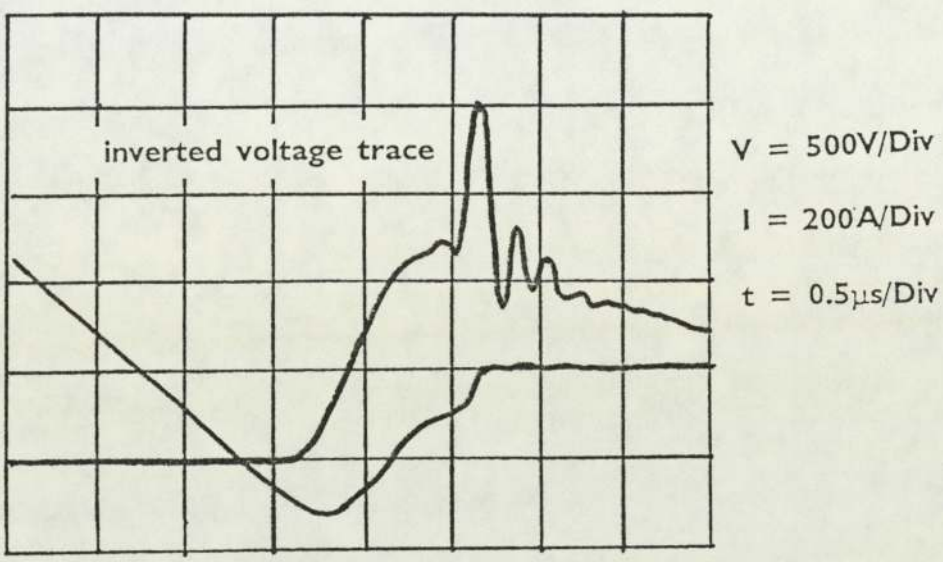


FIGURE 46

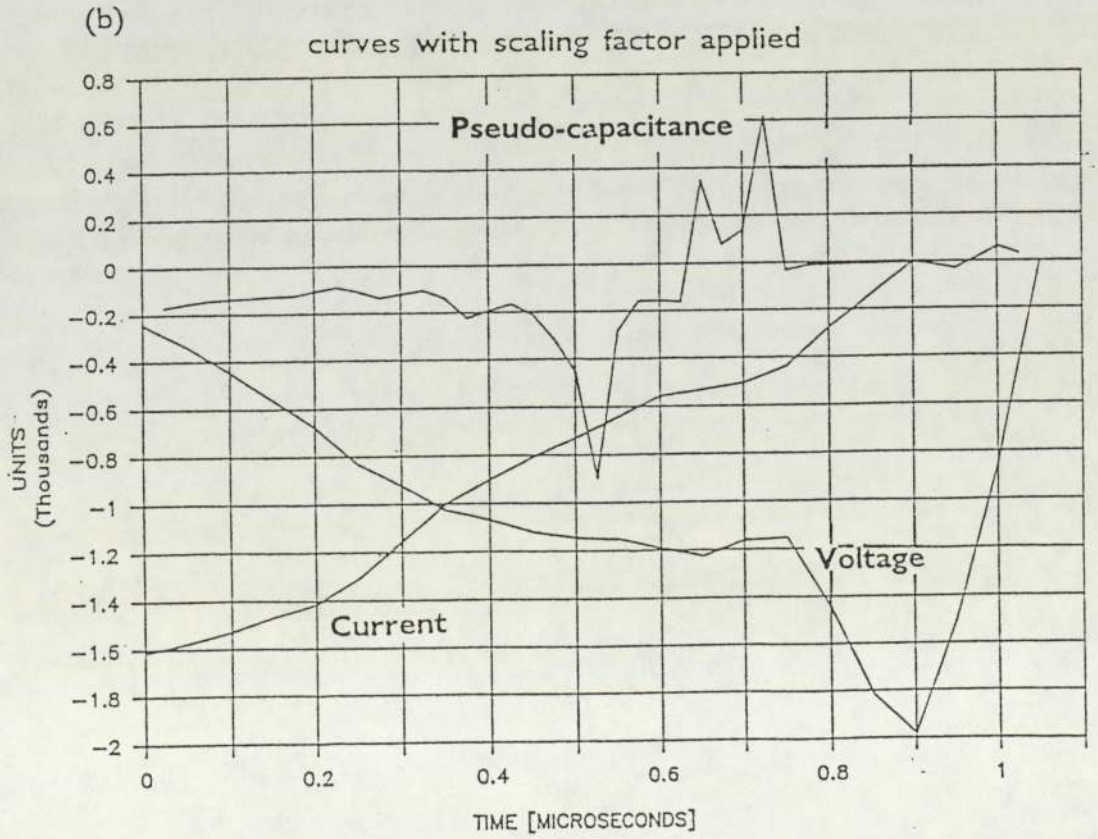
(a) Sketch of oscillogram showing diode snap-off with a snubber network.

(b) Graph showing variation of voltage, current and pseudo-capacitance with time.

(a)



(b)



become abrupt or soft. At this point there is still significant $C_p.dV/dt$ current and also $V.dC_p/dt$ current. Thus the diode reverse current is supported and the recovery is initially 'soft'. Referring to figure 47(a) the variation of snap-off pseudo-capacitance with a snubber network is replotted with time. Using this graph as a basis for calculation, a graph showing the variation of dC_p/dt with time was constructed as shown in figure 47(b). It can be seen that when the diode capacitance drops to zero, dC_p/dt also falls to zero. Thus both the C.dV/dt current and the V.dC/dt are minimal at the same time. This causes the reverse current through the diode to collapse producing a sudden increase in dI/dt. The L.dI/dt overvoltage is limited by the snubber network.

Referring to equation (E59) it can be seen that calculation of the $I_d : dV_d/dt$ ratio is equal to the sum of capacitance C_d plus the product of V_d and dC_d/dV_d.

$$\text{Defining } C_d = \beta.V_d^{-\frac{1}{2}} \quad \text{....[226]} \qquad \text{- (E63)}$$

where β = a constant

$$\text{then} \quad \frac{dC_d}{dV_d} = -\tfrac{1}{2} . \beta.V_d^{-3/2} \qquad \text{- (E64)}$$

Substitution of equation (E64) in equation (E59) gives the following expression:

$$I_d = \frac{dV_d}{dt}. (C_d - \tfrac{1}{2}\beta.V_d^{-1/2}) \qquad \text{- (E65)}$$

Assuming the parallel plate capacitor equation can be applied to the diode capacitance, then:

$$C_d = \varepsilon.A_j/W \qquad \text{- (E66)}$$

where C_d = Diode capacitance

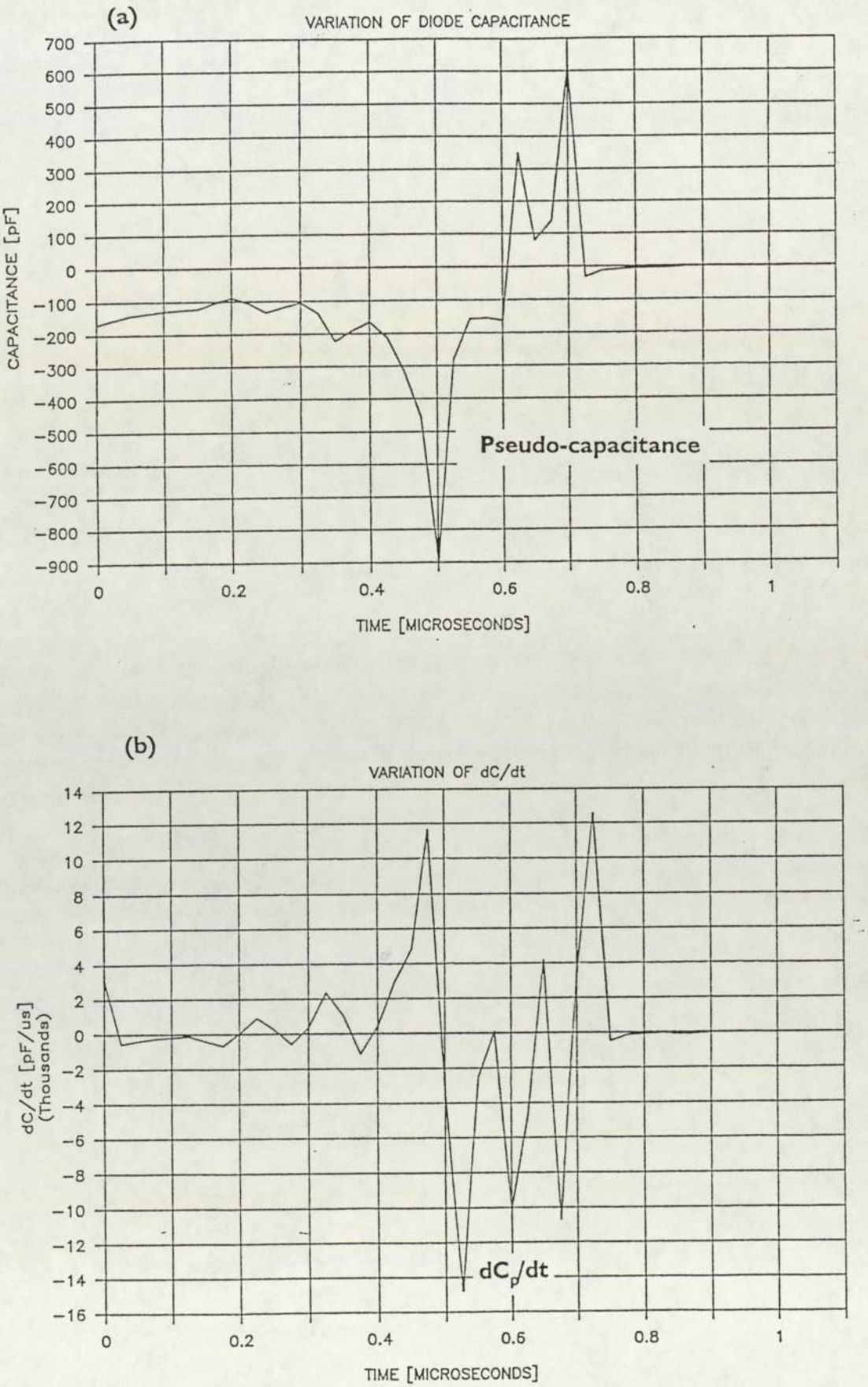
ε = dielectric constant

A_j = Diode junction area

W = Depletion layer width

FIGURE 47

Graphs showing variation of diode pseudo-capacitance and dC_p/dt with time for a diode undergoing snap-off recovery with a snubber network.



By combining equations (E63) and (E66) to eliminate C_d an expression for V_d can be formed.

$$\text{Thus } V_d = \frac{\beta^2.W^2}{\varepsilon^2.A_j^2} \qquad \text{- (E67)}$$

Substitution of equation (E67) into (E65) yields the following expression.

$$I_d = \frac{dV_d}{dt} \cdot \frac{(C_d)}{2} \qquad \text{- (E68)}$$

By defining $2C_1 = C_d$ then calculation of C_1 using the ratio I_d: dV_d/dt would seem to be a valid method of plotting the variation of diode pseudo-capacitance with time. In the general case of:

$$C_d \approx \beta.V_d^{-n} \qquad \text{where } n < 1 \qquad \text{- (E69)}$$

then calculated capacitance C_1 would be related to the parallel plate capacitance by the following relationship.

$$C_1 = C_d/\text{constant} \qquad \text{- (E70)}$$

The value of the constant would be related to 'n' (in practical diodes 'n' can be $\approx$ 0.3). Thus C_1 is a simple fraction of C_d and therefore can be used as an indicator of change of capacitance.

An expression demonstrating how excessive voltage excursions are produced can be constructed by using the substitutions of:

$$\frac{dV_d}{dt} = \frac{dV_d}{dW} \cdot \frac{dW}{dt} \qquad \text{- (E71)}$$

and

$$\frac{dC_d}{dt} = \frac{dC_d}{dW} \cdot \frac{dW}{dt} \qquad \text{- (E72)}$$

then the equation (E54) can be expanded into the following expression

$$I_d = \frac{dW}{dt} \cdot \left[C_d \cdot \frac{dV_d}{dW} + V_d \cdot \frac{dC_d}{dW} \right] \quad \text{- (E73)}$$

Substitution of equation (E67) for V_d and equation (E66) for C_d produces the following expression:

$$I_d = \frac{\beta^2}{\varepsilon . A_j} \cdot \frac{dW}{dt} \quad \text{- (E74)}$$

Thus the diode current is proportional to the propagation velocity of the depletion layer width.

Equation (E74) can now be used to relate the movement of the depletion layer to the peak reverse recovery voltage.

$$\text{Now} \quad V_{pkr} = V_L + V_r \quad \text{- (E75)}$$

where V_{pkr} = the peak reverse recovery voltage

V_L = the overvoltage due to inductance

V_r = the equilibrium recovery circuit voltage when transient voltages due to the inductive effect have receded.

$$\text{Thus} \quad V_{pkr} = L_c \cdot \frac{dI_r}{dt} + L_c \cdot \frac{dI_f}{dt} \quad \text{- (76)}$$

During diode recovery, the recovery current I_r is equivalent to the diode current I_d. Thus by substituting equation (E58) for I_r the following expression is obtained.

$$V_{pkr} = L_c \cdot \left[\frac{\beta^2}{\varepsilon . A_j} \cdot \frac{d^2W}{dt^2} + \frac{dI_f}{dt} \right] \quad \text{-(E77)}$$

Now from equations (E26) and (E32) it can be seen that:

$$Ç = 1 + \frac{\Phi}{L_c \,.\, (dI_f/dt)} \,.\, \frac{d^2W}{dt^2} \qquad \text{-(E78)}$$

Thus the peak reverse recovery voltage is dependent upon the acceleration of the depletion layer, the commutating dI/dt and a constant Φ; where $\Phi = L_c \beta^2/\varepsilon A_j$. The previously described experimental evidence partially supports this equation since L_c, β, A_j and dI_f/dt have all been shown to influence V_{pkr}.

Reduction of (E78) yields the following expression.

$$Ç = 1 + \frac{\Gamma}{(dI_f/dt)} \,.\, \frac{d^2W}{dt^2} \qquad \text{-(E79)}$$

where $\Gamma = \beta^2/\varepsilon.A_j$

Thus the snappiness of the diode is dependent upon the acceleration of the depletion layer during switching. From equation (E79) it can be seen that the quantity Ç is independent of circuit inductance. This is partially supported by the experimental evidence. Figure 16 shows that up to dI_{crit}/dt, Ç is indeed independent of L_c.

4.2.3 **The determination of important physical parameters**

A classic description of diode reverse recovery phenomena has previously been published by Benda and Spenke [50]. Other workers have taken this treatment as their starting point and developed a pin diode model for both the turn-on and turn-off transient [91]. These initial analytical calculations were augmented by a study in which the turn-off transient was treated numerically [141]. The importance of these studies was the insight given into the physical phenomena in diodes during switching rather than their ability to provide readily available and accurate results that could be used for simulations. The equations involved and calculations required, have proved too complicated and time consuming for the ready application to analysis and optimization of a

special circuit. For such simulations a charge control model has been developed [233] and refined [220].

By employing the model suggested by Schunemann and Muller a simple p-i-n charge control model was constructed and then implemented as a software package for computer calculation. It was hoped that such a model would identify which parameters are important during switching events. By also identifying which parameters were unimportant an indication could be obtained as to what parameters could be omitted or reasonably be classed as a constant during the implementation of a simulation model. It was thought that this study would aid in the construction of a numerical model.

4.2.4 **Construction of the p-i-n model**

The equations derived in Appendix A can be assembled into a form suitable for computer evaluation. The first step is to define the known parameters. i.e

μ_i	=	electron mobility	=	1350 $cm^2 .V^{-1}.s^{-1}$
k	=	Boltzmann constant	=	1.38×10^{-23} $J.K^{-1}$
q	=	electronic charge	=	1.602×10^{-19} C

The junction temperature (T) can be assigned a number of values i.e 0 to 400K. These calculations can therefore be used to evaluate the effect of temperature on recovery time. The intrinsic layer width (W_i) can also be assigned a range of values i.e 0 to 10um. Therefore these calculations can be used to evaluate the effect of intrinsic base width on recovery time.

First calculate the intrinsic layer diffusion constant thus:

D_i	=	diffusion constant	=	$\mu_i.k.T/q$

The next step is to calculate the intrinsic layer diffusion length L_i .For example by defining the intrinsic layer charge carrier lifetime as $\tau_i = 8$ μs,

then $L_i = \sqrt{\frac{k.T.\mu_i.\tau_i}{q}}$

Similarly calculate $L_{c\bullet}$ = diffusion length of holes in n contact layer

$$L_{c\bullet} = \sqrt{\frac{k.T.\mu_c.\tau_c}{q}}$$

In the above equation the following are defined as: $\mu_c = 480 cm^2.V^{-1}.s^{-1}$ and $\tau = 8\ \mu s$ (all other parameters have previously been defined).

As an aid to numerical calculation the next step is to define arbitrary variables as equal to the parts of equation (A13) in Appendix A. Thus:

$$X_o = \tfrac{1}{2} . \frac{L_i}{L_{c\bullet}} . \frac{\tau_c}{\tau_i} . \tanh (W_i/2.L_i) \qquad \text{- (E80)}$$

By using the variable 'X_o', 'Y_o' can then be calculated where Y_o is used later to calculate the steady state charge. Then:

$$Y_o = - X_o + \sqrt{X_o^2 + \frac{\tau_c.I_f}{2.L_c.q.P_c.A_j}} \qquad \text{- (E81)}$$

P_c = doping concentration at the contact layers an estimate of this value is $\approx 10^{19}\ cm^{-3}$.

A_j = cross-sectional area of the diode

The area A can be defined but since $J_f \leq 10^3$ A/cm

and $J_f = I_f/A_j$ where I_f = forward current prior to switching

'A_j' may also be defined in terms of the ratio I_f/J_f. There is a lower limit on this value imposed by the maximum current density. If J_f exceeds 10^3 A/cm then the above equation for Y is no longer valid and other relationships must be employed [148]. Hence Q_{co} can be calculated using:

$$Q_{co} = A_j.q.P_c.L_c.Y_o^2 \qquad \text{- (E82)}$$

and

$$Q_{io} = \sqrt{Q_{co}} \cdot \sqrt{\frac{A_j.q.P_c.L_i^2}{L_c}} \cdot 2 \tanh (W_i/2.L_i)$$

The recovery time is then determined by the choice of reverse current since:

$$t_3 = Q_{io}/I_R$$

Therefore the variation of t_3 with the ratio I_f/I_R can be investigated. The reverse current I_R is limited by a similar relationship to that of I_f.

$$J_R \leq 10^3 \text{ where } J_R = I_R/A_j$$

Once the above equations have been evaluated then to calculate the diode voltage at t_3 the variable s must first be calculated by either the trapezoidal or triangular equations. The variable 'a' is used as a test to decide if the carrier distribution is triangular or trapezoidal.

Using $$a = \frac{W_i - (4.D_i.Q_{io})}{W_i.I_R}$$

Then if $a > 0$ use trapezoid distribution and

$$s(t_3) = \frac{W_i}{2} - \sqrt{\left(\frac{W_i}{2} - \frac{a}{2}\right)^2 - \frac{W_i.(W_i-a).I_R.(t_3-t_{23})}{2.Q_{io}}}$$

where $$t_{23} = t_2 + \frac{a.Q_{io}}{W_i.I_R}$$

and $$t_2 = \frac{2.D_i.Q_{io}^2}{W_i^2.I_R^2}$$

If however $a \leq 0$ then the triangular distribution is used hence

$$s(t) = \frac{W_i}{2} - \sqrt{\frac{W_i^2}{4}.\left[1 - \frac{I_R.(t - t_2)}{Q_i(t_2)}\right]}$$

where $Q_i(t_2) = \frac{W_i^2.I_R}{8.D_i}$

and $t_2 = \frac{Q_{io}}{I_R} - \frac{W_i^2}{8.D_i}$

To find the voltage the following equation is then used.

$$|V| = \frac{4}{3} . \sqrt{\frac{2.I_R.s^3}{\varepsilon.A.\mu_i}}$$

The dielectric constant $\varepsilon = 11.9 \times 8.854 \times 10^{-12}$ F.m^{-1}
and the field independent carrier mobility $\mu_i \approx 1350$ cm^2.V^{-1}.s^{-1}

4.2.5 **Results of the computer calculation**

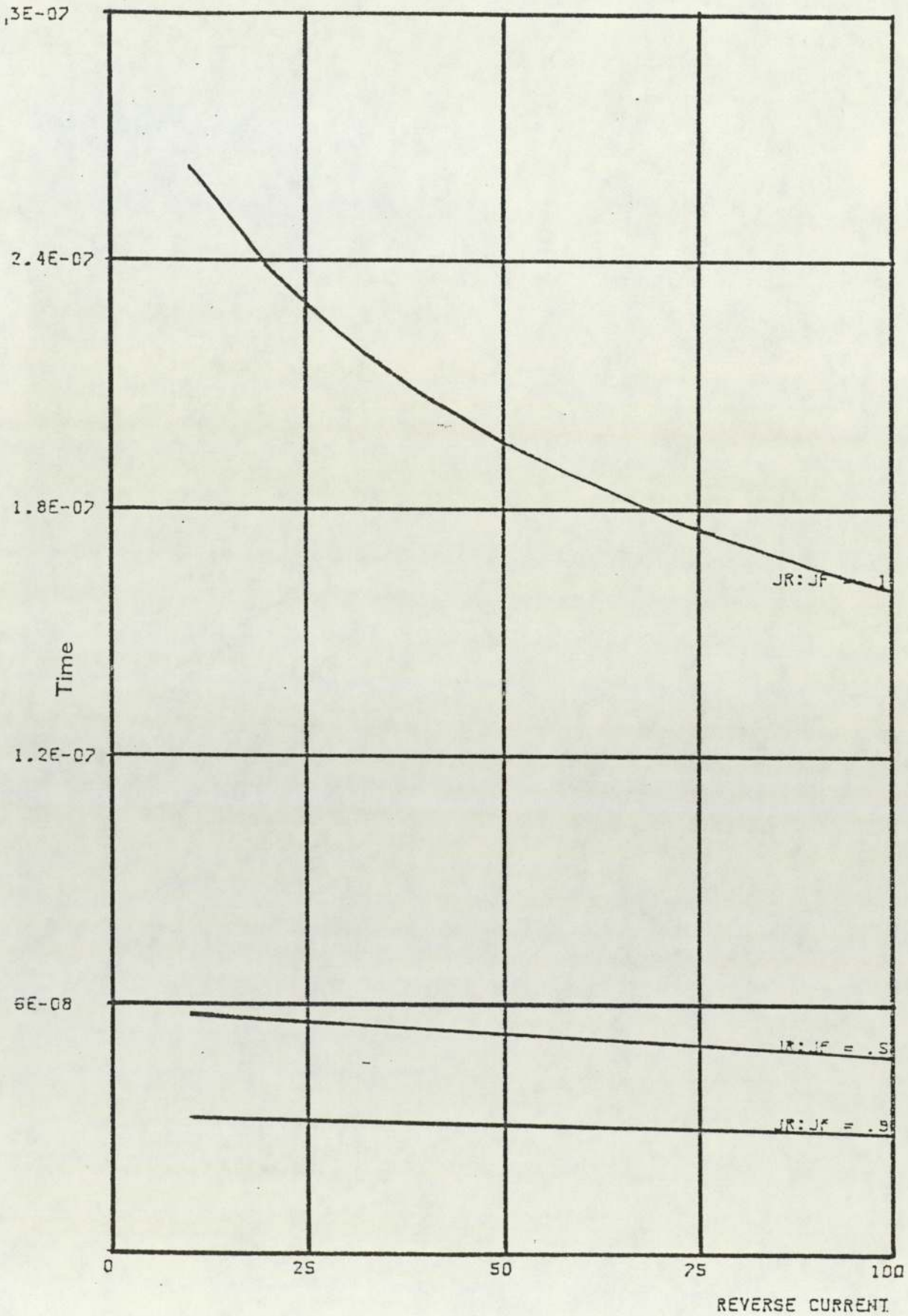
Using the equations described in Appendix A and section 4.2.4 a computer programme was produced. By systematically altering input parameters i.e. the reverse current etc, then graphs could be plotted showing the variation of diode voltage and recovery time with reverse current etc.

Figure 48 shows the variation of diode recovery time with reverse current for various ratios of reverse current to forward current density. It can be seen that generally as the reverse current is increased so the recovery time of the diode decreases. This is an expected result since:

$$t_{rr} = 2.Q_{rr}/I_{rm} \qquad \text{-(E83)}$$

FIGURE 48

Graph showing the variation of recovery time with reverse current.



In addition practical experience indicates that, the higher the value of reverse current that is drawn the quicker the stored charge will be extracted and the quicker the diode will recover.

Curve $J_R : J_F = 0.1$ shows that as the reverse current is increased there is an asymptotic approach towards the x-axis. Thus to decrease the recovery time further the ratio between forward and reverse current needs to be altered. Figure 48 shows that as the ratio $J_R : J_F$ increases then the recovery time decreases. It also indicates that a fundamental limit to recovery time exists, above which further increases in the ratio $J_R : J_F$ and I_R have only a marginal effect.

Figure 49 shows the variation of diode voltage with reverse current. This shows that the junction voltage increases as the reverse current increases. Notice that this calculation predicts that below a certain current no voltage will be produced. Physically, this illustrates that the slower the charge is extracted the lower the voltage will be. If no reverse current is drawn, no stored charge will be extracted. Thus the stored charge will decay internally by recombination and no voltage will be produced.

Figure 50 shows curves produced with similar input parameters to figure 49, but with a quarter of the junction area. Comparing figures 49 and 50 shows that as the junction area is decreased the voltage increases. Figure 51 shows curves produced with the same input parameters as figure 50. Thus comparing figure 48 to figure 51 show that as the junctions area is decreased the diode voltage increases. Physically this is equivalent to increasing or decreasing the cross-sectional area of a uniformly resistive material experiencing a constant current flow. As the cross-sectional area is decreased the resistance thus increases and the ohmic volt drop thus rises.

Figure 52 consists of curves showing how the diode recovery time varies with carrier lifetime. As carrier lifetime is increased so the recovery time increases. This is to be expected since experimental work has shown that:

FIGURE 49

Graph showing the variation of voltage with reverse current.

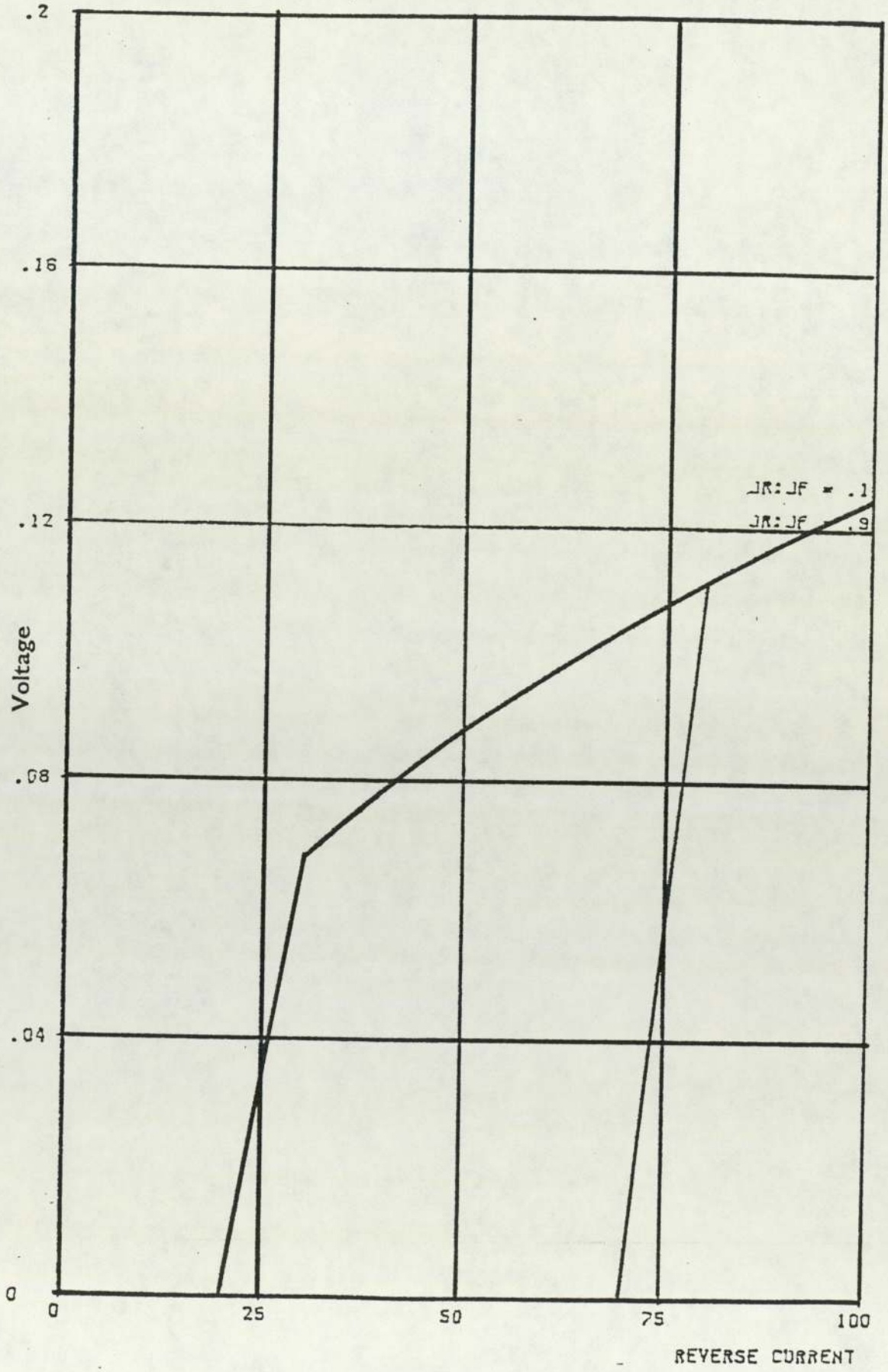


FIGURE 50

Graph showing the variation of voltage with reverse current.

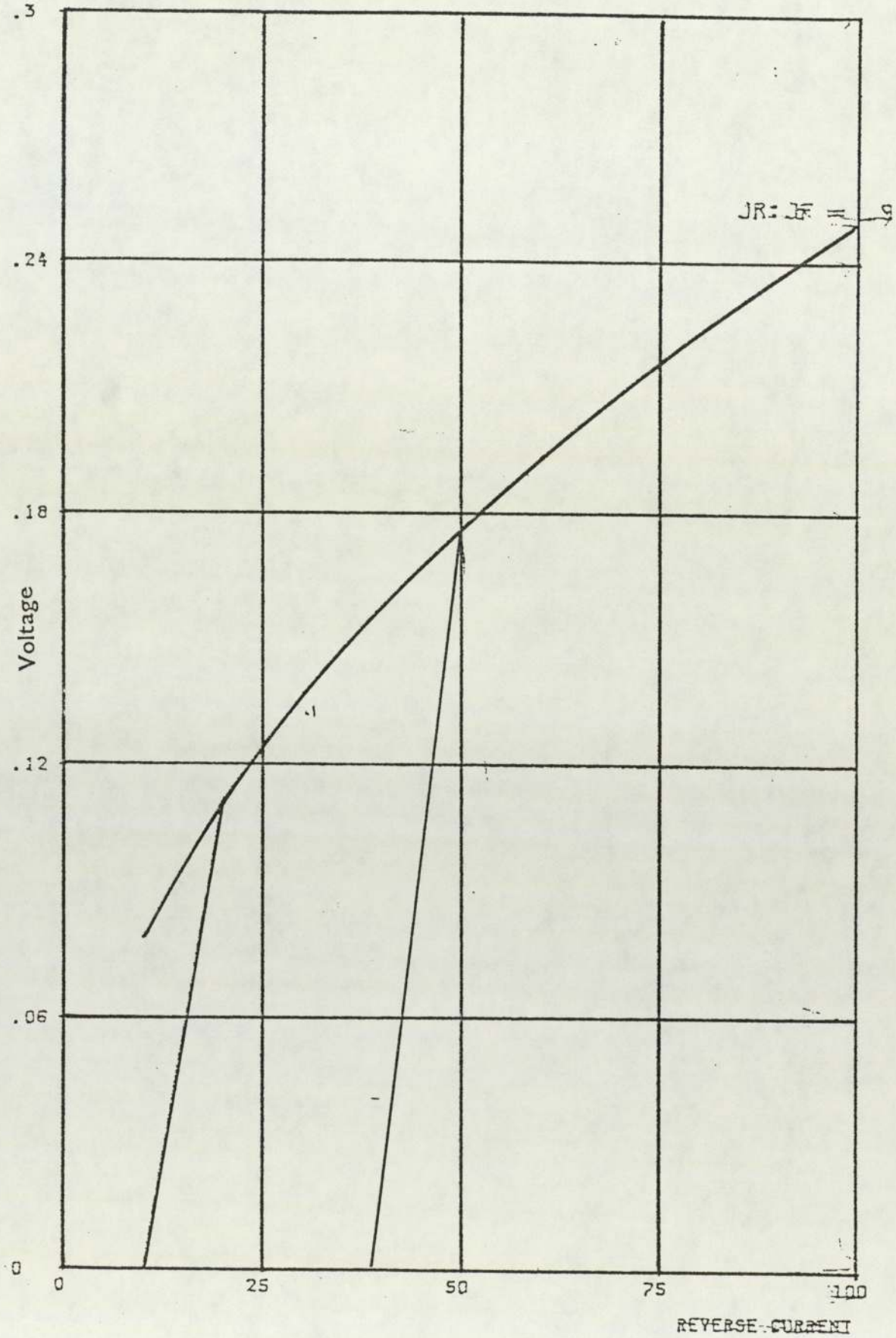


FIGURE 51

Graph showing the variation of recovery time with reverse current.

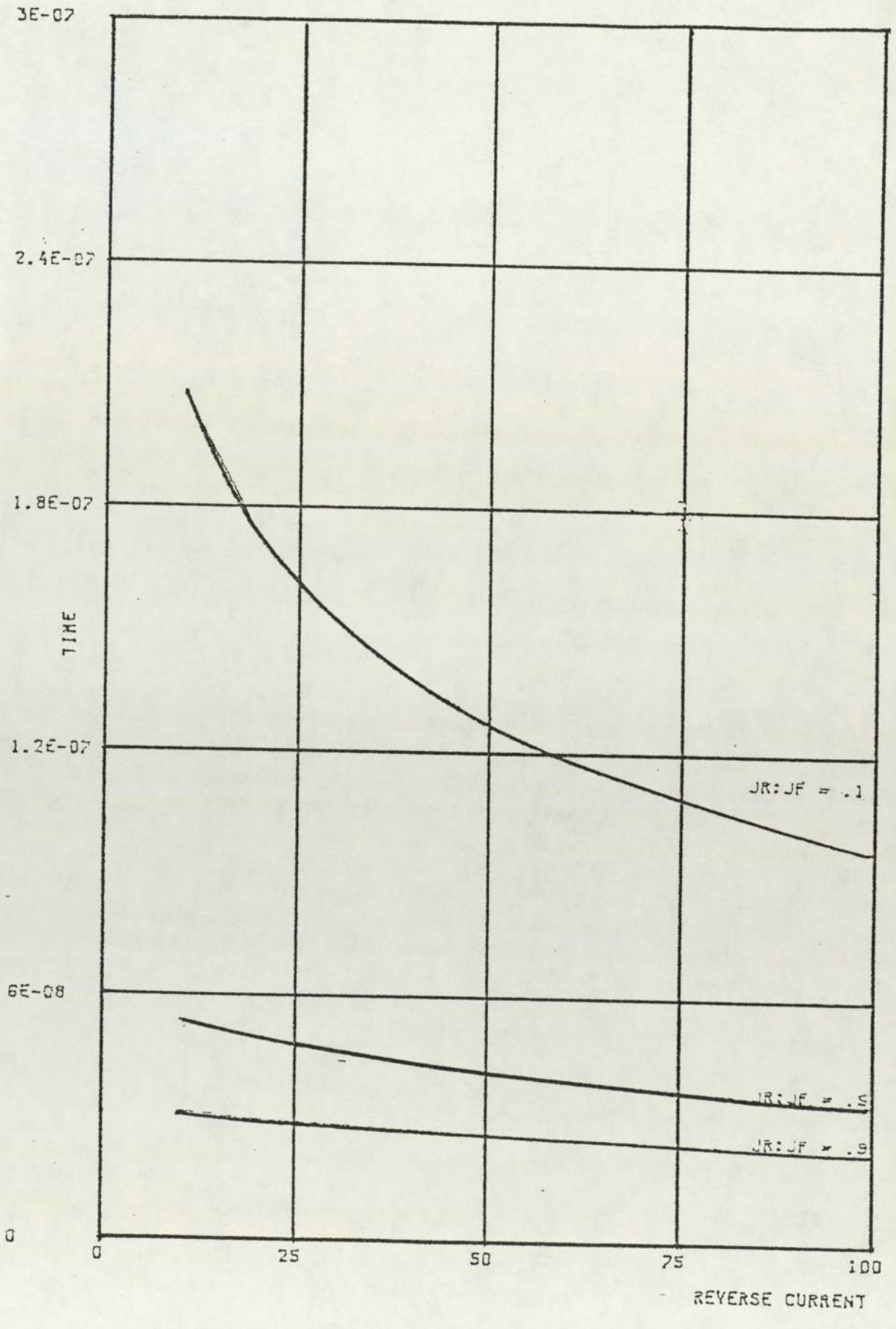
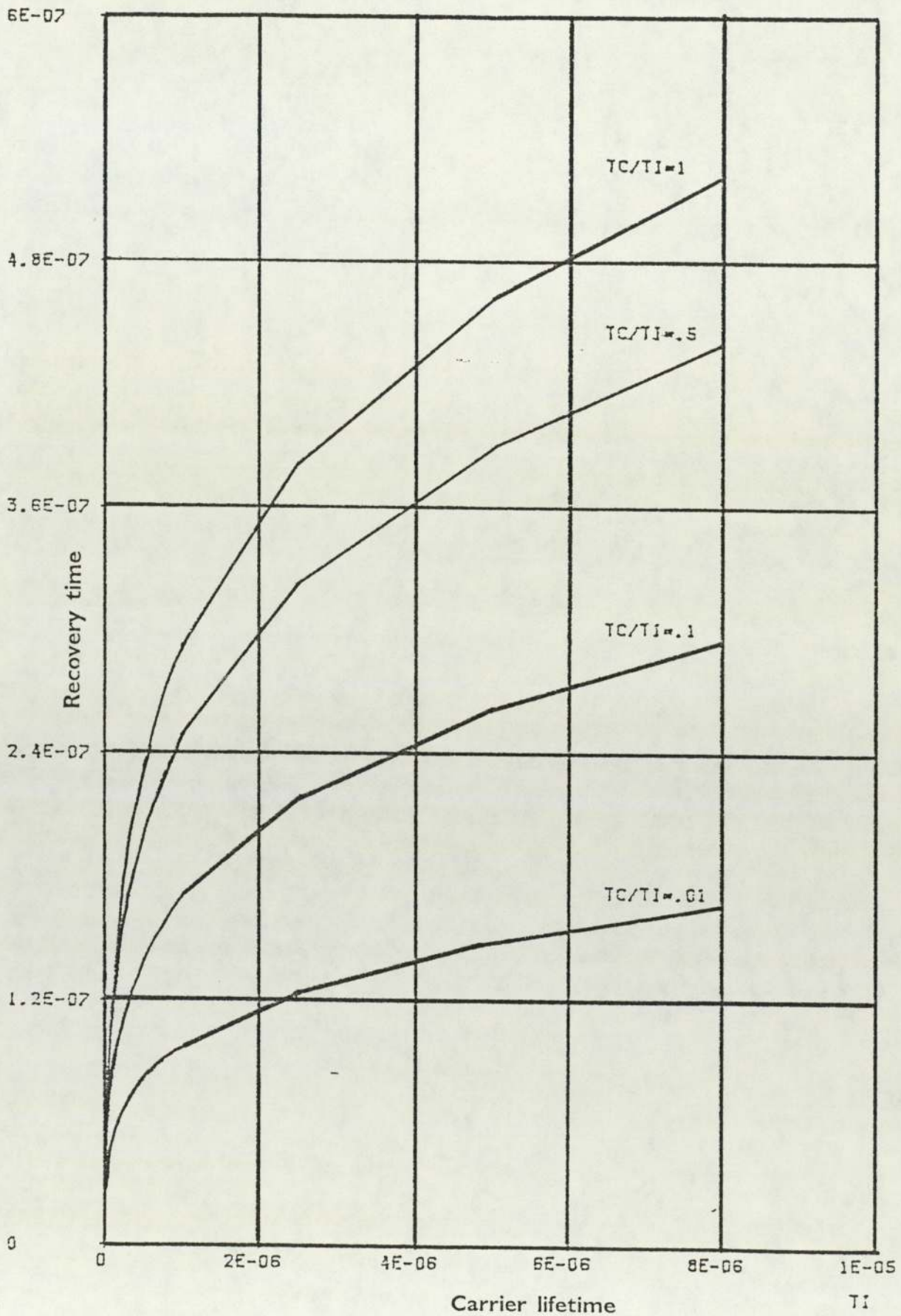


FIGURE 52

Graph showing the variation of recovery time with carrier lifetime.



TEMPERATURE=250 FORWARD CURRENT=100 AREA= 1 JF=100 JR=50

$$t_{rr} \approx 2.I_f.\tau/I_{rm} \qquad \text{-(E84)}$$

The multiple curves also demonstrate that as the carrier lifetime ratio τ_c/τ_i decreases so the diode recovery time decreases.

Comparison of figures 52, 53 and 54 shows that the recovery time decreases with increasing temperature. This is an unexpected result since the stored charge in a diode is a strong function of temperature. However in practical cases the recovery time of ultrafast diodes (i.e those devices manufactured using some carrier lifetime killing technique) is generally a weak function of operating conditions. It would be expected therefore that as the carrier lifetime is increased the effect of temperature is more pronounced.
This expectation coincides with the results shown in figures 52, 53 and 54. A physical interpretation of this would be that as the temperature of the charge carriers increases so does their velocity due to the following equivalence.

$$1/3.k.T = 1/2.m_e.v_e^2 \quad \text{- (equipartition of energy equation)} \qquad \text{-(E85)}$$

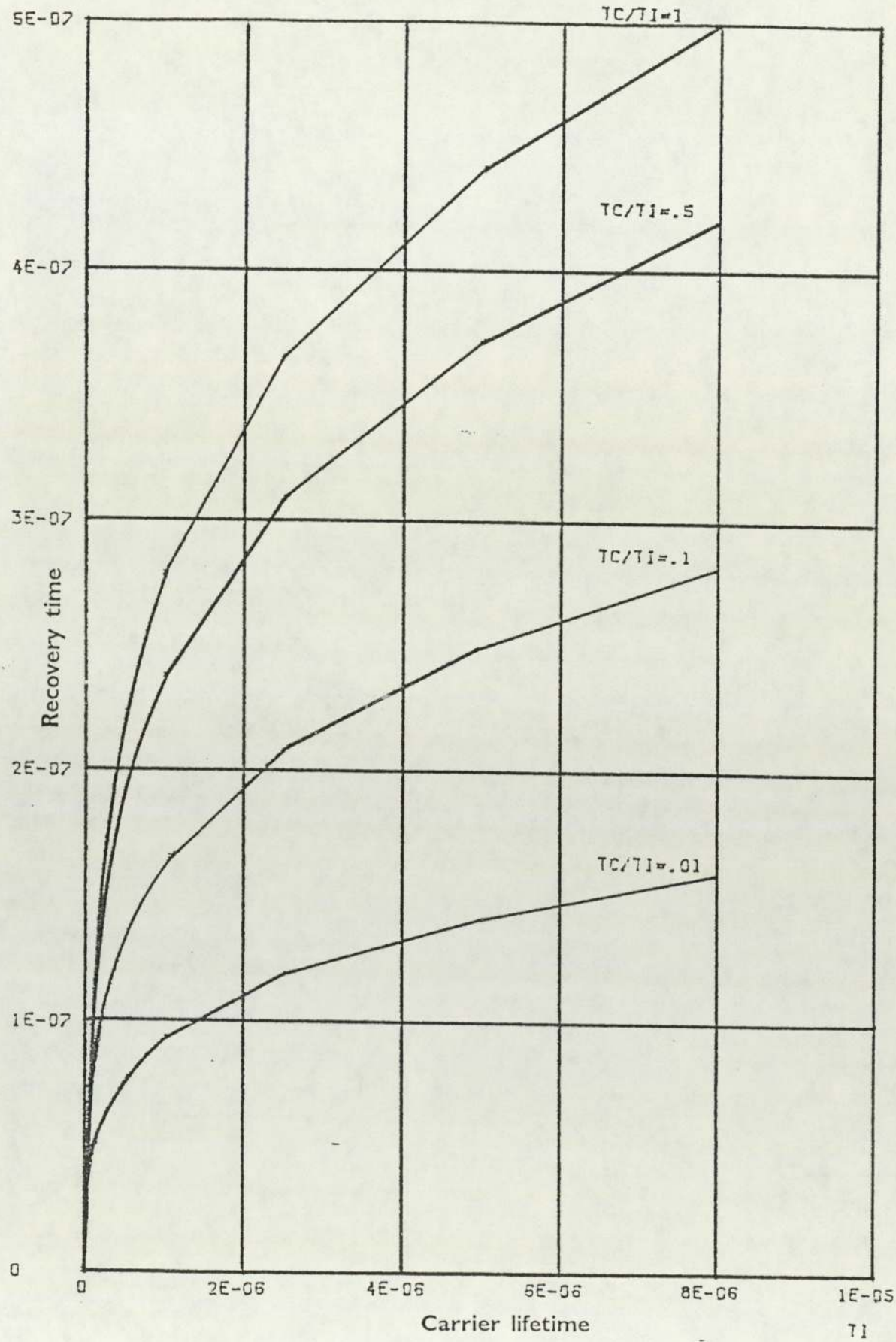
where m_e = mass of electron
v_e = electron velocity

Thus the diffusion velocity near the junction boundary increases with temperature, carriers are therefore extracted more rapidly reducing the recovery time. At the same time as the temperature of the device is increased the stored charge increases and thus the recovery time should increase. The actual recovery time is a function of these conflicting trends.

Figure 55 shows the variation of recovery time against diode base width for three different temperatures. These results are in agreement with those previously presented in figures 52, 53, and 54. The curves show that as the temperature increases the recovery time decreases. However, this is a weak effect. Figure 57 also shows that as the base width of the diode is increased so the recovery time increases. This relationship has a physical explanation in that by increasing the diode width, the volume of silicon and thus the stored charge

FIGURE 53

Graph showing the variation of recovery time with carrier lifetime.



TEMPERATURE=300 FORWARD CURRENT=100 AREA= 1 JF=100 JR=50 WIDTH=1E-04

FIGURE 54

Graph showing the variation of recovery time with carrier lifetime.

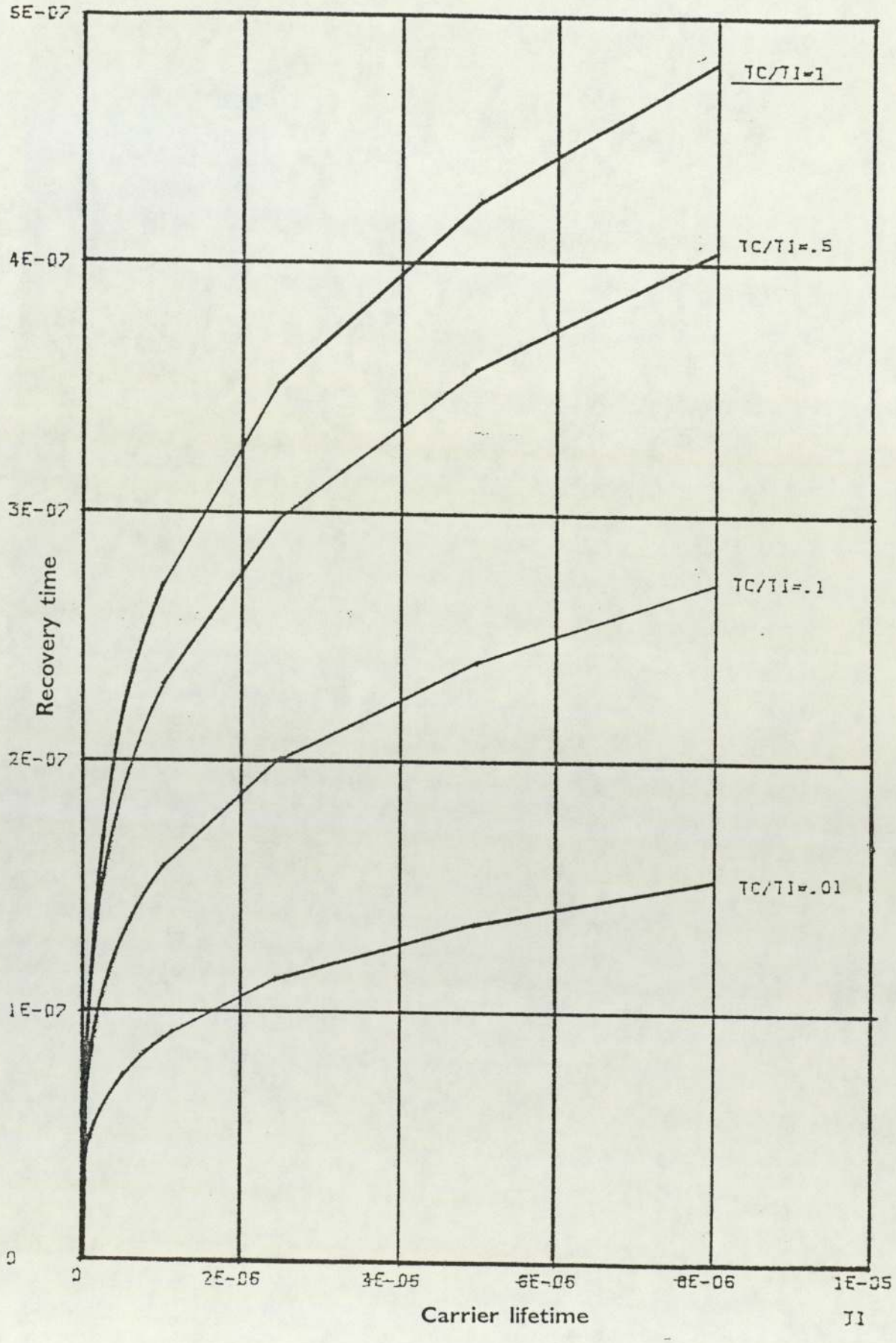
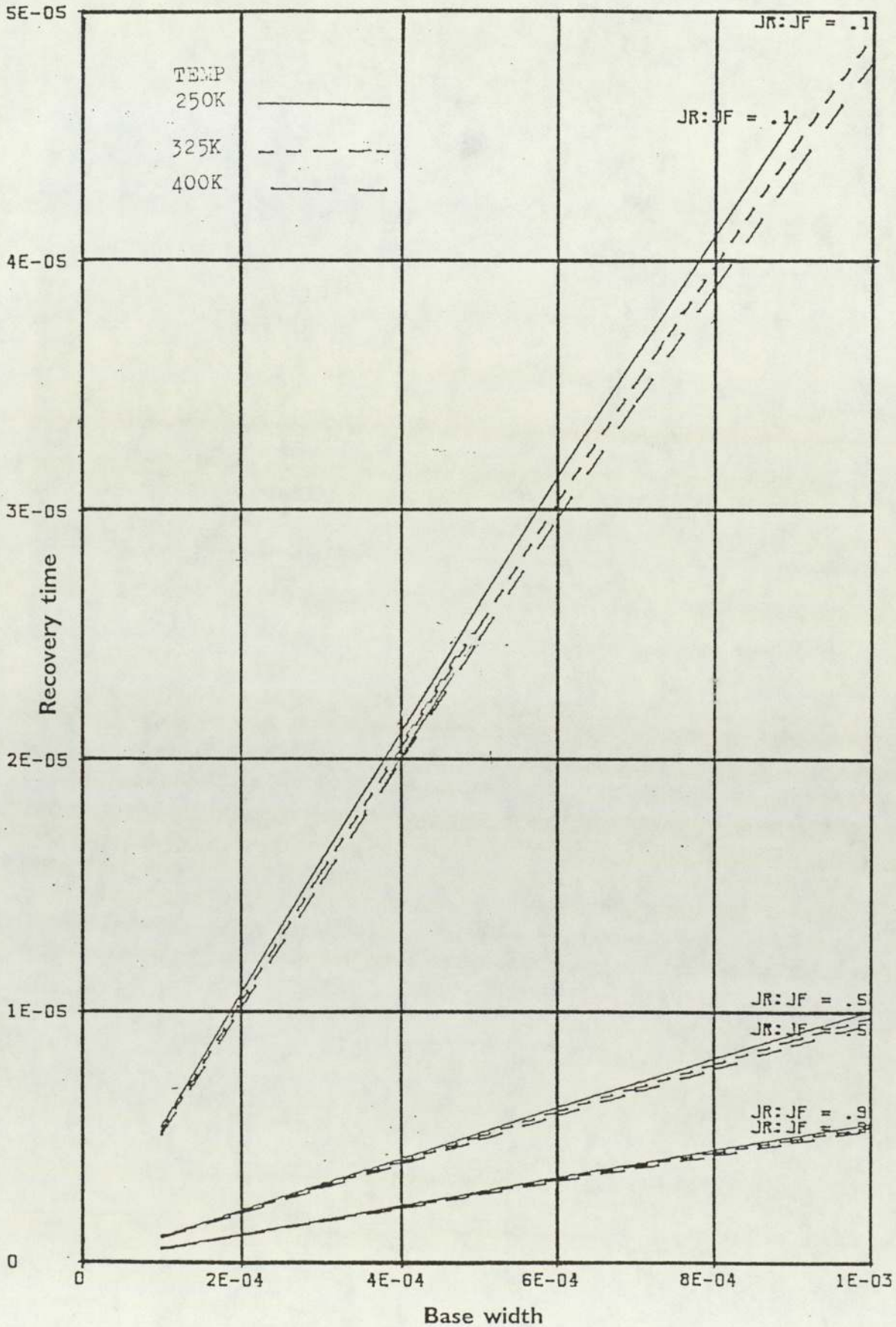


FIGURE 55

Graph showing the variation of recovery time with diode base width.



is increased. Thus not only is there more charge to be extracted, but it has a greater mean distance to travel out of the base region.

This 'volume effect' is more pronounced in figure 56. Here the curves show the variation of recovery time with diode base width for various diameters. As the silicon volume of the device increases so the recovery time becomes greater.

Figure 57 shows the variation of recovery time with diode base width for various values of forward current. As the value of forward current is increased the recovery time also increases.

4.2.6 **Models of physical parameters**

The results described in section 4.2.5 demonstrated that important diode recovery parameters are carrier lifetime and device geometry. Carrier lifetime is determined by the rate of electron/hole recombination. Thus descriptive equations of the recombination process are required if carrier lifetime effects are to be taken account of. The device geometry is a significant factor in determining the rate of charge extraction. To account for this effect descriptive equations are required for carrier mobility.

4.2.6.1 **Recombination**

In a semiconductor crystal shared valence electrons forming a covalent bond can 'escape' after receiving energy (e.g. from a phonon) to produce a free electron and a hole in the bond. This hole can be treated as a positively charged particle. The reverse process when a free electron is 'caught' by a hole is called recombination. An electron does not combine with a hole directly but must first be caught by a trap (usually a discontinuity or dislocation in the lattice structure). When a hole is then caught by the trap, carrier annihilation then occurs as the 'free' electron combines with the hole to form a covalent bond. This type of recombination is known as Shockley-Hall-Read combination [33, 31, 250, 251, 253, 254, 34, 92]. Electron/hole annihilation can

FIGURE 56

Graph showing the variation of recovery time with diode base width.

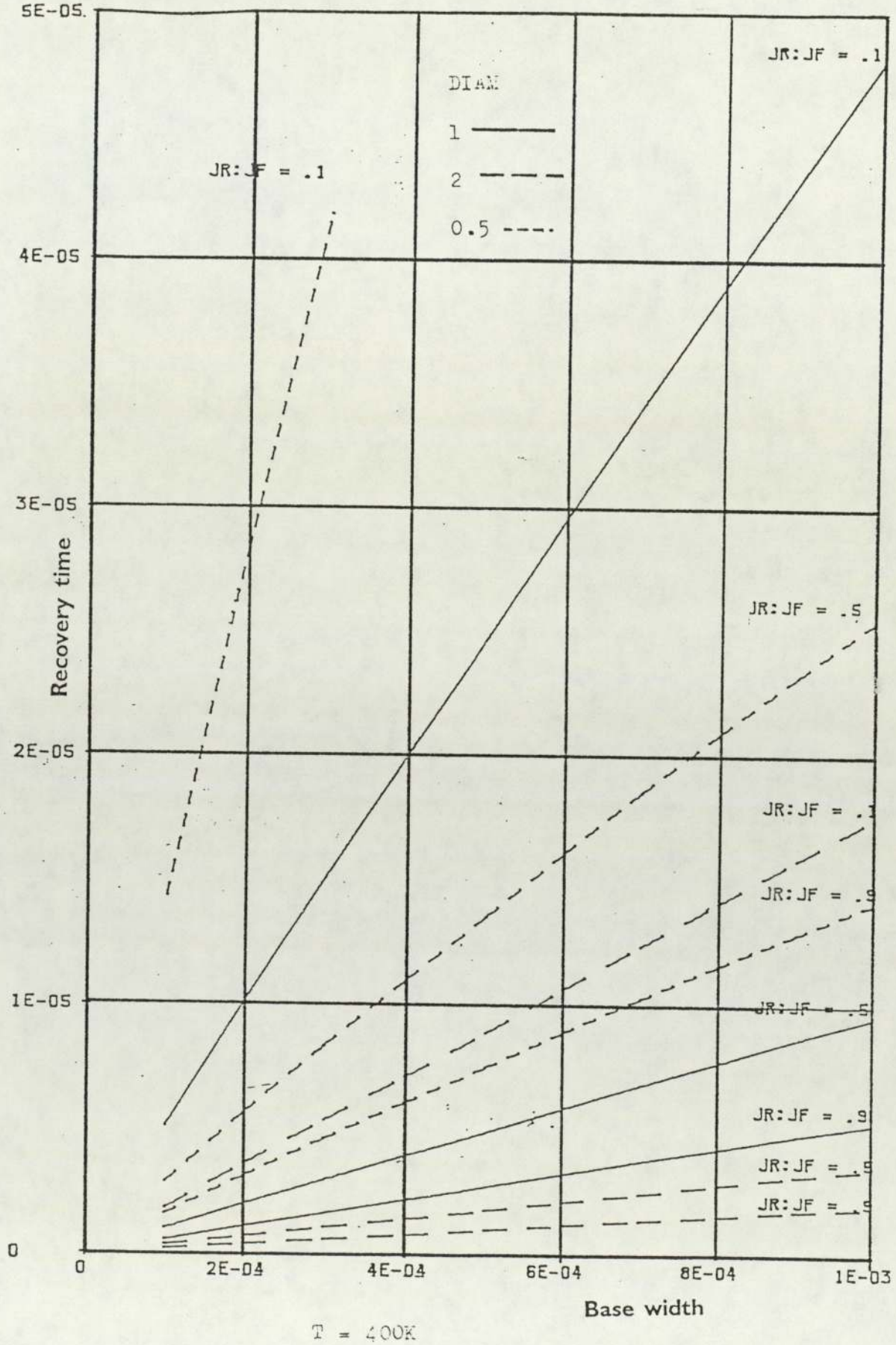
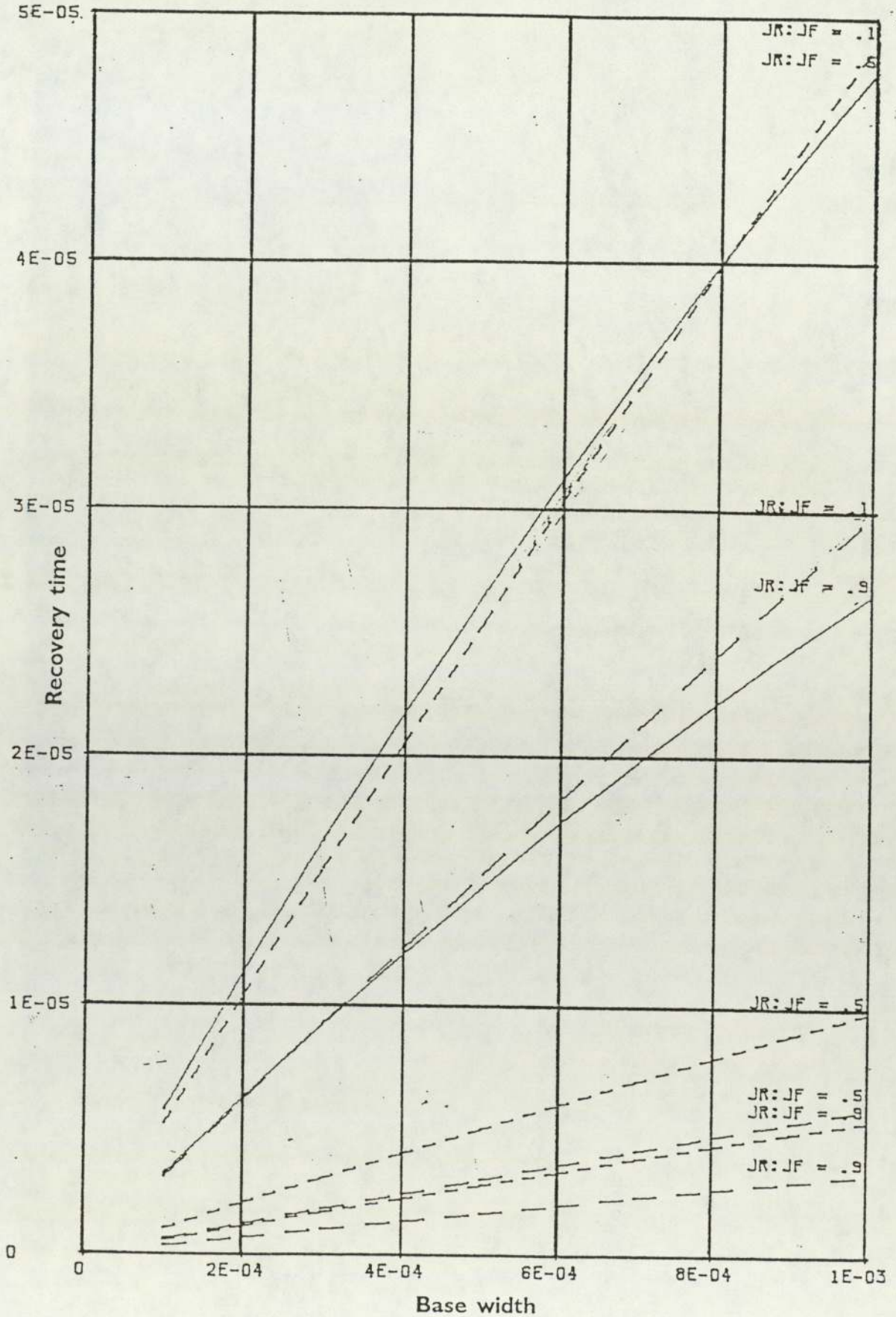


FIGURE 57

Graph showing the variation of recovery time with diode base width.



also occur due to the Auger process [27, 255, 256]. In this process the energy released due to recombination is not released into the lattice in terms of a temperature rise but is transferred to another electron. These two recombination processes are the most important for high power devices. From the published work quoted above the following equations can be stated:

$$R_{SHR} = \frac{p.n - n_i^2}{\tau_{n1}.(p + p_1) + \tau_{p1}.(n + n_1)} \quad - \quad (E86)$$

Where R_{SHR} = Shockley - Hall - Read recombination rate.

p = Hole concentration

n = Electron concentration

n_i = Intrinsic carrier concentration

τ_{n1} = $(c_{n1} . N_T)^{-1}$, Electron lifetime for energy level 1

c_{n1} = Electron capture rate for energy level 1

N_T = Trap concentration

p_1 = Hole concentration if $E_f = E_{T1}$

τ_{p1} = $(c_{p1} . N_T)^{-1}$, Hole lifetime for energy level 1

c_{p1} = Hole capture rate for level 1

n_1 = Electron concentration if $E_F = E_{T1}$

E_F = Fermi energy level

E_{T1} = Trap energy level

Equation E86 refers to traps introduced by Gold diffusion. This process introduces two main energy levels between the valance and conduction band. Since level 1 is dominant, only this energy change is incorporated into the equation.

The Auger recombination rate is given by:

$$R_{AUG} = (p.n - n_i^2).(c_n.n + c_p.p) \quad - \quad (E87)$$

where $c_n = 2.8 \times 10^{-31}$ cm^6 s^{-1}

$c_p = 9.9 \times 10^{-32}$ cm^6 s^{-1}

The total recombination rate is the sum of the Shockley - Hall - Read and Auger rates. Thus the total recombination rate R_o is given by:

$$R_o = R_{SHR} + R_{AUG} \qquad \text{-(E88)}$$

The carrier lifetime is related to the recombination rate by the following equations:

$$\tau_n = (n - n_o) / R_o \qquad \text{-(E89)}$$

and

$$\tau_p = (p - p_o) / R_o \qquad \text{-(E90)}$$

where n_o and p_o are the electron and hole equilibrium concentrations.

4.2.6.2 **Mobility**

The drift velocity of both holes and electrons in an electric field are related by a proportionality parameter termed the carrier mobility [51]. Hence:

$$v_n = -\mu_n.E \qquad \text{-(E91)}$$

$$v_p = \mu_p.E \qquad \text{-(E92)}$$

Although for simplicity many workers assume the carrier mobility to be constant, in reality this is not the case. Variations in the carrier drift velocity are caused by scattering events as the carrier passes through the semiconductor lattice structure. Thus scattering can be caused by:

1) Impact with atoms in the crystal lattice of silicon.
2) Impact with ionized shallow impurity atoms.
3) By colliding with another free carrier.

The velocity of charge carriers also saturates for high electric fields and this condition can exist with high stress transients during switching. Lattice scattering is a function of temperature. This is because as the lattice temperature increases so the vibration of the lattice and thus its collision cross-section is increased. Thus the probability of a collision increases while the

carrier mobility decreases. The magnitude of this effect can be calculated using the following equation [258,61].

$$\mu_T = \mu_o.(T/T_o)^{\Theta} \qquad \text{-(E93)}$$

where μ_T = lattice mobility (scattering due to lattice/carrier collisions)
μ_o = lattice mobility at 300K
T_o = 300K
Θ = - 2.2

There is also a correction to be added to the above equation due to ionized impurity scattering. [259, 260]. As the concentration of ionized impurity increases the carrier mobility decreases since the probability of a scattering event goes up. This relationship is also dependent on temperature. The Brooks-Herring formula [258, 259, 260] can be used to calculate the ionized impurity mobility μ_{ii}. Thus:

$$\mu_{ii} = \frac{Ä\ T^{1.5}}{N_D} . \left[\ln(1+G_o.T^2/N_D) - \frac{G_o\ T^2}{N_D+G_oT^2} \right]^{-1} \qquad \text{(E94)}$$

where μ_{ii} = ionized impurity mobility
$Ä$ = 4.61×10^{17} $cm^{-1}.V^{-1}.s^{-1}.K^{-3/2}$ for electrons
& 1.00×10^{17} $cm^{-1}.V^{-1}.s^{-1}.K^{-3/2}$ for holes
N_D = Shallow impurity concentration
G_o = 1.52×10^{15} $cm^{-3}.K^{-2}$ for electrons
& 6.25×10^{14} $cm^{-3}.K^{-2}$ for holes

The carrier/carrier scattering effect can be compensated for by using the following equation [90].

$$\mu_{cc} = H.T^{1.5}\ (pn)^{-0.5}\ (\ln(1+ ZT^2\ (np)^{-0.3}))^{-1} \qquad \text{-(E95)}$$

where H = 2.00×10^{17} $cm^{-1}\ V^{-1}\ s^{-1}\ K^{-3/2}$
Z = 8.28×10^{8} $cm^{-2}\ K^{-2}$
μ_{cc} = carrier-carrier scattering mobility

The three types of mobility corrections can be combined to yield the following suite of equations.

$$\Phi = \{ 6.\mu_T .(\mu_{ii}^{-1} + \mu_c^{-1})^{-1} \}^{½} \qquad \text{-(E96)}$$

$$f(\Phi) \approx \frac{1.025}{1 + (\Phi/1.68)^{1.43}} - 0.025 \qquad \text{-(E97)}$$

and therefore

$$\mu = \mu_T f(\Phi) \qquad \text{-(E98)}$$

4.2.7 The fundamental semiconductor device equations

From studies in the previous chapters it is thought that the variation of diode capacitance plays a significant role in the generation of voltage spikes. This capacitance variation is dependent upon the movement of depletion layer boundaries. The study outlined in section 4.2.2 demonstrates that the generated voltage spike is specifically dependent upon the rate of change of depletion layer propagation velocity. As a starting point for the calculation of transient capacitance, Poisson's equation can be used.

$$\nabla^2 ¥ = \frac{q}{\varepsilon} . (n-p-N) \qquad \text{-(E99)}$$

To make a complete evaluation the hole and electron continuity equations [59] should also be used to obtain a solution.

$$\nabla. (\mu_p.p.\nabla ¥ + D_p.\nabla p) = R_o \qquad \text{-(E100)}$$

and $$\nabla. (\mu_n.n.\nabla ¥ - D_n.\nabla n) = -R_o \qquad \text{-(E101)}$$

Here p and n are particle numbers of holes and electrons respectively, μ_p and μ_n are the corresponding mobilities. Hence the need for expression given for mobility in section 4.2.6.2. R_o is the recombination term, N the doping profile and ¥ is the electric potential. An expression for the recombination term is given in section 4.2.6.1. This gives a system of three scalar equations for three

quantities ¥, n and p [262]. In the above system the dependent variables are ¥, n and p. These dependent variables can be changed to provide a more linear set of equations that are also more matched in terms of 'scaling'.

The scaling of variables to obtain dimensionless quantities assists in the numerical computation [261]. Thus electrostatic potential can be scaled by the thermal voltage U_T such that $¥_T = ¥/U_T$. Similarly carrier concentrations can be scaled by the order of maximum doping concentration N_m to give $P_D = P/ N_m$. The mobility can be scaled by a constant μ_k so that $\mu_o = \mu/\mu_k$.

One set of variables that have been used successfully in numerical computations is that of ¥, ϕ_n and ϕ_p. The terms ϕ_n and ϕ_p are called quasi-fermi potentials and are related to the carrier concentrations via expressions derived from the classical Boltzmann approximation to Fermi-Dirac statistics. Thus:

$$n = n_i \exp [\sigma (¥ - \phi_n)] \quad - \quad (E102)$$

$$p = n_i \exp [\sigma (\phi_p - ¥)] \quad - \quad (E103)$$

where $\sigma = q/ k.T$

The advantage of using these variables is that they are all of the same order of magnitude reducing the risk of computational overflow/under-flow errors during numerical evaluation. In addition equations (E102) and (E103) guarantee that the carrier concentrations will always be positive - even in the presence of numerical errors. The major disadvantage is the exponential non-linearity in all three equations. Since ϕ_p and ϕ_n depend exponentially on applied voltage, they are highly unusable in practical calculations exceeding 1000 Volts for V_a. Thus ϕ_p and ϕ_n are unsuitable for snap-off calculations where voltages produced are measured in thousands of volts. There are other possible sets of variables, but basically there exists a trade-off between the exponential character of the unknowns to the non-linearity of the equations. Linearisation techniques [84] can greatly simplify the solution strategy. Solving linear equations generally involves less computational effort than solving non-linear equations.

4.3 Solution strategy

4.3.1 Introduction

A literature survey was undertaken to assess the suitability of various solution strategies [47, 48, 53, 56, 58, 72, 78, 80, 111, 119, 134, 201, 208]. Commercially available software was also assessed [68, 107, 108, 109, 181].

This survey covered both device modelling [86, 120, 121, 133, 225] and device/circuit interactions [85, 100, 99, 102, 103, 105, 157]. The finite element method was chosen for further investigation and various iterative methods [49], matrix ordering techniques [117, 118, 135] and convergence considerations [55] were studied.

4.3.2 History of semiconductor device modelling

In the days before powerful digital computers were generally available analytical techniques with closed form solutions were used to solve semiconductor problems. Workers such as Shockley [139] pioneered the segmentation approach of dividing the device into small areas over which linear approximations could be applied. Such a technique provided a basic insight into device behaviour but was unable to offer the accurate solutions that were required for device design and optimisation. The demand for a more rigorous solution could only be satisfied by using a numerical technique applicable to solution by computer.

Early numerical simulations such as Gummel's steady-state transistor simulation [67] were one dimensional in nature. De Mari [224, 248] and Scharfetter et al [249] were also limited to one dimension due to the then available computer power. Advances in computer technology enabled two dimensional models with more realistic descriptive equations to be developed. Slotboom's model [245] for a npn bipolar transistor was one of the first two dimensional models used to investigate spreading and surface effects. This type of model allows non-planar devices to be more rigorously investigated. Thus such important

phenomena as current crowding in thyristors can be accounted for by use of a two dimensional model.

Large scale devices such as high power thyristors, GTO's and snubber diodes have significant three-dimensional effects. Carrier spreading and differential heating, significantly influence the performance of large devices. Thus for a rigorous solution a three dimensional model is desired. Present day three dimensional models are predominantly concerned with the analysis of small geometry VLSI devices. Hence, much of the available information on three dimensional modelling is not applicable to high power large scale devices.

A similar situations exists for two dimensional models. There is a sparse amount of information available on the modelling of high power diode reverse recovery. In addition, the published work that is available is based upon performance in simple circuits i.e. resistive and non-inductive. Such work is not applicable to practical GTO circuits that present the snubber diode with an inductive, low resistance environment. Circuit inductance plays a significant part in determining the diode performance as outlined in section 3 and illustrated by comparison between the derivations in sections 4.2.1 and 4.2.2. Therefore in order to produce such a device model some significant software development was required.

4.3.3 **Successive and simultaneous strategies**

In a transient analysis, space discretization and time integration yield the following coupled non linear system [86].

$$F_{\psi}(\psi, \phi_n, \phi_p) = 0 \quad - \quad \text{(E104)}$$

$$F_n(\psi, \phi_n, \phi_p) = 0 \quad - \quad \text{(E105)}$$

$$F_p(\psi, \phi_n, \phi_p) = 0 \quad - \quad \text{(E106)}$$

Here the argument t^m and the superscripts m are omitted for simplicity. A similar system will be obtained at each bias point for a steady state problem.

Hence in each case 3 N non-linear equations have to be solved. In the 2-Dimensional case the number of grid points N is usually between 300 and 4000. Thus solution of the problem is very time intensive, therefore it is important to choose an efficient numerical algorithm to optimize the solution time.

In the simplest case, each differential equation is decoupled and solved successively. Initially the Poisson equation is solved assuming known quasi-Fermi levels. The solution of Ψ is then used to solve the carrier continuity equations. This sequence is then repeated iteratively to produce a set of self consistent values. This method was pioneered by Gummel [67] and a schematic diagram of this procedure is shown in figure 58(a).

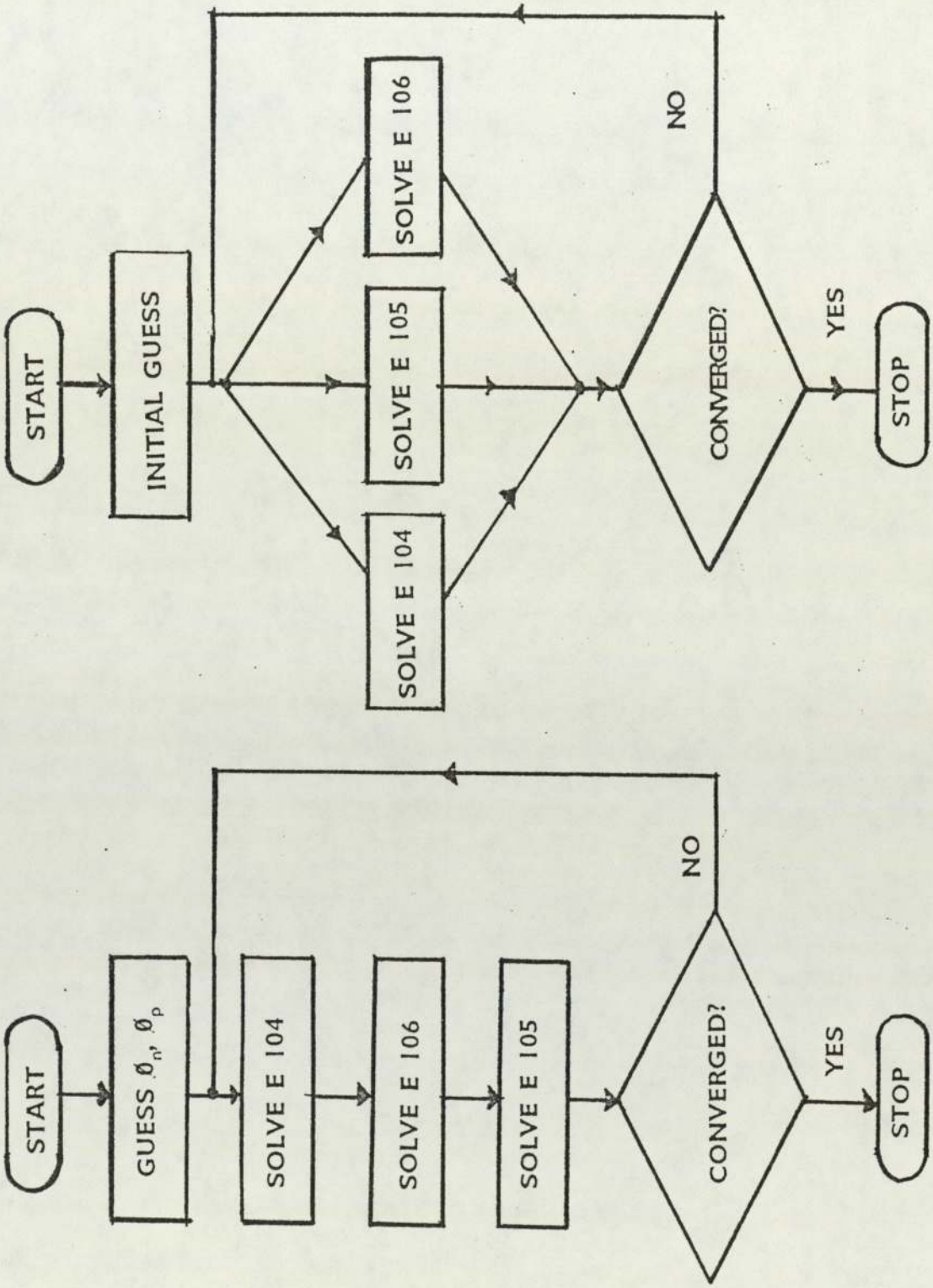
This method has many advantages [110] - not least is its economy of storage space required during the solution of three dimensional structures. It is also known to converge quite well if the coupling between the three equations is weak. Also if the first guess of the quasi-fermi potential of the majority carriers is good enough then the first cycle of the iteration is close to the exact solution.

When using Gummel's algorithm, solution of the three equations is usually achieved by an iterative method since each equation is non-linear. The technique normally used is Newton's method. This method has the advantage of quadratic convergence and thus decreases the solution time. Although simple and robust the Gummel scheme also has some disadvantages. As the three equations become strongly coupled the convergence of the solution becomes slow. Thus for low levels of carrier injections Gummel's method converges well, but as the minority carrier density approaches the majority carrier density this convergence slows down [204, 237] since in this case the carrier continuity equations are linked via the electrostatic potential. In addition simulations involving transients can experience increased coupling due to displacement currents.

In modelling the snap-off of a snubber diode a transient simulation will be

FIGURE 58

(a) Schematic diagram of Gummel Algorithm.
(b) Schematic diagram of simultaneous solution.



required and also high level injection conditions may also prevail in some circumstances. Thus the successive solution method does not appear suitable for diode snap-off simulations. The convergence problem can however, be overcome by solving the equations simultaneously [214] rather than alternatingly. The simultaneous method has the advantage that the mutual coupling between all equations is taken into account by a quadratically converging overall Newton iteration. Figure 58(b) shows a schematic diagram of the simultaneous solution procedures.

Although the simultaneous Newton method has advantages in terms of convergence, for computer implementation it does require a more involved programme structure and an increased available memory (for storage requirements).

Thus comparisons between these two methods [204] not only depend on the device to be modelled, its operating conditions, but also on the algorithms implemented for solving the linearized system of equations [89].

This method has been applied to a one-dimensional system [238]. In this case the linearized system can be solved by Gaussian elimination of LU decomposition. An appropriate ordering of the columns and rows of the Jacobin yields a simple band matrix with mostly seven non-zero diagonals. Thus the implementation of special band solver routines can result in a memory reduction and a decreased solution time [239]. If the bandwidth of the Jacobin matrix is not excessively large this method can also be used on two-dimensional problems [240].

Engl [86] has published a diagram of a five diagonal band matrix as produced in a finite difference evaluations using the decoupled method. Assuming a rectangular grid of N_x and N_y grid lines in the x and y directions, for a direct elimination process, computation times and storage requirements are proportional to $N_v^3 N_x$ and $N_u^2 N_x$ respectively (taking into account the fill in of non zero coefficients within the band width N_y). The threefold increase in size of the Jacobin of the simultaneous scheme produces an increase in the storage

and computation time of a factor of nine compared with one Newton step for each decoupled equation. Because of this, the simultaneous solutions approach requires a large computer resource.

If an irregular grid is used the Jacobin matrix keeps some 'sparseness' but looses the simple band structure. Thus if direct eliminations methods are still to be used the computer programme complexity must be increased. Irregular grids thus require pre-processing of the LU factorization and ordering of the sparse matrix equations [241, 242].

Very often to produce a solution on a computer with limited available memory, an additional internal iteration for the solution of the large systems of linearized equations is required. This is especially true in the case of diode snap-off modelling were a 2 or more desirably a 3 dimensional structure must be modelled. There are a number of such algorithms that have been successfully applied to linear equations. These are, Stones strongly implicit procedure (SIP) [243, 244]; the successive line over relaxation method (SLOR), [243, 245,246] or the incomplete Cholesky decomposition and conjugate gradient (ICCG) method [114, 116, 122, 123, 194, 247, 263].

4.3.4 **Discretization methods**

Each numerical method relies on approximating the solution domain with a number of 'segments'. There are two major [175] methods by which the solution domain may be split into a number of discrete segments, these are the finite difference method and the finite element method. Most of the early device simulations such as those of Gummel, [67], De Mari [224, 248], and Scharfetter and Gummel [249] used the finite difference method. More recent simulations have tended to use the finite element method.

The primary difference between the finite element method and other solution strategies is that the FEM approximation is confined to relatively small sub-domains. Thus an admissible function satisfying the boundary conditions for the entire domain is not required. Admissible functions are defined over element

domains with a simple geometry. The finite difference method is based on differential formulations while the finite element method is based on integral formulations.

Although the finite element method usually requires the use of less nodes than the finite difference method a matrix re-ordering algorithm is normally required to cope with the complex matrix structure that occurs with the FEM. This disadvantage is more than compensated for by the variable mesh size that the FEM can use. Thus the mesh can be graded to provide a fine mesh in regions of rapid change of variable. This localised mesh refinement is generally easier to implement than in finite difference schemes. The finite element method also allows high order approximations to be readily produced. The main disadvantage of the finite element method compared to the finite difference method is the increased programming complexity and greater density of matrix equations. It was considered however, that the advantages of the FEM out-weighed its disadvantages and thus I decided to investigate if this method was suitable for modelling diode snap-off.

4.3.5 **The finite element method (FEM)**

4.3.5.1 **An introduction to FEM**

The earliest finite element models were based on variational principles [71]. Such variational models involve finding a nodal parameter that yields either a maximum or minimum value (i.e. a stationary value) of a specific integral relation known as a functional. Variational methods are closely associated with 'physical intuition' and therefore in many cases it is possible to assign a physical meaning to the integral being extremised. Thus in structural applications (from which the FEM originated) the integral may represent the potential energy in a steel girder. For non-structural problems the weighted residual technique has become important. This method commences with a governing differential equation but avoids making an equivalent variational statement. Instead an approximate solution is substituted into the differential equation. This initial guess will be subject to error. The difference between the real solution and

the approximate solution is called the residual error term E_r. This residual error term cannot be forced to zero, however, it is possible to set the weighted integral of the residual to vanish. Thus:

$$0 = \int E_r.W_f \, dv \qquad - \qquad (E107)$$

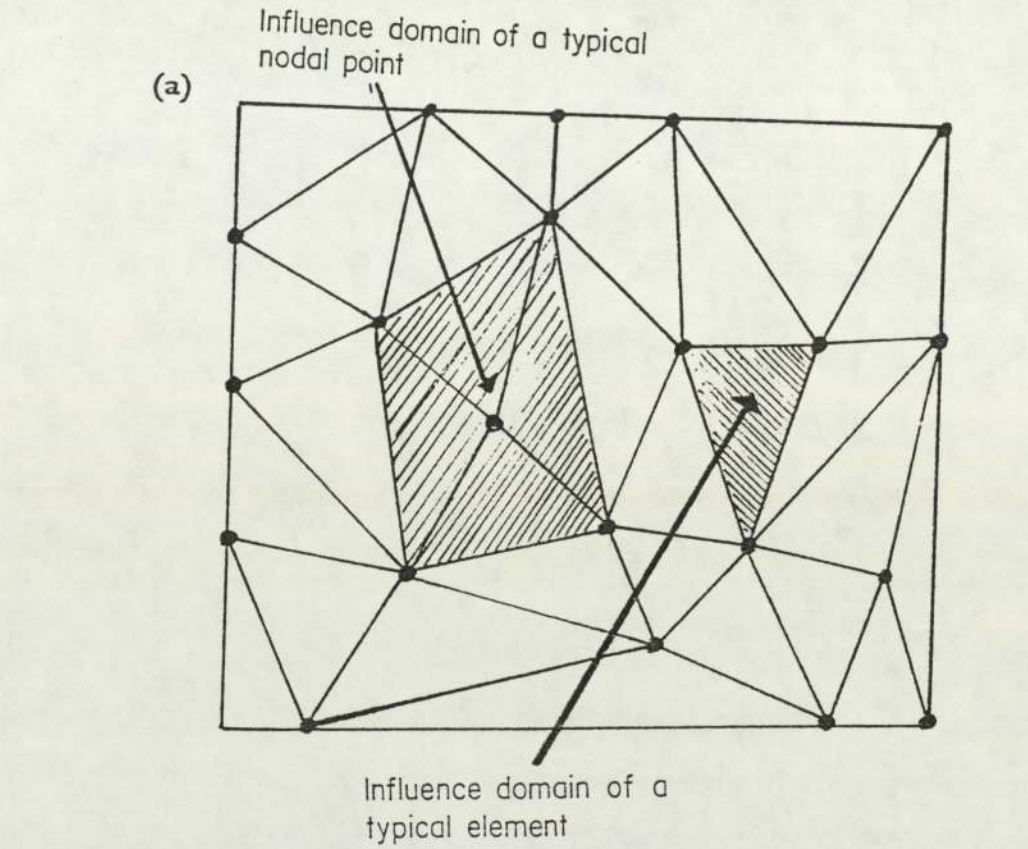
Hence the above equation describes the product of the error residual and a weighted function when integrated over the solution domain as equal to zero. This gives a method of expressing an approximate solution as an integral for use in finite element solutions.

In the finite element method the solution domain is divided into discrete sub-regions or finite elements by means of a mesh structure. This mesh structure is constrained by defined boundaries and constructed using points and lines. These nodal points or nodes can be situated along, or inside, the subdividing mesh lines, but they are usually located at intersecting mesh lines. Thus if the modelling of a curved boundary is required some geometric approximation will be necessary. This fact should however not be viewed as a disadvantage but as an advantage of the finite element method. This is because complex shapes can be modelled by adjusting the size of the element at the defined boundary or by use of a non linear interpolation function between nodes i.e. use of a 'curved' element. In addition elements situated away from the boundary may have a much larger area and thus the number of nodes in a finite element model is usually less than in a finite difference model with the equivalent boundary refinement.

Identifying integer numbers are assigned to each node point and each element is also assigned a unique integer. These integers are known as node numbers and element numbers respectively. Each number is sequential in that they begin at one and extend to a maximum value. Every node within the mesh is assigned a degree of freedom. These are parameters chosen by the modeller to represent the parameters of interest and are therefore initially unknown. Thus the nodal parameters could be electrical potential, hole density and electron density. A typical node will usually influence more than one element.

FIGURE 59

(a) **Typical FEM node and element.**
(b) **Diagram of SPICE diode Model.**



Such domains of influence are shown in figure 59(a) for an arbitrarily chosen node and an arbitrary element. Each element will have a number of nodes associated with it. The degree of freedom per element is therefore defined as the product of the number of nodes in the element and the degrees of freedom of each node.

By a similar argument the number of degrees of freedom in the system is the product of the number of nodes and the degrees of freedom in each node. Each node point must be specified in terms of spatial co-ordinates. It is common to associate an integer code with each nodal point. By means of this code, which nodal parameters have boundary constraints can be identified. During element construction it is important that a list of global node numbers are attached to each element. Which node numbers are associated with which element defines how each element is connected together and thus ultimately the topology of the mesh. This list of nodes is usually present within a computer programme in the form of a data array. This array is then used to establish the matrices necessary for the problem solution. In general such matrices are formed by substituting interpolation functions in the governing integral equations. For historical reasons (since FEM techniques originated in structural analysis) the resulting matrices are known as the stiffness matrix and the load vector.

Once the element equations have been established the contribution of each element is combined to produce system equations. In many cases, symmetric system equations will result and once constructed, boundary constraints are then applied prior to solution of the unknown nodal values. Typical nodal boundary constraints are:

a) Defining explicit values of 'unknown' nodal parameters at the boundary.

b) Defining constraint equations that are linear combinations of the nodal quantities.

Once solutions have been obtained for the parameters at each nodal point some post processing techniques are then required to present the solution in a usable form. Thus the nodal values of electrostatic potential will need to be integrated over the problem domain to provided the total voltage drop. Similarly charge movement over a cross sectional area must be added to calculate the current flow.

One difficulty with the finite element method is that of data generation; for a problem domain with complex geometry many small elements and thus many nodal points are required. To manually input individual co-ordinates for each node would not only be time consuming but also prone to error. To minimise such data preparation time and probability of error there are schemes that have been devised to automatically generate a mesh [73]. This operation is sometimes known as preprocessing.

The approximate solution of a Poisson equation problem by means of finite element methods is therefore composed of five stages.

(i) The problem region is divided into a mesh, this partitions the region into smaller units - in this case triangles.

(ii) The next step is to assign nodes to each element and then choose an interpolation function to represent the variation of the field variable over the element. Polynomials are usually selected for the field variable since these are easy to differentiate and integrate. The sources and imposed boundary values of the problem are also defined.

(iii) Once the finite element model is established the matrix equation and the properties of individual elements are determined. This may be achieved using one of four methods, the energy balance method, the variational method the weighted residual method and the direct method.

(iv) The global matrix is now assembled by matrix transformation of all of the elements and the imposition of the boundary equations.

(v) The assembly process gives a set of simultaneous equations that can be solved to obtain the unknown nodal values of the field variable.

4.3.5.2 **Discretization of the problem**

The finite element method has three sources of approximation. These are: the domain definition, the problem discretization and the solution algorithms. The geometric definition of the domain requires the establishment of a global coordinate axes from which the nodal co-ordinates can be defined. Except for the boundary conditions the governing equations are valid over both the global domain and any portion of that domain. This allows an approximation of the domain to be achieved by assembly of interconnected finite size domains (elements). This approximate discrete domain should then represent the actual continuous domain. The smaller the elements are, the finer the mesh will be and therefore the closer the approximate domain will be to the actual one. However, a fine mesh results in a large number of equations to be solved which increases solution time and may even reduce accuracy. Thus the modeller must seek a trade off to achieve the most efficient element size and type. Such considerations are normally dealt with by using automatic mesh generation techniques [73, 79, 81, 82, 83, 221].

It should be noted that within the finite element strategy there are two types of element; the finite element and the master element. Finite elements are those which when assembled together form the discretized version of the actual continuous domain. They are straight sided (although curved elements may prove useful at boundaries). The physical approximations are controlled by the number of nodes (exterior as well as interior) utilized in defining trial functions (shape functions) for the state variable. Master elements are used in place of finite elements for the purpose of computations in the element

domain. The master element will use global co-ordinates while the finite element will use local co-ordinates.

Choosing a global axes for the entire system and special co-ordinate axes for the finite element eases the construction of trial functions and simplifies integration within the elements. Since the elements will be assembled in the global frame, the necessary co-ordinate transformations will introduce additional computational steps. The transformation of point co-ordinates from a finite element to a master element and vice versa involves mapping; one being the image of the other. Transformation from the element co-ordinate system to the global co-ordinate system involves only rotations. By choosing both the local co-ordinates (x, y, z) and global co-ordinates (X, Y, Z) to be orthogonal, the rotational matrix is also orthogonal i.e. $R^T = R^{-1}$, which simplifies the transformation.

After establishing co-ordinate axes, the element equations are first computed in a master element $\hat{\Omega}_e$. They are then transformed into finite elements Ω_e and then into the global system. Thus:

$$\begin{array}{lcllll} \hat{P}_e & = & \hat{k}_e & \hat{U}_e & \text{in} & \hat{\Omega}_e \\ T\uparrow & & \downarrow & T^{-1} & & \\ P_e & = & k_e & U_e & \text{in} & \Omega_e \\ R_m\uparrow & & \downarrow & R^{-1} \text{ or } R^T & & \\ P_e & = & k_e & U_e & \text{in} & \Omega \end{array}$$

After the solution of the simultaneous equations, the inverse transformation takes place in order to compute the physical entities (current and voltage) in the element domain.

4.3.5.3 **Formulation of the problem**

The physical problem can be either formulated by a set of differential

equations.

$$L.u = f \qquad \text{-(E108)}$$

with boundary conditions, or by an integral equation (a functional),

$$\pi = \int_{\Omega} G\,(x, y, z, t)\, d\,\Omega + \int_{\cap} g\,(x, y, z, t)\, d\cap \qquad \text{-(E109)}$$

subject to a stationary requirement (maximum, minimum or saddle). Equation (E108) is referred to as the operational form of the physical problem while equation (E109) is referred to as the variational form of the problem. Solution of either equations (inversion of L or minimization of π) yields the same results.

In the two dimensional Poisson equation problem equations (E108) and (E109) will take the form.

$$\nabla^2 u - c = 0 \qquad \text{-(E110)}$$

and $$\pi = \int_{A} \{1/2\ (u)^2 + c\ u\}\ dA \qquad \text{-(E111)}$$

Generally if equation (E109) exists then the associated Euler-Lagrange differential equation (equation (E108) can be found. Obtaining equation (E108) from equation (E109) is often referred to as the Euler-Lagrange minimization procedure.

4.3.5.4 **Assignment of approximating functions**

After the state variables and the local co-ordinate system have been chosen, the function can then be approximated. There is a 'physical' approximation of the state variable and a geometrical approximation of the element shape. By choosing elements with straight sides the element can be defined accurately and therefore geometric approximation is unnecessary. The physical approximation can be achieved by a linear function or a higher order function such as a quadratic or cubic equation. For example a function to describe the variation of potential over the element can be represented by a polynomial. This function is usually known as the shape function. The order of the equation is

consistent with the number of nodes on each side. Thus a linear polynomial requires two nodes per side and a quadratic three nodes per side. As the order of polynomial is increased, so the solution becomes more accurate. However, the polynomial equations become more complex and thus a trade-off between accuracy and ease of computation must be sought.

The essence of the finite element method lies in first approximating the potential within each element in a standardised fashion and thereafter interrelating the potential distributions in the various elements so as to constrain the potential to be continuous across interelement boundaries. In a triangular element the potential may be approximated by an expression such as:

$$U = \ddot{a} + bx + cy \qquad \text{-(E112)}$$

The coefficients a,b,c may be found from the three independent simultaneous equations which are obtained by requiring the potential to assume vertex values U_1, U_2, U_3 at three vertices. Thus:

$$\begin{bmatrix} U_1 \\ U_2 \\ U_3 \end{bmatrix} = \begin{bmatrix} 1 & x_1 & y_1 \\ 1 & x_2 & y_2 \\ 1 & x_3 & y_3 \end{bmatrix} \cdot \begin{bmatrix} \ddot{a} \\ b \\ c \end{bmatrix} \qquad \text{-(E113)}$$

The determinant of the coefficient matrix is equal to twice the triangle area; the coefficients can be determined and substitution into the result yields.

$$U = [1 \; x \; y] \cdot \begin{bmatrix} 1 & x_1 & y_1 \\ 1 & x_2 & y_2 \\ 1 & x_3 & y_3 \end{bmatrix}^{-1} \cdot \begin{bmatrix} U_1 \\ U_2 \\ U_3 \end{bmatrix} \qquad \text{-(E114)}$$

which may be rewritten as

$$U = \sum_{i=1}^{3} U_i \, \alpha_i \, (x, y) \qquad \text{-(E115)}$$

where $\alpha_1 = \frac{1}{2.A_t} \{(x_2\, y_3 - x_3\, y_2) + (y_2 - y_3)\, x + (x_3 - x_2)\, y\}$ -(E116)

α_i is a linear function of position only and the remaining two functions are obtained by cyclic interchange of subscripts. 'A_t' represents the surface area of the triangle. The energy associated with a single triangular element may now be determined by integrating over the element. The potential gradient is

$$\nabla U = \sum_{i=1}^{3} U_i \nabla \alpha_i \qquad \text{-(E117)}$$

and the element energy is

$$W^{(e)} = \tfrac{1}{2} \int |\nabla U|^2 \, dS_1 \qquad \text{-(E118)}$$

or $$W^{(e)} = \tfrac{1}{2} \sum_{i=1}^{3} \sum_{j=1}^{3} U_i \int \nabla \alpha_i \,.\, \nabla \alpha_j \, dS_1 \, U_j \qquad \text{-(E119)}$$

Defining matrix elements as:

$$S^{(e)}_{ij} = \int \nabla \alpha_i \,.\, \nabla \alpha_j \, dS_1 \qquad \text{-(E120)}$$

Equation (E119) then becomes

$$W_{(e)} = \tfrac{1}{2} U^T S^{(e)} U$$

written as the matrix quadratic form for any triangle the matrix S is readily evaluated by

$$S^{(e)}_{12} = \frac{1}{4.A_t} \{(y_2-y_3)(y_3-y_1)+(x_3-x_2)(x_1-x_3)\} \qquad \text{-(E121)}$$

4.3.5.5 **Assembly of the element equations**

The total energy associated with an assemblage of many elements is, in general, the sum of all the individual energies. Thus:

$$W_o = \sum_{alle} W^{(e)} \qquad \text{-(E122)}$$

Three potential values are associated with each triangle. Thus all possible states of a pair of elements would be described by a column vector containing six vertex potentials.

$$U^T_{dis} = [U_1\ U_2\ U_3\ U_4\ U_5\ U_6]_{dis} \qquad \text{-(E123)}$$

The total energy of the pair of elements is then

$$W_o = \tfrac{1}{2}\ U^T_{dis}\ S_{dis}\ U_{dis} \qquad \text{-(E124)}$$

Where S_{dis} is the Dirichlet matrix of the disjoint pair of elements.

$$S_{dis} = \begin{bmatrix} S^{(1)} & 0 \\ 0 & S^{(2)} \end{bmatrix} \qquad \text{-(E125)}$$

Since each node may have only one potential, two triangular elements once joined only have four nodes and may be viewed as an element. Thus a rectangular matrix Ö is used to relate the potentials of disjoint element to the potentials of the conjoint set of elements.

$$\text{Hence } U_{dis} = \ddot{O}\ U_{con} \qquad \text{-(E126)}$$

Substituting into (E124) yields

$$W_o = \tfrac{1}{2}\ U^T_{con}\ S_o\ U_{con} \qquad \text{-(E127)}$$

where $S_o = \ddot{O}^T\ S_{dis}\ \ddot{O}$

and represents the assembled coefficient matrix of the connected problem.

4.3.5.6 **The solution of the simultaneous equations**

The finite element method yields a large set of simultaneous equations. Such equations can be written in matrix form as:-

$$\begin{bmatrix} a_{11} & a_{12} & \cdots\cdots & a_{1n} \\ a_{21} & a_{22} & & a_{2n} \\ a_{il} & : & & a_{in} \\ a_{n1} & : & & a_{nn} \end{bmatrix} \cdot \begin{bmatrix} U_1 \\ U_2 \\ U_i \\ U_n \end{bmatrix} = \begin{bmatrix} V_1 \\ V_2 \\ V_i \\ V_n \end{bmatrix} \qquad \text{-(E128)}$$

Coefficient array Unknowns Source array

The coefficient terms 'a' are determined from algebraic expressions associated with unknown terms U and source terms V (formed from the boundary conditions). The coefficient matrix is termed 'sparse' because of the few non-zero coefficients. It is also symmetric about the leading diagonal. There are a number of methods for solving sparse symmetrical matrices, but they may be classified as either direct or iterative. There are two direct methods for solving the matrix equation. The first is achieved by transforming the matrix equation [180] such that $A.x = B$ becomes $x = B.A^{-1}$ (see section 4.3.5.4). The second method is the Gaussian elimination scheme. In this method all the unknown values of x are eliminated [117] until all the coefficients below the leading diagonal are zero. The elimination of one variable at a time until only one equation with one unknown is left, is known as the forward elimination phase. When this has been determined the remainder are found by taking the equations in reverse order, each time substituting the already known values. This phase is called back substitution. The technique is applied to the coefficient matrix (usually positive definite in type), which can be written as

$$S_o = L.L^T \qquad \text{-(E129)}$$

where L is the lower triangular matrix and L^T is the upper triangular transpose matrix. If the equation to be solved is

$$S_o x = y \qquad \text{-(E130)}$$

then S_o is decomposed to $S_o = LL^T$ and rewritten as a pair of equations

$$Lz = y \qquad \text{-(E131)}$$

$$L^T x = z \qquad \text{-(E132)}$$

$$\text{Set } L_{11} = \sqrt{S_{11}} \qquad \text{-(E133)}$$

and then compute the off-diagonal element in each column k in each row using.

$$L_{ik} = (S_i - \sum_{j=1}^{i-1} L_{ij} L_{kj}) / L_{kk} \qquad \text{-(E134)}$$

and the diagonal element by

$$L_{ii} = (S_{ii} - \sum_{j=1}^{i-1} L_{ij}^2)^{1/2} \qquad \text{-(E135)}$$

until all of L has been calculated. Since y is known, z and thus x may be calculated. Both approaches are suitable for computer solution, although the inversion process tends to take longer than the Gaussian elimination because of the greater number of arithmetic operations required.

Iterative methods [49, 212, 215, 217, 135], of which Gauss-Seidel iteration, Successive over-relaxation and Line iteration are examples can also be used for solving large sparse symmetrical matrices. Such methods have the advantage that only the non-zero coefficients are required to be stored and thus large matricies can be solved with a relatively small computer memory. The disadvantage of such a method is that a large number of iterations may be required to achieve an accurate solution. The number of iterations required is determined by the degree of accuracy needed, the method of iteration chosen, the intitial starting values and the conditioning and linearity of the equations

chosen. A disadvantage of many iterative methods is their linear convergence. This increases the solution time or decreases the solution accuracy depending on what trade off the modeller makes.

4.4 Device modelling conclusions

Analysis of the simple circuit theory of diode reverse recovery in an inductive circuit has shown that the present day practice of expressing the snappiness of a diode as the ratio of two time periods is an inadequate measure for diodes under high stress conditions. It is suggested that manufacturers adopt the softness factor Ç as a measure of the abruptness of diode recovery. This factor Ç is equal to the ratio of peak reverse recovery voltage to the final recovery voltage.

The use of an equivalent circuit model to describe the reverse recovery of the diode has shown that the current chop-off phenomena can be explained by the variation of diode capacitance during switching. In this model the type of recovery a diode demonstrates is dependent on the acceleration of the depletion layer movement. Further studies indicate that the recovery characteristics of the diode are determined by the minority carrier lifetime, the transit time, the forward current and the external circuit parameters. In addition the fabrication method determines carrier lifetime and thus influences diode performance. These findings support the conclusions drawn from the experimental investigations. During these investigations, the possible effects of an area term influencing the variation of capacitance (i.e. $dC/dt = (\varepsilon/W).dA/dt$) or inductive effects within the diode [130, 145, 146] were not considered.

Although promising as a technique for device analysis it was found that the finite element modelling technique when applied to the device/circuit simulation problem was far more complex to apply than an equivalent circuit model. Consequently it was decided to simulate the device/circuit interactions in a GTO inverter using the well known SPICE computer programme.

5. DEVICE/CIRCUIT SIMULATION

5.1 An overview of device/circuit modelling

The initial experimental investigations had indicated that a diode snap-off phenomenon could exist in soft recovery diodes when operated under high stress conditions. Further experimental investigations and a literature search identified circuit conditions and diode parameters that are important in producing a snap-off voltage spike. The use of analytical models both provided an insight into the snap-off mechanism and also confirmed the importance of the experimentally identified parameters. An investigation was made into the possibility of modelling diode snap-off using the finite element method. [191, 200, 202, 149, 137, 205]. However this method proved difficult to apply to the 3D time dependent device/circuit problem [68, 104, 103, 105, 115, 124, 152]. Although benefits would have been gained in pursuing this method to analyse the snap-off mechanism, it became apparent that simpler methods could be used to provide a device/circuit transient simulation [37, 101, 181] within the time scale of this project. Thus the method chosen to produce such simulations was by use of the well known SPICE circuit analysis computer programme [222, 181].

5.2 Implementation of the preferred solution technique

5.2.1 The SPICE programme

SPICE which stands for Simulations Programme with Integrated Circuit Emphasis, is a general purpose circuit simulation programme developed at the University of California at Berkeley for non linear dc, non linear transient and linear ac analysis. SPICE has built in models for circuit components from which electrical circuits can be constructed [223]. Thus circuits can contain resistors, capacitors, inductors, mutual inductors, independent voltage and current sources, four types of dependent sources and transmission lines. In addition four of the most common semiconductors devices are also included, these are: diodes, BJTs, JFETs and MOSFETs. The models for these semiconductor

devices are already part of the SPICE programme and therefore the user has just to specify the model parameter values. The model for the BJT is based upon the Gummel-Poon integral charge representation. However if the Gummel-Poon parameters are not specified the model reduces to the simpler Ebers-Moll model. The description of semiconductor devices given in section 2.3 is structured in a progressive manner; building up complex devices from simple PN junctions. This philosophy is consistent with the SPICE strategy of producing complex devices from a combination of simple devices. As stated in section 2.3.2, the thyristor can be represented by a combination of two bipolar transistors. Thus the performance of thyristors can be modelled on SPICE. In the transistor model, charge storage effects ohmic resistors and current-dependent output conductance can be included. The programme has two diode models one for the junction diode and one for the Schottky barrier diode. The MOSFET model includes effects such as channel-length modulation, subthreshold conductions, scattering limited velocity saturation, small-size effects and charge controlled capacitances. This latter effect is of relevance to snubber diode snap-off.

SPICE is node voltage oriented, so any node voltage can be requested. Element currents flowing through independent voltage sources can also be requested. This particular study (snubber diodes in GTO inverter circuits) requires the transient analysis portion of the SPICE programme. In this mode, SPICE computes the transient output variables as a function of time over a user specified time interval.

The initial conditions are automatically determined by a dc analysis. Sources such as power supplies that are not time dependent are set to their dc value. The transient solution is obtained by an iterative process. The calculation is stopped when the following conditions apply:

a) The nonlinear branch currents converge to within a tolerance of 0.1% or 10^{-12} A, whichever is larger.

b) The node voltage converge to within a tolerance of 0.1% or 10^{-6} V, whichever is larger.

The SPICE algorithm is generally very reliable, but will in some circumstances fail to converge to a solution. Should this situation occur the programme prints the node voltages at the last iteration and terminates the job. Therefore there is no guarantee that such printed node values will be close to the solution. A dc analysis convergence failure is usually due to a circuit specifying error, i.e. incorrect circuit connections, element values or nodal parameter values.

Positive feedback and regenerative switching circuits will have difficulty converging in the dc analysis mode unless the OFF option is used for some of the devices in the feedback path or the NODESET card is used to force the circuit to coverage.

When failure to coverage occurs a check for errors in the data input should be initiated. This can be achieved using the LISR and NODE options in the OPTIONS card. If the input data is correct, then failure to converge may be caused in a transient analysis by the internal timestep being too small. This is because SPICE starts to use the time step specified in the TRAN card and if convergence is not achieved within internal specified limits, the programme automatically decreases the internal time step. The time step is divided by 8 each time, until a lower limit is exceeded. There are however a number of actions that can aid convergence.

By using the UIC option without specifying any IC (equivalent to setting to zero) and then applying the power supply only, the circuit will then reach the steady state gradually and the time dependent input sources can then be applied. Another aid to convergence is to change the method of integration from TRAPEZOIDAL to GEAR by using the METHOD parameter in the OPTIONS card. A third method is to alter the parameters LVLTIM, TRTOL and ITL4 on the OPTIONS card. The truncation error time-step control is the default method for deciding when to double the internal time step for easy convergence and when to divide the internal time step by eight if the

convergence is difficult. As TRTOL is increased less importance is given to the truncation error and thus the possibility of dividing the time step by eight recedes. If LVLTIM is changed from 2 to 1 then a change in the time step is dependent only on the number of iterations needed to reach convergence. In this case TRTOL has no more influence and ITL4 must be modified. As ITL4 is increased so the ease of convergence also increases.

The circuit to be analysed by SPICE is described by a set of element cards (which define the circuit topology and element values) and a set of control cards which define the model parameters and the run controls. Each element in the circuit is specified by an element card that contains the element name, the circuit nodes to which the element is connected and the values of the parameters that determine the electrical characteristics of the element. The first letter of the element name specifies the element type. Thus:

R	=	Resistor
C	=	Capacitor
L	=	Inductor
K	=	Mutual Inductor
T	=	Transmission line (lossless)
V	=	Independent voltage source
I	=	Independent current source
G	=	(Non) linear voltage - controlled current source
E	=	(Non) linear voltage - controlled voltage source
F	=	(Non) linear current - controlled current source
H	=	(Non) linear current - controlled voltage source
Q	=	Bipolar junction transistor
D	=	Diode
J	=	JFET
M	=	MOSFET
X	=	Subcircuit

The R and T elements are constants. The elements C,L,G,E,F,H can be expressed as nonlinear polynomials. The model parameters in the elements

Q,D,J and M define their functions, while the sub-circuit is user defined. The independent sources may have their characteristics based on the following functions.

a.	Constants	:	ac or dc constant values
b.	Pulse	:	defined with high and low values rise and fall times, pulse width and repetition rate.
c.	Sinusoidal	:	exponentially decaying sinusoidal.
d.	Exp	:	sum of two exponential waveforms
e.	Piecewise linear	:	tabular function of time
f.	SFFM	:	single frequency, frequency modulated waveform.

The reference (earth) node must be numbered zero while the rest of the nodes must be non-negative integers. The circuit cannot contain a loop of voltage sources and/or inductors and cannot have a pathway consisting of current sources and capacitors. Each node must have a dc path to ground. Every node must have at least two connections.

A subcircuit consisting of SPICE elements can be defined and then used as a single element. Thus two BJTs could be combined to create a thyristor model. The subcircuit is defined in the input deck by a group of element cards. The SPICE programme then automatically inserts the elements wherever the subcircuit is referenced [223].

5.2.2 **Modelling GTO strings in megawatt inverters**

5.2.2.1 **Introduction**

Although dramatic improvements in the power handling capability of large GTO thyristors has taken place over recent years there is still a need to connect devices in series to satisfy the need for high voltage systems. A circuit analysis computer program was therefore used to simulate the behaviour of GTO strings in megawatt inverters [46]. This was based on the SPICE circuit

analysis programme and was implemented by J K Chester. By studying the switching behaviour of GTO's and snubber diodes in synthetic test circuits a wealth of experimental data was obtained. Models simulating the observed behaviour were then incorporated into the SPICE based circuit analysis computer programme and used to study device/circuit interactions and their influence on such characteristics as switching loses, etc. By assembling strings of modular switching elements the effects of variations in such things as device parameters and drive conditions could be assessed. A complete inverter arm can then be assembled from such string modules, to enable the investigation of efficiency and component ratings.

The turn-off capability of the GTO's and the spread in device parameters between them were obviously factors to be considered. However, one less obvious factor that was considered was the problem introduced at turn-on due to the polarised snubber arrangement required by the GTO. Because of the spread in device characteristics and their gate drive tolerances the GTO fired last has significant current flow into its snubber capacitor via its snubber diode. Such a GTO must then reverse the diode current to enable the GTO anode voltage to collapse and the GTO to turn-on. This results in the GTO drawing current at high voltage until all of the diode stored charge is extracted. During this period then a severe inrush duty results, since the inrush current is not circuit limited. This problem can be reduced by close selections of GTO characteristics and gate drives. Such a solution is costly in that either improved manufacturing tolerances are required or increased time must be devoted to testing. Another drawback is that a device cannot be replaced 'off the shelf' but must be closely matched to other devices in the circuit. A circuit measure that could be employed to alleviate this problem would be the introduction of both linear and saturable reactors to reduce the initial dI/dt during the first few microseconds of turn-on current inrush.

Another way would be to reduce the stored charge in the snubber diode. However, this solution may also have penalties in terms of reduced dV/dt protection and the increased probability of a destructive voltage snap-off event. Examples of the modelling of this particular problem are given below.

5.2.2.2 **GTO turn-on and snubber diode models used in SPICE**

The GTO can be described by a two stage turn-on. During the first stage when the voltage across the GTO is high, the current will only be a function of the gate drive current and will be anode voltage, independent. During the second stage the GTO current becomes limited by the external circuit and is dependent on the anode voltage. The point at which the transition between these two stages occurs is governed by how the voltage across the GTO collapses. Theoretical descriptions of turn-on in the GTO are complex since the physical processes involved are essentially three dimensional in nature. Therefore a semi empirical approach was used to construct a device model using experimental data for a specific device under known conditions and exhibiting the two stage behaviour described above. In each example the anode voltage collapse was represented by a piecewise linear voltage source and a gate current generating circuit was used to drive the model.

The type of duty a snubber diode experiences when a series connected GTO is fired late consists of a small transient forward current loop followed by a reverse recovery current waveform where the commutating dI/dt increases rapidly with time i.e. $dI^2/d^2t \neq 0$ and is +ve.

The dc forward characteristic of the ideal diode is modelled by using a non-linear current source. Thus

$$I_d = I_o.(\exp\ (q.V_d/k.T)-1) + V_d.GMIN \qquad \text{-(E136)}$$

for values of $V_d \geq -\ 5.n.k.T/q$ where $1 \leq n \leq 2$

A schematic representation of this diode model is shown in figure 59(b).

To aid convergence a small conductance GMIN is added by SPICE in parallel with every PN junction. The value of this parameter can be adjusted via the OPTIONS card. The user cannot set GMIN to zero and the default value is

10^{-12} mho.

Similarly the dc reverse characteristic of the ideal diode is modelled by using the non-linear current source shown is figure 59(b). In the reverse bias case:

$$I_d = f(V_d) \qquad \text{-(E137)}$$

Therefore equation (E136) is used between the limits : $-5.n.k.T/q \geq V_d \geq 0$ and when $V_d < -5.n.k.T/q$, then:

$$I_d = -I_o + V_d.GMIN \qquad \text{-(E138)}$$

The secondary effects in diodes i.e. small forward bias, large forward bias, large reverse bias and stored charge can be accounted for by the SPICE model. The most important of these from the point of view of modelling snubber diodes and the snap-off phenomenon is the stored charge effect.

In the ideal diode model the charge on one side of the junction can be expressed in the form.

$$Q_d = A_j.q.x_p.N_A = A_j.q.x_n.N_D \qquad \text{-(E139)}$$

In addition

$$\phi_o - V_d = (q/2.\varepsilon).(N_A.x_p^2 + N_D.x_n^2) \qquad \text{-(E140)}$$

A change in V_d requires a change in both x_p and x_n. A change in $-x_p$ and x_n implies a change in the charge associated with the charge layer. Thus to balance any change in the junction voltage charge flows into or is extracted from, the space charge region.

The capacitance associated with a change of dV_d is then:

$$C_d = \frac{dQ_d}{dV_d} \qquad \text{-(E141)}$$

If $N_A >> N_D$ then x_n may be written

$$x_n = \sqrt{\frac{2.\varepsilon_s.(\phi_o - V_d)}{q.N_D}} \qquad \text{-(E142)}$$

Combining equations (E139) and (E142) yields the following expressions.

$$Q_d = \sqrt{A_j.2.\varepsilon_s.q.N_D} \;.\; \sqrt{\phi_o - V_d} \qquad \text{-(E143)}$$

Hence

$$C_d = \frac{dQ_d}{dV_d} = \frac{A_j}{2} \;.\; \frac{\sqrt{2.\varepsilon_s.q.N_D}}{\sqrt{\phi_o - V_d}} \qquad \text{-(E144)}$$

This may be rewritten in the following forms

$$C_d = C_{do}.\{1 - (V_d / \phi_o)\}^{-½} \qquad \text{-(E145)}$$

$$\text{and } C_d = \frac{\varepsilon_s.A_j}{x_n} \qquad \text{-(E146)}$$

Equation (E145) shows that the depletion capacitance is related to the applied bias, the equilibrium capacitance and the built in voltage ϕ_o.

Equation (E146) demonstrates that the capacitance may be calculated by the same expression as a parallel plate capacitor of area A_j and spacing x_n. To obtain the space charge Q_d it is necessary to integrate the space charge capacitance with respect to voltage V_j.

$$\text{hence: } Q_d = \int_o^{Vd} C_d \, dV_d = 2.\phi_o.C_{do}.\{1 - (V_d/\phi_o)\}^{-½} \qquad \text{-(E147)}$$

It can be seen from the above equation that as the value of the V_d/Q_o tends to unity then C_d becomes infinite and Q_d tends to zero.

These basic relationships accounting for the charge storage effect are implemented in the SPICE large signal diode model.

Thus for $V_p < FC \cdot \phi_o$

$$Q_d = \tau.I_d + C_o \cdot \int_o^{Vd} \{1 - (V_d/\phi_o)\}^{-½} \qquad \text{-(E148)}$$

and for $V_d \geq FC \cdot \phi_o$

$$Q_d = \tau.I_d + C_{do}.F_1 + (C_{do}/F_2) \cdot \int_{FC.\phi o}^{Vd} (F_3 + \frac{mV_d}{\phi_o}) \, dV \qquad \text{-(E149)}$$

Alternatively the diode capacitance for $V_d < FC \cdot \phi_o$ may be defined as:

$$C_d = \frac{dQ_d}{dV_d} = \tau \cdot \frac{dI_d}{dV_d} + C_{do}. \{1 - (V_d/\phi_o)\}^{-m} \qquad \text{-(E150)}$$

and for $V_d > FC \cdot \phi_o$

$$C_d = \frac{dQ_d}{dV_d} = \tau \cdot \frac{dI_d}{dV_d} + C_{do} \{1 - (mV_d/\phi_o)\}$$

where $F_1 = \frac{\phi_o}{1-m} [1-(1 - FC)^{1-m}]$

$F_2 = (1 - FC)^{1+m}$

$F_3 = 1 - FC. (1+m)$

From these equations it can be seen that the total charge storage is composed of two separate charge storage mechanisms.

Firstly the charge stored due to the injected minority carrier is accounted for by the exponential expression in equation (E136) via equations (E148) and (E149). In this case I_o is the saturation current, n is the emission coefficient (n=1 for the ideal diode) and τ is the carrier lifetime.

Secondly the space charge Q_d is modelled by the parameter C_o the zero bias or equilibrium junction capacitance ie $V_d = 0$, 'm' the junction grading coefficient, 'ϕ_o' the built voltage and 'FC' the forward bias junction capacitance coefficient. Input values for ϕ_o range from 0.2 volts to about 1.0 Volt. The value of m is 0.5 for an abrupt junction and 0.33 for linearly graded junctions. The parameter FC chooses the calculation method during forward bias. In the default condition FC is equal to 0.5 thus when V_d is greater or equal to the product of FC and ϕ_o SPICE then approximates C_d by a linear extrapolation technique.

5.2.2.3 **Diode snap-off model**

The standard SPICE diode model described in the previous section produces good results under low stress conditions. Thus when modelling series strings of diodes, the diode which recovers last, is exposed to a low stress duty and therefore the above model can be used. Recovery under high stress conditions (in which diode snap-off might be produced) requires a different model. One strategy would be to alter the descriptive equations of the diode model. The standard diode charge control model provided in the SPICE device library assumed a constant injected carrier lifetime. Experimental investigations had revealed that the carrier lifetime is a function of current density. By using the test circuit in figure 60 (a) oscillograms such as 60(b) could be obtained. By measuring the gradient of the curve at the point of current interruption for various values of forward current the carrier lifetime could be calculated [5, 12, 127, 142] thus:

$$\tau = (k.T/q) \cdot (\delta t/\delta V) \qquad \text{-(E152)}$$

where $(\delta t/\delta V)$ is the reciprocal of the gradient of the curve

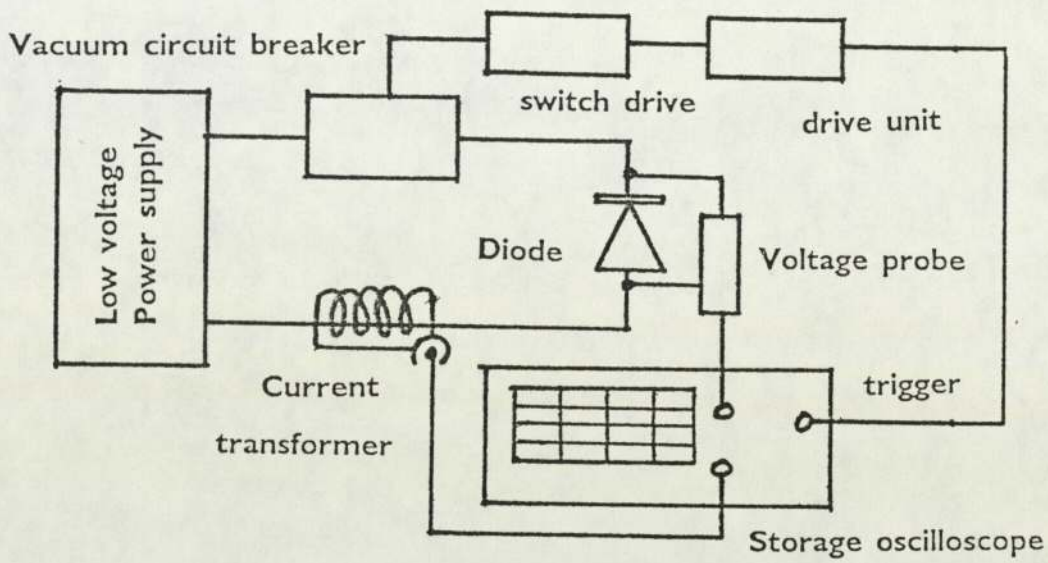
This data could then be used to construct the graphs shown in figures 61(a) and 61(b) demonstrating the variation of carrier lifetime with forward current. Thus the charge control diode model subcircuit used in this simulation incorporated a variable lifetime as a function of the current derived from experimental data. Figure 62 shows how a normal recovery waveform can be

FIGURE 60

(a) Diagram of test circuit using the Open Circuit Voltage Decay method of calculating carrier lifetime.

(b) Oscillogram showing diode voltage decay after open circuit.

(a)



(b)

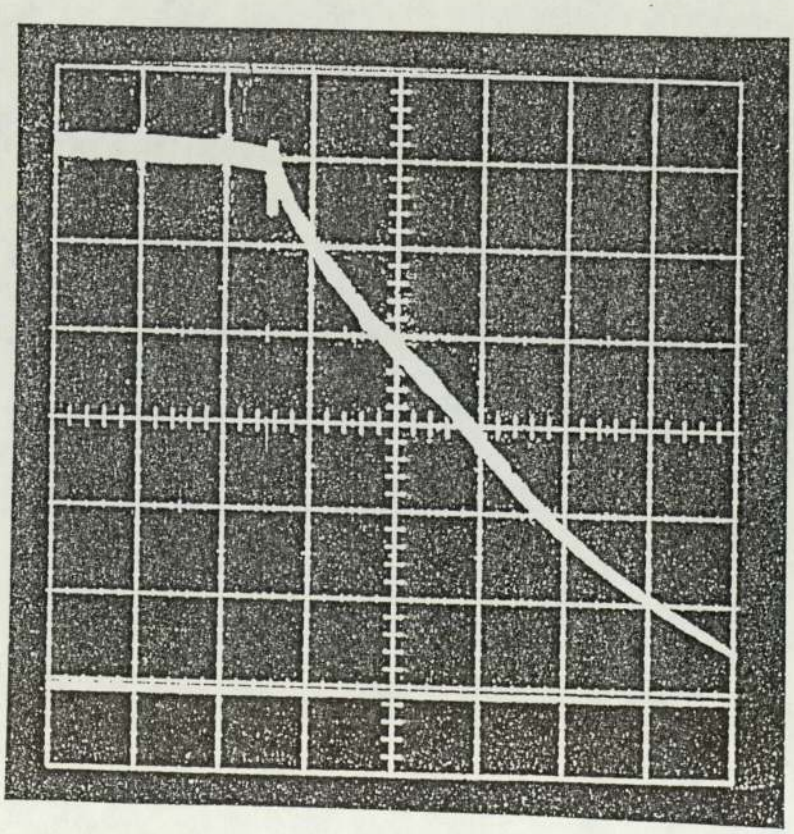
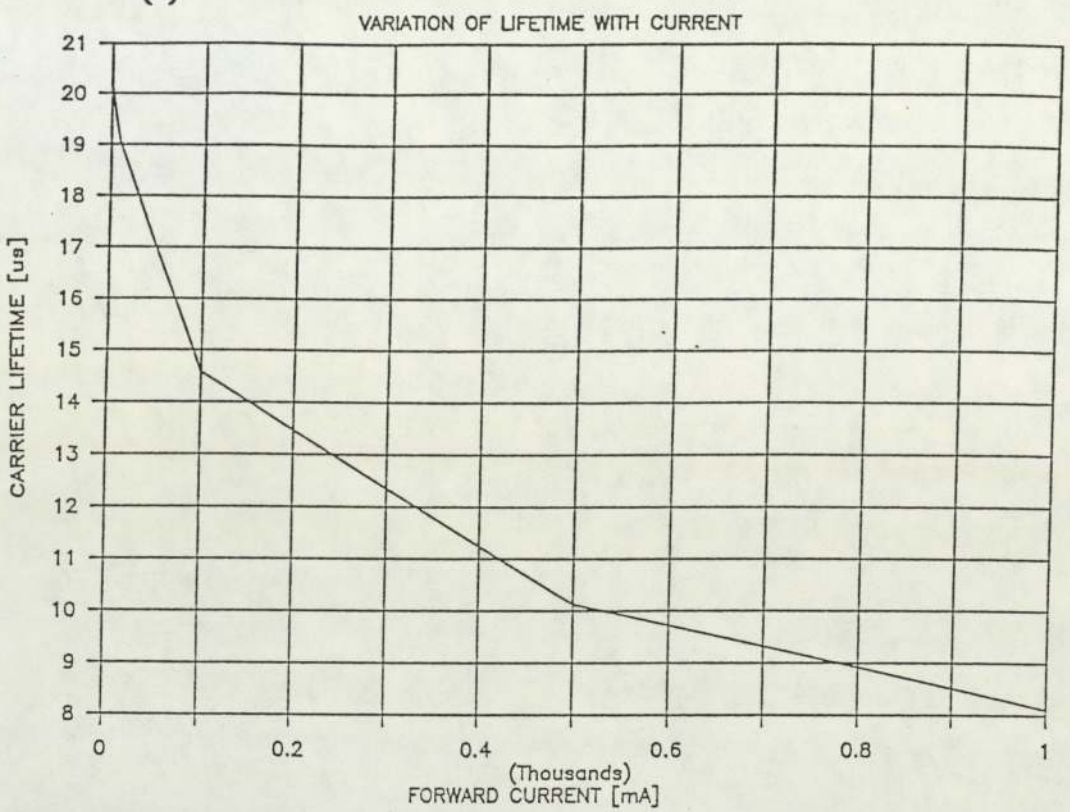


FIGURE 61

Graphs showing the variation of carrier lifetime with forward current.

(a)



(b)

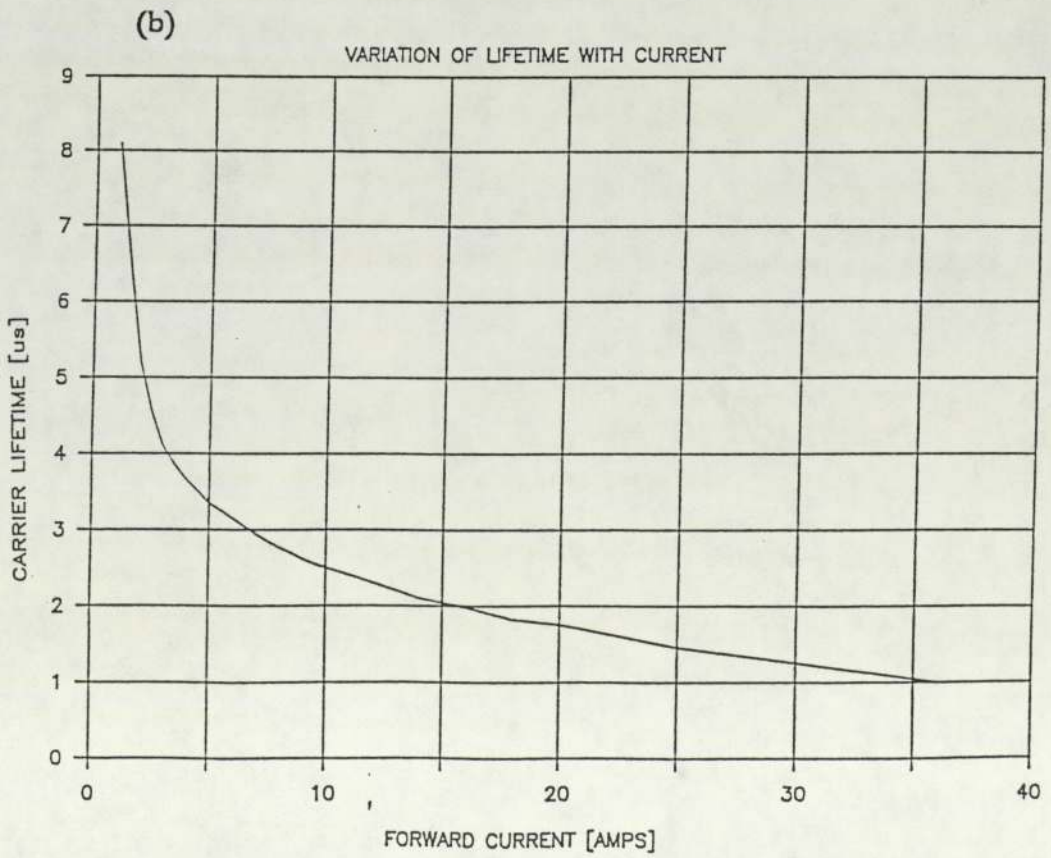
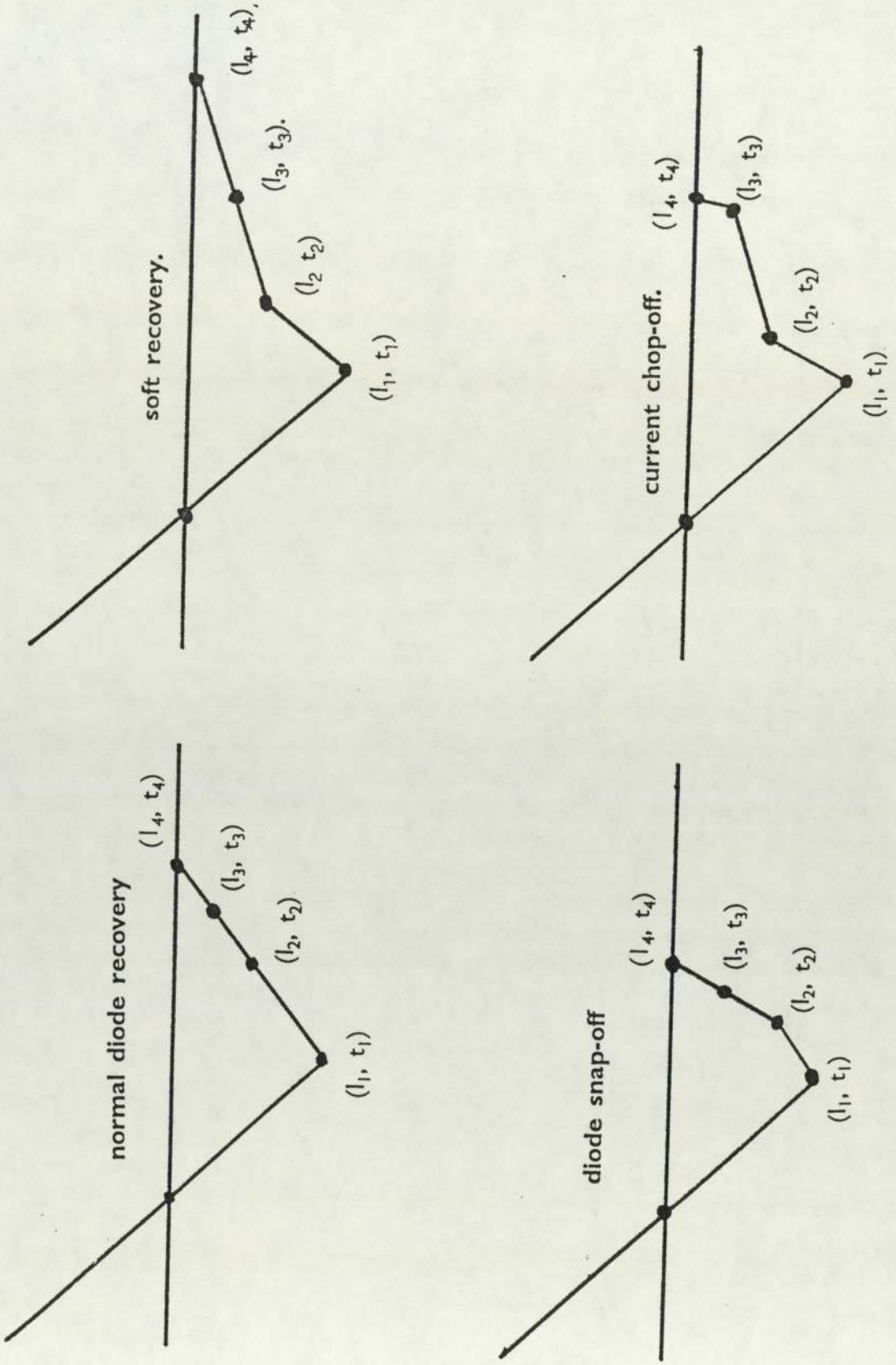


FIGURE 62

Diagram of showing straight line approximation of diode reverse recovery.



described by three straight line approximations to the real curve. These lines are defined by the co-ordinates (I_1, t_1), (I_2, t_2), (I_3, t_3) and (I_4, t_4). Smoothing of the curve can be obtained by defining four additional parameters δI_1, δI_2 ,δI_3 and δI_4. These values represent the difference between the required values and the corner values I_1, I_2 ,I_3 and I_4, Such parameters can then be used to describe a current generator, capacitor, resistor, inductor circuit that simulates diode reverse recovery performance. To obtain a smooth recovery voltage waveform that is a waveform with a slowly varying dV/dt it is necessary for the injected diode current waveform to have a continuous second derivative which requires high order equations for curve fitting.

Inclusion of a lifetime dependent on current density improves the accuracy of the diode model but fails to address the issue of diode snap-off. One method of constructing a diode snap-off model would be by using empirical equations and/or 'look up' tables. Figure 16 shows the variation of critical commutating dI/dt with main circuit series inductance. This curve can be approximated by the power equation.

$$\frac{dI_{crit}}{dt} = A.L_c^{B} \qquad \text{-(E153)}$$

Thus this can be used as a test for snappiness

$$\text{If} \quad \frac{dI}{dt} > A.L_c^{B} \qquad \text{-(E154)}$$

then the diode is snappy

However figure 19 shows that the critical commutating dI/dt also varies with peak forward current.

$$\text{Here:} \quad I_{pkf} = \sqrt{L_c.C}\ . \quad \frac{dI_{crit}}{dt} \qquad \text{-(E155)}$$

By combining equations (E153) and (E155), figure 63 can be constructed. Thus

FIGURE 63

Triaxal graph showing the performance characteristics of the diode.

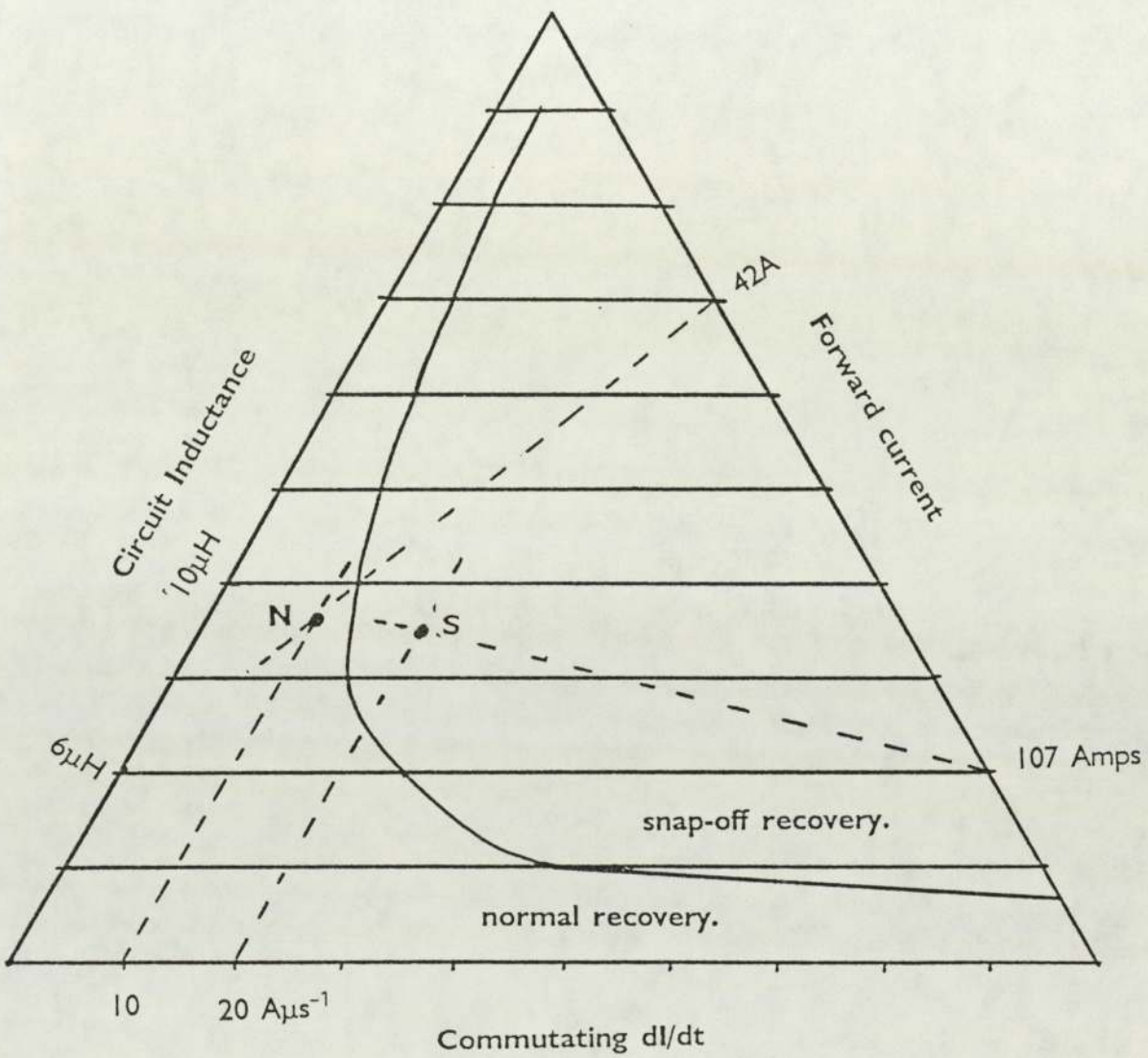


figure 63 demonstrates that the diode may be operated in a safe normal recovery regime depending upon the combination of peak forward current I_{pkf}, main circuit series inductance L_c and commutating dI/dt.

As an example of how to use figure 63, to determine if a diode will be subject to snap-off, first choose a combination of I_{pkr}, L_c and dI/dt.

Thus if $L_c = 6\ \mu H$ and the $\frac{dI_f}{dt} = 10\ A.\mu s^{-1}$

then by using equation (E155) where $C = 2.9\ \mu F$.

$$I_{pkr} = \sqrt{6\ \mu H \times 2.9\ \mu F}\ .10\ A.\mu s^{-1} = 42\ A$$

A line can then be constructed between 6 μH and 42 A. The intersection of this line and the 10 $A.\mu s^{-1}$ line drawn parallel to the inductance gives the diodes operating position i.e. point N on the figure 63. It can be seen from this diagram that a diode operated under these conditions will demonstrate normal, non-snappy recovery.

An example of snappy recovery can be shown by choosing a combination of:

$L_c = 10\ \mu H$ and $\frac{dI_f}{dt} = 20\ A.\mu s^{-1}$, using these parameters:

$$I_{pkf} = \sqrt{10\ \mu H \times 2.9\ \mu F}\ .\ 20\ A.\mu s^{-1} = 107\ Amps$$

By constructing a line from 10μH to 107 Amps the operating point, S, can be found at the intersection with the 20 $A.\mu s^{-1}$ line. Thus at point S the diode is operating with a snappy reverse recovery waveform.

The programme can then choose if the diode is undergoing snappy or normal recovery by implementing the following tests. Thus if:

$$I_{pkf} > \sqrt{L_c C} \cdot \exp \left[\frac{\ln L_c - \ln A}{B} \right] \quad \text{-(E156)}$$

then the diode shows normal recovery, and if

$$I_{pkf} \leq \sqrt{L_c C} \cdot \exp \left[\frac{\ln L_c - \ln A}{B} \right] \quad \text{-(E157)}$$

then the diode shows snappy recovery.

By referring to figure 64 it can be seen that the calculated diode current waveform in the simulated circuit (figure 67) has a progressively increasing commutating dI/dt. As the current waveform prior to peak current is circuit dependent this is entirely consistent with a current waveform found in practical circuits.

A second test that could be employed is:

$$\text{if} \quad \frac{dI_f}{dt} < \exp \left[\frac{\ln L_c - \ln A}{B} \right] \quad \text{-(E158)}$$

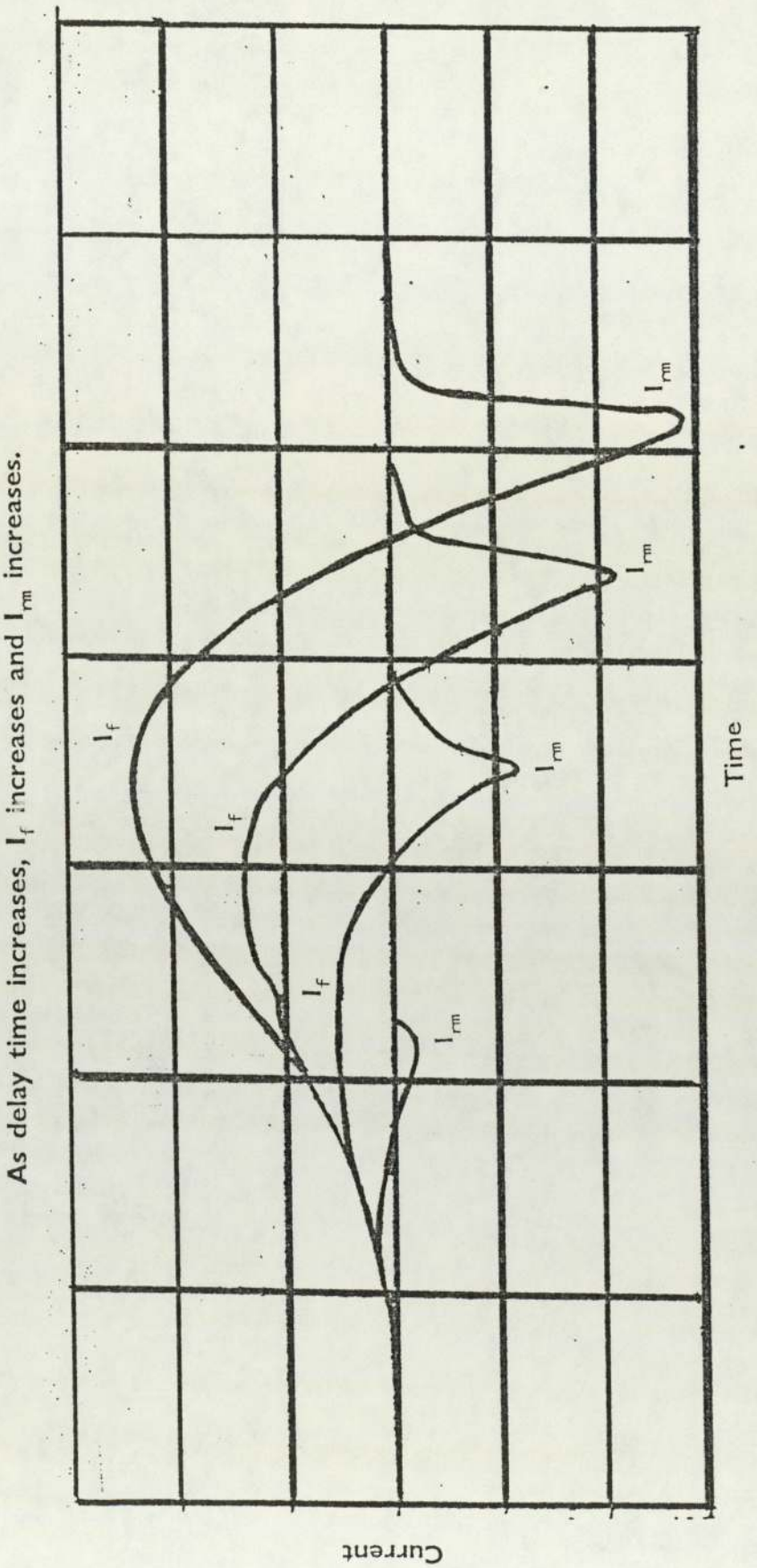
then the recovery is normal.

However because the circuit enforced current waveform has an increasing commutating dI/dt, (as shown in figure 64), this dI/dt will eventually exceed the critical dI/dt and the diode will then snap-off. In a real diode, because of the limited stored charge, the commutating dI/dt may not reach the critical value, since the diode will start to recover and the diode current will then be device dependent.

From section 4, the diode recovery time (t_{rr}) is as follows:

FIGURE 64

Graph showing the variation of snubber diode current with time.



$$t_{rr} = t_a + t_b \quad \text{-(E159)}$$

In the idealized triangular waveform shown in figure 36 the recovered charge Q_{rr} can be represented by the following equation:

$$Q_{rr} = \tfrac{1}{2} \cdot I_{rm} \cdot t_{rr} \quad \text{-(E160)}$$

Thus:

$$Q_{rr} = \tfrac{1}{2} \cdot I_{rm} \cdot (t_a + t_b) \quad \text{-(E161)}$$

Since: $S = t_b / t_a$ then $t_b = t_a.S$ -(E162)

and $Q_{rr} = \tfrac{1}{2} \cdot I_{rm} \cdot (t_a + t_a.S)$ -(E163)

For very fast extraction of stored charge [70].

$$Q_{rr} \approx Q_s = I_f \cdot \tau \quad \text{-(E164)}$$

assuming $I_{pkf} = I_f$ -(E165)

Then $I_{pkf} \cdot \tau = \tfrac{1}{2} \cdot I_{rm} \cdot (t_a + t_a.S)$

Hence $t_a = \dfrac{2.\tau.I_{pkf}}{(1+S).I_{rm}}$ -(E166)

Since $Q_{rr} = Q_a + Q_b$ -(E167)

and $Q_a = \tfrac{1}{2} \cdot I_{rm} \cdot t_a$ -(E168)

Then by substituting (E166) into (E168)

$$Q_a = \frac{\tau \cdot I_{pkf}}{(1+S)} = \frac{\tau \cdot I_{pkf}}{Ç} \quad \text{-(E169)}$$

In the real diode (with a changing commutating dI/dt)

$$Q_a = \int_o^{ta} I_r \cdot dt \qquad \text{-(E170)}$$

Thus at the point where

$$\int_o^{ta} I_r \cdot dt = \frac{I_{pkf} \cdot \tau}{\zeta} \qquad \text{-(E171)}$$

if $$\frac{dI_f}{dt} \geq \exp \left[\frac{\ln L_c - \ln A}{B} \right]$$

then the diode will become snappy and if

$$\frac{dI_f}{dt} < \exp \left[\frac{\ln L_c - \ln A}{B} \right] \qquad \text{-(E172)}$$

the diode will exhibit normal recovery.

When equation (E171) holds, the recovery dI/dt and thus the peak reverse recovery voltage can be determined. If the diode shows a normal recovery waveform then:

At $t = t_a$, $I_r(t_a) = I_{rm}$

and $$\frac{dI_r}{dt} = \frac{I_{rm}}{t_b} = \frac{I_{rm}^2}{2.Q_b} \qquad \text{-(E173)}$$

hence $$\frac{dI_r}{dt} = \frac{I_{rm}^2.(1+S^{-1})}{2 \cdot I_{pkf} \cdot \tau} \qquad \text{-(E174)}$$

and neglecting the effect of snubbers.

$$V_{pkr} = \frac{L_c.I_{rm}^2.(1 + S^{-1})}{2 \cdot I_{pkf} \cdot \tau} + V_r \qquad \text{-(E175)}$$

If the diode shows snappy recovery then

$$V_{pkr} = \frac{L_c . I_{rm}^2 . (1 + S^{-1})}{2 . I_{pkf} . \tau} + V_r + V_s \qquad \text{-(E176)}$$

Where V_s is the additional voltage contributed to the recovery voltage due to snap-off. The magnitude of V_s is best determined by impressing the calculated device dependent recovery waveform on the SPICE diode current generator as a piecewise linear approximation.

5.3 Verifying the model

5.3.1 The limitations of non-circuit coupled device calculations

Sections 3.3.1 to 3.3.9 have dealt with the performance of individual devices. Obviously the ultimate performance of the device will be dependent upon the circuit in which it operates. Thus the purpose of sections 3.3.1 to 3.3.3 inclusive was to investigate the effect of just such parameters e.g. main circuit series inductance and main circuit series capacitance. In addition the operating parameters were also investigated in sections 3.3.1 to 3.3.4, e.g. magnitude of forward current, commutating dI/dt and junction temperature.

Experience indicates however that the inclusion alone of relationships drawn from the above investigations would not by themselves construct a successful model. This is because when a circuit is constructed, inductive and capacitance contributions are created in addition to the value of the discrete components (i.e. inductors and capacitors) included in the circuit. These additional contributions are known as stray inductance and stray capacitance. It was thought that stray capacitance would reduce the magnitude of the voltage spike but it was unknown if stray inductance would increase or decrease the snap-off phenomenon or indeed if the relationship was even that simple.

Therefore in keeping will the policy statement in section 2.1 the importance of these second order effects was investigated as an aid to verifying the SPICE circuit model.

5.3.2 **The test circuit**

A test circuit similar to that shown in figure 12 and described in section 3.2 can be used to investigate second order effects by connecting additional circuit components across the device under test.

The effect of parallel capacitance on the diode peak reverse recovery voltage represents the practical case of stray circuit capacitance. This effect can therefore be investigated by placing various discrete capacitors across the test diode. The effect of stray inductance can also be investigated using discrete inductors.

One experimental point to note is that care should be taken to ensure that current and voltage measurements were made only on the device under test. Referring to figure 12 it can be seen that the current measuring CT and voltage probe was placed inside of any external snubber circuit. This will ensure that only the diode parameters were recorded i.e. diode current flow was recorded and not the sum of diode current and snubber current.

5.3.3 **The effect of parallel capacitance on diode recovery voltage**

The commutating dI/dt can be kept constant and the recovery voltage can be measured for different capacitance values. By increasing the 'stray' capacitance across the diode, snap-off will not be prevented but both the rate of rise of recovery voltage and the magnitude of the peak value will be limited. The energy associated with the voltage spike will be dissipated by charging up this 'stray' capacitance. Now since: $C = Q/V$ and Energy $= \frac{1}{2} . C . V^2 = E_c$ then for a spike of constant energy:

$$V = \sqrt{2.E_c / C} \qquad - \qquad (E177)$$

It can be seen therefore that as the stray capacitance is increased the voltage spike decreases. The experimental investigation also showed that as the voltage spike was reduced the frequency of the accompanying oscillations was also reduced.

As the capacitance across the diode increases, eventually the second recovery voltage peak exceeds the first recovery voltage peak. In addition as the capacitance across the diode increases the forward current drawn during subsequent oscillations also increases. The positive dI/dt is high enough to produce a transiently high forward voltage drop and thus cause increased power dissipation. Figure 65 shows a graph of peak reverse recovery voltage against stray capacitance. It can be seen that even a small amount of additional parallel capacitance (0.4nF) can reduce the initial voltage peak by approximately half. Further increases in stray capacitance would produce a diminishing improvement in spike reduction.

5.3.4 **The effect of parallel resistance on recovery voltage**

In practical inverter circuits an equivalent circuit analysis can show that there is effectively a resistive path in parallel to the snubber diode. During the switching transient a low resistance discrete resistor presents a lower impedance path than the transient impedance of the diode. Thus the peak reverse voltage generated during diode snap-off would be reduced. Unfortunately as the value of this resistance is reduced so the RC time constant for capacitor discharge will also be reduced, thereby increasing the turn-on duty of the GTO.

5.3.5 **The effect of parallel inductance on the recovery voltage**

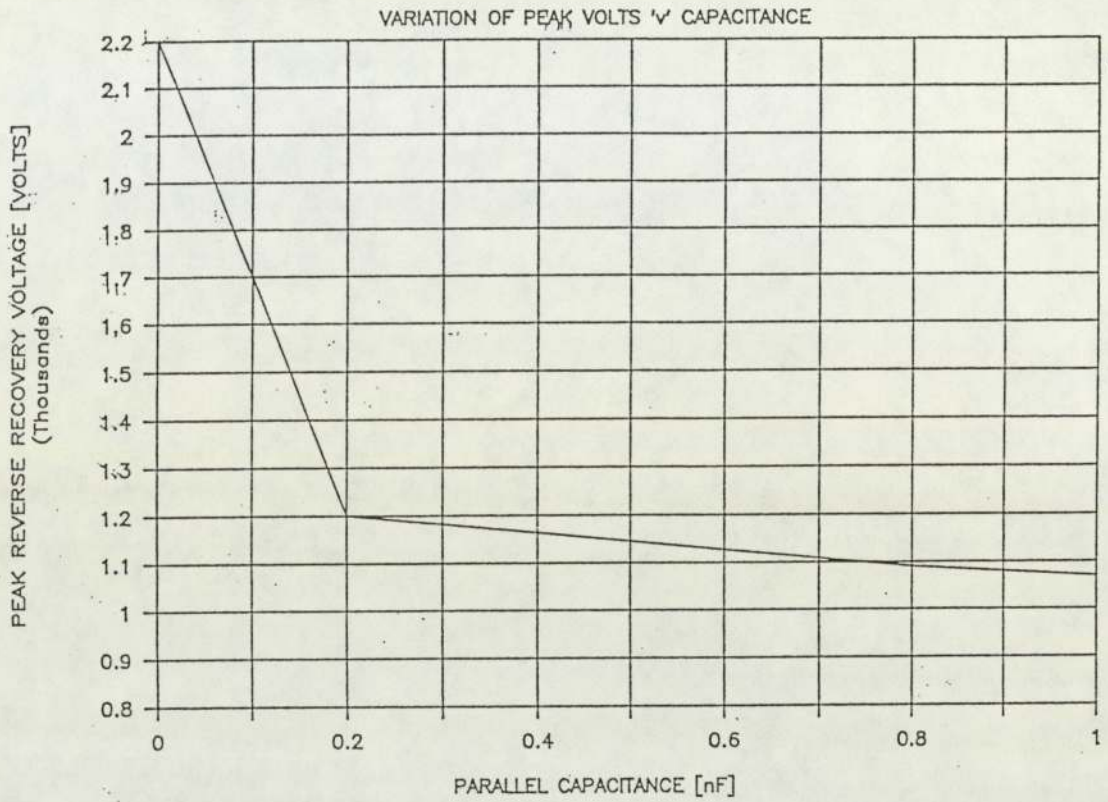
A series connected combination of discrete inductance and resistance placed in parallel with the test diode represents the practical case of a wire wound high power resistor. Following the procedure outlined in section 3.4.1 the effect of inductance connected in parallel with the device under test can be investigated. The critical dI/dt (at which snap-off commenced) will increased by the addition of these components. However as the parallel inductance is increased the critical dI/dt will be lowered.

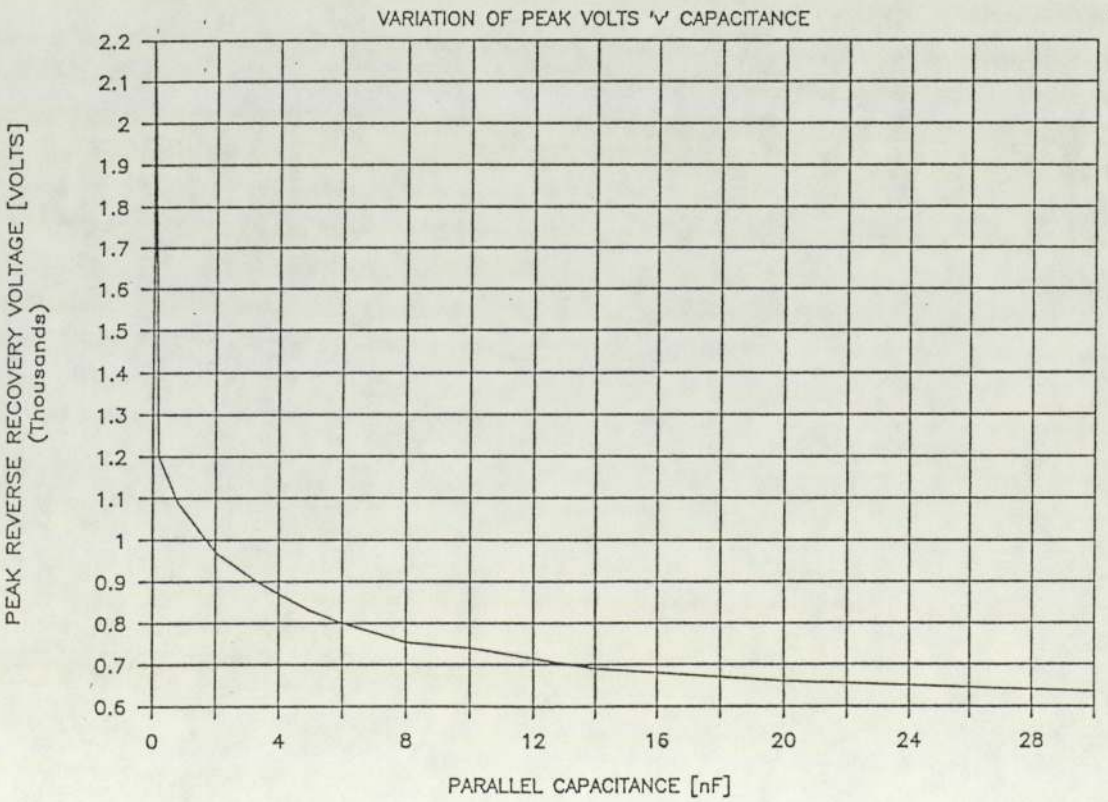
5.3.6 **The effect on recovery voltage of connecting devices in series**

Although the voltage rating of devices is improving, under certain circumstances

FIGURE 65

Graphs showing the variation of peak reverse recovery voltage against parallel capacitance for constant commutating dI/dt.





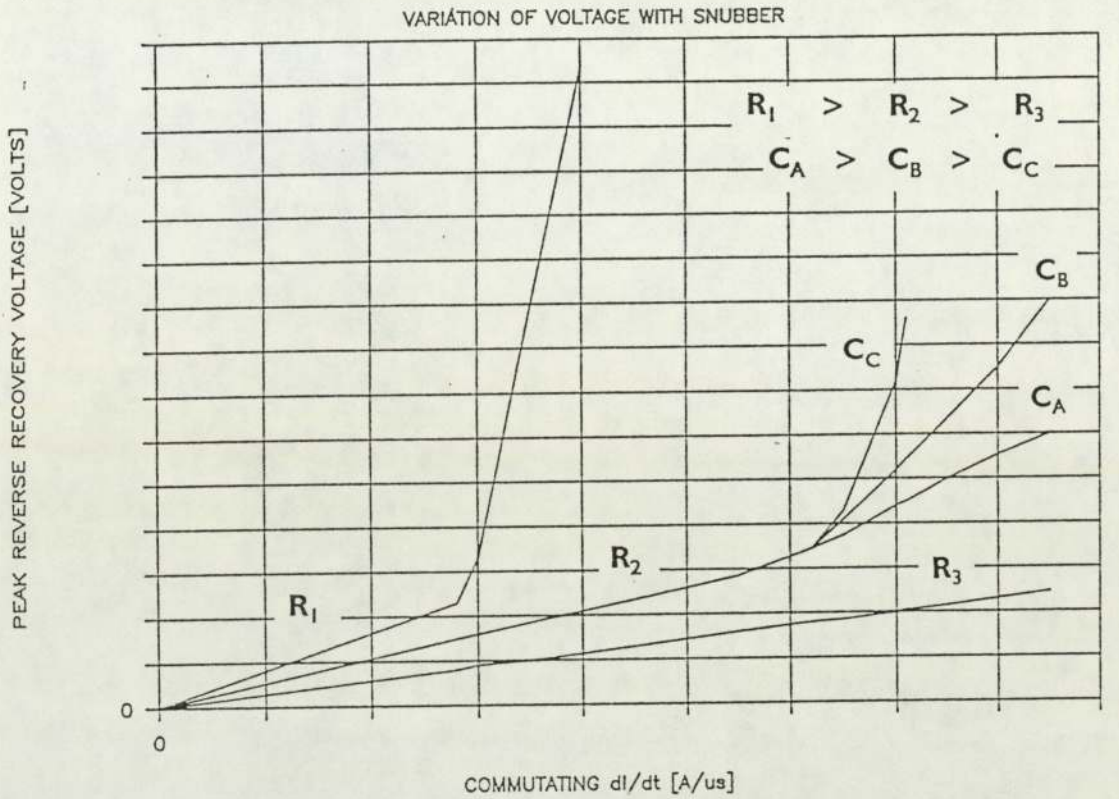
it may be necessary to connect two devices in series to achieve the desired voltage rating. Alternatively over-rated series connected diodes could be added to a circuit to provide a measure of redundancy. A third reason why this may occur would be to achieve a better trade off between voltage withstand and stored charge. This situation is analogous to connecting two parallel plate capacitors in series. The sum of the series connected capacitance is less than the capacitance of one capacitor of equivalent voltage withstand. However, whatever the reason for connecting devices in series, unless the diodes are perfectly matched in terms of stored charge [7], a voltage sharing network will be required. In a pair of unmatched diodes, the diode that recovers first will see the entire recovery voltage; such a voltage could destroy that device. It is known that such voltage sharing networks improve the dc voltage sharing of the devices and also affect the transient performance [62,63].

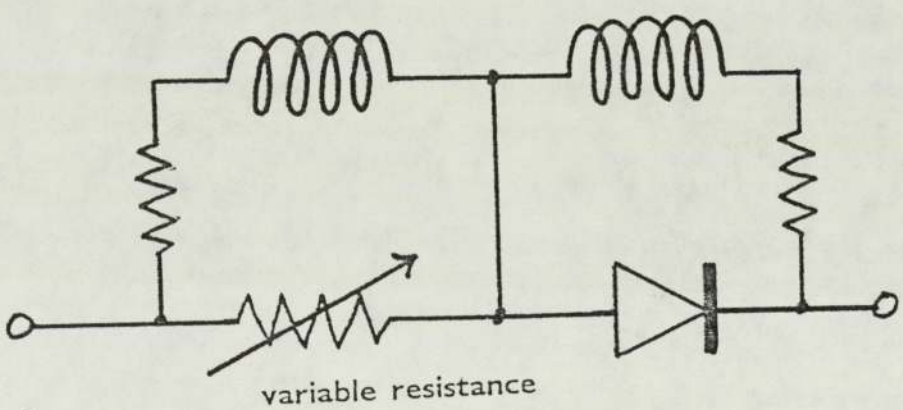
Mismatched pairs can show an apparent reduction in voltage sharing when grading resistors were used. When the diodes are conducting in the forward direction the inductive resistive snubber is effectively shorted out. When reverse bias is applied, initially reverse current is drawn until the stored charge is extracted and the diodes start to produce blocking layers. With two diodes in series, the diode with the lowest stored charge determines the impedance of the current path and consequently is the first to develop significant volts across it. The development of this voltage is controlled by the snubber inductance of $2L_s$ and the snubber resistance of $2R_s$. If the variation in stored charge between diodes is significant and a centre tapped snubber is used, then during commutation as one diode starts to turn off, the other diode can still be in a low impedance state, allowing reverse current to be drawn through it via the snubber network. Each diode is in the equivalent circuit shown in figure 66. When the non-linear resistance R is high then the series circuit inductance is increased by L_s and when the non-linear resistance is low the snubber inductance and snubber resistance are decreased by L_s and R_s respectively.

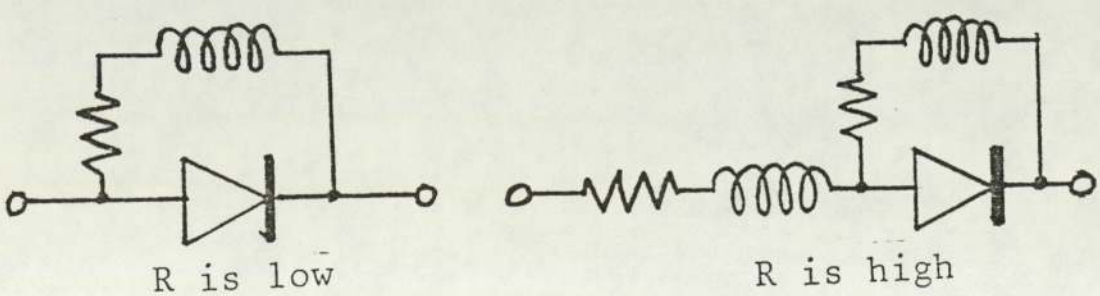
The first diode to turn off has an L_s and R_s snubber network across it, decreasing the normal reverse recovery voltage, increasing the critical snap-off dI/dt and decreasing any voltage spikes that are generated. The second diode

FIGURE 66

Graph and diagrams showing the effect of snubber networks on series connected diodes.







to turn off has an R_sL_s snubber network across it but an increased circuit inductance of $L_c + L_s$ and a circuit resistance of $R_c + R_s$.
If the magnitude of the decrease in critical dI/dt due to increase in circuit inductance is greater than the magnitude of the increase in the critical dI/dt due to the decrease in parallel inductance then the conditions for snappy turn off are enhanced.

5.4 Predictions and simulations

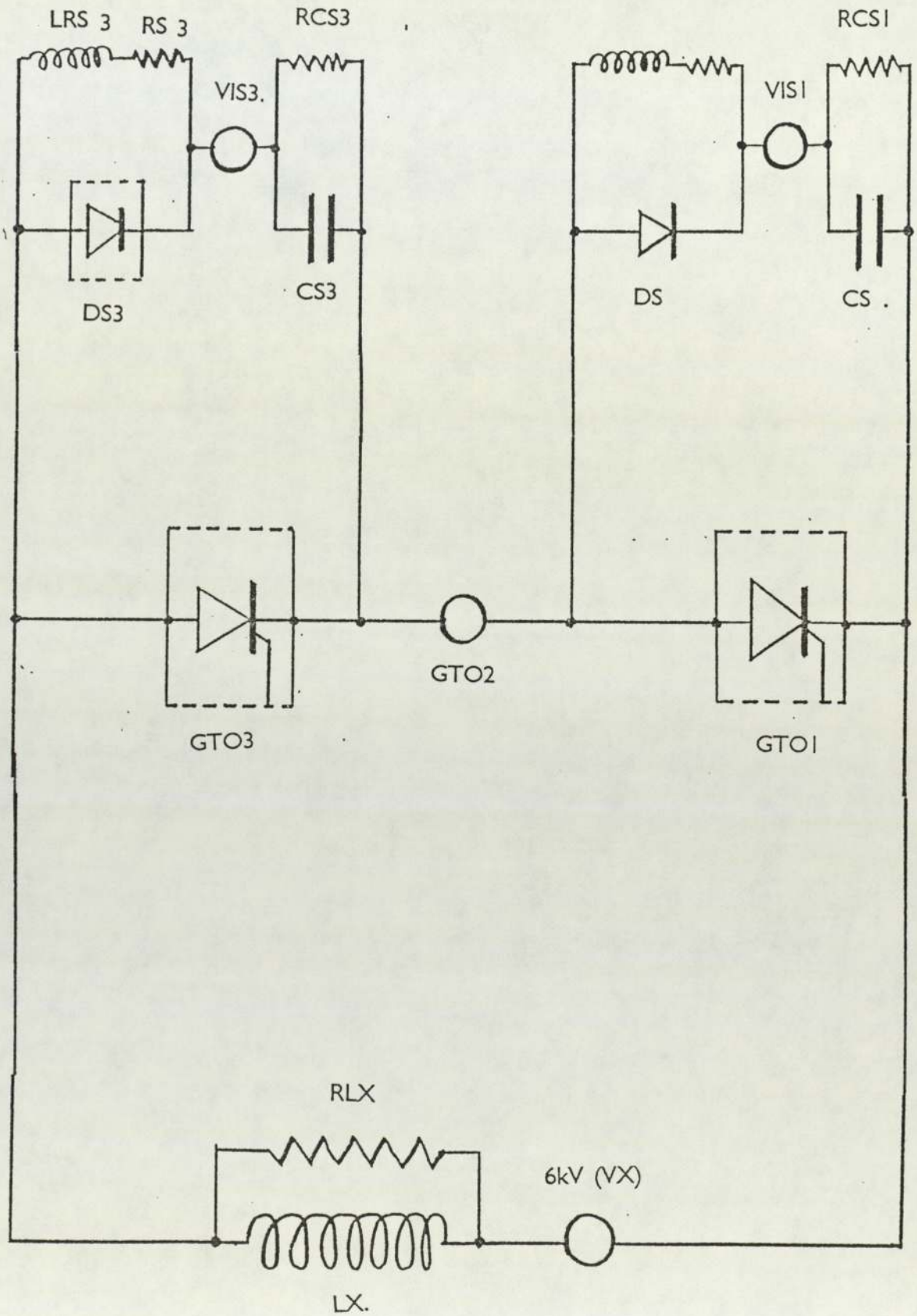
5.4.1 The simulation circuit

The basic circuit used for simulating the turn-on of three series connected GTO thyristors is shown in Figure 67. The voltage source of 6kV (VX) feeds the series GTO's via a 30μH inductor termed LX. During a simulation where one of the GTO's is characteristically different or is perhaps fired at a later time, then GTO's 1 and 2 are defined as being identical (along with their snubber networks) and GTO 3 is defined as the different device. GTO1 and GTO3 are described by two separate models while GTO2 and its associated snubber network are represented by a voltage source generating a voltage equal to that across GTO1 and its snubber. Since the snubber diode across GTO1 is always in the off state during a turn-on event the standard SPICE diode model was used for this component while the snubber diode across GTO3 was modelled in some detail. A requirement of SPICE forced the inclusion of resistances RCS1 and RCS3 across the capacitors to provide a dc path to ground. The value of these resistors was chosen as 1.0MΩ each. To assist convergence a damping resistor RLX of 10kΩ was placed across the circuit series inductance LX. To monitor the current flowing in each snubber network a zero voltage generator was added to the snubber i.e VIS1, VIS3.

The gates of each GTO were driven by a 50A current waveform. The GTO temperature was set at the maximum safe working junction temperature of 110°C.

FIGURE 67

Diagram of test circuit simulation.



5.4.2 **Results of the computer simulation**

Some of the results of this study have been published [46]. These results were produced by running simulations of increasing the firing delay of GTO3 relative to GTO's 1 and 2 from 0 to 2μs in 0.4μs steps.
In the initial stages of GTO1 and 2 turn-on, the GTO current (which is initially circuit independent) is drawn via LX and can only flow via the GTO3 snubber network. Thus the current flows through the snubber diode DS3 in the forward direction, and into the snubber capacitor CS3 slowly raising its voltage. At the commencement of device turn-on in GTO3, current will start to flow through the GTO, contributing to the current being drawn from LX and reducing the contributions required from CS3. Eventually the current flowing through GTO3 equals the current being drawn through LX by GTO's 1 and 2. At this point the current in DS3 will reach zero and then reverse direction until stored charge has been recovered. Until this time the snubber capacitor CS3 keeps the voltage across it, due to size of the capacitor and the small current levels. The capacitor will then be effectively connected across the GTO3 by the very low diode impedance. Hence, the voltage across GTO3 will remain high until the snubber diode DS3 snaps-off. It can be seen therefore that delaying the firing of GTO3 substantially increases its power dissipation. Figure 64 shows that by increasing the firing delay the snubber diode forward current, reverse current and commutating dI/dt are all increased. It should be noted that a 2μs firing delay in the GTO3 will result in a commutating dI/dt of $\approx$ 3000 $A.\mu s^{-1}$ being applied to the snubber diode. This progressively increasing dI/dt caused the snap-off to become more severe, resulting in the more rapid collapse of the voltage across GTO3. A kink in the voltage collapse wave-form is produced when the current starts to depend on the impedance of the external circuit instead of depending only on the gate current as it does in the early transistor like regime.

The main series inductance LX was reduced from 30 μH to 20 μH. This resulted in a doubling of the peak power dissipation and an almost double energy dissipation in GTO3 with a firing delay of 1.2 μs.

By altering the snubber resistor RS to LRS with an inductance of 5μH the same maximum power dissipation in GTO3 was found but the energy dissipation was reduced. This occurred because the additional inductance lowers the diode snap-off threshold producing a faster diode turn-off. The voltage across GTO3 thus collapsed more rapidly causing the power dissipation to drop to a low level immediately after reaching its peak.

If a non-uniform initial voltage distribution was placed across the series connected GTO's then a higher initial voltage across GTO3 increased its power dissipation in proportion to the voltage split. Similarly the dissipation is GTO1 and GTO2 also increased when a high initial voltage was placed across these devices. The effect of variations in GTO turn-on characteristics proved to be important since a 20% increase in GTO3 switching time produced a 70% increase in energy and power dissipation. Similarly increasing the gate drive amplitude to GTO3 from 50A to 100A produced a 50% reduction in power dissipation while reducing the gate drive from 50A to 40A produced a 100% increase in power dissipation.

5.5 SPICE model conclusions

1) Comparisons between experimental data and computer generated results, has shown that the SPICE model of the GTO circuit can accurately simulate in-service duty.

2) Under certain combinations of GTO firing delay the snubber diode can be subjected to a non-linear, progressively increasing commutating dI/dt. Such a situation could induce diode snap-off.

3) The diode model provided in SPICE is not suitable for modelling snap-off.

4) The effect on the circuit of a sudden chop-off of diode current can be simulated using the suggested diode model.

6. REVIEW OF THE ACHIEVEMENTS OF THIS STUDY

The achievements of this study can be described in three parts:

1) Experimental work (Section 3)

a) The effect of circuit parameters, operating conditions and diode design on the type of recovery a diode exhibits were categorised.

2) Device Modelling (Section 4)

a) A simple capacitive diode model is suggested which explains the diode snap-off phenomena in terms of the propagation of the depletion layer.

b) The task of incorporating the above findings into a finite element model proved difficult. This study identified that an alternative to the FEM using an equivalent circuit model of the diode could perform the necessary simulation task.

3) Device/Circuit Simulation (Section 5)

a) Using the SPICE programme the performance of a high power, high voltage diode was simulated.

b) Predictions of in-service circuit performance were made.

7. REFERENCES

1. Shockley. W : "The theory of pn junctions in semiconductors and pn junction transistors"; BELL SYSTEM TECHNICAL JOURNAL, Volume 28, Page 345-489, July 1949.

2. Somos. I : "Switching characteristic of Silicon power controlled rectifiers, II - Turn-off action and dv/dt self switching"; AIEE TRANS COMUN ELEC, Page 861-871, November 1964.

3. Herring. C : "Theory of transient phenomena in the transport of holes in an excess semiconductor"; BELL SYSTEM TECHNICAL JOURNAL, Volume 28, Page 401-427, 1949

4. Giorgis. J : "Understanding Snap diodes"; ELECTRONIC EQUIPMENT ENGINEERING, Page 61-64, November 1963.

5. Somos. I : "Commutation and destructive oscillation in diode circuits"; AIEE TRANS COMUN ELEC, Page 162-173, May 1961.

6. Gutzwiller. F.W : "Rectifier Voltage transients"; ELECTRICAL MANUFACTURING, Page 167-173, December 1959.

7. Tarnaja. K.S ,Geary. T.B : "Importance of recovered charges in fabrication and series operation of silicon powered diodes"; ELECTRONIC EQUIPMENT ENGINEERING CONFERENCE RECORD PS-TUE-AWDS IAS, Page 117-125, Milwaukee, 1972.

8. Kennedy. D.P, Murley. P.C : "Minority carrier characteristics of diffused emitter junction"; IRE TRANSACTIONS ON ELECTRON DEVICES, Page 136-144, March 1962.

9. Steele. E.L : "Charge storage in junction diodes"; JOURNAL OF APPLIED PHYSICS, Volume 25, Number 7, Page 916-918, July 1954.

10. Henderson. J.C, Tillman J.R : "Minority carrier storage in semiconductor diodes"; PROCEEDINGS OF THE IEE, Volume 104B, Page 318-336, January 1957, (Paper No 2393)

11. Velmre. E.E, Udal. A.E, Dermenzhi. P.G : "Influence of the lifetime distribution of Electrons and holes on the reverse recovery process of P^+.N.N diodes"; ELEKTROTEKHNIKA, Volume 55, No. 3 Page 47-51, 1984.

12. Ko. W.H : "The reverse transient behaviour of semiconductor junction diodes"; IRE TRANSACTIONS ON ELECTRON DEVICES, Volume ED-8, Page 123-131, 1961.

13. Nakajima. O, Nagata. K, Yamauchi. Y, Ito. H, Ishibashi. T : "High performance AlGaAs/GaAs HBT's utilizing proton implanted buried layers and highly doped base layers"; IEEE TRANSACTIONS ON ELECTRON DEVICES, Volume ED-34, Number 12, Page 2393-2398, December 1987.

14. Silber. D, Nowak. W.D, Wondrak. W, Thomas. B, Berg. H : "Improved dynamic properties of GTO thyristors and diodes by proton implantation"; IEDM 85, (IEEE PUBLICATION NUMBER CH2252-5/85/0000-0162), Page 162-165, 1985.

15. Dudeck. I, Kassing. R.J : "Gold as an optimal recombination center for power rectifiers and thyristors"; SOLID STATE ELECTRONICS, Volume 20, Page 1033-1036, 1977.

16. Baliga. B.J : "Improvement of power rectifier and thyristor characteristics by lifetime control"; IEEE PESC 77 RECORD, Page 11-16, 1977.

17. Tarneja. K.S, Bartko. J : "Electron irradiation - a method of producing fast switching high power diodes"; IEEE PESC 75 RECORD, Page 269-272, 1975.

18. Sun. Y.E : "Lifetime control in semiconductor devices by electron irradiation"; IAS 77, Page 648-655, 1977.

19. Rai-Choudhurry. P, Bartko. J. Johnson.J.E ; "Electron irradiation induced recombination centers in silicon-minority carrier lifetime control"; IEEE TRANSACTIONS ON ELECTRON DEVICES, Volume ED-23, Number 8, Page 814-818, August 1976.

20. Baliga. B.J, Sun. E : "Lifetime control in power rectifiers and thyristors using gold, platinum and electron irradiation"; IED MEETING (WASHINGTON), IEEE PUBLICATIONS, page 495-498, December 1976.

21. Carlson. R.O, Sun. Y.S, Assalit. H.B. : "Control of lifetime in silicon power devices using electron or gamma irradiation"; IEEE PESC 77 RECORD, Page 5-10, 1977.

22. Miller. M.D, Schade. H, Nuese. C.J : "Use of platinum for lifetime control in power devices"; IEEE CONFERENCE ON ELECTRONIC DEVICES, Page 180-183, 1975.

23. So. L, Whiteley. S, Ghandhi. S.K, Baliga. B.J : "Lifetime control by Palladium diffusion in silicon"; SOLID STATE ELECTRONICS, Volume 21, Page 887-890, 1978.

24. Lisiak. K.P, Milnes. A.G : "Platinum as a lifetime control deep impurity in silicon"; JOURNAL OF APPLIED PHYSICS, Volume 46, Number 12, Page 5229-5235, December 1975.

25. Miller. M.D, Schade. H, Nuese. C.J : "Lifetime controlling recombination centers in platinum diffused silicon"; JOURNAL OF APPLIED PHYSICS, Volume 47, Number 6, Page 2569-2578, June 1976.

26. Sixt. G, Kappert. H, Schwullke. G.H : "Minority carrier lifetime and defect structure in silicon after Cesium implantation"; PHYS. STAT. SOL, Volume 43, Page 119-131, 1977.

27. Svantesson. K.G, Nilsson. N.G : "The temperature dependence of the Auger recombination coefficient of undoped silicon"; SOLID STATE PHYSICS, Volume 12, Page 5111-5120, 1979.

28. Schwab. G, Bernt. H. Reichl. H : "Measurement of minority carrier lifetime profiles in silicon"; SOLID STATE ELECTRONICS, Volume 20, Page 91-94, 1977.

29. Yang. K.H. Kappert. H.F. Schwutte. G.H : "Minority carrier lifetime in annealed silicon crystals containing oxygen"; PHYS. STAT.SOL, Volume 50, Page 221-235, 1978.

30. Baliga. B.J. Krishna. S : "Optimization of recombination levels and their capture cross section in power rectifiers and thyristors"; SOLID STATE ELECTRONICS, Volume 20, Page 225-232, 1977.

31. Haug. A. Schmid. W : "Recombination mechanism in heavily doped silicon"; SOLID STATE ELECTRONICS, Volume 25, Number 7, Page 665-667, 1982.

32. Graff. K. Pieper. H : "The carrier lifetime of heat treated silicon crystals"; JOURNAL OF ELECTRONIC MATERIALS, Volume 4, Number 2, Page 281-298, 1975.

33. Shockley. W. Read W.T : "Statistics of the recombinations of holes and electrons"; PHYSICAL REVIEW, Volume 87, Number 5, Page 835-842, September 1952.

34. Cornu. J, Sittig. R, Zimmermann. W : "Analysis and measurement of carrier lifetimes in the various operating modes of power devices"; SOLID STATE ELECTRONICS, Volume 17, Page 1099-1106, 1974.

35. Efanov. V.M, Kardo-Sysoev. A.F : "Generation of nanosecond kilovolt gradients by fast recovery drift diodes"; INSTRUM AND EXP TECH (USA), Volume 29, Number 4, Part 1, Page 862-863, 1986.

36. Rohatgi. A, Rai-Choudhury. P : "Defects and carrier lifetime in silicon"; CONFERENCE ON SILICON PROCESSING SAN JOSSE CA, USA, Page 389-404, 19-22 January, 1983.

37. Beresford. R : "Survey of circuit simulators"; VLSI SYST. DES (USA), Volume 8, Part 8, Page 70-81, 1987.

38. Crow. T.T : "Solutions to Laplace's equation using spreadsheets on a personal computer"; AM. J. PHYS, Volume 55, Part 9, Page 817-23, 1987.

39. De Bruyne. P, Lawatsch. H : "Blocking voltage characteristic during turn-off of a semiconductor power device in R.C. connection"; BROWN BOVERI REVIEW - 5, Volume 62, Page 220-224, May 1975.

40. Spenke. E, Schuster.K : "The voltage step at the switching of alloyed pin rectifiers"; SOLID STATE ELECTRONICS, Volume 8, Page 881-882, 1965.

41. Berz. F : "Ramp recovery in p-i-n diodes"; SOLID STATE ELECTRONICS, Volume 23, Page 783-792, 1980.

42. Locher. R.E : "Optimizing the ultra-fast POWER planar rectifier diode for switching power supplies"; FAIRCHILD APPLICATION NOTE DIS-1, April 1984.

43. Aranov D.A, Mamatkulov. R : "On the theory of transient process after reversal of a p-i-n diode current from forward to reverse direction (II)"; PHYS. STAT. SOL (A), Volume 15, page 351-359, 1973.

44. Zastrow. E.E, Galloway. J.H : "Commutation behaviour of diffused high current rectifier diodes"; IEEE INTERNATIONAL CONVENTION RECORD, Volume 12, Part 4, Page 106-118, 1964.

45. Hoban. P.T : "The characterisation of snubber diodes for use with high voltage GTO thyristors"; THE 3RD INTERNATIONAL CONFERENCE ON POWER ELECTRONICS AND VARIABLE SPEED DRIVES, LONDON,IEE CONFERENCE PUBLICATION NUMBER 291, July 1988.

46. Chester. J.K, Gibson. H, Robinson. D.R, Hoban. P.T : "Computer modelling of GTO strings in megawatt inverters"; THE 3RD INTERNATIONAL CONFERENCE ON POWER ELECTRONICS AND VARIABLE SPEED DRIVES, LONDON, IEE CONFERENCE PUBLICATION NUMBER 291, July 1988.

47. Bank. R.E, Coughran. W.M, Fichtner. W, Grosse. E.H, Rose. D.J, Smith. R.K : "Transient simulation of silicon devices and circuits"; IEEE TRANSACTIONS ON ELECTRON DEVICES, Volume ED-32, Number 10, Page 1992-2005, October 1985.

48. Fitchtner. W, Rose. D.J, Bank. R.E : "Semiconductor device simulation"; IEEE TRANSACTIONS ON ELECTRON DEVICES, Volume ED-30, Number 9, Page 1018-1029, September 1983.

49. Rafferty. C.S, Pinto. M.R, Dutton. R.W : "Iterative methods in semiconductor device simulation"; IEEE TRANSACTIONS ON ELECTRON DEVICES, Volume ED-32, Number 10, Page 2018-2027, October 1985.

50. Benda. H, Spenke. E : "Reverse recovery processes in silicon power rectifiers"; PROCEEDING OF THE IEEE, Volume 55, Number 8, Page 1331-1354, August 1967.

51. Van Roosbroeck. W : "The transport of added current carriers in a homogeneous semiconductor"; PHYSICAL REVIEW, Volume 91, Number 2, Page 282-289, July 15, 1953.

52. Van Roosbroeck. W ; "Theory of the flow of electrons and holes in Germanium and other semiconductors"; BELL SYSTEM TECHNICAL JOURNAL, Volume 29, Page 560-607, 1950.

53. Adler. M.S, Temple. V.A.K, Rustay. R.C ; "Theoretical basis for field calculations on multi-dimensional reverse biased semiconductor devices"; SOLID STATE ELECTRONICS, Volume 25, number 12, Page 1179-1186, 1982.

54. Gummel. H.K : "Hole-electron product of pn junctions"; SOLID STATE ELECTRONICS, Volume 10, Page 209-212, 1961.

55. Mock. M.S : "Convergence and accuracy in stationary numerical models"; ISBN-0-906783-04-6, Page 53-67, 1981.

56. Van Dell. W.R ; "Accuracy and efficiency in high power semiconductor device modelling"; NASECODE III, Page 281-286, 1983.

57. Mayergoyz. I.D : "Solution of the nonlinear Poisson equation of semiconductor device theory"; JOURNAL OF APPLIED PHYSICS, Volume 59, part 1, Page 195-199, 1 January 1986.

58. Baines. M.J, Please. C.P, Sweby. P.K : "Numerical solution of dopant diffusion equations"; NASECODE III, Page 271-286, 1983

59. Selberherr. S, Griebel. W, Potzl. H : "Transport physics for modelling semiconductor devices"; ISBN-0-906674-38-7, Page 133-152.

60. Boronin. K, Dermenzhi. P.G : "The dependence of the turn off time for p-n-p-n structures on their parameters and the measurement conditions"; RADIO ENG AND ELECTRON PHYS (USA), Volume 18, Number 11, Page 1714-1721, November 1976.

61. Murray. S.J, Mole. P.J : "Towards a physical model carrier mobility device simulation"; NASECODE III, 1983

62. Evans. P.D, Mestha. L.K : "Analysis of conventional snubber circuits for PWM inverter using bipolar transistors"; PROCEEDINGS OF THE IEE, Volume 135, part B, number 4, Page 180-192, July 1988.

63. Tobin. W.H, Somos. I.L, Piccone. D.E : "Calculation of snubber circuits for two series-connected thyristors of unequal recovery current"; IAS 75, Page 109-124, September 1975.

64. Moloney. M.J : "Justifying the simple diode equation"; AM. J. PHYS, Volume 54, part 10, Page 914-917, October 1986.

65. Jacoboni. C, Conali. C, Ottaviani. G, Alberigi Quaranta.A : "A review of some charge transport properties of silicon"; SOLID STATE ELECTRONICS, Volume 20, Page 77-89, 1977.

66. Hall. R.N, Dunlap. W.C : "PN Junctions prepared by impurity diffusion', physical review"; Volume 80, Number 3, Page 467-468, November 1950.

67. Gummel. H.K : "A self-consistent iterative scheme for one-dimensional steady state transistor calculations"; IEEE TRANSACTIONS ON ELECTRON DEVICES, Volume ED-11, Page 455-4, 1964.

68. Ostergaard. D.F : "Adapting available finite element heat transfer programs to solve 2-D and 3-D electrostatic field problems"; JOURNAL OF ELECTROSTATICS, Volume 19, Page 151-164, 1987.

69. Melchior. H, Strutt. M.J.O : "Small signal equivalent circuit of unsymmetrical junction diodes at high current densities"; IEEE TRANSACTIONS ON ELECTRON DEVICES, Volume ED-12, Page 47-55, 1965.

70. Hoffmann. A. Schuster. K : "An experimental determination of the carrier lifetime in p-i-n diodes from the stored carrier charge"; SOLID STATE ELECTRONICS, Volume 7, Page 717-724, 1964.

71. Buturla. E.M : "A finite element tutorial"; ISBN 0-906-783-04-6, Page 9-15, 1981.

72. Tomizawa. M, Yokoyama. K, Yoshii. A. : "Semiconductor device simulations for high speed devices"; EXTENDED ABSTRACTS OF THE 19TH CONFERENCE ON SOLID STATE DEVICES AND MATERIALS, TOKYO, Page 375-378, 1987.

73. Ho-Le.K ; "Finite element mesh generation methods: a review and classification"; COMPUTER AIDED DESIGN, Volume 20, number 1, Page 27-38, 1988.

74. Cross. P.D : "The development of 350 kVA traction inverter system"; IEE CONFERENCE PROCEEDINGS ON 'RAILWAY FOR A NEW CENTURY', Page 101-108, October 1987.

75. McMurray. W : "Efficient snubbers for voltage source GTO inverters"; IEEE TRANSACTIONS ON POWER ELECTRONICS, Volume PE-2, Number 3, Page 264-272, July 1987.

76. McMurray. W : "Thyristor commutation in DC choppers a comparative study"; IEEE TRANSACTIONS ON INDUSTRY APPLICATIONS, Volume IA-14, Number 6, Page 547-554, November/December 1978.

77. Gentry, Gutzwiller, Holonyak, Von Zastrow : "Semiconductor controlled rectifiers : principles and applications of p-n-p-n devices"; PRENTICE HALL, 1964, Library of Congress catalogue card number 64-21172.

78. Grossman. B.M, Hargrove : "Numerical solution of the semiconductor transport equations with current boundary conditions"; IEEE TRANSACTIONS ON ELECTRON DEVICES, Volume ED-30, Number 9, Page 1092-1096, September 1983.

79. Castillo. J.E, Steinberg. S, Roache. P.J : "Mathematical aspects of variational grid generation II"; JOURNAL OF COMPUTATIONAL AND APPLIED MATHEMATICS, Volume 20, page 127-135, 1987.

80. Machek. J, Selberherr. S : "A novel finite element approach to device modelling"; IEEE TRANSACTIONS ON ELECTRON DEVICES, Volume ED-30, Number 9, Page 1083-1091, September 1983.

81. Arney. D.C. Flaherty. J.E : "A two-dimensional mesh moving technique for time dependent partial differential equations"; JOURNAL OF COMPUTATIONAL PHYSICS, Volume 67, Page 124-144, 1986.

82. Armstrong. G.A, Ferguson. R.S, Flynn. J.G : "Solution of semiconductor equations using a fully adaptive mesh strategy"; ELECTRONICS LETTERS, Volume 22, Number 16, Page 856-858, 31st July 1986.

83. Eiseman. P.R : "Adaptive grid generation"; COMPUTER METHODS IN APPLIED MECHANICS AND ENGINEERING, Volume 64, Page 321-376, 1987.

84. Buturla. E.M, Cottrell. P.E, Grossman. B.M, Salsburg. K.A : "Finite element analysis of semiconductor devices : The fielday program"; IBM. J. RES. DEVELOP, Volume 25, Number 4, Page 218-231, July 1981.

85. Bisio. G.R, Pidatella. S : "Numerical simulation of turn off characteristics of power rectifiers"; LABORATORIO CIRCUIT ELETTRONICI, C.N.R, GENOVA, ITALY.

86. Engl. W.L, Dirks. H.K, Meinerzhagen. B : "Device modelling"; PROCEEDINGS OF THE IEEE, Volume 71, Number 1, Page 10-33, January 1983.

87. Makarenko. E.N : "Superconvergence of the finite-element method for Poissons equation on regular meshes"; MOSC. UNIV. COMPUT. MATH. CYBEM. (USA), Volume 4, Page 74-77, 1987.

88. Porst. A : "Reverse transient behaviour of power rectifiers"; IEEE CONF RECORD OF THE INDUSTRY APPLICATION SOCIETY, Page 645-654, 1974.

89. Buturla. E.M : "Linearization methods"; ISBN 0-906783-04-6, Page 16-21, 1981.

90. Porst. A, Schuster. K : "Switching processes in diffused rectifiers-II, Experiment"; SOLID STATE ELECTRONICS, Volume 11, Page 13-24, 1968.

91. Schunemann. K : "The PIN-Diode, theory and performance"; A.E.U, Volume 25, Part II, Page 509-520, 1971.

92. Wilson. P.G : "Recombination in silicon p-π-n diodes"; SOLID STATE ELECTRONICS, Volume 10, Page 145-154, 1967.

93. Benda. H, Dannhauser. F : "Switching processes in diffused rectifiers-I, Theory"; SOLID STATE ELECTRONICS, Volume 11, Page 1-11, 1968.

94. Spenke. E, Hoffmann. A : "Switching processes in alloyed pin rectifiers"; SOLID STATE ELECTRONICS, Volume 8, page 693-697, 1965.

95. Schunemann. K, Muller. J : "A charge control model of the pin diode"; IEEE TRANSACTIONS ON ELECTRON DEVICES, Volume ED-23, Number 10, Page 1150-1158, 1976.

96. Moore. J.S, Holonyak. N, Sinkis. M.D : "Space charge and oscillation effects in gold doped silicon p-i-n diodes"; SOLID STATE ELECTRONICS, Volume 10, Page 823-832, 1967.

97. Hikin. B, Roach. T, Rodov. V : "Reverse recovery process with non uniform lifetime distribution in the base of a diode"; IEEE INDUSTRY APPLICATIONS SOCIETY, IAS/IEEE 12TH CONF RECORD, Page 644-647, 1977.

98. Benda. H, Hoffmann. A, Spenke. E : "Switching processes in alloyed pin rectifiers"; SOLID STATE ELECTRONICS, Volume 8, Page 887-906, 1965.

99. Abbas. C, Lietz. M, Sittig. R : "Turn-off behaviour of power rectifiers"; ELECTRONICS TO MICROELECTRONICS, W.A. KAISER AND W.E. PROEBSTER (EDS), North Holland publishing Company, Page 364-366, 1980.

100. Pong. M.H, Jackson. R.D : "Computer aided design of power electronic circuits"; PROCEEDINGS OF THE IEE, Volume 132, Part B, Number 6, Page 301-306, November 1985.

101. Barros. G : "A survey of circuit simulation Programs"; VLSI SYSTEMS DESIGN RUSA, Volume 7, Part 7, Page 32-44, 1986.

102. Navon. D.H : "Numerical analysis of circuits containing semiconductor devices"; ISBN 0-906674-38-7.

103. Navon. D.H : "Modelling of device-circuit interaction"; ISBN 0-906674-38-7.

104. Palm. E, Van de Wiele. F : "Two dimensional transient simulation of semiconductor devices coupled to an external circuit"; ISBN 0-906674-38-7, 1984.

105. Dirks. H.K : "Integration of device and circuit simulations"; IEEE CUSTOM INTEGRATED CIRCUITS CONF, Page 196-202, 1986.

106. Franz. A.F, Franz. G.A, Selberherr. S, Markowich. P : "The influence of various mobility models on the iteration process and solution of the basic semiconductor equations"; NASECODE III, Page 117-121, 1983.

107. Battell. R.D, Wallace. J.C : "PC based CAD for the electronics designer"; CIRCUIT WORLD (UK), Volume 14, Part 1, Page 15-17, 1987.

108. Crowley. J.M : "Electrostatic fields on PC spreadsheets"; JOURNAL OF ELECTROSTATICS, Volume 19, Page 137-149, 1987.

109. Basore. P.A : "Numerical analysis of semiconductor devices on personal computers"; PROCEEDING OF 6TH BIENNIAL UNIV/GOVT/INDUST. MICROELECTRONICS SYMPOSIUM, AURBURN, USA, 11-13 June 1985, Page 73-76.

110. Kerkhoven. T : "On the effectiveness of Gummel's method"; SIAM.J. SCI. STAT. COMPUT (USA), Volume 9, Part 1, Page 48-60, 1988.

111. Donea.J, Quartapelle, Selmin. V : "An analysis of time discretization in the finite element Solution of hyperbolic problems"; JOURNAL OF COMPUTATIONAL PHYSICS, Volume 70, Page 563-499, 1987.

112. Whight. K.R, Gough. P.A : "On state modelling of semiconductor floating regions using Gummel's algorithm"; NASECODE III, Page 607-614, 1983

113. Agler. W, Markowich. P.A, Selberherr. S : "A singular perturbation analysis of discretisation methods for the parabolic semiconductor device equations"; NASECODE III, Page 85-90, 1983.

114. Fletcher. R, Reeves. C.M : "Function minimization by conjugate gradients"; THE COMPUTER JOURNAL, Page 149-153, 1964.

115. Kapitza. H, Eppel. D : "A 3-D Poisson solver based on conjugate gradients compared to standard iterative methods and its performance on vector computers"; JOURNAL OF COMPUTATIONAL PHYSICS (USA), Volume 68, Part 2, Page 474-484, 1987.

116. Axelsson. O : "Conjugate gradient type methods for unsymmetric and inconsistent systems of linear equations"; LINEAR ALGEBRA AND ITS APPLICATIONS, Volume 29, Page 1-16, 1980.

117. Gentleman. W.M : "Row elimination for solving sparse linear systems and least squares problems"; LECTURE NOTES IN MATHEMATICS, ISBN 3-540-07610-7, Page 122-133, 1975.

118. Zlatev. Z : "A survey of the advances in the exploitation of the sparsity in the solution of large problems"; JOURNAL OF COMPUTATIONAL AND APPLIED MATHEMATICS, Volume 20, Page 83-105, 1987.

119. Ferguson. R.S, Ryan. W.D : "Algorithms for the numerical solution of semiconductor devices"; NASECODE I, Page 213-217, 1979.

120. Masszi. F, Tove. P, Bohlin. K, Norde. H : "Computer modelling and comparison of different rectifier (M-S, M-S-M, p-n-n^+) diodes"; IEEE TRANSACTION ON ELECTRON DEVICES, Volume ED-33, Number 4, Page 469-476, April 1986.

121. Engl. W.L, Dirks. H : "Numerical device simulation guided by physical approaches"; NASECODE I, Page 65-93, 1979.

122. Papadrakakis. M, Yakoumidakis. M : "A partial preconditioned conjugate gradient method for large eigenproblems"; COMPUTER METHODS IN APPLIED MECHANICS AND ENGINEERING, Volume 62, Page 195-207, 1987.

123. Fletcher. R : "Conjugate gradient methods for indefinite systems"; LECTURE NOTES IN MATHEMATICS, ISBN-3-540-07610-7, Page 73-89, 1975.

124. Mock. M.S : "Time dependent simulation of coupled devices"; NASECODE II, Page 113-131, 1981.

125. Goodrich. L.E : "Evaluation of least squares time stepping procedures for transient field problems"; PROC. INT. CONF. ON NUMERICAL METHODS FOR COUPLED PROBLEMS, Swansea, U.K, Page 40-48, 1981

126. Balestra. F, Audaire. L, Lucas. C : "Mos transistors at very low temperature: influence of substrate freeze out on the electrical characteristics"; 16TH EUROPEAN SOLID STATE DEVICE RESEARCH CONFERENCE, Europhysics Abstracts Volume 109, Cambridge University, 8-11 September 1986.

127. Lindholm. F.A, Sah. C.T : "Circuit technique for semiconductor-device analysis with junction diode open circuit voltage decay example"; SOLID STATE ELECTRONICS, Volume 31, Number 2, Page 197-204, 1988.

128. Cogan. A, Blanchard. R.A : "Discrete semiconductor switches, still improving", P.C.I.M. Page 15-22, January 1986.

129. Fodor. G.T : "Schottky power rectifiers"; ELECTRONICS INDUSTRY, Page 24-29 July 1980.

130. Nishizawa. J., Watanabe.Y : "Semiconductor inductance diode"; INTERNATIONAL SOLID STATE CIRCUITS CONFERENCE, Philidephia, Page 84-85, 12th February 1960.

131. Schunemann. K : "Turn on transient of PIN-diodes"; AEU, Volume 25, Part 4 Page 187-192, 1971.

132. Abramov I.I : "Approximation of Poisson's equation in the problem of the numerical analysis of semiconductor devices"; RADIO ELECTRON AND COMMUN SYST (USA), Volume 27, Part 6, Page 108-110, 1985.

133. Kus'Min. V.A : "Mathematical models of power semiconductor devices"; SOVIET ELECTRICAL ENGINEERING, Volume 49, Number 6, Page 14-20, 1978.

134. Kraut. E.A., Murphy. W.D : "Application of parabolic partial differential equations to semiconductor device modelling"; NASECODE III, Page 150-154, 1983.

135. El-Amawy. A, Porter. W.A., Arauena. J.L : "Array architectures for iterative matrix calculations"; PROCEEDINGS OF THE IEE, Volume 13, Part 3, Page 149-154, May 1987.

136. Nassif. N.R : "Variational methods for the numerical determination of the characteristics of certain semiconductors"; NASECODE I, Page 240-245, 1979.

137. Savini. A : "Finite element modelling of junction terminations in reverse-biased semiconductor devices"; NASECODE III, Page 252-257, 1983.

138. Mock. M.S : "Quadrilateral Elements and the Scharfetter-Gummel method"; ISBN 0-906674-38-7, Page 299-309, 1984.

139. Shockley, W : "A unipolar field effect transistor", PROCEEDINGS OF THE IRE, Page 1365-1377, November 1952.

140. Abbas. C.C : "Transient one-dimensional numerical analysis of bipolar power semiconductor devices"; Ph.D Thesis number 7614, SWISS FEDERAL INSTITUTE OF TECHNOLOGY, Zurich, Switzerland, 1984.

141. Kurata. M : "Design considerations of step recovery diodes with the aid of numerical large signal analysis": IEEE TRANSACTIONS ON ELECTRON DEVICES, Volume ED-19, Number 11, Page 1207-1215, November 1972.

142. Gossick. B.R : "On the transient behaviour of semiconductor rectifiers"; JOURNAL OF APPLIED PHYSICS, Volume 26, Number 11, Page 1356-1365, November 1955.

143. Davies. L.W : "The use of P-L-N structures in investigations of transient recombination from high injection levels in semiconductors"; PROCEEDINGS OF THE IEE, Volume 51, Page 1637-1642, 1963.

144. Aranov. D.A, Mamatkulov. R : "On the theory of transient process after reversal of a p-i-n diode current from forward to reverse direction (I)"; PHYS. STAT.SOL, Volume 14, Page 695-704, 1972.

145. Lindmayer. J, Wrigley. C : "A new aspect of the semiconductor diode"; JOURNAL OF ELECTRONICS AND CONTROL, Volume 14, Page 289-301, 1963.

146. Kanai. Y : "On the inductive part in the ac characteristics of the semiconductor diode"; J. PHYS. SOC JAPAN, Volume 10, Page 718-720.

147. Munoz-Yague. A, Leturcq. P : "High level behaviour of power rectifiers : a quantitative analysis of the forward voltage drop"; IEEE TRANSACTIONS ON ELECTRON DEVICES, Volume ED-25, Number 1, Page 42-49, January 1978.

148. Herlet. A : "The forward characteristic of silicon power rectifiers at high current densities"; SOLID STATE ELECTRONICS, Volume 11, Page 717-742, 1968.

149. Mock. M.S : "Analysis of mathematical models of semiconductor devices"; BODE PRESS, DUBLIN, ISBN 0-906783-07-0, 1983.

150. Sah. C.T : "New integral representations of circuit models and elements for the circuit technique for semiconductor device analysis"; SOLID STATE ELECTRONICS, Volume 30, Number 12, Page 1277-1281, 1987.

151. Guerrieri. R. Rudan. M : "Optimization of the finite element solution of the semiconductor device Poisson equation"; IEEE TRANSACTIONS ON ELECTRON DEVICES, Volume ED-30, Number 9, Page 1097-1103, 1983.

152. McCowen. A, Towers. M.S : "Algorithms for one dimensional and two dimensional transient simulators"; NASECODE IV, Page 157-166, 1985

153. Chu. C.K, Johnson. J.E, Karstaedt. W.H., Meenas D.F : "Design consideration on high voltage soft recovery rectifiers" IEEE IAS-82 CONFERENCE RECORD, Page 721-726, 1982.

154. Chu. C.K, Bartko. J, Felice. P.E : "Electron radiated fast switch power thyristor, IEEE IAS-75 CONFERENCE RECORD, Page 180-183, 1975.

155. Chu. C.K, Johnson, J.E, Spisak. P.B; Kao. Y.C : "Design consideration on high power soft recovery rectifiers"; IEEE CH1575-0/80/000-0720, Page 720-722, 1980.

156. Cooper. R.W, Jaggers. K.A : "Design and performance of fast high-voltage epi-diodes"; IEEE PESC-83 CONFERENCE RECORD, Page 150-153, 1983.

157. Bisio. G.R, Icardi. M.Di Zitti. E, Portesine. M, Tenconi. S : "Switching performance of high power fast recovery rectifiers"; IEEE PESC-81 CONFERENCE RECORD, Page 244-251,1981.

158. Wolley. E.D, Bevacqua. S.F : "High speed, soft recovery epitaxial diodes for power inverter circuits"; IEEE IAS-81 CONFERENCE RECORD, Page 797-800, 1981.

159. Cordingley.B.V : "Fast-diode losses under high-current pulse conditions"; AEI SEMICONDUCTORS LTD.

160. Ramsbottom. M.J : "Fast power diodes and thyristors - 1"; SEMICONDUCTORS, Page 27-40, 19th February 1980.

161. Ramsbottom. M.J : "Fast power diodes and thyristors - 2"; SEMICONDUCTORS, Page 24-31, 4th March 1980.

162. Assalit. H.B, Eriksson. L.O, Wu.S.J : "High power controlled soft recovery diode design and application"; IEEE IAS-79 CONFERENCE RECORD, Page 1056-1061, 1979.

163. Eugster. E : "Recent developments in silicon power rectifiers"; THE BROWN BOVERI REVIEW, Votre 53, Number 10, Page 626-635, 1966.

164. Eugster. E : "Principle and operation of a new surge-proof silicon power diode"; THE BROWN BOVERI REVIEW, Volume 53, Number 1/2, Page 35-41, 1966.

165. Vitins. J, De Bruyne. P, Taube. M : "Fast high power diodes with soft reverse recovery: physical and electrical properties"; IEEE IAS-79 CONFERENCE RECORD, Page 1062-1067, 1979.

166. Pinkham. R, Anderson.D.F : "A technique for modelling p-n junction depletion capacitance of multiple doping regions in integrated circuits"; SOLID STATE ELECTRONICS, Volume 29, Number 8, Page 773-777, 1986.

167. Liou. J.J : "Non-quasi-static capacitance of P/N junction space-charge regions"; SOLID STATE ELECTRONICS, Volume 31, Number 1, Page 81-86, 1988.

168. Eriksson. L.O, Tobin. W.H : "Evaluation and application of high power, controlled recovery diodes"; IEEE IAS-78 CONFERENCE RECORD, Page 1036-0143, 1978.

169. Kao. Y.C, Page.J : "Theoretical limits for high voltage rectifiers and thyristors"; IEEE 77CH 1275-7ED, Page 313 - 318, 1977.

170. Yee. J.H, Orvis. J, Khanaka. G.H, Lair. D.L : "Failure and switching mechanisms in semiconductor P-N junction devices"; IEEE PESC-83, Page 154-159, 1983.

171. Leturcq. P : "Power Junction Devices"; NORTH-HOLLAND PUBLISHING COMPANY, 1981.

172. Adler. M.S, Beatty. B.A, Krishna. S, Temple V.A.K, Torreno. M.L : "Physical mechanisms influencing power device design"; IEEE IAS-75 CONFERENCE RECORD, Page 175-179, 1975.

173. Van Overstraeten.R, Nuyts. W : "Comparison of theoretical and experimental values of the capacitance of diffused junctions"; JOURNAL OF APPLIED PHYSICS, Volume 43, Number 10, page 4040 - 4050, October 1972.

174. Selberherr.S, Ringhofer C.A : "Implications of analytical investigations about the semiconductor equations on device modelling programmes"; IEEE TRANSACTIONS ON COMPUTER AIDED DESIGN, Volume CAD-3, Number 1, page 52-64, January 1984.

175. Selberherr. S, Ringhofer. Ch : "Discretization methods for the semiconductor equations"; NASECODE III, Page 31-45, 1983.

176. Lindholm, F,A, Liou.J.J : "Quasistatic capacitance of p/n junction space-charge layers"; JOURNAL OF APPLIED PHYSICS, Volume 63, Number 2, Page 561-564, 15th January 1988.

177. Donskio, A.V, Smorodinov. V.V, Starvnov B.M: "Modelling of commutation processes accompanying turn-off of power semiconductor rectifiers"; ELEKTROTEKHNIKA, Volume 55, Number 7, Page 36-38, 1985.

178. Dermenzhi. P.G : "Charge and recovery time of diodes with linear forward-current decay"; ELEKTROTEKHNIKA, Volume 55, Number 7, Page 32-34, 1984.

179. Baliga. J.A, Torreno. M.L : "Influence of low lifetime regions on recombination in high lifetime regions"; INTERNATIONAL JOURNAL OF ELECTRONICS, Volume 40, Number 4, Page 393 - 408, 1976.

180. Jeter. M.W, Pye. W.C, Robinson. C.E : "An alternative way of computing matrix inverses"; MATH. COMPUT. EDUC. (USA), Volume 21, Part 3, Page 182-186, 1987.

181. Hines. J.R : "Circuit simulation adds spice to PC: Three PC - Based versions of SPICE"; ELECTRONICS TEST (USA), Volume 10, Part 9, Page 29-30, 1987.

182. Cornu. J, Sittig. R, Zimmermann. W : "Analysis and measurement of carrier lifetimes"; SOLID STATE ELECTRONICS, Volume 17, Page 1099-1106, 1974.

183. Engl. W.L, Dirks. H : "Models of physical parameters"; ISBN 0-906783-04-6, Page 42-46, 1981.

184. Zimmermann, W : "Measurement of spatial variations of the carrier lifetime in silicon power devices"; PHYS. STAT. SOL, Volume 12, Page 671, 1972.

185. Baliga. J.B, Adler. M.S : "Measurement of carrier lifetime profiles in diffused layers of semiconductors"; IEEE TRANSACTIONS ON ELECTRON DEVICES, Volume ED-25, Number 4, Page 472 - 477, April 1978.

186. Bianco. B, Bisio. G.R, Deffino. R : "Analytical solution for reverse recovery of power rectifiers"; IEEE TRANSACTIONS ON ELECTRON DEVICES, Volume ED-27, Number 9, page 1834-1836, 1980.

187. Kleinknecht. P.H : "Space-charge capacitance of asymmetric, abrupt p-n junction"; COMMUNICATIONS ON ELECTRONICS, Page 3034-3035, 1967.

188. Seiwatz, R,Green. M : "Space charge calculations for semiconductors"; Volume 29, Number 7, Page 1034-1040, July 1985.

189. Mott, N.F : "Recombination; a survey"; SOLID STATE ELECTRONICS, Volume 21, Page 1275-1280, 1978.

190. Buget. LL, Wright. G.T : "Space charge limited current in silicon"; SOLID STATE ELECTRONICS, Volume 10, Page 199-207, 1967.

191. Barnes. J.J Lomax.R.J : "Finite-element methods in semiconductor device simulation"; IEEE TRANSACTIONS ON ELECTRON DEVICES, Volume ED-24, Number 8, Page 1082 - 1089, August 1977.

192. Adler. M.S, Temple V.A.K : "Analysis and design of high power rectifiers"; ISBN 0- 306-41131-8, Page 183-211, 1982

193. Mohammad. S.N : "Boundary conditions and current-voltage relations for heavily doped p-n diodes"; SOLID STATE ELECTRONICS, Volume 30, Number 7, Page 713-718, 1987.

194. Axelsson. O : "A general conjugate gradient, least square methods"; NUMERISCHE MATHEMATIK, Volume 51, Page 209-227, 1987.

195. Ridders. C.J.F : "Curve fitting of a junction capacitance"; INTERNATIONAL JOURNAL OF ELECTRONICS, Volume 63, Number 3, Page 371-374, 1987.

196. Ringhofer. C : "An asymptotic analysis of a transient p-n junction model"; SIAM J. APPL. MATHS, Volume 47, Number 3, Page 624-642, 1987.

197. Park. J.S. Lindholm. F.A, Neugroschel.A : "An analytical study of the p-n junction space charge region under high forward voltage"; JOURNAL OF APPLIED PHYSICS, Volume 62, Part 3, Page 948-953, 1st August 1987.

198. Boisson. V.Le Helley. M. Chante J.P : "Etude de l'influence de s'epasseur de la region n pour l'optimisation de la tenue en tension des structures p-n-n+"; REVUE DE PHYSIQUE APPLIQUEE, Tome 22, No 7, Page 473-476, Juillet 1987.

199. Gummel H.K, Scharfetter D.L : "Depletion layer capacitance of p^+n step junctions"; JOURNAL OF APPLIED PHYSICS, Volume 38, Number 5, Page 2148-2153, April 1967.

200. Zlamal. M : "Finite element solution of the fundamental equations of semiconductor devices (1)"; MATHEMATICS OF COMPUTATION, Volume 46, Number 173, Page 27-43, January 1986.

201. Yoshi.A, Tomizawa. M, Yorkuyama. K : "Investigation of numerical algorithms in semiconductor device simulations"; SOLID STATE ELECTRONICS, Volume 30, Number 8, Page 813-820, 1987.

202. Hoburg. J.F, Davies J.L : "A student oriented finite element program for electrostatic potential problems"; IEE TRANSACTIONS ON EDUCATION, Volume E-26, Number 4, Page 138-142, November 1983.

203. Grekhov. V.I, Rabkin. P.B : "Influence of p^+ emitter doping level on reverse recovery process in p^+-n-n^+ power diodes"; ELEKTROTEKHNIKA, Volume 56, Number 9, Page 27-31, 1985.

204. Burtula. E.M; Cottrell. P.E : "Simulation of semiconductor transport using coupled and decoupled solution techniques"; SOLID STATE ELECTRONICS, Volume 23, Page 331-334, 1980.

205. Bank. R.E, Rose D.J, Fichtner W : "Numerical methods for semiconductor device simulation"; IEEE TRANSACTIONS ON ELECTRON DEVICES, Volume ED-30, Number 9, Page 1031-1041, September 1983.

206. Houston. D.E, Adler, M.S, Wolley E.D : "Measurement and analysis of carrier distribution and lifetime in fast switching power rectifiers", IEEE TRANSACTIONS ON ELECTRON DEVICES, Volume ED-27, Number 7, Page 1217-1222, 1980.

207. Khan. W.I : "A new theoretical model for a p-n junction realistic diode"; SOLID STATE ELECTRONICS, Volume 30, Number 12, Page 1221-1225, 1987.

208. Fitzimons. C.J : "A novel method for solving the continuity equations"; COMPEL, Volume 6, Number 2, Page 71-76, 1987.

209. Houston. D.E, Adler M.S, Wolley. E.D : "Measurement and analysis of charge distributions and their decay in fast switching power rectifiers"; IEEE, 77CH1275-7ED, Page 308-312.

210. Kao. Y.C : "The design of high-voltage power silicon junction rectifiers"; IEEE TRANSACTIONS ON ELECTRON DEVICES, Volume ED-17, Number 9, Page 765-660, September 1970.

211. Balenovich. J.D, Tarneja. K.S : "High voltage, high power, fast recovery silicon rectifier for chopper applications"; IEEE IAS 75, Page 184-188, 1975.

212. Mayergoyz. I.D, Korman. C : "A parallel and globally convergent iterative method for the solution of the nonlinear Poisson equation of semiconductor device theory"; IEEE Cat No 87TH01925, Volume 1, Page C1-C9, 1987.

213. Douglas. J, Martinez-Gamba. I, Squeff. M.C.J : "Simulation of the transient behaviour of a one dimensional semiconductor device"; MAT. APLIC. COMP, Volume 5, Number 2, Page 103-122, 1986.

214. Patterson. C, Bagdatlioglu. N.I : "On the use of coupler numerical models for refined structural analysis"; ISBN-0-906674-13, Page 105-114, 1981.

215. Raffy. M : "On some iterative methods for non linear coupled problems"; ISBN-0-906674-13-1, Page 173-182, 1981.

216. Schilders. W.H.A, Polak. A.J : "On the influence of quadrature rules in the new Sharfetter - Gummel scheme"; ISBN-0-906674-38-7, Page 310-318, 1984.

217. Den Heiger. C : "Preconditioned iterative methods for nonsymmetric linear systems"; ISBN 0-906674-38-7, Page 267-285, 1984.

218. Sever. M : "An alternative approach to lumped element modelling"; ISBN 0-906674- 13-1, Page 349-361, 1981.

219. Marini L.D, Savini A : "Accurate computation of electric field in reverse-biased semiconductor devices; a mixed finite-element approach"; COMPEL, Volume 3, Number 3, Page 123-135, 1984.

220. Varshney. R.C, Roulston. D.J : "Turn-off transient behaviour of p-i-n diodes"; SOLID STATE ELECTRONICS, Volume 14, Page 735-745, 1971.

221. Smith R.E, Eriksson. L.E : "Algebraic grid generation"; COMPUTER METHODS IN APPLIED MECHANICS AND ENGINEERING, Volume 64, Page 285-300, 1987.

222. Antognetti, P, Guiseppe. M : "Semiconductor device modelling with SPICE"; ISBN 0-07-002107-4, McGraw-Hill, 1987.

223. UNIVERSITY OF MANCHESTER REGIONAL COMPUTER CENTRE : "SPICE; A circuit analysis program", March 1983.

224. De Mari, A : "An accurate numerical steady state one dimensional solution of the p-n junction"; SOLID STATE ELECTRONICS, Volume 11, Page 33-58, 1968.

225. Snowden. C.M : "Introduction to semiconductor device modelling"; ISBN 9971-50-142-2, WORLD SCIENTIFIC PUBLISHING CO, 1986.

226. Rosenberg. H.M : "The Solid State"; ISBN 0-19-8151844-7, OXFORD UNIVERSITY PRESS, 1978.

227. Kittel. C : "Introduction to Solid State Physics"; ISBN 0-471-49024-5, JOHN WILEY AND SONS INC, 1976.

228. Van der Ziel, A : "Solid State Physical Electronics"; PRENTICE-HALL INC.

229. Dosse. J : "The Transistor"; VAN NOSTRAND COMPANY LTD, 1964.

230. Millman. J, Halkais. C.C : "Integrated Electronics; Analogue and digital circuits and systems"; MCGRAW-HILL, 1972.

231. INTERNATIONAL RECTIFIERS : "Data book on high power rectifiers"

232. "Transistors and diodes in power processing"; THOMSON - CSF. PUBLICATION, Page 79.

233. Moll. J.L, Hamilton. S.A : "Physical modelling to the step recovery diode for pulse and harmonic generation circuits"; PROCEEDINGS OF THE IEEE, Volume 57, Page 1250-1259, 1969.

234. Le Can, Hart, deRuyter : "Schalteigenschaften von diodes and transistorers"; PHILLIPS TECH BIBL, 1963.

235. Shockley, W, Prim, R.C : "Space-charge limited emission in semiconductors"; PHYSICAL REVIEW, Volume 90, Page 753-758, 1963.

236. Jonscher. A.K : "PNPN switching diodes"; JOURNAL OF ELECTRONICS, Volume 3, Page 573-586, 1957.

237. Manck. O, Heimeier. H.H, Engl. W.L : "High injection in a two-dimensional transistor"; IEEE TRANSACTIONS ON ELECTRON DEVICES, Volume ED-21, Page 403, 409, 1974.

238. Hachtel. G.D, Joy. R.C, Cooley. J.W : "A new efficient one-dimensional analysis programme for junction device modelling"; PROCEEDINGS OF THE IEEE, Volume 60, Page 86-98, 1972.

239. Engl. W.L, Dirks. H : " Functional device simulation by merging numerical building blocks"; Numerical Analysis of Semiconductor Devices and Integrated Circuits, B.T. brown and J.J.H. Miller, Eds: Dublin, Ireland; BOULE PRESS, 1981.

240. Engl. W.L, Manck.O, Wielder. A.W : "Modelling of bipolar devices in Process and Device modeling for integrated circuit design"; F.Van de Wiele, W.L. Engl, P.G Jespers: Eds: Leyden, The Netherlands, NO-ORDHOFF INT, PUBL, Page 377- 418, 1977.

241. Adachi. T; Yishii. A, Sudo. T : " A two dimensional semiconductor analysis using finite element method"; IEEE TRANSACTIONS ON ELECTRON DEVICES, Volume ED-26, Page 1026 - 1031, 1979.

242. Hachtel. G.D, Mack. M.H, O'Brien. R.R, Speelpenniny. B : "Semiconductor analysis using finite elements - Part 1: Computational aspects"; IBM J.RES, DEVELOP, Volume 25, Page 232, 245, 1981.

243. Heimeier. H.H : "A two dimensional numerical analysis of a silicon n-p-n transistors", IEE TRANSACTIONS ON ELECTRON DEVICES, Volume ED-20, Page 708 - 714, 1973.

244. Selberher. S. Schutz. A, Potzl. H.W : "Minimos - A two dimensional MOS transistor analyser"; IEEE TRANSACTIONS ON ELECTRON DEVICES, Volume ED-27, Page 1540-1549, 1980.

245. Slotboom. J.W : "Computer aided two dimensional analysis of bipolar transistors"; IEEE TRANSACTIONS ON ELECTRON DEVICES, Volume ED-20, Page 669-679, 1973.

246. Vandorpe. D, Borel. J, Merckel. G. Saintot, P : "An accurate two-dimensional numerical analysis of the MOS transistor"; SOLID STATE ELECTRONICS, Volume 15, Page 5470, 1972.

247. Wada.T, Dany R.L.M : " Modification of ICCG method for application to semiconductor device simulators", ELECTRON LETT, Volume 18, Page 265-266, 1982.

248. De Mari. A : " Accurate numerical steady state and transient one dimensional solutions of semiconductor device"; Report, California, Institute of Technology, Division of Eng and Appl Science, October 1967.

249. Scharfetter. D.L, Gummel, H.L : "Large signal analysis of a silicon Read diode oscillator"; IEEE TRANSACTIONS ON ELECTRON DEVICES, Volume ED-16, Number 1, Page 64 - 67, 1969.

250. Hall. R.N : "Germanium rectifier characteristic", PHYSICAL REVIEW, Volume 83, Page 228, 1951.

251. Hall. R.N : "Electron - Hole recombination in Germanium"; PHYSICAL REVIEW, Volume 87, Page 387, 1952.

252. Collins. C.B : "Properties of Gold doped silicon"; PHYSICAL REVIEW, Volume 105, Page 1168-1173, February 1957.

253. Sah. C.T, Shockley. W : "Electron-Hole recombination statistics in semiconductors", PHYSICAL REVIEW, Volume 109, Page 1103-1115, February 1958.

254. Shockley. W, "Electron, Holes and Traps", PROCEEDINGS OF THE IRE, Volume 46, Page 973-990, June 1958.

255. Hall, R.N : "Silicon photovoltaic cells"; SOLID STATE ELECTRONICS, Volume 24, Page 595-161, 1981.

256. Dziewoir. J, Schmid. W : "Auger coefficients for highly doped and highly excited silicon"; APPLIED PHYSICS LETTERS, Volume 31, Page 346-348, September 1977.

257. Lander, C.W : "Power Electronics"; MCGRAW-HILL, ISBN 0-07-084162-4, 1987.

258. Dorkel. J.M, Leturcq. P : "Carrier mobilities in silicon semi empirically related to temperature"; SOLID STATE ELECTRONICS' Volume 24, Page 821-825, 1981.

259. Brooks. H : "Scattering by ionized impurities in semiconductors ", PHYSICAL REVIEW, Volume 83, Page 879, 1951.

260. Debye. P.P, Conwell. E.M : "Electrical properties of n-type Germanium", PHYSICAL REVIEW, Volume 93, Page 693-706, February 1954.

261. Miller. J.J.H : "Some numerical techniques for the solution of problems related to semiconductors"; ISBN 0444701400.

262. Selberherr. S : "Analysis and simulation of semiconductor devices"; SPRINGER-VERLAG, VIENNA, 1984.

263. Kershaw. D.S : "The Incomplete Cholesky - Conjugate Gradient Method for the iterative solution of systems of linear equations"; JOURNAL OF COMPUTATIONAL PHYSICS, Volume 26, Page 43 - 56, 1978.

264. Borst. D. W, Cooper. D : "Circuit applications of fast recovery power rectifier diodes"; INTERNATIONAL RECTIFIERS APPLICATION NOTE,(Describing the test method adopted by committee JS-1 of the Joint Electron Device Councils [JEDEC]).

APPENDIX A

Construction of the p-i-n model

For the purposes of this model and indeed this study it is assumed that the on state time prior to turn off greatly exceeds the turn-on time and thus the turn on transient. Therefore turn-on transients have decayed away and the diode is assumed to be in a steady state condition prior to turn-off. Thus the diode has a forward current density of J_f for times $-\infty < t < o$ and at $t=o$ the current drops instantly to a reverse current density of $-J_R$.

To simplify the model the following assumptions are made:

1) abrupt p-i and n-i junctions.
2) one dimensional geometry (diode area A) with infinitely long contact layers.
3) intrinsic middle layer.
4) impressed time-independent current.
5) recombination in the i-layer is negligible during turn-off.
6) symmetrical diode model with respect for minority carrier lifetimes, diffusion constants and doping level of the contact layers.

To satisfy the requirements for an analytical treatment the square well doping profile of assumptions (1) and (3) were necessarily implemented. In addition to eliminate a diode parameter, infinitely long contact layers were assumed. The justification for assumption (5) is that carrier life-time in the i-layer is much larger than the extraction time during the turn-off transient in high stress conditions. The symmetry contraint in assumption (6) cannot readily be justified in physical terms because this is not usually met in practice. However, introduction of this assumption does reduce the calculation required for solution by a factor of 2 and also the influence of unsymmetrical phenomena is a 2nd order effect.

The above assumptions limit the validity of the turn-off transient calculations but since the model was used to identify trends and parameters of most significance this was not considered too great a drawback.

The starting point of any charge-control model is the continuity equation.

$$\frac{dQ_t}{dt} + \frac{Q_t}{\tau} = I_d \qquad \text{- (A1)}$$

This relates the total stored charge to the diode current I_d. The effective carrier lifetime is denoted by the symbol τ, while Q_t denotes the total stored charge. For a pin diode the total stored charge is the sum of i-layer charge and contact layer charge. Thus:

$$Q_t = Q_i + 2Q_c \qquad \text{- (A2)}$$

where Q_i = stored charge in the intrinsic region

Q_c = stored charge in the contact layers

Assigning carrier lifetime in the contact and intrinsic regions symbols τ_c and τ_i respectively allows the expansion of equation (A1). Thus:

$$\frac{dQ_i}{dt} + \frac{Q_i}{\tau_i} + \frac{d2Q_c}{dt} + \frac{2Q_c}{\tau_c} = I_d \qquad \text{- (A3)}$$

Equation (A3) must now be solved for Q_i and Q_c by constructing a second relationship between these two unknowns. This can be done by first considering the forward conducting steady state to establish such an additional relationship between Q_c and Q_i. In this case:

$$Q_i = Q_{io} \qquad \text{- (A4)}$$

$$Q_c = Q_{co} \qquad \text{- (A5)}$$

$$\frac{dI}{dt} = 0 \qquad \text{- (A6)}$$

and $I_d = I_f = J_f.A$ - (A7)

Neglecting the i-layer component, the voltage drops across the two junctions amounts to half of the forward voltage V_F minus the total contact potential V_D.

$$\tfrac{1}{2} V_F - V_D = 2V_c \quad \text{- (A8)}$$

where V_c = junction volt drop

According to Boltzmann statistics the stationary hole concentration in the i-layer can be written as:

$$P_i(x) = P_c \frac{\cosh (x/L_i)}{\cosh (W_i/2L_i)} \exp \{-e(V_D - V_F)/2.k.T\} \quad \text{- (A9)}$$

where $-W_i/2 \leq x \leq W_i/2$ - (A10)

In equation (A9) the x-coordinate origin is taken as the centre of the i-layer. L_i is the diffusion length for electrons and holes in i-layer, P_c the doping concentration at contact layers and kT/e the thermal voltage. Under the condition of low level injection in highly doped contact layers the minority carrier diffusion tails can be described by the following equation:

$$P_c (x) = P_c.\exp \{-(x-\tfrac{1}{2}.W_i)/L_{c*}\}. \exp\{-e.(V_D - V_F)/k.T\} \quad \text{- (A11)}$$

where $x \geq W_i/2$

Here P_c is the hole concentration in the n-contact layer and L_{c*} the corresponding diffusion length. Integrating (A9) and (A11) yields the stored charges Q_{io} and Q_{co} respectively. Using the steady state continuity equation:

$$Q_{io}/\tau_i + 2Q_{co}/\tau_c = I_f \quad \text{- (A12)}$$

V_F can be elimated to produce:

$$v = \exp\{-3(V_D - V_F)/2.k.T\}$$

$$= -\frac{L_i}{2.L_{c*}} \cdot \frac{\tau_c}{\tau_i} \cdot \tanh \frac{W_i}{2.L_i} + \sqrt{\frac{L_i.\tau_c}{2.L_{c*}.\tau_i}.\tanh(W_i/2.L_i)^2 + \frac{\tau_c.I_f}{2.L_{c*}.e.P_c.A_j}} \quad \text{-(A13)}$$

Thus

$$Q_{co} = A_j.e.P_c.L_{c*}.v^2 \quad \text{- (A14)}$$

and

$$Q_{io} = 2.\tanh\{(W_i/2.L_i)\} \cdot \{(A_j.e.P_c.L_i^2)/L_{c*}\}^{1/2} \cdot (Q_{co})^{1/2} \quad \text{- (A15)}$$

The recovery of the diode can be described as being split into three time intervals. In the first interval the i-layer stored charge remains unaffected by the applied reverse bias but the contract layer stored charge is recovered. In the second phase the stored charge in the i-layer is recovered. The third and final phase occurs as space charge layers develop at the contact layers and then propagate across the i-region to eventually combine.

During the first phase i.e. $0 \leq t \leq t_1$ the reverse current is produced by the extraction of the $2Q_c$ stored charge. At $t=t_1$ the minority carrier concentrations at the junctions become zero. According to LeCan et al [234] t_1 can be obtained by a geometrical calculation as indicated in figure A1 (a). The exponential hole distribution of the n-type contact-layer diffusion tail is replaced by a straight-line approximation yielding the same Q_{co} i.e constant area. Then the gradient of the hole distribution near the junction $x= W_i/2$ is proportional to $J_f/2$. At $t=t_1$ the border concentration is zero. The gradients of the straight line approximation to the hole distribution shown in figure A1 are given by:

$$\tan \Theta_1 = J_f / 2.e.D_c = P_c.v^2 / 2.L_{c*} \quad \text{- (A16)}$$

where D_c = diffusion constant = $\mu_c.k.T/e$ - (A17)

where L_{c*} = diffusion length = $(D_c \cdot \tau_c)^{1/2}$ - (A18)

and

$$\left.\frac{dp_c}{dx}\right|_{x = Wi/2} = \tan \Theta_2 = J_R / 2.e.D_c \qquad \text{- (A19)}$$

At $t=t_1$ the border concentration is zero, therefore the recovered charge is

$$\delta Q_{c1} = \frac{\tan \Theta_1}{\tan \Theta_1 + \tan \Theta_2} \cdot Q_{co}.\exp(-t_1/\tau_c) \qquad \text{- (A20)}$$

The exponential term is introduced to account for recombination due to the short minority carrier lifetime in the contact layer.

Equating δQ_{c1} to $I_R \cdot \frac{1}{2}t_1$ -(A21)

and accounting for equations (A13),(A14) and (A15) produces the contact-layer recovery time.

$$t_1 = \frac{2.Q_{co}}{I_R.(1 + \tan \Theta_2/\tan \Theta_1)} \cdot \exp(-t_1/\tau_c) \qquad \text{-(A22)}$$

The hole distribution in the n-type contact for $t > t_1$ can be approximated as shown in figure A1. The residual current is assumed to decrease linearly with time until,

$\tan \Theta_2 = \tan \Theta_1$ at $t = t_{12}$ - (A27)

and the recovered residual charge is then δQ_{c2}.

For $t > t_1$ the reverse current is made up from extracting both Q_{io} and Q_{co}. Because of the residual contact-layer current $-I_c(t)$, Q_{io} is only recovered by the difference current $I_R - I_c$ and at $t=t_{12}$ the contact-layer storage charge has shrunk to

$$Q_c(t_{12}) = \frac{1}{2}.Q_{co}.\exp(-t_{12} / \tau_c) \qquad \text{- (A24)}$$

Again the exponential term accounts for losses due to recombination.

The charge is therefore approximated by,

$$\delta Q_{c2} = Q_{co}.(\tfrac{1}{2} - \frac{1}{1 + \tan \Theta_2 / \tan \Theta_1}) . \exp (t_{12}/\tau_c) \qquad \text{- (A25)}$$

This is recovered during the time period $(t_{12} - t_1)$

Equating δQ_{c2} to the charge transported by $I_c(t)$ produces an expression for t_{12}. Thus:

$$t_{12} = t_1 + \frac{2Q_{co} \cdot \left[\tfrac{1}{2} - \frac{1}{1 + \tan \Theta_2 / \tan \Theta_1} \right] . \exp (-t_{12}/\tau_c)}{I_R + 2.e.A_j.D_c.\tan \Theta_1} \qquad \text{- (A26)}$$

For $t > t_{12}$ an exponential residual current decay is assumed;which then produces the following equation:

$$I_c(t) = I_c(t_{12}) .\exp \left[\frac{2.D_c}{L_{c*}^2} .(t_{12} - t) \right] .\exp \{(t_{12} - t)/\tau_c\} \qquad \text{-(A27)}$$

where $t \geq t_{12}$

In the above equation the second exponential term accounts for recombination effects. Defining $L_{c*}^2 = D_c.\tau_c$ - (A28)

and

$$I_c(t) = I_R - (2.e.A_j.D_c \tan \Theta_1 - I_R). \frac{t_1 - t}{t_{12} - t_1} \qquad \text{- (A29)}$$

for $t_1 \geq t \geq t_{12}$

produces the following equation,

$$I_c(t) = I_{co}.\exp (-3.t/\tau_c) \qquad \text{- (A30)}$$

where $I_{co} = 2.e.A_j.D_c.\tan \Theta_1 . \exp (3.t_{12}/\tau_c)$ - (A31)

for $t \geq t_{12}$.

This expression describes the exponential decay of the residual current.
The above equation describes the contact layer current. To obtain a full

description of the recovery process the charge recovery process in the i-layer must now be treated. For $t > t_1$ the current is primarily supported by the stored charge in the i-region. Prior to $t=t_{12}$ the i-layer charge of

$$\delta Q_i(t_{12}) = \int_{t1}^{t12} (I_R - I_c)\, dt \qquad \text{- (A32)}$$

has been recovered. Hence

$$Q_i(t_{12}) = Q_{io} - (I_R - 2.e.A_j.D_c \tan \Theta_1) \quad - \frac{t_{12} - t_1}{2} \qquad \text{- (A33)}$$

This is used as the initial condition for the continuity equation,

$$\frac{dQ_i}{dt} = - (I_R - I_c) \qquad \text{- (A34)}$$

which is then used to calculate $Q_i(t)$, $t \geq t_{12}$ with I_c being obtained from equation (A30). Thus:

$$Q_i(t) = Q_{io} - (I_R - 2.e.A_j.D_c \tan \Theta_1) \quad . \quad \frac{t_{12} - t_1}{2} + I_R.(t_{12} - t) \qquad \text{- (A35)}$$

$$+ \frac{I_{co}.\tau_c}{3}.[\exp(-3.t_{12}/\tau_c) - \exp(-3.t/\tau_c)]$$

By linearizing the i-layer charge carrier distribution, t_2 can be calculated. By definition the border concentrations are zero. Therefore because the carrier flow at $x = +/- W_i/2$ is due to diffusion only. The gradient of the carrier distribution is therefore given by:

$$\left.\frac{dP_i}{dx}\right|_{x=-Wi/2} = \frac{I_R - I_c}{2.e.A_j.D_i} \qquad \text{- (A36)}$$

The i-region charge carrier profile may either be a triangular or a trapezoidal approximation to the actual distribution. Which approximation is chosen depends upon the device physical structure and reverse current density. The stored charge at $t=t_2$ is calculated and used with equation (A36) to produce a transcendental equation which can then be solved for t_2. For a trapezoidal

distribution at $t=t_2$ the 'curve' has a height of:

$$P_{io} = Q_{io} / e.W_i.A_j \quad \text{see figure A2} \qquad \text{- (A37)}$$

and a roof of width 'a'. Consequently,

$$\left.\frac{dP_i}{dx}\right|_{x=-Wi/2} = \frac{2P_{io}}{W_i-a} = \frac{2.Q_{io}}{e.A_j.W_i.(W_i-a)} \quad \text{at} \quad t=t_2 \qquad \text{-(A38)}$$

and

$$Q_i(t_2) = (Q_{io}/2) \, . \, \{ 1 + (a/W_i)\} \qquad \text{- (A39)}$$

By combining the equations (A36), (A38) and obtaining I_c from equation (A30) an expression for 'a' can be produced. Thus:

$$a = W_i - \frac{4.D_i.Q_{io}}{W_i.[I_R - I_{co}.\exp(-3.t_2/\tau_c)]} \qquad \text{- (A40)}$$

Combining equations (A35),(A39) and (A40) an equation can be obtained which can then be solved for t_2. In this case,

$$\frac{-t_{12} - t_1}{2Q_{io}} \, . \, (I_R - 2.e.A.D_c.\tan\Theta_1) + \frac{I_R.(t_{12} - t_2)}{Q_{io}}$$

$$+ \frac{I_{co}.\tau_c}{3.Q_{io}} [\exp(-3.t_{12}/\tau_c) - \exp(-3.t_2/\tau_c)]$$

$$= \frac{-4.D_i \, . \, Q_{io}}{W_i^2.[I_R - I_{co} \exp(-3.t_2/\tau_c)]} \qquad \text{-(A41)}$$

The solution must be performed numerically. Once a solution has been obtained if 'a' is less than zero, then the triangular distribution must be used. Referring to figure 48(b), the triangular distribution has a height equal to or less than P_{io}. The stored charge at $t=t_2$ is then:

$$Q_i(t_2) = (W_i^2/8.D_i) \, . \, (I_R - I_c) \qquad \text{-(A42)}$$

Combining equation (A42) with equation (A35) produces the following.

$$Q_{io} - (I_R - 2.e.A.D_c.\tan\Theta_1) \cdot \frac{t_{12} - t_1}{2} + I_R.(t_{12} - t_2)$$

$$+ \frac{I_{co}\,\tau_c}{3}.[\exp(-3.t_{12}/\tau_c) - \exp(-3.t_2/\tau_c)]$$

$$= \frac{W_i^2}{8.D_i}.[I_R - I_{co}\exp(-3.t_2/\tau_c)] \qquad \text{-(A43)}$$

Again t_2 must be calculated numerically.

In the third stage of the diode recovery ie $t_2 \leq t \leq t_3$ the space charge layer gradually widens until occupying the entire i-region as shown in figure 48(c). The two space charge zones grow from the junctions into the i-layer. The width of these zones is measured by a space coordinate 's'. As the trapezoidal distribution shrinks it eventually becomes a triangular distribution at $t=t_{23}$. From figure A2 it can be seen.

$$Q_i(t_{23}) = \tfrac{1}{2}.Q_{io}.\{1 - (a/W_i)\} \qquad \text{-(A44)}$$

By combining equations (A35), (A40) and (A44) an equation for calculating t_{23} is produced.

$$1 - \frac{t_{12} - t_1}{2.Q_{io}}.(I_R - 2.e.A_j.D_c.\tan\Theta_1) + \frac{I_R.(t_{12} - t_{23})}{Q_{io}}$$

$$+ \frac{I_{co}.\tau_c}{3.Q_{io}}[\exp(-3.t_{12}/\tau_c) - \exp(-3.t_{23}/\tau_c)]$$

$$= \frac{2.D_i.Q_{io}}{W_i^2.[I_R - I_{co}.\exp(-3.t_2/\tau_c)]} \qquad \text{-(A45)}$$

When $Q_i(t_3) = 0$ the diode is fully recovered and $t=t_3$. Thus:

$$Q_{io} - \frac{t_{12} - t_1}{2}.(I_R - 2.e.A_j.D_c.\tan\Theta_1) + I_R.(t_{12} - t_3)$$

$$+ \frac{I_{co}.\tau_c}{3}[\exp(-3.t_{12}/\tau_c) - \exp(-3.t_3/\tau_c)] = 0 \qquad \text{- (A46)}$$

The recovery time t_3 can be calculated by solving the above equation numerically.

Finally the transition time is calculated. During this time the electric field will have exceeded its saturation value then the drift velocity, u_s, of electrons will effectively be constant. For silicon: u_s = const $\approx 2 \times 10^5$ m/s.
Therefore the transition time will be

$$(t_4 - t_3) = \tfrac{1}{2}.W_i/u_s \qquad \text{- (A47)}$$

At t= t_4 the i layer will be free from all mobile carriers and then the current flow through the device will cease.

Neglecting the voltage drop across the diode during the initial charge extraction and assuming the dominant component of volt drop is due to the establishment of space charge regions then the space charge voltage across the i-layer is given by the equation due to Shockley and Prim [235]. Thus:

$$|V| = \frac{4}{3}\sqrt{\frac{2.(I_R - I_c).s^3}{\varepsilon.A.\mu_i}} \qquad \text{- (A48)}$$

where ε is the dielectric constant and the carrier mobility μ_i is assumed to be field independent. The symbol s denotes the width of the space charge layer and is time-dependent. Thus s must be known to calculate $|V|$. Again either a trapziodal or triangular initial charge distribution (at $t=t_2$) are used to calculate 's'.

In the case of the trapezoidal distribution the increase in the amount of recovered charge is related to the increase in the width of the space-charge

zones via:

$$dQ_i = 2.e.A_j.P_{io}.ds \quad \text{- (A49)}$$

Using $dQ_i = (I_R - I_c) .dt$ - (A50)

and combining equations (A490) (A50) and I_c from equation (A30) yields.

$$\frac{2.Q_{io}}{W_i} ds = [I_R - I_{co}.\exp(-3.t/\tau_c)] dt$$

$$t_2 \leq to \leq t_{23} \quad \text{- (A51)}$$

By defining, $s(t_2) = 0$, as the boundary condition then the solution can be expressed as:

$$s = \frac{W_i}{2.Q_{io}} \{I_R.(t - t_2) + \frac{I_{co}.\tau_c}{3} .[\exp(-3.t/\tau_c) - \exp(3.t_2/\tau_c)]\}$$

$$t_2 \leq t \leq t_{23} \quad \text{- (A52)}$$

By using the expression for s the diode voltage can be calculated via equation (A48). Referring to figure A3 it can be seen that the reduction in the triangular distribution during the time period $t_{23} \leq t \leq t_3$ can be used to produce an equation linking dQ_i and ds. Thus:

$$dQ_i = \frac{2.q_{io}}{W_i.(W_i - a)} . (W_i - 2s) ds \quad \text{- (A53)}$$

Combining the above with the following

$$dQ_i = (I_R - I_c) dt$$

produces a differential equation, thus:

$$\frac{2.Q_{io}}{W_i.(W_i-a)} . (W_i - 2.s) ds = [I_R - I_{co}.\exp(-3.t/\tau_c)] dt$$

$$t_{23} \leq t \leq t_3 \quad \text{- (A54)}$$

Using the boundary equation $s(t_{23}) = a/2$, a solution for s is found. Hence:

$$s = \frac{W_i}{2} - \sqrt{\left(\frac{W_i}{2} - \frac{a}{2}\right)^2 - W_i.\frac{(W_i - a)}{2.Q_{io}}.\left\{I_R\,(t - t_{23}) + \frac{I_{co}\,\tau_c}{3}\right.}$$

$$\left. \left[\exp\,(-3.t / \tau_c) - \exp\,(-3.t_{23} / \tau_c)\right]\right\}$$

$$t_{23} \leq t \leq t_3 \qquad \text{- (A55)}$$

Thus equation (A55) can then be used to calculate $|V|$ via equation (A48). In the case when the initial charge distribution is triangular a different expression for s is called for. Referring to figure A3 it can be seen that

$$dQ_i = 4.Q_i(t_2).\{(W_i - 2.s)/W_i^2\}\ ds \qquad \text{- (A56)}$$

it then follows that

$$4.Q_i(t_2).\{(W_i - 2.s)/W_i^2\}\ ds = [I_R - I_{co}.\exp\,(-3t/\tau_c)]\ dt$$

$$t_2 \leq t \leq t_3 \qquad \text{- (A57)}$$

Using the boundary condition $s(t_2) = 0$ the solution is

$$s = \frac{W_i}{2} - \sqrt{\frac{W_i^2}{4}\left\{1 - \frac{I_R.(t - t_2) + I_{co}.\tau_{co}/3\ [\exp\,(-3.t/\tau_c)}{Q_{io} - \frac{1}{2}\,(t_{12} - t_1)(I_R - 2.e.A_j.D_c.\tan\,\Theta_1)}\right.}$$

$$\left. \frac{- \exp\,(-3t_2/\tau_c)]}{+ I_R.(t_{12} - t_2) + I_{co}.\tau_c/3\ [\exp\,(-3.t_{12}/\tau_c) - \exp(3t_2/\tau_c)]}\right\}$$

$$t_2 \leq t \leq t_3 \qquad \text{- (A58)}$$

Thus by inserting this equation for s into equation (A48) the diode voltage can be calculated.

As can be seen from the above equations the calculation of the diode voltage

is very complicated during the transition phase. However, Schunemann [91] has shown that the diode voltage rises approximately 50% from its value at t_3 until reaching t_4 and in addition this rise is nearly linear since $(t_4 - t_3) \leq t_3$.

$$\text{Thus} \quad |\, V(t) \,| \approx |\, V(t_3) \,| + \left|\, \frac{V(t_3)}{2} \,\right| . \frac{t - t_3}{t_4 - t_3} \qquad \text{-(A59)}$$

$$t_3 \leq t \leq t_4$$

Also since the residual contact-layer current has only a marginal influence on switching times and voltages I_c may be neglected. Thus simple formulae can then be used to calculate the diode voltage.

$$\text{Hence} \quad t_2 = \frac{2.D_i.Q_{io}^2}{W_i^2.I_R^2} \qquad \text{(trapezoidal distribution)} \qquad \text{-(A60)}$$

$$t_2 = \frac{Q_{io}}{I_R} - \frac{W_i^2}{8.D_i} \qquad \text{(triangular distribution)} \qquad \text{-(A61)}$$

The choice between trapezoidal and triangular distribution can be determined from the following equation

$$a = W_i - \{(4.D_i.Q_{io})/(W_i.I_R)\} > 0 \qquad \text{-(A62)}$$

and

$$t_{23} = t_2 + \{(a.Q_{io})/(W_i.I_R)\} \qquad \text{-(A63)}$$

The recovery time is approximately given by

$$t_3 \approx Q_{io}/I_R \qquad \text{-(A64)}$$

The transition time is given by

$$(t_4 - t_3) = \tfrac{1}{2}.W_i/u_s \qquad \text{-(A65)}$$

The diode voltage can then be calculated from the following,

$$|V| = \frac{4}{3}\sqrt{\frac{2.I_R.s^3}{\varepsilon.A.\mu_i}} \qquad t_2 \le t \le t_3 \qquad \text{-(A66)}$$

The space charge layer width s for a trapezoidal distribution is:

$$s(t) = \frac{W_i.I_R}{2.Q_{io}} . (t - t_2) \qquad \text{-(A67)}$$

for the time period $t_2 \le t \le t_{23}$

$$s(t) = \tfrac{1}{2}W_i - \sqrt{(\tfrac{1}{2}W_i - \tfrac{1}{2}a)^2 - \frac{W_i.(W_i - a).I_R.(t-t_{23})}{2.Q_{io}}} \qquad \text{-(A68)}$$

for the time period $t_{23} \le t \le t_3$

and for a triangular distribution is:

$$s(t) = \tfrac{1}{2}W_i - \sqrt{\frac{W_i^2}{4}\left[1 - \frac{I_R.(t - t_2)}{Q_i(t_2)}\right]} \qquad \text{-(A69)}$$

In the above case

$$Q_i(t_2) = \frac{W_i^2.I_R}{8.D_i} \qquad \text{-(A70)}$$

for additional information on the derivation of the above diode model, the reader should consult the following references: [40, 41, 50, 91, 93, 94, 95, 98].

FIGURE A1

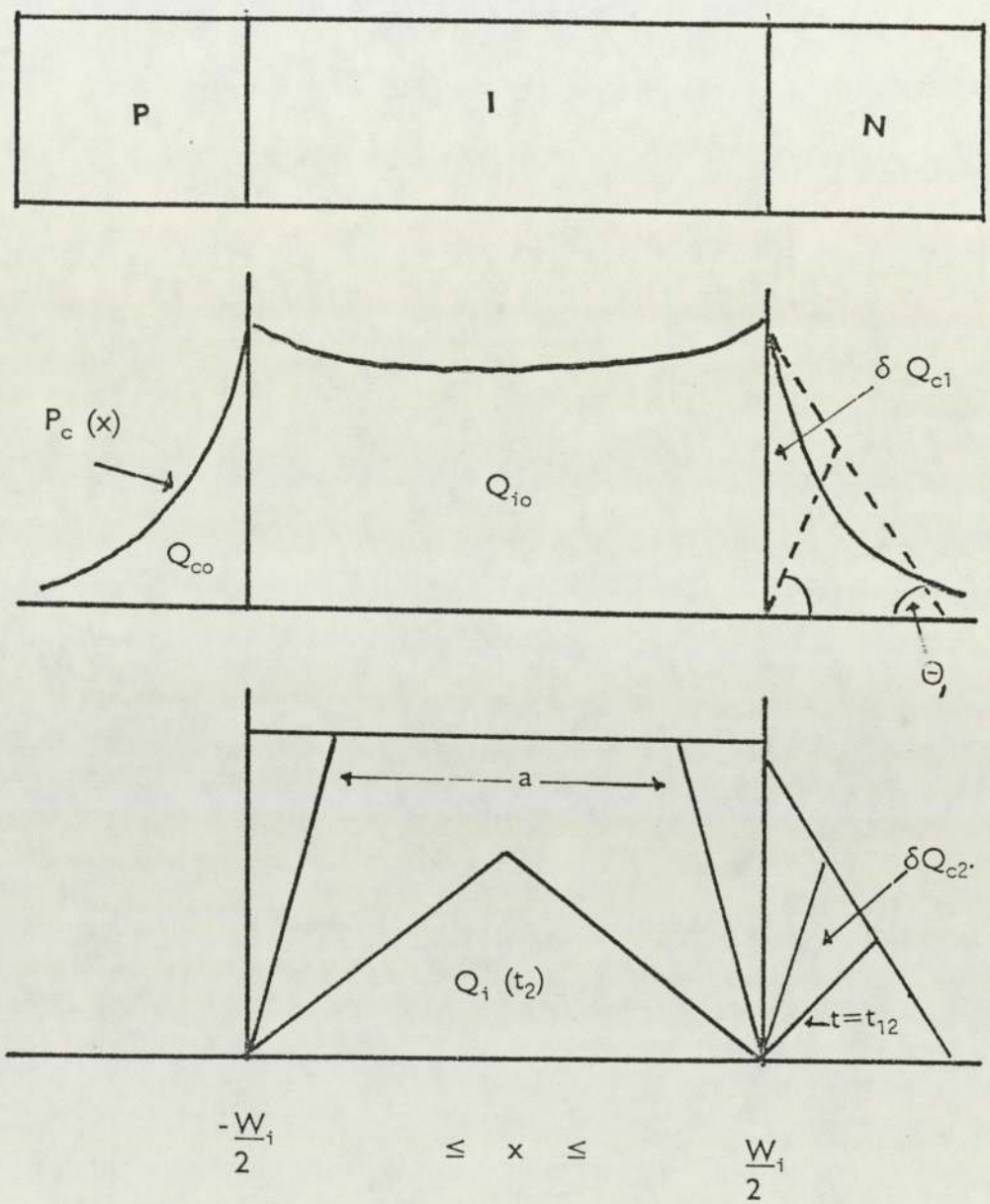
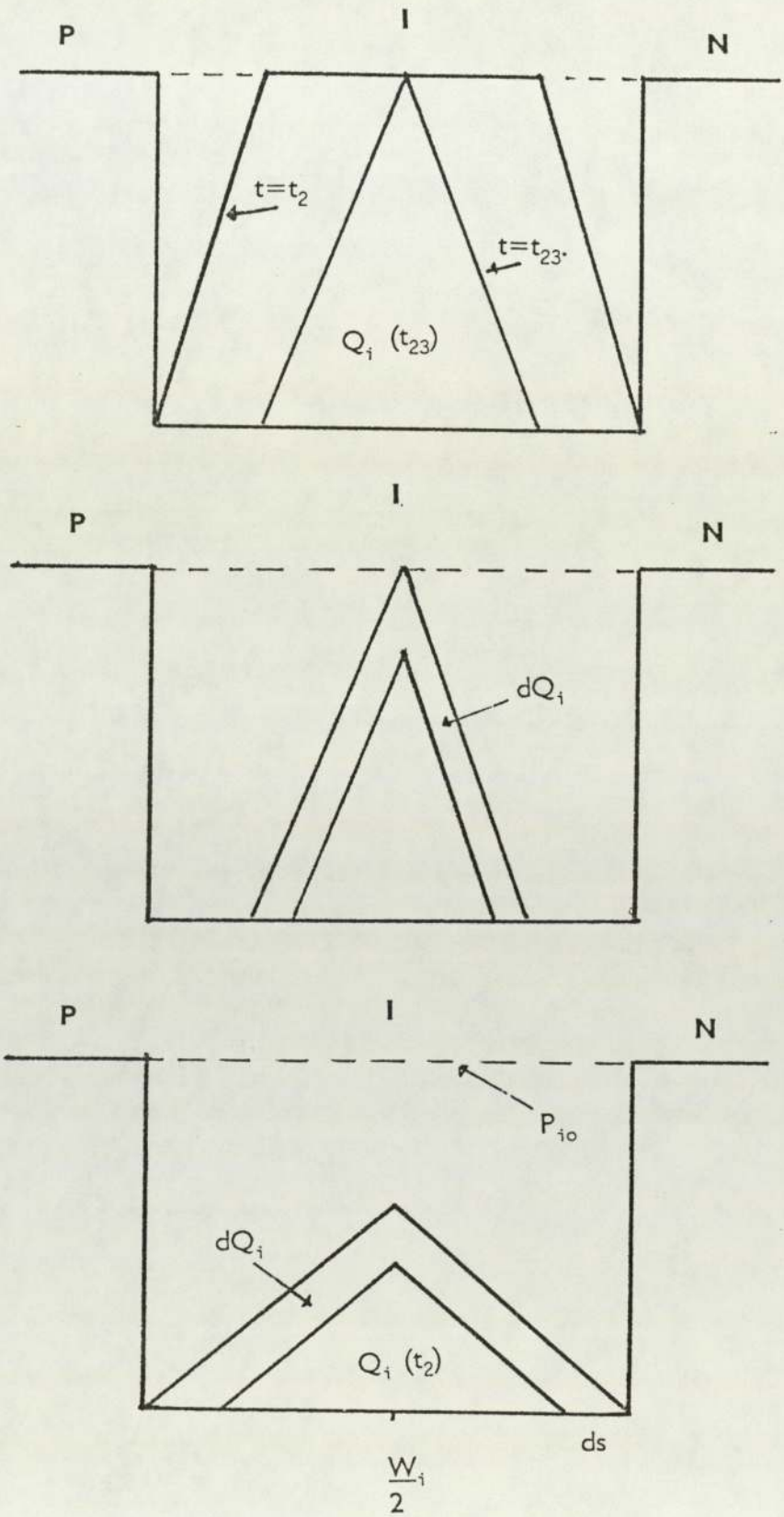

P
I
N
P_c (x)
Q_{co}
Q_{io}
δQ_{c1}
Θ_1
a
Q_i (t_2)
δQ_{c2}
$t=t_{12}$
$-\frac{W_i}{2}$ ≤ x ≤ $\frac{W_i}{2}$

FIGURE A2



APPENDIX B

LIST OF SYMBOLS

A	=	Equation (E114) constant
A_j	=	Diode junction area
A_t	=	Surface area of triangular finite element
Ä	=	Equation (E94) constant
B	=	Equation (E114) constant
C	=	Main circuit series capacitance
C_d	=	Diode Capacitance
C_{diode}	=	Steady state reverse bias diode capacitance
C_{Isol}	=	Value of isolating capacitor
C_{meas}	=	Measure value of capacitance
C^*_t	=	Average depletion layer capacitance
C_t	=	Capacitance at time t.
C_o	=	Capacitance [Farad]
Ç	=	Softness factor = V_{pkr}/V_r
D	=	Diffusion constant
D_c	=	Pin diode contact layer diffusion constant
D_i	=	Pin diode intrinsic layer diffusion constant
D_n	=	Electron diffusion constant
D_p	=	Hole diffusion constant
E	=	Energy
E_c	=	Capacitor stored energy
E_F	=	Fermi energy level
E_{TI}	=	Trap energy level
E_r	=	Residual error
F_1	=	Equation E149 function
F_2	=	Equation E149 function
F_2	=	Equation E149 function
G_o	=	Equation E94 constant
G	=	FEM example in E109

LIST OF SYMBOLS

H	=	Equation E95 constant
I	=	Current [Amperes]
I_d	=	Diode current
I_f	=	Steady state forward current
I_c	=	Pin diode contact layer current
I_R	=	Reverse current in resistive circuit
$I_c(t)$	=	Pin diode contact layer current at time t
I_{co}	=	Pin diode initial contact layer current
I_o	=	Reverse saturation current
I_F	=	Forward current in resistive circuit
I_r	=	Reverse current
I_{rm}	=	Maximum reverse current
I_f	=	Forward current
I_{pkf}	=	Peak forward current
J	=	Current density [Amperes/square metre]
J_f	=	Forward current density
J_R	=	Reverse current density
K	=	Snappiness ratio = t_a/t_b
L	=	Matrix in LU decomposition
L_c	=	Main circuit series Inductance [Henries]
L_s	=	Stray circuit inductance
L_i	=	Pin diode intrinsic layer diffusion length
L_{c*}	=	Pin diode contact layer diffusion length
M	=	Matrix notation in FEM
N	=	N - type material; predominance of electrons
N_T	=	Carrier trap concentration
N_n	=	Density of donor atoms
Ö	=	Matrix notation in FEM
P	=	P - type material; predominance of holes
P_c	=	Pin diode doping concentration at the contact layers
$P_i(x)$	=	Pin diode stationary hole concentration in intrinsic region.
$P_c(x)$	=	Pin diode stationary hole concentration in the n-contact layer.

LIST OF SYMBOLS

Q = Charge [Coulombs]

Q_d = Diode charge

Q_s = Stored charge

Q_{rr} = Recovered charge

Q_a = Recovered charge during time t_a

Q_b = Recovered charge during time t_b

Q_c = Pin diode charge in contact region

$Q(t)$ = Charge at time t

Q_{io} = Pin diode initial i-layer stored charge

Q_{co} = Pin diode initial contact layer stored charge

Q_t = Total stored charge

Q_i = Pin diode charge in intrinsic region

Q_{c1} = Pin diode contact layer recovered charge at t_1

Q_{c2} = Pin diode contact layer recovered charge at t_{12}

Q_s = Stored charge

R = Resistance [Ohms]

R_o = Recombination term

R_o = Total recombination rate

R_{SMR} = Shockley-Hall-Read recombination rate

R_{AUG} = Auger recombination rate

S = Snappiness factor = t_b/t_a

T = Absolute temperature [degrees Kelvin]

T_o = 300K

R_m = Matrix

R^T = Transpose of matrix R_m

U = Electric potential [Volts]

V = Electric potential [Volts]

V_{bo} = Breakover Voltage

V_a = Anode voltage

V_{ch} = Initial capacitor voltage

V_D = Contact voltage

V_d = Diode voltage drop

V_{pkr} = Peak reverse recovery voltage

LIST OF SYMBOLS

V_F = Forward voltage

V_m = Maximum voltage withstand

V_r = Reverse recovery voltage

W = Base width [Metres]

W = Depletion layer width

W_i = Pin diode intrinsic layer width

X = Global co-ordinate in FEM

X_o = Equation E80 variable

Y_o = Equation E81 variable

Y = Global co-ordinate in FEM

Z = Global co-ordinate in FEM

Z_o = Equation E95 constant

ä = Polynomial constant in FEM (equation E112)

a = Pin diode variable

b = Polynomial constant in FEM (equation E112)

c_o = Straight line equation constant

c = Polynomial constant in FEM (equation E112)

c_i = Intrinsic carrier concentration

c_n = Auger electon recombination constant

c_{n1} = Electron capture rate for gold energy level 1

c_{p1} = Hole capture rate for gold energy level 1

d = base width

d = Base width

e = Electron charge

g = FEM example in E109

i = Intrinsic material

i_c = Capacitive current

i_n = Current due to flow of electrons

j = current density

k = Boltzmann's constant

m_o = Gradient of a curve

m_e = Mass of electron

LIST OF SYMBOLS

n	=	Number of electrons
n_i	=	Intrinsic carrier concentration
n_o	=	Equilibrium electron concentration
p	=	Hole concentration
p_o	=	Equilibrium hole concentration
p_1	=	Hole concentration if $E_F = E_{t1}$
q	=	Unit charge
s	=	Pin diode equation variable
t	=	Time [Seconds]
t_a	=	Time from current zero to I_{rm}
t_b	=	Time from I_{rm} to second current zero
t_{rr}	=	Diode recovery time
t_s	=	Diode storage time (time from current zero to junction volt reversal)
v	=	Pin diode equation variable
v_e	=	electron velocity
x	=	local co-ordinate in FEM
y	=	Local co-ordinate in FEM
z	=	Local co-ordinate in FEM
α_1	=	Pin diode linearized carrier concentration angle
α_2	=	Pin diode linearized carrier concentration angle
β	=	Proportionality constant between voltage and capacitance
Γ	=	$\beta^2/\varepsilon.A_j$
Θ	=	Equation E93 constant
Φ	=	$L_c.\beta_2/\varepsilon.A_j$
ϕ	=	Quasi-fermi level
ϕ_n	=	Electron quasi-fermi level
ϕ_p	=	Hole quasi-fermi level
Ω	=	Matrix element
μ	=	Mobility constant
μ_{cc}	=	Carrier - carrier scattering mobility constant
μ_n	=	Effective electron mobility
μ_p	=	Effective hole mobility
μ_i	=	Carrier mobility in intrinsic region of pin diode

LIST OF SYMBOLS

μ_{ii} = Ionised impurity mobility constant

μ_T = Lattice mobility constant

μ_o = Lattice mobility at 300K

$¥$ = Electrostatic potential

τ = Carrier lifetime

τ_i = Pin diode intrinsic layer carrier lifetime

τ_c = Pin diode contact layer carrier lifetime

τ_n = Electron lifetime

τ_p = Hole lifetime