Short-Circuit and Ground Fault Analysis and Location in VSC-Based DC Network Cables

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Abstract—The application of high-power voltage-source converters (VSCs) to multiterminal dc networks is attracting research interest. The development of VSC-based dc networks is constrained by the lack of operational experience, the immaturity of appropriate protective devices and the lack of appropriate fault analysis techniques. VSCs are vulnerable to dc cable short-circuits and ground faults due to the high discharge current from the dc-link capacitance. However, faults occurring along the interconnecting dc cables are most likely to threaten system operation. In this paper, cable faults in VSC-based dc networks are analyzed in detail with the identification and definition of the most serious stages of the fault that need to be avoided. A fault location method is proposed because this is a prerequisite for effective design of a fault protection scheme. It is demonstrated that it is relatively easy to evaluate the distance to a short-circuit fault using voltage reference comparison. For the more difficult challenge of locating ground faults, a method of estimating both the ground resistance and the distance to the fault is proposed by analyzing the initial stage of the fault transient. Analysis of the proposed method is provided and is based on simulation results, with a range of fault resistances, distances and operational conditions considered.

Index Terms—Fault analysis, fault location, voltage-source converter (VSC), multiterminal dc network.

I. INTRODUCTION

FAULT vulnerability and protection are significant issues that constrain the development of voltage-source converter (VSC) based dc networks, especially in high-power scenarios. This is primarily due to the lack of mature commercial dc switchgear products. However, VSC-based high-voltage direct current (HVDC) power transmission is attracting more research interest as it provides greater operational flexibility which suits renewable energy sources. One typical application of VSC-HVDC is for large-scale offshore wind farm integration to onshore utility grids [1]-[3] where a reliable dc network is a prerequisite.

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Cable faults do occur more frequently compared with other parts of the system. The most common reason for a cable fault is insulation deterioration and breakdown. There can be several causes [4]: physical damage, environmental stresses, electrical stresses, and cable aging. There have been discussions about the influence of dc faults on dc networks at transmission and distribution levels. The following aspects regarding dc system fault analysis have been reported:

1) *Line-commutated, Current-Source Converter HVDC Systems*: HVDC transmission systems based on conventional line-commutated current-source converters (CSC) are robust to dc fault overcurrents because of their current-regulated nature [5]. The overvoltage phenomenon of this CSC-HVDC system has been discussed [6]-[8]. Recently, HVDC protection research has been focused on specific cable fault location approaches. Protection coordination is seldom studied because of the lack of development in multiterminal dc networks.

2) *Cable Fault Location Techniques*: At the current time, cable fault location research is primarily focused on offline techniques [9]-[13]. Techniques widely used in industry are trace methods using acoustic or electromagnetic approaches [9] which are time-consuming. Traveling wave based methods have also been researched using different algorithms [10]-[13]. However, when the system structure is complex (for example, meshed for multiterminal connection) many reflections occur which will influence location results. A detailed cable model is required for accurate fault location using the transient response to a high-frequency pulse. For ac network and line-commutated CSC-HVDC, these methods are adequate because fast fault location may not be critical. However, for VSC-based systems, a fast and accurate fault location is required for effective operation of protective devices [14].

3) *VSCs with AC-Side Faults*: VSCs are widely used as rectifiers or inverters for electrical power conversion. If each conversion element of a dc wind farm is a VSC, it can control both active power and reactive power. The VSC control can cope with grid-side ac disturbances, during which appropriate control and protection methods can be used to protect its power electronic devices [15], [16]. The short-circuit current contribution of VSC-HVDC systems for ac system faults are also analyzed in respect of ac system protection [17].

4) *VSC Internal Faults*: In terms of fault-tolerant VSCs, the research aims are to protect the system from possible IGBT faults (for example, short-circuits) where there are many opportunities to allocate backup function or include redundant devices [18]-[20].

5) *VSC System DC Faults*: In terms of dc network faults, with parallel-connected VSCs, severe overcurrents due to discharge of the dc-link capacitances are a major issue: the converters' power electronic devices, particularly the freewheel diodes, are subject to overcurrents. Therefore, the converter is defenseless against dc side faults, such as a dc-link short-circuit, dc cable short-circuits and dc cable ground faults. These fault conditions need to be analyzed and simulated in detail for effective protection system prior to the development of practical high-power VSC-HVDC networks. Relevant works are now summarized:

5.1) *VSC-Based DC Distribution Systems*: For dc distribution networks with VSCs, the following research has been reported: a) fault simulation of a dc micro-grid and switchgear / fuse allocation [21]; b) fault analysis of a VSC-based dc distribution system for a shipboard application [22], [23] - by replacing diodes with controllable gate power-electronic devices to provide bidirectional current blocking function; c) dedicated discharge overcurrent protection for dc-link capacitors [23], [24].

5.2) *VSC-HVDC Systems*: Fault detection and location for meshed VSC-HVDC systems is discussed in [25], [26] at the transmission level. The technique in [25] extracts the fault signature by comparing initial current change, the current rise time interval, or current oscillation pattern at different switch locations. Based on that, [26] proposes a fault location and isolation method. This relies on ac-side circuit breakers (CBs), and no dc switchgear configuration is discussed due to cost considerations. VSC-HVDC cable overvoltage protection under line-to-ground faults is analyzed in [27]. However, the protection scheme is not designed specifically for overcurrents flowing through power electronic devices, which are the most vulnerable devices of the system.

5.3) *Summary*: Most of the research reported on dc fault analysis with VSC configurations are based on numerical simulations without a theoretical basis through circuit analysis. The speed requirement for dc CBs can only be configured after identifying critical time limits under various fault conditions. AC-side switchgear is not considered fast enough to cope with the rapid rise of fault current characteristic of freewheel diode conduction which can damage power electronic devices in several milliseconds. In addition, most work focuses on the dc short-circuit faults at the dc rails [23]. However, a cable short-circuit fault is potentially more common than a dc rail fault and the impact of a dc fault on the freewheel diodes in the VSC can be worse than that of a direct dc rail short circuit due to the increased inductive component in the discharge path. Although underground cables are seldom short-circuited in comparison to overhead lines, it is a critical condition and needs to be analyzed particularly for switchgear relay and protection design. In contrast, ground faults are more common but less serious. However, accurate fault location for effective protection coordination is required for high-impedance ground faults.

In this paper, theoretical analysis of VSC cable fault is performed. From definition of the stages of this nonlinear system under different fault conditions, critical stages are
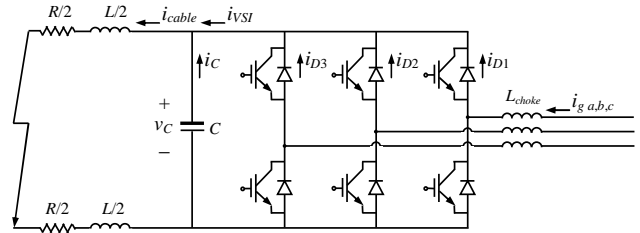

Fig. 1. Voltage-source converter with cable short-circuit fault condition.

identified to instruct effective fault location. Even for a multiterminal dc network with loops, the VSCs are parallel-connected through different cable routes. Therefore, in terms of the equivalent circuit, the fault analysis detailed here could be applied to a complex multiterminal VSC-HVDC system. A decision-based fault location method is proposed for radial dc system protection and relay coordination without the need for accurate fault distances [28]. However, in a meshed dc network, an accurate distance evaluation result is required for coordination among the dc bus connected power-electronic CBs, especially for economical, unidirectional blocking CBs. Therefore, a location method based on the circuit analysis of the first stage is proposed for distance calculation.

Furthermore, the proposed fault location approach is tested under different fault conditions. The large capacitive discharge through the dc cable is a low frequency response which does not require a detailed frequency dependent cable model. Errors in fault distance estimation and resistance evaluation are provided. An iterative calculation is applied to reduce numerical solving errors and improve the distance estimate.

The paper is organized as follows. In Section II, the dc cable short-circuit and ground faults are analyzed in terms of nonlinear system stages. Fault overcurrent and voltage collapse expressions are given as the basis for fault location in Section III. Selected PSCAD/EMTDC simulations are provided in Section IV for fault location verification.

II. VSC DC Cable Fault Analysis

This section analyzes cable short-circuit and positive-to-ground faults in VSC-based dc systems. According to circuit theory, dc bus faults are the same as dc cable faults and different in protection coordination strategy merely because of possible complex structured multiterminal connection. The theoretical solution of the nonlinear system that represents the faulted network can be defined by different stages which assist in understanding system response. The characteristics of the dc fault current response are analyzed for accurate fault location.

A. VSC DC Cable Short-Circuit Fault Analysis

A dc short-circuit fault is the most serious condition for VSCs. The IGBTs can be blocked for self-protection during faults, leaving reverse diodes exposed to overcurrent. Regardless of where the dc cable short-circuit occurs, it can be expressed by an equivalent circuit shown in Fig. 1, where R and L are the π-model equivalent resistance and inductance of the positive and negative cables from the VSC to the location of the short-circuit. The cable grounding capacitor is omitted here which is dominated by

the dc-link capacitance. Multilevel VSCs are especially promising for high-power conversion applications, such as diode neutral-point-clamp converters and flying capacitor converters [29], [30]. The main fault characteristics are in common with the two-level converter in Fig. 1: a closed loop via the freewheel diodes is available for capacitance discharge. Therefore the treatment of these multilevel converters is similar to the 2-level system analyzed here. In the multilevel modular converter (MMC), the large dc-link capacitance is replaced with low-value cascaded capacitors. Therefore it is different to the analysis proposed here. With appropriate fault control methods for the converter switches, the MMC can be tolerant to dc fault conditions.

To solve the complete response of this nonlinear circuit, the different stages of the fault, as it progresses, are analyzed individually. Expressions for the dc-link voltage and cable current are provided.

1) Capacitor Discharge Stage (Natural Response):

This stage occurs as the dc-link capacitor discharges and the equivalent circuit represented in Fig. 2(a). Under the condition $R < 2\sqrt{L/C}$, the solution of the second-order circuit natural response gives an oscillation. Assuming the fault happens at time t_0, the natural response (without inverter-side current i_{VSI}) under the initial conditions of $v_C(t_0) = V_0$, $i_{cable}(t_0) = I_0$ is

$$v_C = \frac{V_0 \omega_0}{\omega} e^{-\delta t} \sin(\omega t + \beta) - \frac{I_0}{\omega C} e^{-\delta t} \sin \omega t \tag{1}$$

$$i_{cable} = C \frac{dv_C}{dt} = -\frac{I_0 \omega_0}{\omega} e^{-\delta t} \sin(\omega t - \beta) + \frac{V_0}{\omega L} e^{-\delta t} \sin \omega t \tag{2}$$

where

$\delta = R/2L$, $\omega^2 = 1/LC - (R/2L)^2$, $\omega_0 = \sqrt{\delta^2 + \omega^2}$, $\beta = \arctan(\omega/\delta)$.

The time when capacitor voltage drops to zero is

$$t_1 = t_0 + (\pi - \gamma)/\omega \tag{3}$$

where $\gamma = \arctan[(V_0 \omega_0 C \sin \beta)/(V_0 \omega_0 C \cos \beta - I_0)]$.

2) Diode Freewheel Stage (after $v_C = 0$, Natural Response):

This stage is initiated as the cable current commutates to the VSI freewheel diodes when the dc-link voltage reaches zero and the cable inductance drives current around the freewheel path. It is solved using the first-order equivalent circuit, Fig. 2(b). The cable current has an initial value $i_{cable}(t_1) = I'_0$. The expression of cable inductor current, where each phase-leg freewheel diode current carries a third of the current, is

$$i_{cable} = I'_0 e^{-(R/L)t}, \quad i_{D1} = i_{cable}/3. \tag{4}$$

This is the most challenging phase for VSI freewheel diodes, because the freewheel overcurrent is abrupt with a high initial value, which can rapidly damage the diodes. t_2 is the time of the pure inductor discharge of one phase before current is fed from the grid-side, see Fig. 3 phase-c.

3) Grid Side Current Feeding Stage (Forced Response):

During this stage, the dc-link capacitor and cable inductor have a forced current source response (with i_{VSI} when the VSC IGBT gate control signals are blocked, v_C is not necessarily zero) shown in Fig. 2(c). To calculate the fault current contribution from the inverter, a three-phase short circuit current expression is obtained by three-phase short circuit
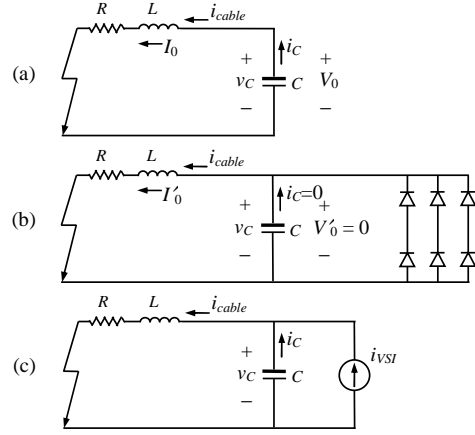

Fig. 2. Equivalent circuit for VSI cable short circuit fault: (a) stage 1 – capacitor discharge; (b) stage 2 – diode freewheel; (c) stage 3 – grid current feeding.

analysis. For phase a, assume the grid voltage post-fault is

$$v_{ga} = V_g \sin(\omega_s t + \alpha) \tag{5}$$

where V_g is the grid voltage amplitude, ω_s is the synchronous angular frequency, α is the phase a voltage angle at t_1. The phase current is

$$i_{ga} = I_g \sin(\omega_s t + \alpha - \varphi) + [I_{g|0|} \sin(\alpha - \varphi_0) - I_g \sin(\alpha - \varphi)]e^{-t/\tau} \tag{6}$$
$$= I_g \sin(\omega_s t + \alpha - \varphi) + I_{gn} e^{-t/\tau}$$

where $\varphi = \arctan[\omega_s(L_{choke} + L)/R]$, $\tau = (L_{choke} + L)/R$, $I_{g|0|}$ and φ_0 are the initial grid current amplitude and phase angle, L_{choke} is the grid side choke inductance.

The positive i_{ga} current flows from diode D_1 to contribute to the i_{VSI}, with those of i_{gb} and i_{gc}, so the total i_{VSI} is the summation of the positive three phase short circuit currents.

$$i_{VSI} = i_{D1} + i_{D2} + i_{D3} = i_{ga,(>0)} + i_{gb,(>0)} + i_{gc,(>0)}. \tag{7}$$

Here only the phase-a part $i_{ga,(>0)}$ response is analyzed, phase b and c can be superimposed afterwards. To analyze the most serious condition, the phase that has the highest current magnitude (phase a in this case), with grid voltage angle zero at the initiation of this stage of the fault. The cable currents are solved as

$$i_{cable} = A\sin(\omega_s t + \gamma) + Be^{-t/\tau} + [C_1 \omega_0 e^{-\delta t} \sin(\omega t + \beta)]/\omega + (C_2 e^{-\delta t} \sin \omega t)/\omega \tag{8}$$

$$v_C = Ri_{cable} + L\frac{di_{cable}}{dt} \tag{9}$$

where $A = I_g[(1 - \omega_s^2 LC)^2 + (RC\omega_s)^2]^{-1/2}$, $\gamma = \alpha - \varphi - \theta$, $\theta = \arctan[(RC\omega_s)/(1 - \omega_s^2 LC)]$, $B = I_{gn}[\tau^2/(\tau^2 - RC\tau + LC)]$, $C_1 = -(A\sin\gamma + B)$, $C_2 = B/\tau - \omega_s A\cos\gamma$.

The above analysis is verified by PSCAD/EMTDC simulations. The simulation system including a vector controlled SPWM-VSI and π-model dc cables. Simulation system parameters, initial values, and calculated stage times are listed in Table I. Fig. 3 shows the PSCAD/EMTDC simulation results. The peak overcurrent occurs during stage 1 with the most severe freewheel diode overcurrent at the start of stage 2.
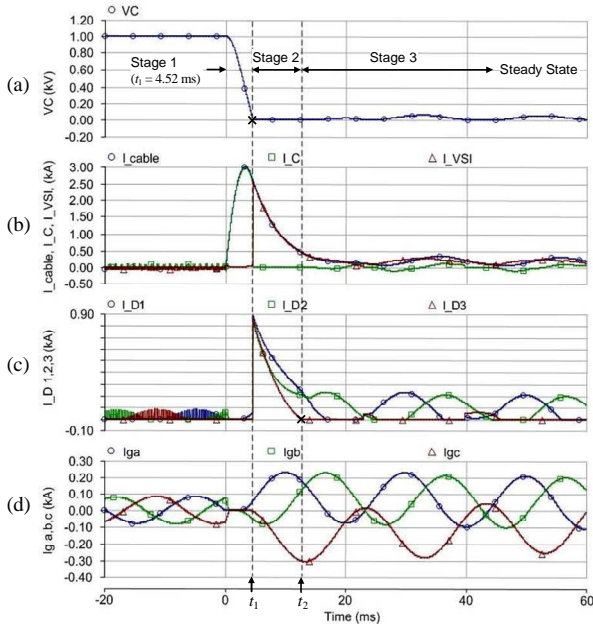
Fig. 3. VSC cable short circuit fault and stage definition: (a) dc-link capacitor voltage v_C (kV); (b) cable current i_{cable} (kA), capacitor current i_C (kA), VSI feeding current i_{VSI} (kA); (c) three-phase diode current $i_{D\ 1,2,3}$ (kA); (d) grid side three-phase currents $i_{g\ a,b,c}$ (kA).
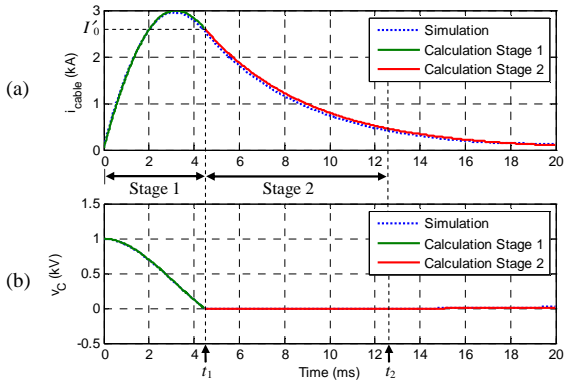

Fig. 4. Calculation and simulation comparison: (a) cable inductor current i_{cable}(kA); (b) DC-link capacitor voltage v_C(kV).

TABLE I SIMULATION PARAMETERS AND CALCULATED INITIAL VALUES AND TIMES FOR A SHORT-CIRCUIT FAULT

Simulation system parameters	Initial values	Times
$R = 0.12\ \Omega$	$V_0 = 1.0$ kV (DC)	$t_0 = 0$ s
$L = 0.56$ mH	$I_0 = $ -0.063 kA (DC)	$t_1 = 4.52$ ms
$C = 10$ mF	$I'_0 = 2.585$ kA (DC)	$t_2 = 12.61$ ms
$R = 0.12 < 2\sqrt{\dfrac{L}{C}} = 0.473$	$V_g = 0.392$ kV (AC)	
	$|Z| = |R + j\omega(L_{choke}+L)| = 2.691$	
$L_{choke} = 8$ mH	$I_g = 0.392/2.691 = 0.146$ kA	

The first two stages of the fault analyzed above are shown in Fig. 4 and compare the simulation and calculation results. The first wave front happens during stage 1 and the freewheel effect happens at the beginning of stage 2, which has the biggest impact on the system. From Fig. 4 the simulation results and the analytical calculations are identical.

The most vulnerable component – the freewheel diodes – suffer during the freewheel phase, in which the current in this
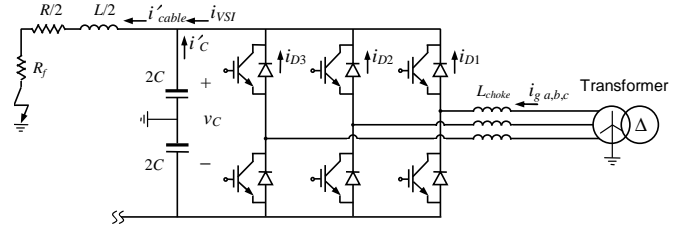

Fig. 5. Voltage source converter with positive cable ground fault condition.

model can be 10 times the nominal value (from 0.085 kA to 0.862 kA) and rises rapidly. The capacitor delivers the discharge current. This current could be eliminated by including a dedicated dc capacitor CB [23], adding capacitor overcurrent protection [24], or using high-speed fuses as for distribution system capacitor banks [31]. The dc cables should be protected from overcurrent but they are more robust than the power electronic devices due to the cable's thermal mass.

4) Influence of Fault Resistance:

Usually, the fault resistance is such that $R < 2\sqrt{L/C}$, where the circuit will experience oscillation. In cases of short-circuit faults, fault resistances are generally small. Sometimes however a fault resistance exists and a large fault resistance R_f will make the condition $R_f + R > 2\sqrt{L/C}$. This is a first order damped process. The dc-link voltage will not drop to zero, so no freewheel diode conduction occurs. Hence the most critical phase can sometimes be avoided. The overcurrent protection relay time setting is not that critical in this case. The damped fault response will be shown with the cable ground fault scenario in which the ground resistance is always considerable.

B. VSC DC Cable Ground Fault Analysis

The ground fault analysis depends on the grounding of the dc system. Usually, the grounding points in a dc network include: the neutral-ground link of the step-up transformer and the dc-link mid-point [22], [32], as shown in Fig. 5. The dc-link grounding point is used to reduce imbalance between the positive and negative currents and voltages.

A ground fault will form a ground loop with the grounding points. The IGBT-blocked-VSI will act like an uncontrolled rectifier with the dc-link voltage modified to the rectified voltage, so fault current will flow through the freewheel diodes. This current depends on the impedance between the transformer and the ground fault point. The difference between faults on the positive and negative side of the dc-link is the direction of current and the bridge diodes that conduct. The ground fault resistance cannot be ignored – it usually varies from smaller than ohms to hundreds of ohms. The equivalent circuit is shown in Fig. 6 for the fault calculation, which is divided into three stages.

1) Capacitor Discharge Stage (Natural Response):

This is the dc-link capacitor discharging stage as represented by Fig. 6(a). Under the condition of $R_f + R/2 < 2\sqrt{L/4C}$, the solution of the second-order circuit natural response gives a non-oscillating discharge process. The dc-link voltage will not
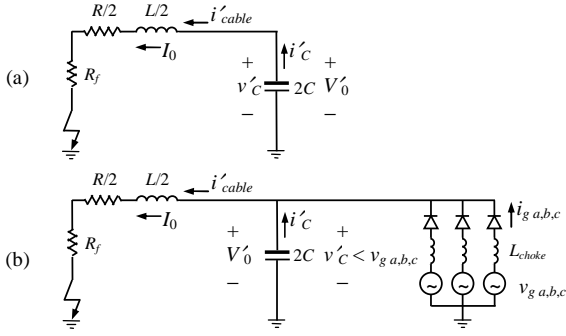
Fig. 6. Equivalent circuit for VSI cable ground fault: (a) stage 1 – capacitor discharge; (b) stage 2 – grid current feeding.

drop to zero so no freewheel diode conduction occurs. Assume the fault happens at time t_0, the natural response (without inverter side current i_{VSI}) under initial conditions of $v'_C(t_0) = V_0$, $i'_{cable}(t_0) = I_0$ are

$$v'_C = A_1 e^{p_1 t} + A_2 e^{p_2 t} \qquad (10)$$

$$i'_{cable} = 2C \frac{dv'_C}{dt} = A_1 p_1 e^{p_1 t} + A_2 p_2 e^{p_2 t} \qquad (11)$$

where $p_{1,2} = -\dfrac{R_f + R/2}{L} \pm \sqrt{\left(\dfrac{R_f + R/2}{L}\right)^2 - \dfrac{1}{LC}}$,

$A_1 = \dfrac{1}{p_2 - p_1}\left(p_2 V_0 + \dfrac{I_0}{2C}\right)$, $A_2 = \dfrac{1}{p_2 - p_1}\left(-p_1 V_0 - \dfrac{I_0}{2C}\right)$.

This stage is an *RLC* circuit until the positive dc voltage drops to below any grid phase voltage. It is difficult to determine an analytical expression for the time t_1 when capacitor voltage drops below any grid phase voltage but numerical methods can be used to find the time solution.

2) Grid Side Current Feeding Stage (Forced Response):

This transient phase can be expressed by third-order state-space equations

$$\begin{pmatrix} \dot{v}'_C \\ \dot{i}'_{cable} \\ \dot{i}_{L_{choke}} \end{pmatrix} = \begin{pmatrix} 0 & -\dfrac{1}{2C} & \dfrac{1}{2C} \\ \dfrac{1}{L/2} & -\dfrac{R_f + R/2}{L/2} & 0 \\ -\dfrac{1}{L_{choke}} & 0 & 0 \end{pmatrix} \begin{pmatrix} v'_C \\ i'_{cable} \\ i_{L_{choke}} \end{pmatrix} + \begin{pmatrix} 0 \\ 0 \\ 1/L_{choke} \end{pmatrix} v_{g\,a,b,c} \qquad (12)$$

where v'_C, i'_{cable}, and $i_{L_{choke}}$ are the state variables. The choke inductance can also include the transformer and its star-grounding inductance in case of an arc-distinguishing coil connected in low or medium voltage situations. Equation (12) provides a theoretical method of determining the short-circuit fault response. However, it is difficult to derive analytical expressions for the voltages and currents during the fault so it is numerically simulated. There are no particular effects on the diodes (unlike the freewheel phase during short-circuits). The capacitor voltage drops to a new steady state in 30 milliseconds; meanwhile the inductor current experiences a large transient of 0.8 kA (11 times rated current), Fig. 7(a).

It cannot be solved continuously because of commutation between diodes. Therefore, for each diode conduction period, the status equations of (12) need to be solved using the previous variable as the initial state for the present calculation.

3) Steady State:

The steady-state equations can be determined. The total impedance is

$$Z = (R_f + R + j\omega_s L)\|(1/j\omega_s C) + j\omega_s L_{choke} = |Z|\angle\theta' \qquad (13)$$

Then the current through diode is

$$i_{D1} = i_{ga,(>0)} = \frac{V_g\angle\alpha}{|Z|\angle\theta'} = \frac{V_g}{|Z|}\angle\alpha - \theta'. \qquad (14)$$

Simulation results are shown in Fig. 7. System parameters and calculation results are shown in Table II. In simulation, it is assumed that the dc power source is tripped immediately after the fault to avoid a dc-link capacitor overvoltage on the negative side. Each phase diode conducts when the dc voltage drops below its phase voltage, shown as an "✕" along the dc voltage in Fig. 7. The diode current during the transient state peaks at 0.185 kA, Fig. 7, about twice rated current magnitude. The steady-state amplitude is 0.1661 kA, which is slightly lower than the maximum.
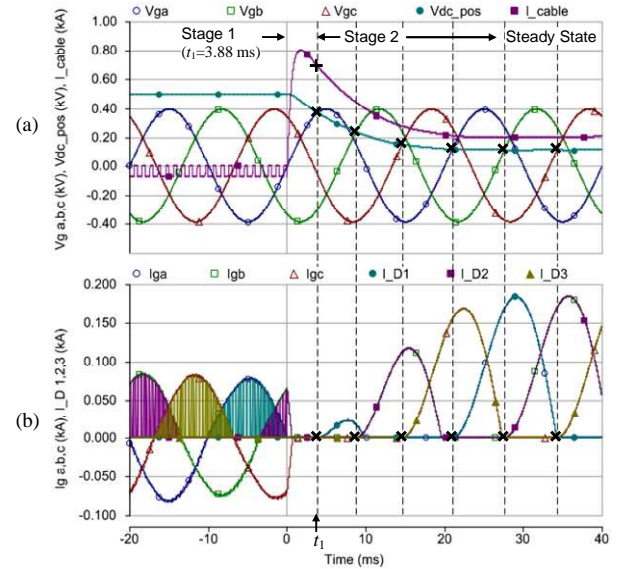

Fig. 7. VSC cable ground fault and stage definition: (a) grid three-phase voltages $v_{g\,a,b,c}$ (kV), dc-link positive voltage v_{dc_pos} (kV), cable current i_{cable} (kA); (b) grid three-phase currents $i_{g\,a,b,c}$ (kA), three-phase diode current $i_{D\,1,2,3}$ (kA).

TABLE II SIMULATION PARAMETERS AND CALCULATION FOR GROUND FAULT

Simulation system parameters	Initial / Calculation values	Times
$R/2 = 0.06\,\Omega$, $R_f = 0.5\,\Omega$	$V_0 = 0.5$ kV (DC)	$t_0 = 0$ s
$L/2 = 0.28$ mH	$I_0 = -0.063$ kA (DC)	$t_1 = 3.88$ ms
$2C = 20$ mF	$V_g = 0.392$ kV (AC)	
$R_f + R/2 = 0.56 > 2\sqrt{L/4C} = 0.237$	$Z = 2.36\angle 88.96°$	
$L_{choke} = 8$ mH	$I_g = 0.1661$ kA (AC)	

For the fault analysis, other components in practical application should be considered in the analysis. For example, the capacitor protection itself – such as a snubber acting as a current limiter [22] can be included. If required, the ac grid impedance can also be combined with the choke inductance. The oscillation and damping calculations from the analysis described are still applicable.

III. DC FAULT LOCATION

Traditional ac network distance protection uses impedance to represent the distance from the relay point to fault point. The distance judgment is made with a mho characteristic or an impedance circle. However, for a dc system in fault transient state, the frequency changes abruptly. No grid fundamental frequency impedance can be defined for distance protection. Therefore, electrical circuit parameter evaluation can be used to represent fault distance. Online fault location methods for short-circuit and ground faults will be proposed based on the analysis in Section II.

A. Short-Circuit Fault Location

System short-circuit response is featured by distance characteristics of overcurrent value and critical time for the freewheel effect. This critical time limit is when the dc-link voltage drops to zero and the freewheel diodes conduct, assuming that there is no dedicated or effective dc-link capacitor protection to prevent the discharge. This critical time should be the upper limit before which both the main and the backup dc circuit breakers operate. Using equation (3), in respect of the distance x, the critical time is

$$t_c = t_1 - t_0 = \left[\pi - \arctan\left(V_0 C \omega' / (V_0 C \delta - I_0)\right)\right] / \omega' \quad (15)$$

where $\omega' = \sqrt{\omega_0^2 / x - \delta^2}$. $\quad (16)$

The total freewheel overcurrent is the cable current at this critical time. The critical freewheel current and time in respect to distance are shown in Fig. 8. The critical time is the strict upper limit for the time allowed for the switchgear to operate. The current–distance curve in Fig. 8(a) can be used for relay configuration. As distance increases the fault overcurrent reduces and the critical time increases.

Because of the small critical time available, a rapid fault location method for short-circuit faults is required. In [28] a method using one more reference voltage sensor to avoid distant communication requirement is proposed. Two dc voltage dividers are used for distance measurement and representation. The measurements and distance relationship are illustrated in Fig. 9. The fault voltage at switchgear relay point (n) is:

$$v_{(n)} = v_{(flt)} + x^* r i_{(n)} + x^* l \frac{di_{(n)}}{dt} = R_f i_{(flt)} + x^* \left(r i_{(n)} + l \frac{di_{(n)}}{dt} \right) (17)$$

where x^* is the real fault distance, R_f is the fault resistance.

Another relay voltage sensor unit (r) is used as reference for the relative voltage calculation; it is located near the main relay point on the same section of cable, as shown in Fig. 8, to avoid communications over distance. The measured value using voltage dividers are $v_{m(n)} = k_v v_{(n)}$, $v_{m(r)} = k_v v_{(r)}$, where k_v is the voltage divider ratio. The distance between them is known, d, so the fault distance measured from this reference is

$$x = \frac{v_{(n)}}{v_{(n)} - v_{(r)}} d = \frac{v_{m(n)}}{v_{m(n)} - v_{m(r)}} d \quad (18)$$

where

$$v_{(n)} - v_{(r)} = d \left(r i_{(n)} + l \frac{di_{(n)}}{dt} \right). \quad (19)$$

For metallic grounding or short-circuit fault, $v_{(flt)} = R_f i_{(flt)} = 0$,

so the cable impedance is in proportion to distance, and measured distance $x = x^*$. For high resistance faults, which are more common in ground faults, the existence of R_f and difference between $i_{(flt)}$ and $i_{(n)}$ make the evaluation of x^* difficult. Equation (19) presents the real voltage drop between the two relay points, which reflects the real voltage drop excluding the influence of $R_f i_{(flt)}$. However, R_f still can not be exactly obtained even with the source side tripped, i.e. $i_{(flt)} = i_{(n)}$. Usually, this kind of fault is not as serious as the metallic grounding or short-circuit, so may not require fast time-response protection and which can be fulfilled by overcurrent setting. [28] proposes a method to estimate the cable distance without accurate fault resistance (the fault resistance is equivalent to another length of cable under fault) by considering the backup configuration. In the following section, a more accurate online ground distance evaluation method is proposed.
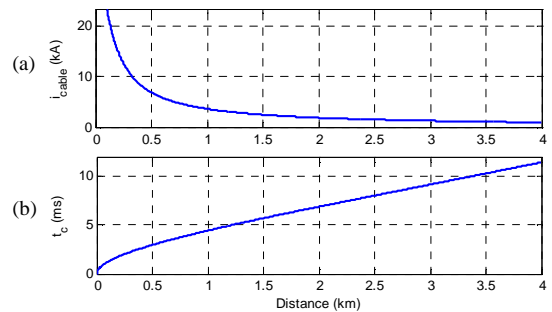

Fig. 8. Influence of short-circuit fault distance on the system performance: (a) initial freewheel current according to the fault distance; (b) variation of time for the dc-link voltage to collapse with distance.
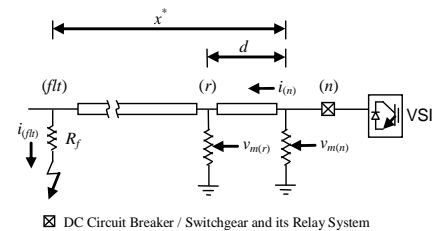

⊠ DC Circuit Breaker / Switchgear and its Relay System

Fig. 9. Distance evaluation with two voltage divider measurements.

B. Ground Fault Location and Ground Resistance Evaluation

In three-phase ac systems, distance protection uses symmetrical component analysis to avoid the above influence of fault resistance [5]. However, in dc systems this is not available. Ground faults are not as serious as short-circuit condition as the grounding is always with a large fault resistance; however, they occur more frequently. Moreover, the large fault resistance results in inaccurate evaluation of distance for protection coordination. Generally, as resistance and distance increases the fault overcurrent reduces and the time the diodes start conducting increases.

Based on the above analysis, a new fault location approach for distance and ground resistance evaluation is proposed here for online applications. The results can also be used for offline maintenance and fault location without injecting signals into a faulty cable, or a prediction before the application of the time-consuming tracing location methods. With the measurement

values of $v'_{C,mea}$ and $i'_{cable,mea}$, and the time when $v'_{C,mea}$ drops to below any phase value of the grid voltages $v_{g\ a,b,c}$ - $t_{1,mea}$, the fault loop total resistance R_{total} and inductance L_{total} can be solved from

$$\begin{cases} v'_{C,mea} = A_1 e^{p_1 t_{1,mea}} + A_2 e^{p_2 t_{1,mea}} \\ i'_{cable,mea} = A_1 p_1 e^{p_1 t_{1,mea}} + A_2 p_2 e^{p_2 t_{1,mea}} \end{cases} \quad (20)$$

where A_1, A_2, p_1, p_2 are functions of R_{total} and L_{total} as shown in equations (10) and (11).

For dc cables, assume that the per meter resistance and inductance are r and l respectively. With a given r/l ratio of the cable, the grounding resistance R_f and distance x can be solved from equation (21), if the resistance and inductance of other parts of the circuit can be neglected, such as those of IGBTs and diodes

$$\begin{cases} R_{total} = R_f + r \cdot x \\ L_{total} = l \cdot x \end{cases}. \quad (21)$$

IV. FAULT LOCATION EXAMPLES AND VERIFICATION

The proposed location method is applied to different fault conditions and verified by calculations with PSCAD/EMTDC simulations. For ground fault location, robust tests to various ground resistance, fault distances and operation conditions are carried out. An iterative method to reduce calculation error is proposed for more accurate evaluation results.

A. Short-Circuit Fault Location

A short-circuit fault is simulated 1 km from the VSI. The cable π-model parameters are r = 0.06 Ω/km, l = 0.28 mH/km. Cable grounding capacitances are omitted. The VSI parameters are given in Table I. Voltage measurements (Fig. 10) used for distance evaluation are at t = 0.5 ms. At this moment after fault occurs, the positive relay point voltage $v_{\_pos}$ drops to about 0.49 kV, with a reference point measurement voltage $v_{\_r}$ at about 0.44 kV. According to the distance evaluation (18), x = $d \times 0.4914$ / (0.4914–0.4419) = 992.73 m, where the distance between the two voltage measurements, d, is known as 100 m. This evaluated distance is accurate enough (-0.727% relative error), because the short-circuit resistance applied is almost zero in this case (1×10^{-6} Ω). Here it is assumed that the measurements and calculation can be completed within the time in which the overcurrent is reached.
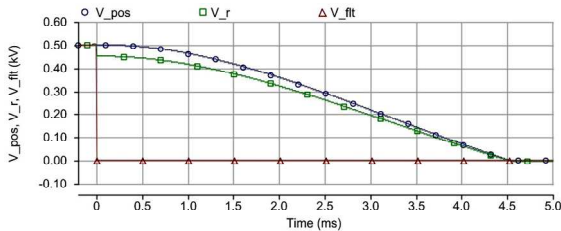

Fig. 10. Relay point voltage measurements under short-circuit fault: positive cable relay $v_{\_pos}$, reference voltage $v_{\_r}$, and fault point voltage $v_{\_flt}$ (kV).

B. Cable Ground Fault Location

The calculation to find the location of the cable ground fault (20) is assessed using relative errors under different conditions: various ground resistances and fault distances, different operating conditions including system protection operation.

1) Distance Estimation under Various Ground Resistances and Fault Distances:

Ground resistances under test are 0.1, 0.2, 0.5, 1, 5, and 10Ω. VSI and cable π-model parameters are the same as above. The rectifier side is tripped immediately at the occurrence of the fault, with the IGBTs blocked instantly at the same time. This gives the best stage 1 calculation to test the accuracy of the location estimate. Fault distance ranges from 500m to 3000m.

The calculated distance and ground resistance from (20) are expressed as relative errors (Table III and IV). Due to the small inductance compared with large ground resistances, the calculation errors for distances increase when ground resistance dominates the system response. That is also why the resistance evaluation has much lower errors in Table IV.

The measurement time t_1 used for calculation is listed in Table V, which also shows that the dominant influence of a large resistance on the system time-response. With large ground resistance, the time response requirement for the dc switchgear system is not critical (in milliseconds even for the smallest ground resistance condition). This is plenty time for dc solid-state CB (SSCB) to operate.

In Table III, when increasing R_f, the calculation error for distance increases dramatically, however, most fault resistance errors are still within 5 %. Therefore the evaluated ground resistances are used in a single-iteration to improve the error. From equation (17), considering when the estimated R_f is large, $i_{(flt)} \approx i_{(n)}$, then

$$\hat{x} = \frac{v_{(n)} - R_f i_{(n)}}{v_{(n)} - v_{(r)}} d \quad (22)$$

It needs to be noted that the errors in R_f are partially because of the high error in distance. Therefore, by choosing a lower $i_{(n)}$ measurement value in (22), the R_f error at distance can be reduced, hence an improved $\hat{x}$ can be obtained. The improved distance results are listed in Table VI.

Now the improved errors are almost all within 2% tolerance. If relay setting using 10% error tolerant for protection tripping, such as that for most strict dc bus faults, this is accurate enough. If this is not the case, another iteration can be performed to further improve the estimate. The accuracy of calculation also depends on the initial guess values for solution of (20). Operational experience or prior simulation results can then be used to initialize the calculation.

TABLE III GROUND FAULT DISTANCES ESTIMATION RELATIVE ERROR (%)

Distance	R_f=0.1Ω	R_f=0.2Ω	R_f=0.5Ω	R_f=1Ω	R_f=5Ω	R_f=10Ω
500 m	-1.172	-1.558	-6.258	-21.642	99.998	99.999
1000 m	1.329	1.611	4.264	15.114	288.04	685.714
1500 m	2.7693	3.1307	5.7093	17.086	257.14	614.29
2000 m	0.3395	0.3695	0.5715	1.4695	20.6695	51.4305
2500 m	1.5072	1.5072	1.6644	2.6916	21.15	42.8572
3000 m	-3.8013	-3.6320	-3.3653	-3.4583	6.6917	42.857

TABLE IV GROUND FAULT RESISTANCE ESTIMATION RELATIVE ERROR (%)

Distance	R_f=0.1Ω	R_f=0.2Ω	R_f=0.5Ω	R_f=1Ω	R_f=5Ω	R_f=10Ω
500 m	1.2	0.4	0.32	0.55	0.79	0.4
1000 m	-1.6	-0.5	-0.22	-0.66	-2.61	-4.014
1500 m	-6.0	-2.4	-0.72	-1.15	-4.404	-5.367
2000 m	-0.6	-0.2	-0.04	-0.09	-0.464	-0.586
2500 m	-4.4	-1.8	-0.44	-0.26	-0.596	-0.614
3000 m	13.5	5.55	1.40	0.54	-0.22	-0.746

TABLE V CALCULATION TIME WITH FAULT RESISTANCE VARIATION (MS)

Distance	R_f=0.1Ω	R_f=0.2Ω	R_f=0.5Ω	R_f=1Ω	R_f=5Ω	R_f=10Ω
500 m	2.36	2.76	3.68	9.12	24.72	51.14
1000 m	2.84	3.12	3.88	9.70	24.94	51.18
1500 m	3.14	3.36	4.04	9.76	30.62	51.22
2000 m	3.40	3.60	4.20	9.82	30.62	51.24
2500 m	3.64	3.80	4.38	9.88	30.64	51.26
3000 m	3.80	3.98	4.54	9.92	30.66	51.36

TABLE VI IMPROVED GROUND DISTANCE ESTIMATION EXPRESSED AS RELATIVE ERROR (%)

Distance	R_f=0.1Ω	R_f=0.2Ω	R_f=0.5Ω	R_f=1Ω	R_f=5Ω	R_f=10Ω
500 m	-0.084	-0.075	-0.131	-0.228	-2.593	-7.823
1000 m	-0.016	-0.020	-0.020	0.010	1.390	7.490
1500 m	-0.013	-0.027	-0.040	0.053	0.520	2.787
2000 m	-0.035	-0.040	-0.040	-0.045	0.125	0.795
2500 m	-0.004	-0.004	-0.008	-0.012	0.076	0.400
3000 m	-0.253	-0.243	-0.230	-0.230	-0.187	0.377

TABLE VII ESTIMATED FAULT RESISTANCE AND DISTANCE UNDER VARIOUS OPERATING CONDITIONS

Cases	Fault Resistance R_f(Ω)	Fault Distance x (m)	1-Iteration Distance $\hat{x}$ (m)	Fault Resistance Error (%)	Fault Distance Error (%)	1-Iteration Distance Error (%)
Case I	0.4989	1042.64	999.80	-0.22	4.264	-0.020
Case II	0.5203	1175.50	994.18	4.06	17.55	-0.582
Case III	0.5090	751.857	978.06	1.80	-24.8143	-2.194
Case IV	0.5330	846.786	993.56	6.60	-15.3214	-0.644

The iteration requires continuous monitoring of system operation status and data recording equipment. Reliable measurement, monitoring and sensor devices are required for practical application.

2) Distance Estimation under Different Operating Conditions:

The aforementioned analysis is based on ideal operation with immediate blocking of the IGBTs and source side tripping at the instant the fault occurs. The fault resistance and distance estimation is now performed with the IGBT blocking function at a threshold current limit (2.0 p.u.) and with the possibility of slow tripping of the source side. The system performance under different conditions is compared with a fault distance of 1 km and 0.5 Ω fault resistance. The following four cases are considered:

Case I: IGBTs and source side are immediately blocked and tripped, respectively;

Case II: The IGBTs are blocked immediately with source side tripping after an ac CB operation period of 20 ms;

Case III: The source side still trips immediately, IGBTs are blocked once they reach a threshold current limit (2.0 p.u.);

Case IV: IGBTs are blocked once they reach their current limit (2.0 p.u.); source side trips after the 20 ms switchgear period.

Simulation results (Fig. 11 and 12) show the difference between the four operating conditions. Without source side tripping, the pulsed dc current still feeds into the negative cable which results in the ripple of cable currents (*Case II* and *IV*). For *Case III* and *IV*, the VSI IGBTs are blocked after 12.45 ms at 2 p.u. (0.17 kA). When any IGBT detects an overcurrent higher than 2.0 p.u., all the IGBTs are blocked at the same time. The time instants used for fault location are detailed in Fig. 12 (indicated with an "✕"). The estimated fault resistance and distance under different conditions are listed in Table VII, with values obtained through one modifying iteration. Although the results are similar, *Case II*, *III*, and *IV* yield higher percentage errors. This is due to the much smaller inductance relative to the resistance: 0.28×10^{-3} compared to 0.5+0.06. However, using the iterative process reduces this calculation error to well below 5%.
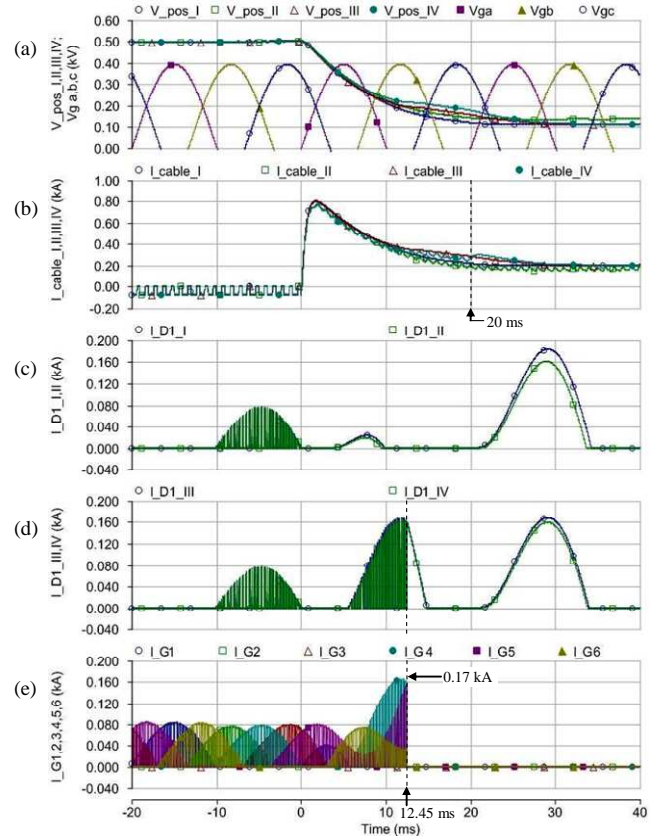

Fig. 11. Fault location measurement under different operation conditions: (a) dc-link positive voltages for *Case I, II, III* and *IV* $v_{pos\_I,II,III,IV}$ (kV), and grid side three-phase voltages $v_{g\,a,b,c}$ (kV); (b) cable currents $i_{cable\_I,II,III,IV}$ (kA); (c) diode current $i_{D1\_I,II}$ (kA); (d) diode current $i_{D1\_III,IV}$ (kA); (e) IGBT currents $i_{G1,2,3,4,5,6}$ (kA).
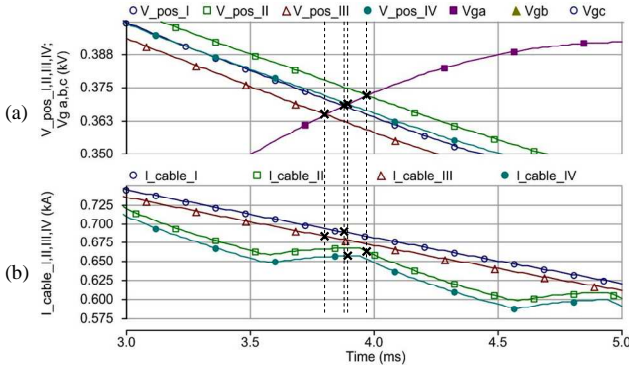
Fig. 12. Zoomed fault location measurement under different operation conditions: (a) dc-link positive voltages for *Case I, II, III* and *IV* $v_{pos\_I,II,III,IV}$ (kV), and grid side three-phase voltages $v_{g\ a,b,c}$ (kV); (b) cable currents $i_{\_cable\_I,II,III,IV}$ (kA).

For the fast time-response dc protection devices, if the main protection and backup coordination are capable of securely protecting the system, at the protection stage, there is no need to estimate what the exact distance is to the fault point. Rough distance evaluation is enough for a relay decision to effectively protect the system. Therefore, the accuracy of evaluation can be flexible for different fault protection device requirements. For example, even if the error is larger than 2% for *Case III* after one iteration in Table VII, this may still be enough for effective protection judgment.

Even if R_f is large, theoretically, the dominant feature of stage 1 of the ground fault is still an *RLC* discharge. Therefore, more accurate location can be acquired with more iterations of the calculation. Although this will take more time for calculation and decision, with large R_f, the fault isolation is not as time critical. Other offline/slow location approaches can also be incorporated to determine a more accurate fault location with larger values of R_f.

V. CONCLUSION

Integration of high-capacity offshore renewable energy onto transmission networks is increasing the applications of VSC-HVDC transmission networks. In this paper, short-circuit and ground fault analysis of VSC-based dc systems is performed. Definitions of the stages of the fault response are provided and assist in identifying the most serious stage of a fault, which must be avoided through protection. The analysis of the most serious short-circuit fault provides a critical time limit for switchgear operation. Also, it is easier to locate a short-circuit by measuring reference voltages than to locate a ground fault which may have a relatively large impedance. Therefore, a fault location method is proposed for ground faults with analysis and simulation provided under various fault distances, resistances and operating conditions. The simulations verify the operation of the technique. A method using an additional single-iteration is proposed and is shown to improve the accuracy of the distance and resistance estimate. The proposed method is a prerequisite for online determination of fault location in order to meet the requirements of effective dc system relay coordination and protection.

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