Switched Capacitor Converters
A New Approach for High Power Applications

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Abstract

High-power, high-voltage and high voltage-conversion ratio DC-DC converters are an enabling technology for offshore DC grids of the future. These converters are required to interface between offshore wind farms and an offshore DC grid and a key design issue is the size and weight of the converter, which significantly impacts the cost of the associated off-shore platform. In addition to this application, some rural communities, particularly in Canada, Australia and South Africa, which are located far away from the electrical power generators, can take the advantages of this technology by tapping into existing HVDC transmission line using a high voltage-conversion ratio DC-DC converter. The work described in this thesis is an investigation as to how such DC-DC converters may be realised for these applications.

First a review of existing DC-DC converters was carried out to assess their suitability for the target applications. A classification of DC-DC converters into Direct and Indirect converters was proposed in this work based on the manner in which the energy is transferred from the input to the output terminal of the converter. Direct DC-DC converters, particularly Switched Capacitor (SC) converters are more promising for high-voltage, high-power and high voltage-conversion ratio applications, since the converter can interface between the low-voltage and the high-voltage terminals using low-voltage and low-power power electronic modules. Existing SC topologies were examined to identify the most promising candidate circuits for the target applications.

Four SC synthesis techniques were proposed in order to derive new SC circuits from existing topologies. A new 2-Leg Ladder, modular 2-Leg Ladder and bi-pole 2-Leg Ladder were devised, which had significant benefits in terms of size and weight when compared with existing circuits.

A scaled power 1 kW converter was built in the laboratory in order to validate the analysis and compare the performance of the new 2-Leg ladder circuit against a conventional Ladder circuit, where it was shown that the new circuit had higher efficiency, smaller size and lower output voltage ripple than the Ladder converter.

Dedicated to:

Mina

&

Sam

Contents

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List of Symbols and Acronyms

DC	Direct Current	
HVDC	High Voltage DC	
SC	Switched Capacitor	
LCC	Line Commuted Converter	
IGBT	Isolated Gate Bipolar Transistors	
VSC	Voltage Source Converter	
XLPE	Cross-linked polyethylene	
PWM	Pulse Width Modulation	
MMC	Multilevel Modular Converter	
DFIG	Doubly Fed Induction Generator	
SWER	Single Wire Earth Return	
D	Duty Cycle	
V_{in}	Input DC voltage	V
I_{in}	Input DC current	A
V_o	Output DC voltage	V
I_o	Output DC current	A
R_L	Load resistance	Ω
V_{switch}	Switch Voltage	V
I_{switch}	Switch Current	A
EMI	Electromagnetic Interface	
MOSFET	Metal–Oxide–Semiconductor Field-Effect Transistor	
V_{AB}	Voltage difference between leg A and B of Full bridge DC-DC converter	V
β	Phase shift between leg A and leg B of Bridge Converter	$Radian$
α	Overlap period in Full Bridge DC-DC Converter	$Radian$
L_s	Stray inductance	H
f_s	Switching frequency	Hz
n	Turn ratio of transformer	

SAB	Single Active Bridge	
V_o'	Output DC voltage referred to the primary side of the transformer	*V*
v_p	Primary side voltage of transformer	*V*
v_s	Secondary side voltage of transformer	*V*
DAB	Dual Active Bridge	
P_o	Output power	*Watt*
d	DC conversion ratio	
L_o	Output filter inductor	*H*
C_o	Output filter capacitor	*F*
SRC	Series Resonant Converter	
PRC	Parallel Load Resonant Converter	
Q	Quality Factor	
HV	High Voltage	
LV	Low Voltage	
SC	Switched Capacitor	
EV	Electric Vehicle	
n_c	Number of cells	
DCP	Dixon Charge Pump	
MMSCC	Multilevel Modular SC Converter	
SMMSCC	Symmetrical Multilevel Modular SC Converter	
R_{loop}	Equivalent resistance of charge transfer loop	Ω
C_{loop}	Equivalent capacitance of charge transfer loop	*F*
L_{loop}	Equivalent inductance of charge transfer loop	*H*
ESR	Equivalent series resistance	Ω
R_{eq}	Output equivalent resistance of SC converter	Ω
T_s	Switching period	*s*
k	Switching phase of a SC converter	
$E_{i,k}$	Energy loss in component *i* and during switching phase *k* of a SC converter	*Joules*
m	Number of components in a SC converter	

$R_{i,k}$	Equivalent resistance of component *i* for switching phase *k*	Ω
RMS	Rout Mean Square	
$i_{i,k}$	current following through component *i* during switching phase *k*	*A*
$I_{rms,i,k}$	RMS current following through component *i* during switching phase *k*	*A*
$I_{avg,i,k}$	Average current following through component *i* during switching phase *k*	*A*
T_k	Switching period of phase *k*	*s*
$a_{i,k}$	Charge multiplier for component *i* for switching phase *k*	
$k_{i,k}$	Form factor of current following through component *i* during switching phase *k*	
$R_{eq,i,k}$	Partial equivalent resistance of component *i* for switching phase *k*	Ω
$R_{ds_{on}}$	on resistance of switch	Ω
FSL	Fast Switching Limit	
SSL	Slow Switching Limit	
$\tau_{loop,i,k}$	Time constant of charge transfer loop for component *i* during switching phase *k*	*s*
$\beta_{i,k}$	Ratio of switching period *k* to $\tau_{loop,i,k}$	
$R^*_{eq,i,k}$	Normalised partial equivalent resistance of component *i* for switching phase *k*	Ω
L_r	Resonance Inductor	*H*
C_r	Resonance Capacitor	*F*
$\omega_{0,i,k}$	Resonant frequency of the equivalent RLC circuit	*Rad/s*
$\omega_{d,i,k}$	Damped resonant frequency of the equivalent RLC circuit	*Rad/s*
$Q_{i,k}$	RLC circuit quality factor	
dT_k	Ratio of switching period for phase *k* over total switching period	
$R^*_{eq,i,k}$	Normalised equivalent resistance for component *i* and switching phase *k*	
dT_d	Ratio of half of damped resonant period over total switching period	
f_d	Damped resonant frequency	*Hz*
V_{eq}	Equivalent output voltage drop	*V*
V_D	Diode on-state voltage	*V*
R_{SW}	Equivalent switch branch resistance	Ω
R_{ESR}	Equivalent capacitor branch resistance	Ω

K_r	Ratio of switch branch resistor to capacitor branch resistor	
K_l	Ratio of switch branch inductor to capacitor branch inductor	
L_p	Parasitic inductance	H
R_p	Parasitic resistance	Ω
R_T	Total resistance	Ω
C_T	Total capacitance	F
L_T	Total inductance	H
SG	Savitzky-Golay	
M2LSCC	Modular 2-Leg Switched Capacitor Converter	
SM2LSCC	Symmetrical Modular 2-Leg Switched Capacitor Converter	
VHDL	Verilog Hardware Description Language	
FPGA	Field Programmable Gate Arrays	
V_{ds}	Drain Source Voltage	V
I_d	Drain Current	A

1. Introduction

In recent years, there has been an increasing interest in developing high-power and high-voltage DC-DC converters for power system applications. There are different applications which can benefit from high power DC-DC converters such as:

- Emerging DC microgrids and distribution systems [1, 2]
- Interfacing DC storage systems with the electric grid [3, 4]
- Interfacing DC power sources such as solar cells in megawatt ranges to the electric grid [5, 6]
- High-speed train power systems [7]
- Interfacing offshore wind generators to an offshore DC grid [8, 9]
- Tapping into an High-Voltage DC (HVDC) power transmission lines to feed remote communities [10-12]
- Interconnection of two HVDC bulk transmission systems working at different voltage levels [13]

This thesis discusses two of the applications from above, namely interfacing offshore wind generators and feeding remote communities. This decision was driven by the industrial sponsor for the project - Alstom Grid - who sees these applications as being important new markets, which could complement their existing HVDC business. Offshore wind DC grids and remote load feeding require high-power and high-voltage DC-DC converters with voltage-conversion ratios of typically ten or above. The purpose of this research work was to investigate different DC-DC converter topologies and assess their suitability for high-power, high-voltage and high voltage-conversion ratio applications. This thesis looks at new topologies based on Switched Capacitor (SC) converters and examines their suitability for DC-DC conversion in the HVDC area.

The remainder of this chapter starts with a brief overview of HVDC technology and its applications. The application of HVDC for the integration of offshore windfarms to offshore DC grids and remote load feeding through an HVDC line will then be discussed in more detail. Finally, an outline requirement specification for the DC-DC converter, which covers both these applications, will be presented at the end of this chapter.

Chapter 2 reviews different DC-DC converter topologies and examines their suitability for high-voltage, high-power and high voltage-conversion ratio applications. Furthermore, an introduction to the most common SC converter topologies that have been proposed over the years and how these circuits are synthesised from a basic SC cell will be discussed in Chapter 2. Chapter 3 then discusses two popular analysis methods that have been reported in the literature and highlights

their limitations, and proposes a more general and intuitive approach. Chapter 4 investigates the effects of circuit parasitic on the operation and the efficiency of SC converters. Analysis of coupled SC converters and the effects of coupling on the operation of SC converters will be discussed in Chapter 5. In Chapter 6, four SC synthesis techniques will be introduced and new topologies will be derived based on these synthesis techniques and will be compared with conventional SC topologies. The design and experimental results from a 1 kW scaled, prototype of this new topology are presented in Chapter 7. Finally, Chapter 8 will include conclusions and discuss future work.

1.1 HVDC Technology and Applications

HVDC has been primarily used for bulk power transmission over long distance overhead lines and underground cables and the interconnection of asynchronous systems. The line and transmission losses for HVDC is less than AC for the same power capacity [14]; however, the additional cost of the AC-DC and DC-AC power converters required at both ends of the HVDC line is high when compared to an AC substation and only over a certain transmission distance, the so called "break-even distance", does the HVDC provide economical alternative to AC transmission. The break-even distance, as shown in Figure 1-1 depends on several factors. For example, the break-even point for overhead lines is typically 600-800 km but it is only around 90 km for underground cables [15]. This is due to high electrical capacitance of cables when compared to overhead lines, which leads to a high reactive current in the line.

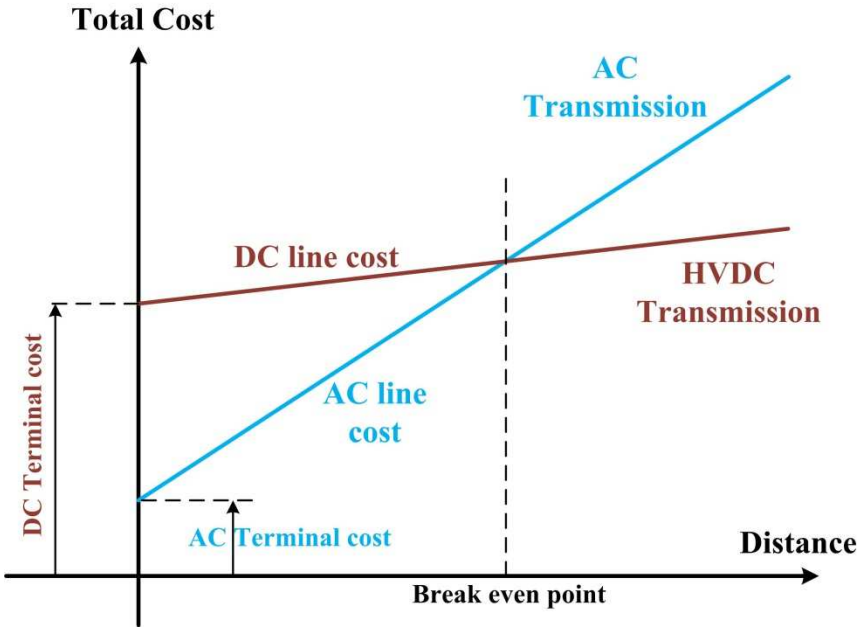


Figure 1-1. HVDC vs. AC Transmission Cost

To date there are two basic converter topologies that exist for AC-DC / DC-AC conversion in modern HVDC transmission systems, namely conventional Line Commuted Converters (LCC)

and newer self-commuted Voltage Source Converters (VSCs) [14, 16]. LCC is based on thyristor valves and is the most cost-effective technology for bulk power transmission over long distances, with the capability of up to 7.2 GW at voltages up to 800 kV [17]. Thyristors rely on a reversal of the anode/cathode current to turn-off, therefor the LCC converter needs to be connected to a strong AC network to ensure commutation of the thyristor valves. Furthermore LCC converters operate at poor power factor due to the high harmonic content of the current as well as its lagging fundamental. An LCC HVDC station therefore needs significant compensation and filtering at both the sending and receiving ends.

HVDC transmission with VSC is a new technology, which is based on self-commuted devices such as Isolated Gate Bipolar Transistors (IGBTs). VSC HVDC offers several advantages over conventional LCC technology. VSC technology can control both the active and reactive power flows independently. It can even inject reactive power into a weak grid for compensation. In addition it can supply a passive grid or black-start an active system. Furthermore VSC converters operate with close to sinusoidal current so that the need for external harmonic filter is almost negligible. Therefore the overall size of the HVDC station is dramatically reduced. One other significant advantage that VSC has over LCC is that it reverses the DC current rather than the voltage to change the power direction; therefore power reversals are much quicker and XLPE cables can be used instead of more expensive mass impregnated cables.

The first generation of VSC HVDC was based on the two or three level Pulse Width Modulation (PWM) converter, first developed by ABB, known as HVDC Light, in the late 1990s [18]. A series connection of switching devices is required in this configuration to achieve a high voltage capability. IGBTs, which are commonly employed in VSC converters, have fast switching transitions and sharing of the voltage across individual devices during switching is very difficult in this type of converter. Voltage sharing is achieved using complex active gate-drive control and requires IGBTs having closely matched parameters. ABB, who are an IGBT manufacture, can select device appropriately and this is the most likely reason that they have been the only company to make this technology a commercial success.

A more recent technology for VSC HVDC using a Multilevel Modular Converter (MMC) topology, commercially known as “HVDC PLUS”, was introduced in 2007 [19]. In this technology, the AC voltage is synthesised from several levels of DC capacitor voltages, producing a waveform with a large number of steps, which approximates a sinusoidal wave with minimum harmonic distortion [19, 20]. With a modular structure any number of modules can be added in series in order to reach a high voltage capability. For example, this technology has been practically implemented in the INELFE France-Spain interconnector, which consist of two independent 1000MW bipolar HVDC links using VSC converters operating at ±320 kV [21].

Because of the need for self-commutated switches such as IGBTs, VSC currently has a much lower rating than thyristor based LCC converters. It is therefore not suitable for bulk power transmission, but is instead used for lower power applications such as offshore wind farms, and smaller submarine connections. In particular, because of its unipolar DC voltage, VSCs can be connected in parallel allowing the interconnection of different links. This enables the concept of a DC-grid to be realised, such as the coupling of different off-shore submarine links. However, this would require a DC-DC converter to connect together systems that typically operate at different voltage levels – the same function that a transformer has in an AC system. The differing voltage levels arise because most of the HVDC schemes currently considered or already built are of point-to-point type and are developed and supplied by different manufacturers. Due to the absence of a common DC grid code, the voltage can be freely chosen by the manufacturer.

The interconnection of bulk point-to-point HVDC systems would require a high voltage, high power DC-DC converter having a low voltage-conversion ratio less than 3 [13]. This application is currently being considered by Alstom Grid in collaboration with Imperial College London and is therefore outside the scope of this thesis.

Two other applications for DC-DC converters that Alstom Grid are interested in, which have a lower power requirement are:

1) The connection of individual turbines or turbine arrays to a central off-shore collector, or the connection of the collector back to shore.
2) Feeding electrical power to small, remote communities. For example, this can be done by long-distance HVDC transmission or tapping off from an existing bulk DC power transmission link. The voltage at the DC line is then stepped down using a high voltage-conversion ratio DC-DC converter followed by low-voltage DC-AC conversion.

Unlike the interconnection of DC bulk transmission lines these two applications require high step-up voltage-conversion ratios with typical values of greater than 10 compared with 1.5 to 5 for bulk transmission.

The two applications described above were those that Alstom Grid decided would be the main focus of the project and these are discussed in more details in the following sections.

1.2 HVDC Applications of DC-DC Converter Considered in This Work

1.2.1 Interconnection of Offshore Windfarms

Electric power generated by offshore wind farms is now starting to make an important contribution to the world's electric energy production. Installed wind turbine capacity by the end

of 2012 in Europe was 5 GW and this will be increased to 40 GW by 2020 and 150 GW by 2030 in order to meet 14% of EU electricity demand [22].

Offshore wind farms are receiving more attention than onshore wind farms because of the more consistent winds that can be found over the oceans. In addition, they can generate substantially more energy than their onshore counterparts [15, 23]. In addition, locating wind turbines offshore overcomes the problems of acoustic noise that are prevalent with onshore turbines [24].

However offshore windfarms are considerably more expensive to build than on-shore. Offshore wind turbines require complex structures which are mounted on the ocean floor to support the turbine above the water. The construction cost of these supports, which depends considerably on the weight of the turbine, contributes to more than 20% of the cost of offshore facilities [25]. Research and development projects are therefore aiming to reduce the weight of turbine materials and equipment since larger wind turbines with increased generation capacity are needed in order to meet rising energy demand. For example turbines up to 8 MW such as the Vestas V164 have now been developed and commercialised.

Almost all wind turbines use AC generators to convert mechanical power into electric power. Variable speed wind turbine technology is used in high-power, off-shore applications in order to utilise a wider range of wind speed and maximise the captured energy. However, variable speed wind turbines require a power electronic converter interface in order to connect to the grid.

The most commonly used variable speed wind turbine systems are the Doubly Fed Induction Generator (DFIG) and Full-Power Rated Converter technologies. In a DFIG system, the stator is directly connected to the grid and a back-to-back power electronic converter connects the grid to the turbine rotor through slip rings in order to control the slip frequency, Figure 1-2(a). The power electronic converter, which is typically rated to 40 % of the nominal turbine power, allows a ±40 % speed variation around synchronous speed. Wind turbine manufactures, Senvion's Senvion 6.XM, formerly REpower Systems, and Guodian United Power's UP6000-136, with an output voltage 6.6 kV, employ a DFIG arrangement.

In a Full-Power Rated Convertor system, the stator is connected to the grid through a fully rated, back-to-back voltage source converter to allow variable speed operation, as shown in Figure 1-2(b). Normally a Permanent Magnet Synchronous Generator (PMSG) or a Squirrel Cage Induction Generator (SCIG) is employed in this configuration. The full-rated converter system offers more flexibility for grid connection; however it is more costly than a DFIG as it requires a fully-rated power electronic converter. Wind turbine manufactures such as Vestas (V164-8.0), Alstom Power (Haliade 150-6MW), Siemens (SWT-6.0-154), GE (GE 4.1-113), Goldwind, Guodian United Power (SCD 6MW), Gamesa, Dongfang and MingYang employ permanent

magnet synchronous generator and Sinovel (SL6000) employs a squirrel cage induction generator in their latest products [26].

A typical output voltage from a wind turbine machine is around 400-690 V. However, higher voltage wind generators such as the ACCIONA AW3000 [27] have recently come to the market with an output voltage of 12 kV. The company claims that this higher voltage means that a bulky step-up transformer is not required. However, transmission voltages would then be limited to 12 kV. Since this project investigates the use of HVDC transmission systems, which inherently require power electronic converters for voltage step up, then interfacing to such HV generators would require very expensive high-voltage rated converters, such as multi-level circuits. An AC transformer could be used to step-up the voltage to a VSC AC-DC converter; however this nullifies the claimed advantage of the HV machine in that it does not require a transformer. Therefore only machines having an output voltage of up to 1kV are considered in this thesis.

A major challenge regarding offshore wind farms is to efficiently transmit the power generated from individual turbine machines through to final integration into the onshore AC system. For large offshore wind farms located far from shore, an HVDC transmission system may provide an economical solution for bringing the power back to the grid compared with its AC counterpart due to the cost breakeven point discussed previously [15, 23]. Furthermore, in order to increase the stability and security of the offshore grid it is more efficient and cost effective to interconnect different offshore wind farms, which can share a single transmission line to bring the power to shore [23].

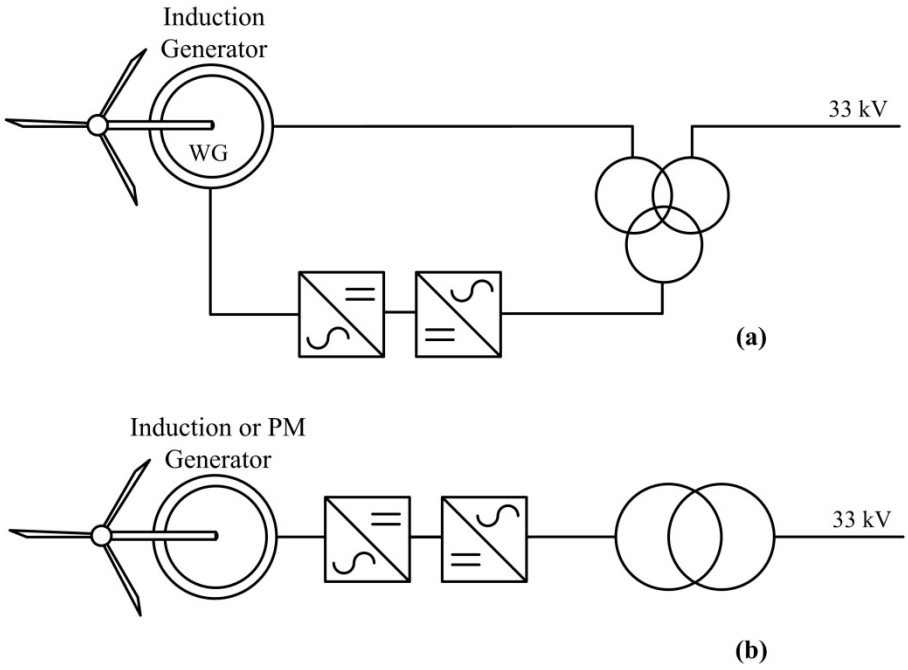


Figure 1-2. Large offshore Wind turbine configurations (a) Variable speed doubly-fed induction generation (DFIG) (b) Variable speed Squirrel Cage Induction Generator or Permanent Magnet Synchronous Generator with full-scale power electronic converter[28]

HVAC systems

Different scenarios and solutions have been adopted for AC based windfarm-to-shore connections [15, 23]. For small windfarms located typically less than 10 km from shore, the voltage generated by each wind turbine is increased to typically 33 kV by a transformer located in the tower of the wind turbine. The outputs of individual turbine transformers are connected together and the power is transmitted to shore via a single medium voltage submarine cable as shown in *Figure* 1-3(a). The Kentish Flats offshore windfarm in UK located 9 km off the coast of Kent is an example for this layout. It is capable of 90 MW generated power using 30 Turbines. Each 3 MW turbine is connected together locally and then transmitted to shore via an individual 3-core medium voltage submarine cable. A shunt reactor is required at the receiving end of the transmission line in order to compensate for the cable capacitance.

Larger wind farms with power rating of hundreds of megawatts are typically located further from shore due to better wind profiles and the larger availability of space. In this case an offshore transformer substation is required, which acts as a common connection point for the turbines and steps up the voltage to transmission levels, typically 150 kV. A high transmission voltage is needed in order to reduce the conduction losses in the cables over the long distance to shore. A typical layout for this configuration is illustrated in *Figure* 1-3(b). Individual offshore wind turbines are connected together at a 33/150 kV transformer, which is mounted on its own offshore platform. This connection node is known as a “collection point” or “collector”. The collector is

then connected to shore using a single 150 kV cable and again a shunt reactor is required at the receiving end of the line. The London Array and the Greater Gabbard offshore windfarms are examples of this layout.

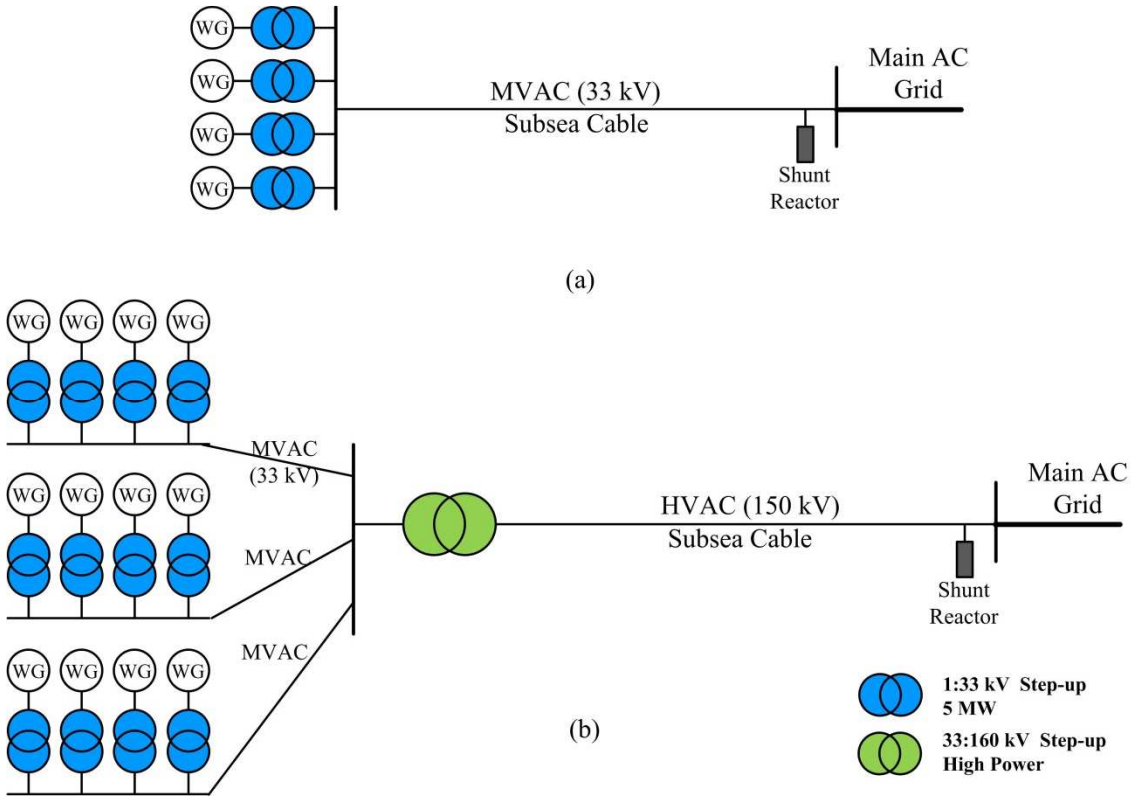


Figure 1-3. AC connection of offshore windfarms (a) without transformer substation (b) with transformer substation

Other examples of the layout shown in Figure 1-3(b) are firstly the London Array offshore windfarm, which had its first phase completed in 2013, and is located 20km off the North Foreland on the Kent coast in United Kingdom. The windfarm has 175 turbines and a total power rating of 630 MW. The turbines are connected together at two off-shore collector substations using 210 km of 33 kV cable. The two collector substations are connected to an onshore substation by four 150 kV AC subsea cables, having a total length of 220 km. Secondly, the Greater Gabbard windfarm is rated at 504 MW and was constructed in 2012 and is located 23 km off the coast of Suffolk in England. A 33/132kV collector with three 180 MVA transformers is used to transmit power to shore using three, three-phase 132 kV XLPE submarine cables.

HVDC systems

As the power rating of windfarms has gradually increased over the years and they are located further offshore in order to exploit higher, more consistent wind energy, HVDC transmission has

offered a better performance and lower cost than AC transmission system due to the longer transmission distance involved and the corresponding economic break-even point discussed previously. A typical HVDC transmission scheme for offshore windfarms is shown in Figure 1-4.

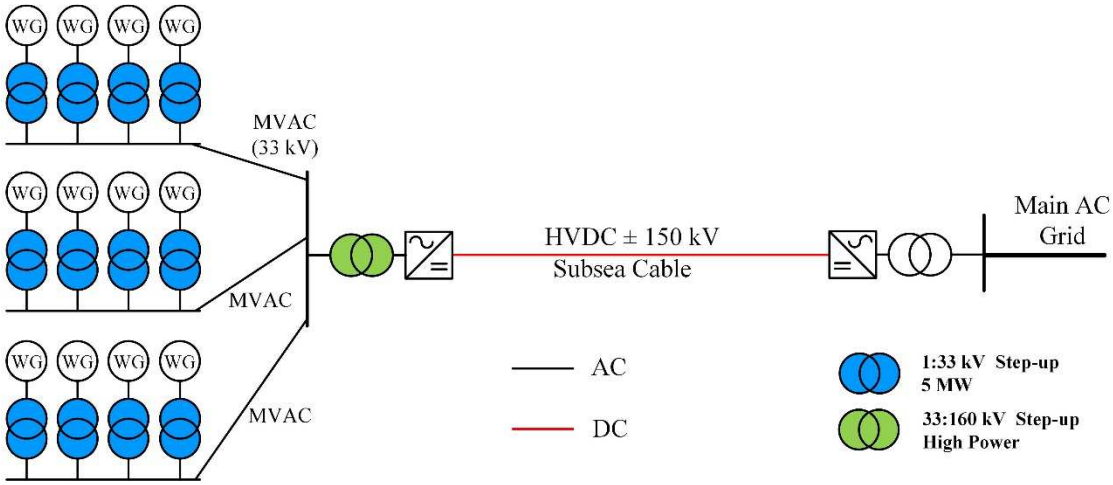


Figure 1-4. A typical HVDC transmission system for offshore windfarm

In this configuration each individual turbine has a transformer to step up the wind generator voltage to a medium AC voltage of typically 25-40 kV. A medium voltage submarine cable is used to interconnect the array of wind turbines to a local collector where a step-up transformer and a VSC HVDC converter is used to convert the medium voltage AC voltage to high voltage DC for the transmission of power back to shore. Another HVDC converter is required at on-shore to convert the DC back to AC for grid connection.

An example of this scheme is BorWin1, which is located 130 km off the German coast in the North Sea, and consists of 80 wind turbines with power ratings of 5 MW, and was the first VSC HVDC scheme for offshore wind farms. Generated electrical power is collected at 36 kV on an offshore platform, where it is stepped up to around 160 kV using a transformer. An HVDC VSC converter station is located on the same platform to convert the power to DC. The power is transmitted through two ±150 kV HVDC submarine cables to an onshore converter station at Diele, where it is integrated in to the German 380 kV grid. Another example is HelWin1, which is located in the North Sea and has a 576 MW offshore collector platform using a 130 km bipolar cables operating at 250 kV DC to feed the German 380 kV AC grid.

So far, AC systems have been used to connect the generated power from the offshore wind turbines to the local collector. However, the feasibility of a DC collection system was studied in [23]. Along with all the advantages that DC offers over AC for submarine cables, it can also significantly reduce the construction cost of the wind turbine.

For a DC collection system the arrangement of the power electronic converters needs to be changed within the wind turbine as shown in Figure 1-5. For a DFIG type system whilst there is no need for the AC-DC converter in the rotor circuit, an additional fully rated DC to AC converter is needed in the stator circuit. Therefore for a DC collection system the DFIG type generator would not be the most appropriate arrangement due to high cost and therefore it is not considered further in this thesis. However, for the full scaled type PM wind turbine system the AC-DC-AC converter that is used in an AC system is reduced to just an AC-DC converter, which makes it far more cost effective than the DFIG arrangement if the DC voltages on the rotor and stator are similar.

Therefore by using a DC collection system the converter requirements within the turbine are significantly reduced. In addition there is no need for the bulky and heavy AC transformer which is installed in the tower of wind turbine of an AC system to step-up the voltage to distribution level for collection. However, whilst an additional compact low-weight DC-DC converter is then needed for voltage step-up in the DC system, this arrangement can significantly reduce the cost of the offshore wind turbine system.

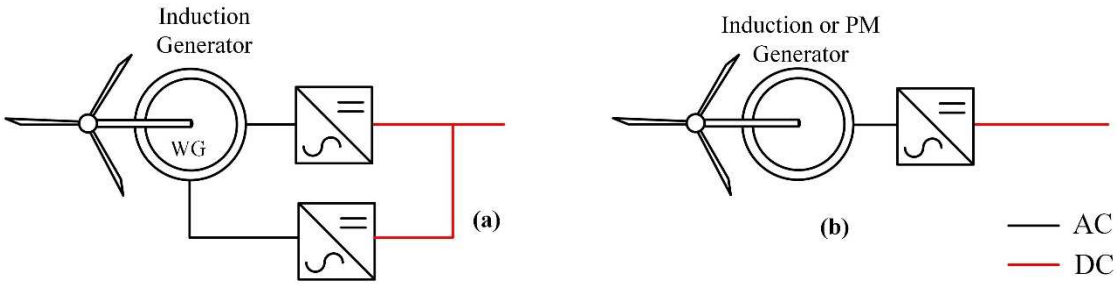


Figure 1-5. Large offshore Wind turbine configurations to interface with DC collection system (a) Variable speed doubly-fed induction generation (DFIG) (b) Variable speed Squirrel Cage Induction Generator or Permanent Magnet Synchronous Generator

By using DC collection, different schemes can be considered to bring the generated power from wind farm to shore as shown by the examples in Figure 1-6. In the first configuration shown in Figure 1-6(a), low voltage DC is used to connect each turbine to the collector where a single high-power step-up converter with a high voltage-conversion ratio (greater than 10) is used to generate the transmission voltage to connect to shore. Since the power rating of the converter is high, the converter is optimised to operate at high efficiency. However, this configuration has high losses in the collection system since the distribution voltage level is limited by the wind generator, which is typically 5 kV. This configuration may be suitable for small wind farms where the losses in the collection system are low due to the short cable lengths.

The second configuration shown in Figure 1-6(b) uses two stages of DC-DC conversion. The first DC-DC converter has a low power rating and is located within each turbine and is used to

increase the output voltage of the turbine generator to distribution levels, typically 25-40 kV. The second converter, which is located at the collection point has a high power rating and increases the voltage to transmission level. This configuration is suitable for large offshore windfarms where the cable length to the collection system is high. However this scheme requires separate DC-DC converters for individual wind turbines.

The third configuration shown in Figure 1-6(c) is single stage DC-DC conversion at the turbine. The DC-DC converter needs to be designed for very high voltage-conversion ratio as it should be connected directly to the transmission network; however the power rating is quite low (1-6 MW) which may reduce the efficiency of the converter due to poor utilisation of components [23]. However, a number of turbines can be connected in parallel for better utilisation of the DC-DC converter. This scheme has lower cable losses compared to the other schemes due to its higher overall system voltage. The major advantage is that there is no need for an offshore collector platform as each turbine or couple of turbines is directly connected to the HVDC line through the DC-DC converter.

The advantages and disadvantages of the three DC collection scenarios are summarised in Table 1-1.

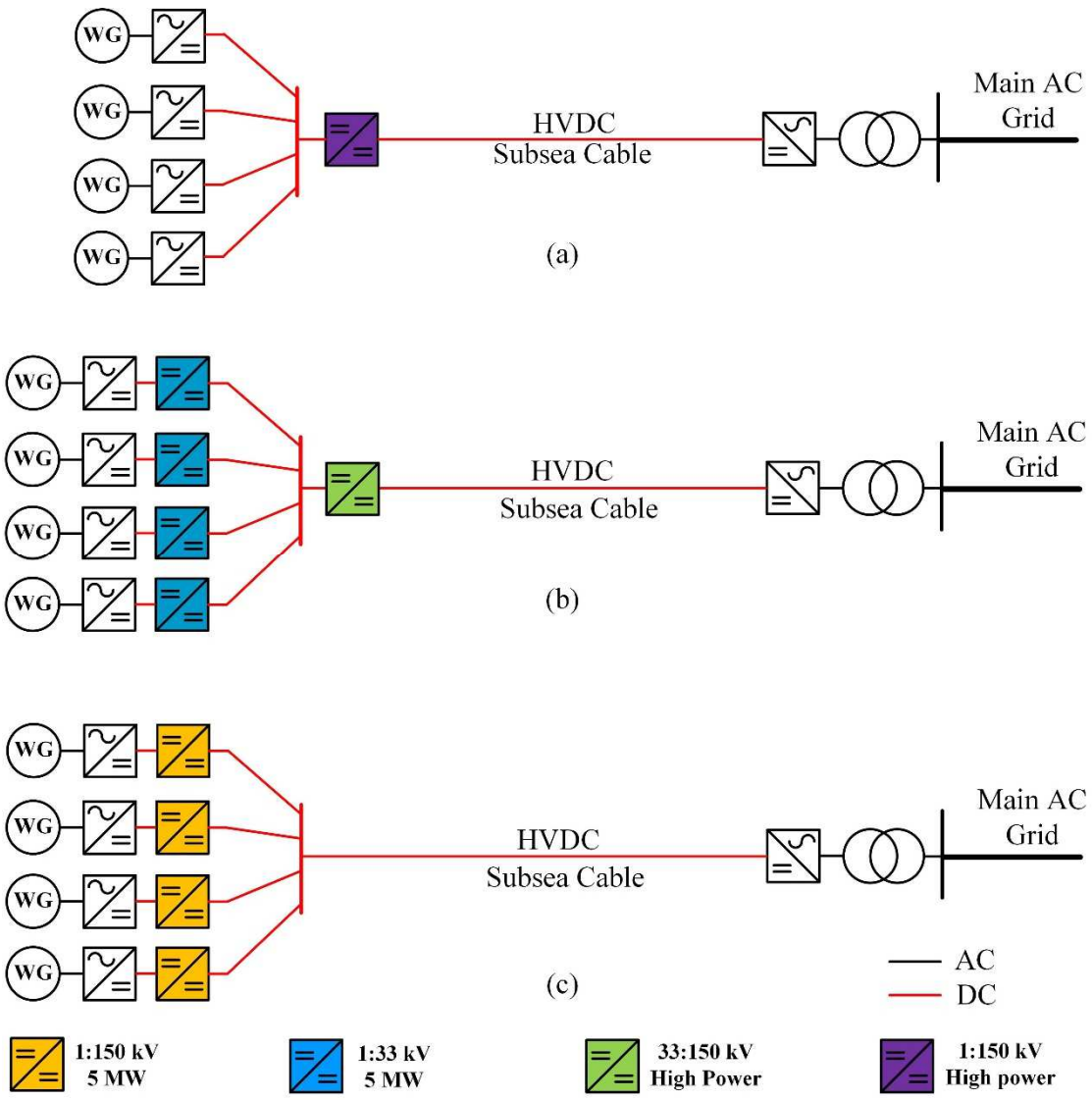


Figure 1-6. DC offshore schemes (a) Collection step-up (b) Two-stage step-up (c) Turbine step-up

Table 1-1. Summary of advantages and disadvantages of different offshore DC collection systems

	Advantages	Disadvantages
Collection point step-up, Figure 1-6(a)	-Minimum number of DC-DC converters required -High converter efficiency -Low converter losses	-High cable losses at the distribution level -Need for additional offshore platform for the DC-DC converter
Two stages step-up, Figure 1-6(b)	-Low cable losses at the distribution level -Individual voltage control	-High converter losses -Need for additional offshore platform for the DC-DC converter
Turbine step-up, Figure 1-6(c)	-Lowest cable losses -No need for offshore platform	-Need a low power and very high voltage-conversion ratio DC-DC converter

In [29-31] another configuration has been proposed for offshore DC grid application and is shown in Figure 1-7. In this structure each converter has its own isolated DC-DC converter. The output voltages of individual converters are connected in series to sum to the transmission voltage. Therefore, there is no need for an offshore collection platform and its associated high-power DC-DC converter to step-up the voltage to transmission level. However, the disadvantages for this configuration are the need for an isolated DC-DC converter and a complex control system to ensure equal sharing of the HVDC bus voltage across the converters. Due to difference in the output power of wind turbines, which may be up to 30% in adjacent turbines, and because the secondary-side current of each converter must be the same, the DC-DC converters in this configuration requires voltage control capability over a wide range in order to control the power through each converter. The requirement for variable voltage operation can reduce the efficiency of the converters, for example series-resonant DC-DC converters have a reduced efficiency at light load.

In the configurations shown in Figure 1-6, a controlled rectifier can be used to control the DC voltage on the input terminal of the DC-DC converter as the output power of the wind turbine generator changes. Furthermore, the DC-DC converter needs to have a voltage regulation capability in a narrow range in order to control the power flow in the DC Grid. However if the DC-DC converter has fix conversion ratio the output voltage of the DC-DC converter can be controlled from its input terminal via the controlled rectifier or an additional low power isolated DC-DC converter can be connected in series with the main DC-DC converter for voltage regulation.

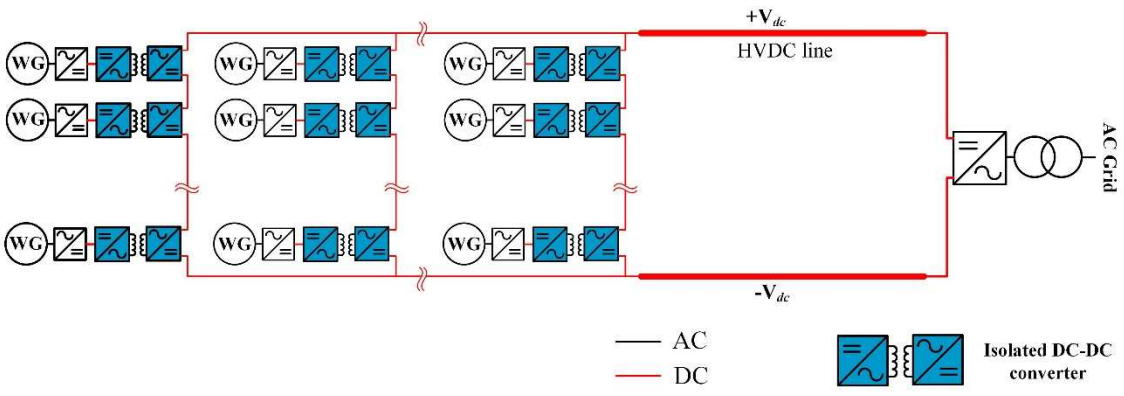


Figure 1-7. DC offshore scheme using series connected, isolated DC-DC converters

A furthermore significant disadvantage of this scheme is the need for isolation. This is achieved using a high frequency transformer embedded within the DC-DC converter which will minimise the size and weight of the unit. However as discussed below, high-voltage, high frequency transformers are not commercially available at the moment with megawatt ratings. In addition,

whilst with a large number of series turbines the step-up ratio of each individual transformer does not have to be very high, the primary-secondary isolation voltage would have to be rated at the transmission voltage level. However, different research groups are working to develop a medium frequency transformer for this type of application. Figure 1-8 summarises recent achievements from different research groups in this area. The most promising work is from ETH University in Switzerland where they have developed 166 kW/20 kHz transformer employed in a 400:2000 V DC-DC converter. The aim of this work is to develop a high-step up ratio, high power converter by series connection of the converter modules on the high voltage side, and a parallel connection on the low voltage side [32]. But again, the isolation voltage of the transformer must be rated to the total series voltage on the secondary side.

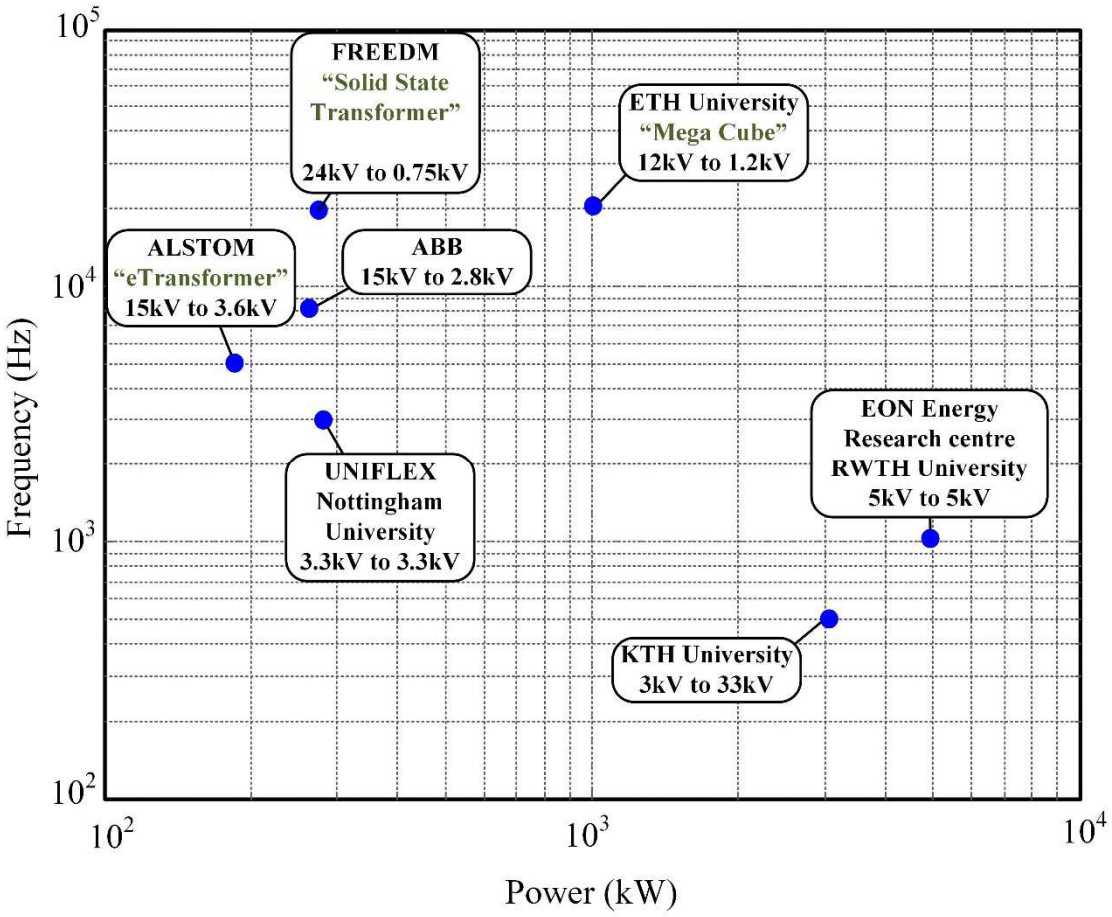


Figure 1-8. Volume and power reached by different research groups for medium frequency transformers [33]

At the moment all offshore wind schemes are point-to-point, windfarm-to-shore connections. However, with an increasing number of offshore windfarms being installed; interconnection of HVDC lines in DC schemes has the potential to increase system reliability, transmission capacity and open up new electricity market opportunities. In addition, offshore oil and gas platforms can benefit from this technology allowing them to tap in to an existing HVDC line by means of a

DC-DC converter. A typical arrangement for such an offshore DC power grid is shown in Figure 1-9. An HVDC meshed network provides a transmission backbone to interconnect different offshore windfarms and integrate with the AC grid on shore. AC clusters can connect to this HVDC grid through an HVDC converter. DC clusters which may have one of the configurations shown in Figure 1-6 can be connected directly to the HVDC grid through DC-DC converters. Furthermore, the HVDC grid can be extended to tap to remote renewable energy sources on shore. For example the HVDC grid will be needed in near future in Europe, where there are a lot of different renewable sources in different places, for example Hydro power in Scandinavia and the Alps, wind in the North Sea and solar energy in the South, and in order to optimise the use of these energy sources an HVDC grid would be the best solution. Again, a key component in such a scheme is a DC-DC converter with a high voltage-conversion ratio.

The aim of this project is therefore to design and develop a modular DC-DC converter with high voltage-conversion ratios to connect offshore wind turbines to an offshore DC collection grid as shown in Figure 1-6(c). This converter would also be a major component within future off-shore DC grids as shown in Figure 1-9. However with a modular design the converter can be modified to suit the two stage step-up scheme shown in Figure 1-6(b).

The second application considered in this thesis is remote load feeding through HVDC line and will be discussed in following section.

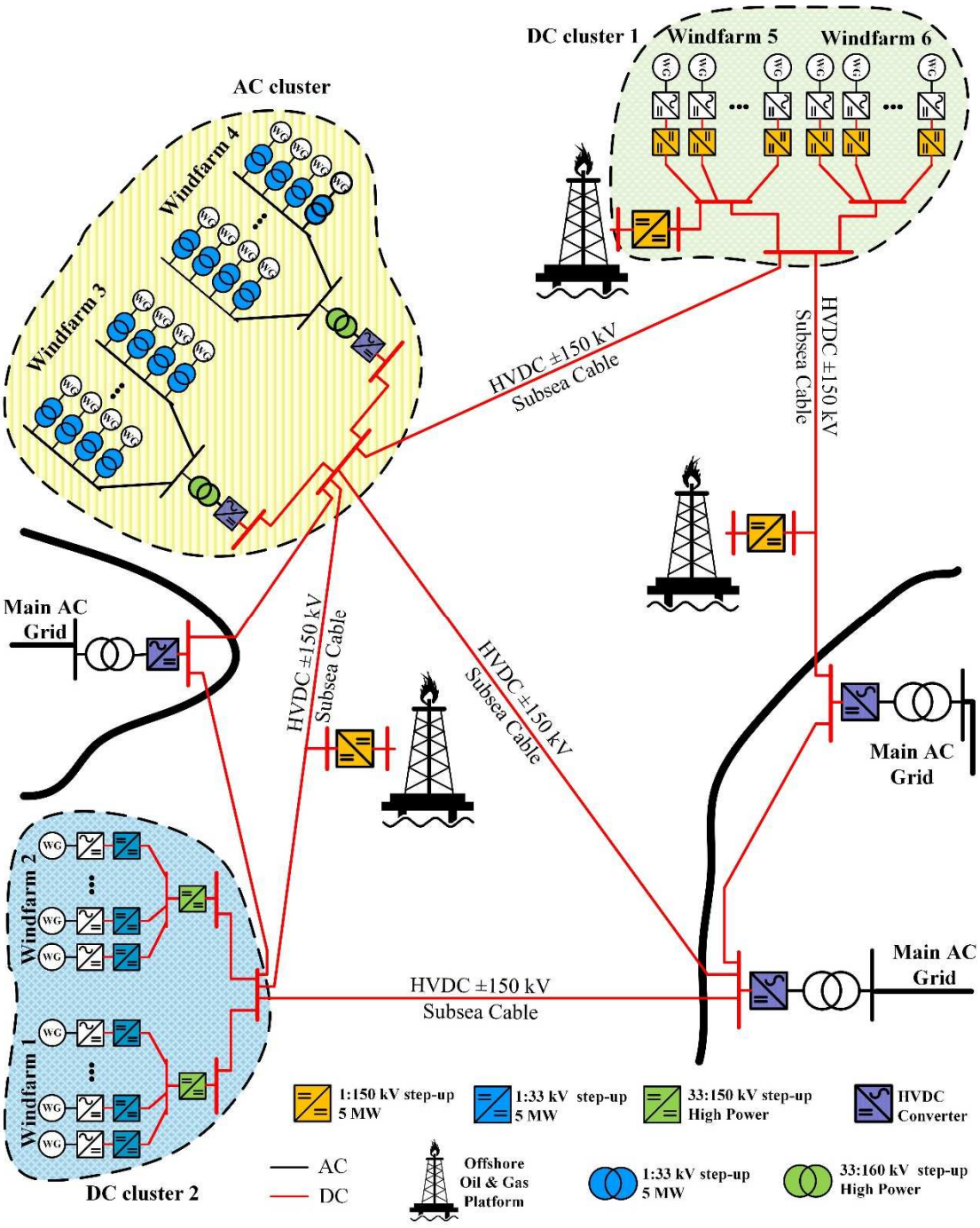


Figure 1-9. Typical configuration for future offshore DC Grid concept

1.2.2 Remote Load Feeding Through an HVDC Line

There are some areas where communities are separated by long distances from a source of electrical power. There are different solutions to energise these communities; the most common approach is the use of a local diesel electric power plant. However, diesel electric power plants have high capital and operating cost and the cost of diesel fuel is high for remote areas due to high transportation and storage costs. A number of alternative approaches have been discussed in the literature as follows:

a) Many communities can use local energy resources such as hydro, wind, solar, coal, gas, biomass or other locally available resources in order to generate electric power. However, even if local resources are available, in most cases these alternatives are extremely costly and cannot be economically justified for small sized communities.

b) For small communities the high-cost of a) above may be overcome by using an electrical intertie to connect a number of widely spread villages together, so that the sharing of alternative energy resources may be economically justified. Furthermore, the interconnection can lower the cost of diesel generation by consolidating small diesel power plants and provide a bulk fuel facility. In [10] a scheme for supplying remote loads has been presented, where the transmission voltage is 50 kV, and in [30] which uses a higher voltage of 100 kV. Taking this concept further it is possible to connect a single remote community, or a number of communities located along a narrow corridor using a dedicated long-distance transmission line to directly connect into an established AC transmission network that may be located faraway from these communities,.

   The problem with this solution is that the installation cost for such a conventional AC intertie system is high in remote rural areas. For example it can range from $140,000 to over $400,000 per mile for rural Alaska and many AC intertie systems may not be cost effective at this price [10].

c) A monopole HVDC link using a single wire earth return (SWER) can significantly lower the cost of the long-distance AC transmission described in b) above as it only needs a single wire to transmit power, which dramatically simplify the design of the transmission line [10]. A medium voltage, monopole HVDC system with a ground return, using a single-wire has been proposed in [10]. A SWER HVDC configuration offers several advantages over a conventional AC intertie system for this application. First of all, the installation cost for an overhead transmission line for SWER is much less than for a 3- or 4-wire AC system. Furthermore, DC transmission does not suffer from the cable capacitance and reactive charging current and losses, so that power can be transmitted over long distances without any need for reactive power compensation. However, in some areas where SWER HVDC is not appropriate, a two wire monopole HVDC line can still offer a cost effective solution compared to a conventional AC intertie [10].

d) Tapping into an existing, local bulk-transmission line can be a cost effective approach to energise a remote community [12]. For example there are many long-distance, trans-continental HVDC links that pass through remote areas of the world such as South-America, Africa and China. Tapping of the HVDC line can be achieved by means of a low-power, high-voltage, high voltage-conversion ratio, step-down, HVDC converter.

There are two alternatives for tapping into this HVDC line: 1) convert the DC voltage to AC by a high voltage, low power inverter and then step down the voltage by a line-frequency transformer, 2) taking the voltage stress by a high voltage-conversion ratio, step-down DC-DC converter and then use a commercially available DC-AC inverter to supply the village AC grid. The second method is a more economical solution for stepping-down the DC voltage as it requires a lower number of devices.

Alstom Grid is interested in DC schemes such as (b) and (d) above, which require the same high voltage-conversion ratio DC-DC converter that was identified for the wind-turbine application in the previous section. For the purposes of this thesis a remote-load transmission voltage of 50kV has been decided and a load power of 1MW is to be considered, with the option that either the voltage and/or the power can be scaled to higher levels at a later date. Furthermore a remote community may have embedded generation capability such as solar arrays, wind turbines, in which case a bidirectional converter capability may also be desirable.

The next section outlines a specification for such a converter that would ideally meet the requirements of remote-load feeding as well as wind-turbine applications.

1.3 DC-DC Converter Requirements Specifications

a) High voltage side:

- **Connection of offshore wind turbine to DC grid**

  The high voltage side of the DC-DC converter for the turbine step-up scheme shown in Figure 1-6(c) is connected to the HVDC transmission line which is typically 150 kV. However if the two stage step-up scheme shown in Figure 1-6(b) is considered the voltage is distribution level and suggested typical values is 25-40 kV.

- **Remote load feeding**

  The high voltage side of the DC-DC converter is connected to the HVDC line. The voltage of the HVDC line has a significant effect on the cable loss and the size of the power electronics converters. In [10] a scheme for supplying remote loads only has been presented, where the transmission voltage is chosen as 50 kV considering the cable losses and the size and losses in power electronics converters, and [30] where the voltage is higher at 100 kV.

b) Low voltage side:

- **Connection of offshore wind turbine to DC grid**

  The input voltage of the DC-DC converter is defined by the output voltage of the wind turbine generator. Most of the wind generators operating today have an output voltage of typically 400-690 V. In this research work the low voltage side for this application is set to 1 kV.

- **Remote load feeding**

  The stress of the voltage in the HVDC line will be taken by the DC-DC converter at a convenient point where a standard DC/AC inverter is located to interface with the communities' three-phase power grid. Medium voltage DC/AC converters with voltage rating of up to 13.8 kV are available from different manufactures. The output voltage of the DC/DC converter can be chosen freely as the AC transformer at the front end can adjust the voltage to interface with village AC grid. Here the output voltage of the DC-DC converter is set to 1 kV.

c) Power rating:

- **Connection of offshore wind turbine to DC grid**

  A typical power rating for modern wind turbine generators is around 5 MW. However higher power wind turbine generators up to 8 MW are now becoming available. Some examples for recent wind generators are Multibird M5000 from AREVA with a power rating of 5 MW and output voltage 3.3 kV, Haliade 150 from Alstom Power has a power rating of 6 MW and an output voltage of 900 V, SWT-6.0-120 from SIEMENS is 6 MW and V164/8000 is an 8 MW wind generator from Vestas.

  In this work a power rating of 5 MW is considered for the DC-DC converter keeping in mind that the power rating can be scaled up to 10 MW to meet the requirement for large wind turbines.

- **Remote load feeding**

  The power consumed by communities varies over a wide range depending on the size of the village. Typical loads of 200 kW to 2 MW are common. For the purposes of this thesis a load power of 1 MW has been decided, with the option that the power can be scaled to higher levels at a later date.

d) Bidirectional capability:

- **Connection of offshore wind turbine to a DC grid**

  During normal operation of an offshore platform the power is transferred from the wind turbine to shore. However during periods where the wind is not blowing or the wind speed is below the turn-on speed of wind turbine, the loads associated with the wind turbines such as the control system need to be supplied by the DC grid, which could then require a bidirectional DC-DC converter. However this load is a low percentage of the nominal power of wind turbine and can be supplied by an additional low power step-down DC-DC converter or an AC line which runs parallel with the high power DC connection.

- **Remote load feeding**

  As discussed earlier some communities may have embedded generation capability such as solar arrays, wind turbines, in which case a bidirectional converter capability would then be desirable.

1.4 Converter Specification Summary

Table 1-2 summarises the specification requirement for the DC-DC converter for both off-shore wind turbine interfacing and remote load feeding applications:

Table 1-2. Requirements of DC-DC converter for remote feeding and offshore interface applications

Specification / Application	Input voltage	Output voltage	Power	Bidirectional Capability	Conversion ratio
Off-shore interface	1 kV-6.6 kV	150 kV	1 MW - 10 MW	Yes Asymmetrical Power	> 10
Remote feeding	50 kV – 100 kV	1 -10 kV	200 kW – 2 MW	Yes (if the village has embedded generator)	> 10

It can be seen from this table that a high voltage-conversion ratio DC-DC converter is required, with a low power rating (< 10 MW). Ideally the converter would be modular, allowing different voltage-conversion ratios and power levels of both the wind-turbine and remote load feeding applications to be accommodated. The aim of this thesis is therefore to evaluate different topologies of DC-DC converters and develop a high-efficiency, high-power DC-DC converter that meets all of the above requirements.

In the next chapter different DC-DC converters topologies will be examined in more detail and their suitability for implementation in high voltage-conversion ratio, megawatt range applications will be evaluated. This evaluation will be based on the need to build the converter using existing power electronic component technologies available in the market. Emerging switched technologies such as wide band-gap devices will be also considered in this evaluation.

2. Overview of DC-DC Converters and Suitability for High-Power and High-Voltage Applications

2.1 Introduction

The aim of this chapter is to review existing switch-mode DC-DC converter topologies and identify their suitability for use in high-voltage and high-power applications.

Switch-mode DC-DC converters have been widely used in DC energy conversion systems for several decades. These converters are primarily used to step up/down voltage and generate a regulated DC voltage from an unregulated DC power supply with very high efficiency. They are also used in applications where a variable DC voltage is required such as DC motor servo drives. Applications for DC-DC converters can range from several milliwatts in integrated circuits applications to several hundred megawatts in DC transmission applications.

Conventional PWM DC-DC converters such as Buck and Boost converters – step-down and step-up respectively - are one of the most widely used topologies and have been extensively used in low-voltage and low-power applications [34]. Several variations of these classical DC-DC converters as well as new topologies have been proposed in order to improve the efficiency, power density and power rating of these circuits [34-36].

High-voltage and low-power DC-DC converters also have been proposed for, for example medical X-ray, food processing, water treatment, high intensity discharge lamps, radio-frequency generation, exhaust gas treatment, ozone generation, travelling-wave tubes, engine ignition and ion implantation [37-40].

High-power and high-voltage DC-DC converters are not commercially available in the market at present; however, due to the need for this type of converter in the near future, particularly for offshore windfarms applications, several research groups all over the world are trying to develop a practical, high-power and high-voltage DC-DC converter with a megawatt power range [29, 41-47].

The next section describes the basic energy conversion mechanism in switch mode DC-DC converters, which gives an insight into the operation of DC-DC converters and hence the issues around using them for high-power and high-voltage applications.

2.2 Switched DC-DC Converters

In switch mode DC-DC converters, one or more conversion stages shown in Figure 2-1 may be required in order to change an input DC voltage/current to an output DC voltage/current.

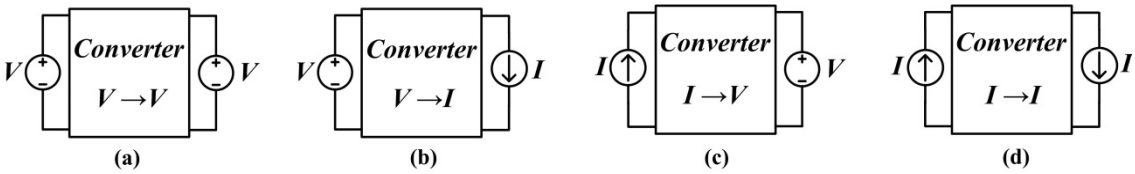


Figure 2-1. Conversion stages of DC-DC converters

Usually the aim of voltage-to-voltage or current-to-current conversion shown in Figure 2-1(a) and (d) is to change the voltage or current levels between the input and the output. In general step up/down operation in switch-mode DC-DC converters is achieved by temporarily storing energy from the input and releasing it to the output at a different voltage or current level. The energy can be stored either in the magnetic field of an inductor or the electric field of a capacitor.

Here we define a voltage-to-voltage or current-to-current convertor, Figure 2-1(a) and (d) as a *transformer* and a voltage-to-current or current-to-voltage convertor, Figure 2-1(b) and (c) as a *gyrator* [48].

We can specify two ways in which these circuits can be used to achieve a voltage or current step-up or step-down function:

1) The cascade of two gyrators, converters (b) and (c) for voltage-to-voltage conversion and (c) and (b) for current-to-current conversion. This will be denoted as an Indirect method.
2) The individual use of converter (a) or (d). This will be denoted as a Direct method.

It should be noted that a similar function can be achieved using a wound transformer based conversion where the conversion stages are DC→AC→wound-transformer→AC→DC. However, in general for voltage-to-voltage conversion this method is usually incorporated into (1) to optimise the utilisation of components in the converter and/or provide galvanic isolation.

The following section discusses the Indirect and Direct conversion methods in more detail.

2.2.1 Indirect Conversion

For voltage-voltage conversion this method uses the cascade of two gyrators, converters (b) and (c) as shown in Figure 2-2, and (c) and (b) for current conversion as shown in Figure 2-3.

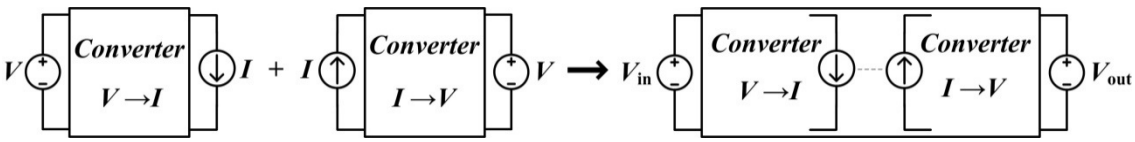


Figure 2-2. Indirect voltage-voltage conversion

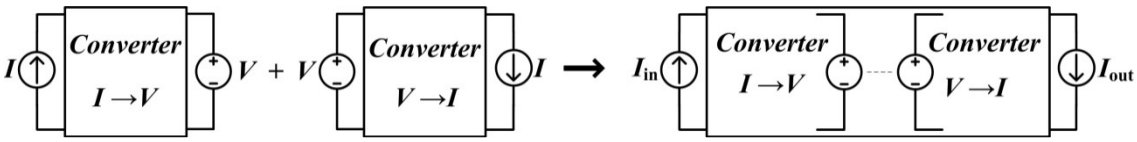


Figure 2-3. Indirect current-current conversion

The Indirect method uses an intermediate source of energy which can be a current source or a voltage source or in some cases a combination of these two. The intermediate energy source for voltage-voltage conversion is a current source, which is implemented by the application of a high-frequency AC voltage waveform across an inductor. The current source then feeds the load, where the magnitude of both the current and load determines the output voltage of the converter. A general circuit for such an inductor based converter, which can step up/down a DC voltage is shown in Figure 2-4. In Boost mode, S_{BOOST} continuously switches between the up and down states, whereas the S_{BUCK} switch is permanently in the up position.

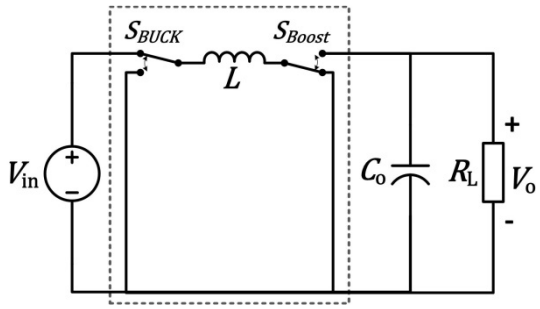


Figure 2-4. Indirect Buck/Boost voltage converter

In Buck mode, switch S_{BUCK} switches between the up and down positions and S_{BOOST} is permanently in the up position.

If all the components are lossless then both the Boost and Buck conversion processes are 100 % efficient. In addition, continuous control of the output voltage magnitude is possible by means of adjusting the duty-cycle of the active switch.

Assuming the inductor current is continuous, then for the Buck converter the inductor current has a DC component which is given by $V_{in}D/R$, where V_{in} is the converter input voltage, D the switch duty cycle and R the load resistance. The inductor can therefore be represented as two averaged current sources as shown in Figure 2-5.

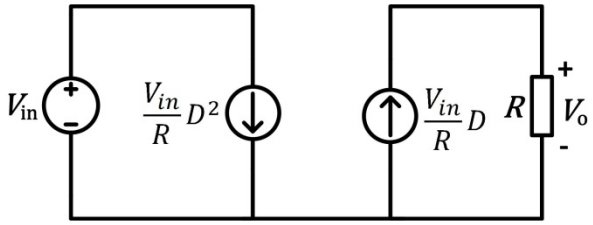


Figure 2-5. Average model of indirect buck voltage converter

The above figure highlights that the converter consists of two cascade gyrator stages. The magnitude of the right-hand currents source is controlled by the duty cycle D, and this source can be used to set the output voltage to any value between $0 \rightarrow V_{in}$. It is the initial conversion of voltage-to-current that is therefore fundamental to this Indirect process of changing the voltage levels between input and output in a lossless manner. A similar averaged circuit can also be derived for the Boost converter.

The circuit for Indirect, Buck and Boost current-current conversion is shown in Figure 2-6. Here a capacitor is used as an intermediate voltage source. In Boost mode, S_{BOOST} continuously switches between the up and down states, whereas the S_{BUCK} switch is permanently in the up position. In Buck mode, switch S_{BUCK} switches between the up and down positions and S_{BOOST} is permanently in the up position.

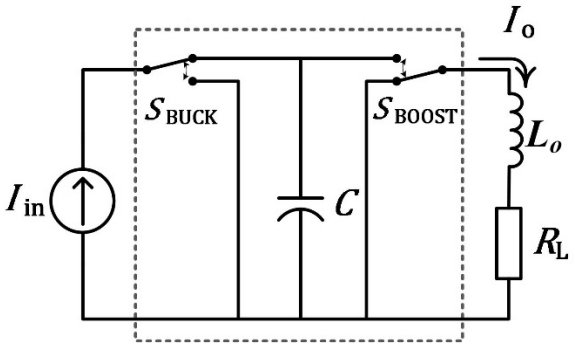


Figure 2-6. Indirect Buck/Boost voltage converter

Continuous control of the output current is possible by means of adjusting the duty-cycle of the active switch. Again if all the components are lossless then both the Boost and Buck conversion processes are 100% efficient. In addition, the averaged circuit is represented by the cascade of current-to-voltage followed by voltage-to-current gyrators.

2.2.2 Direct Conversion

Direct converters do not have an intermediate voltage-current or current-voltage gyrator stage to step up/down a voltage or current. The conversion mechanism in Direct conversion method is completely different from that in the Indirect one. For capacitor based voltage conversion, during part of the switching cycle the energy from the input DC source is transferred to a number of

intermediate capacitors. For the remainder of the switching cycle the topological re-arrangement of the voltage on these capacitors is used to obtain the desired output voltage. Therefore in Direct conversion method only quantised conversion ratios can be attained.

Figure 2-7 shows a simple direct voltage converter where the output voltage V_o is twice the input voltage V_{in}, this converter is commonly known as a Doubler circuit. The switches operate with a fixed duty cycle of 50 %. When S_1 is in the down position and S_2 in the up position, capacitor *C* is charged by the supply voltage to V_{in}. When S_1 is in the up position and S_2 in the down position, the supply and capacitor C are connected in series across the output capacitor C_o and load R_L so that $V_o = 2V_{in}$. The input voltage is therefore boosted by a factor of 2. If the output capacitor and load resistor are interchanged with the supply voltage, then the circuit operates in Buck mode where the input voltage is reduced by a factor of 1/2.

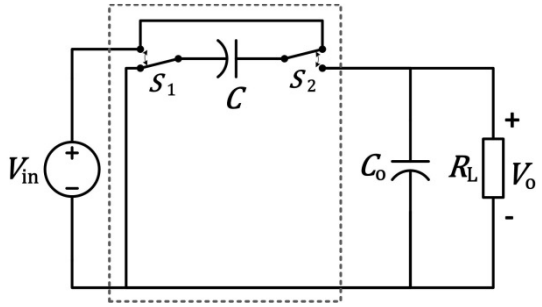


Figure 2-7. Direct voltage Doubler

A similar circuit for direct current conversion is shown in Figure 2-8, which boosts the input current by the factor of 2. In this case, when switch S_1 is in up position and S_2 is in down position, the inductor is immediately charged to the supply current I_{in}. When S_1 is in the down position and S_2 is in the up position, the supply current source is connected in parallel with the inductor and energy is transferred to the output filter inductor and the load so that $I_o = 2I_{in}$.

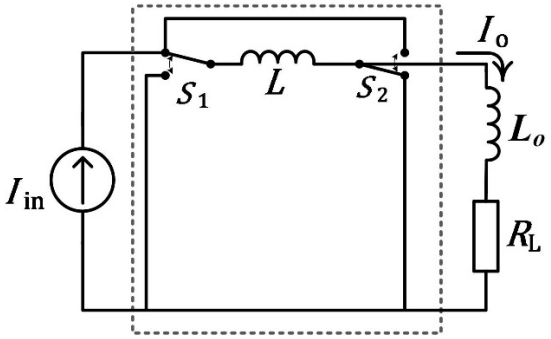


Figure 2-8. Direct current Doubler

Unlike the Indirect conversion method, the energy conversion process in the Direct method is inherently lossy even if the components are ideal. The proof of this can be shown by considering

the energy stored in the capacitors C_1 and C_2 shown in Figure 2-9, before and after the switch *S* operates.

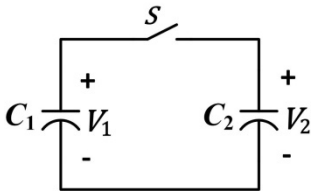


Figure 2-9. Connection of two capacitors with different voltages

If the initial voltage on capacitors C_1 and C_2 is V_1 and V_2 respectively, then the total charge Q_{tot} and stored energy U before the switch operates is given by

$$\begin{aligned} Q_{tot} &= C_1V_1 + C_2V_2 \\ U &= \frac{1}{2}C_1V_1^2 + \frac{1}{2}C_2V_2^2 \end{aligned} \tag{2-1}$$

After switch *S* closes, the total charge and stored energy is given by,

$$\begin{aligned} Q_{tot} &= (C_1 + C_2)V \\ U &= \frac{1}{2}(C_1 + C_2)V^2 \end{aligned} \tag{2-2}$$

where V is the new steady-state voltage on the capacitors. From charge conservation, the total charge on the capacitors Q_{tot} before and after the switch operates must be equal so that from equations (2-1) and (2-2),

$$V = \frac{C_1V_1 + C_2V_2}{C_1 + C_2} \tag{2-3}$$

The energy lost in the circuit ΔU is the difference in the capacitor stored energies before and after the switch has closed, so that from (2-1) and (2-3),

$$\Delta U = \frac{1}{2} \cdot \frac{C_1C_2}{C_1 + C_2} \cdot (V_1 - V_2)^2 \tag{2-4}$$

which shows that if the capacitors voltages before and after the switch is closed are different, then energy is lost during the energy transfer process, which is proportional to the square of difference in the voltage of capacitors before switch operates. The finite energy loss predicted by this equation is counter-intuitive since the components were assumed ideal and the losses would therefore be expected to be zero. However, what is usually overlooked when making this assumption is the radiated loss due to the flow of current around the circuit. This effect is always present; however it is usually small compared with the resistive losses that usually dominate.

Whether radiated or resistive losses are the main loss mechanism, or the two losses are comparable, the total loss is always equal to that given by equation (2-4) [49].

A similar result regarding losses can be derived using flux conservation for Direct current-current conversion where two inductors with different initial currents are connected in series.

Whilst the above discussion has considered Direct DC-DC voltage conversion by capacitors, as mentioned previously DC→AC→wound-transformer→AC→DC stages can also be used to perform this function. Here high-frequency switches working with a fixed 50% duty cycle are used to synthesis the AC waveforms. Just like the capacitor voltage conversion method the conversion ratio is fixed, and is determined by the turns-ratio of the transformer.

2.3 Comparison of Direct and Indirect Methods for High-Power, High-Voltage and High Voltage-Conversion Ratio Applications

The Indirect and Direct conversion methods are compared here in order to assess their suitability for the high-power, high-voltage and high voltage-conversion ratio applications, namely off-shore wind farms and remote load feeding that were discussed in Chapter 1. This comparison is based on the rating and utilisation of the switch, which is commonly the most critical component in HVDC applications. As an example, the conventional Boost converter shown in Figure 2-10(a) which is an Indirect conversion method is compared against the Direct conversion Doubler circuit shown in Figure 2-10(b).

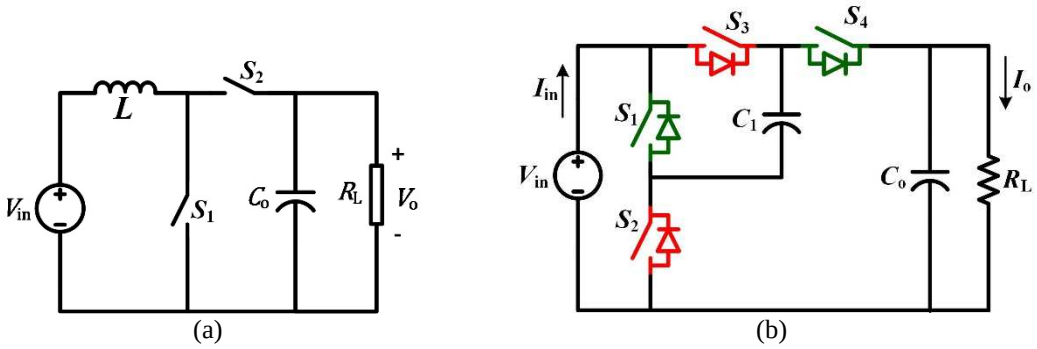


Figure 2-10. (a) Boost converter – Indirect method and (b) Voltage doubler - Direct method

A comparison of the peak voltage and current of the switches for each converter are shown in Table 2-1, where the Boost converter operates with duty cycle 0.5 to achieve a voltage step-up ratio of 2. Also shown is the VA rating of the switch, which is the product of the peak voltage and current. Note that if this VA rating is normalised to the converter input power it corresponds to "switch utilisation" as defined for example in [34].

Table 2-1. Peak voltage, current and VA rating for semiconductor devices for conventional Boost converter and the voltage Doubler

Conventional boost converter				Direct voltage doubler			
Device	**Peak voltage**	**Peak current**	**VA**	**Device**	**Peak voltage**	**Peak current**	**VA**
S_1-S_2	$2V_{in}$	I_{in}	$2V_{in}I_{in}$	S_1-S_4	V_{in}	I_{in}	$V_{in}I_{in}$
	Total Switch VA		$4V_{in}I_{in}$		Total Switch VA		$4V_{in}I_{in}$

The Boost converter has two switches both with voltage ratings of $2V_{in}$ and current ratings of I_{in}. Therefore the total VA rating of the switches is $4V_{in}I_{in}$. The voltage Doubler requires 4 switches all with voltage rating of V_{in} and current rating of I_{in} and therefore it also has a total VA rating of $4V_{in}I_{in}$. In summary, whilst the Boost converter requires individual switches with a higher voltage rating both the converters need the same total overall switch VA of $4V_{in}I_{in}$ to achieve a voltage step-up of 2.

For higher conversion ratios the duty cycle of the Boost converter is reduced, whereas, for the Direct convertor, additional intermediate switch/capacitor stages are required. However, the switch VA rating of the Boost converter becomes much higher than that for the Direct converter. For example, if the voltage conversion ratio is now increased to 8, the Boost converter duty cycle is reduced to 0.125, whereas the Direct convert topology requires two additional cascaded stages and becomes Figure 2-11.

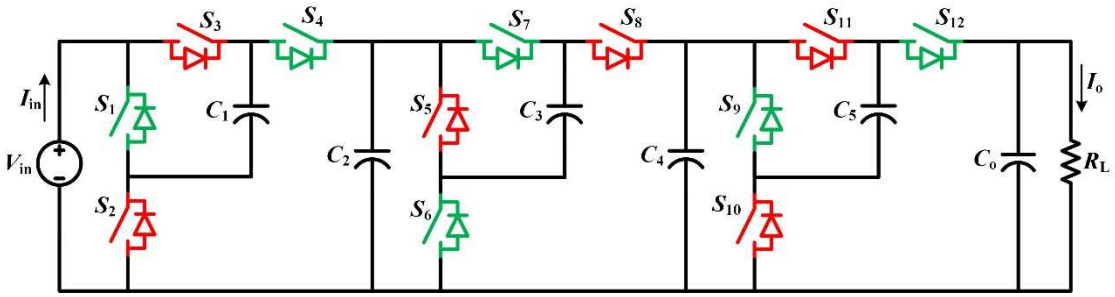


Figure 2-11. Cascaded Doubler with voltage gain 8, Direct method

A comparison of switch ratings for the two converters for a voltage conversion ratio of 8 is shown in Table 2-2.

Table 2-2. Peak voltage, current and VA rating for semiconductor devices for direct voltage Doubler and the conventional Boost converter

Conventional boost converter				Direct voltage doubler			
Device	**Peak voltage**	**Peak current**	**VA**	**Device**	**Peak voltage**	**Peak current**	**VA**
S_1-S_2	$8V_{in}$	I_{in}	$8V_{in}I_{in}$	S_1-S_4	V_{in}	I_{in}	$V_{in}I_{in}$
				S_5-S_8	$2V_{in}$	$I_{in}/2$	$V_{in}I_{in}$
				S_9-S_{12}	$4V_{in}$	$I_{in}/4$	$V_{in}I_{in}$
	Total Switch VA		$16V_{in}I_{in}$		**Total Switch VA**		$12V_{in}I_{in}$

It can be seen that whilst the Boost converter needs two switches with individual voltage ratings that are at least twice the rating of the cascaded Doubler converter, its overall switch VA rating is now 30% higher. As the voltage conversion ratio is increased further so does the difference in the total VA rating of switches. In [50], a similar comparison is made, but based on switch conduction losses for the two converters. However their conclusion remains the same in that the switch VA rating of a Boost converter becomes much higher than Direct conversion as the voltage-conversion ratio is increased.

The expression for the total switch VA rating for a Boost converter to achieve a voltage conversion ratio of *n* can be calculated as:

$$Total\ switch\ VA\ rating = \sum_{Switches} V_{switch} I_{switch} = 2nV_{in} I_{in} \tag{2-5}$$

Where V_{switch} and I_{switch} are the peak voltage and peak current of switch respectively and the number of *Switches* = 2.

The total switch VA rating for the cascaded Doubler converter to obtain a voltage gain *n* is;

$$Total\ switch\ VA\ rating = \sum_{Switches} V_{switchs} I_{switch} = 4V_{in} I_{in} \log_2 n \tag{2-6}$$

where the number of $Switches = \log_2 n$.

Comparison of the total switch VA rating of these converters in terms of voltage conversion ratio is plotted in Figure 2-12, where the VA rating has been normalised to the converter input power. It can be seen that for conversion ratios greater than around 10, the total VA rating for the Boost converter becomes significantly larger than that for the cascaded Doubler circuit, which makes it unsuitable for applications requiring a high voltage-conversion ratio. It should be noted that the VA switch rating of the Boost converter can be significantly reduced by exploiting the AC nature of some of the intermediate conversion stages and adding a wound high-frequency transformer to the circuit to provide the necessary voltage step-up or step-down, for example a Forward converter. However, as already discussed in Chapter 1 high-power, high-voltage, high-frequency transformer technology is not commercially available at present.

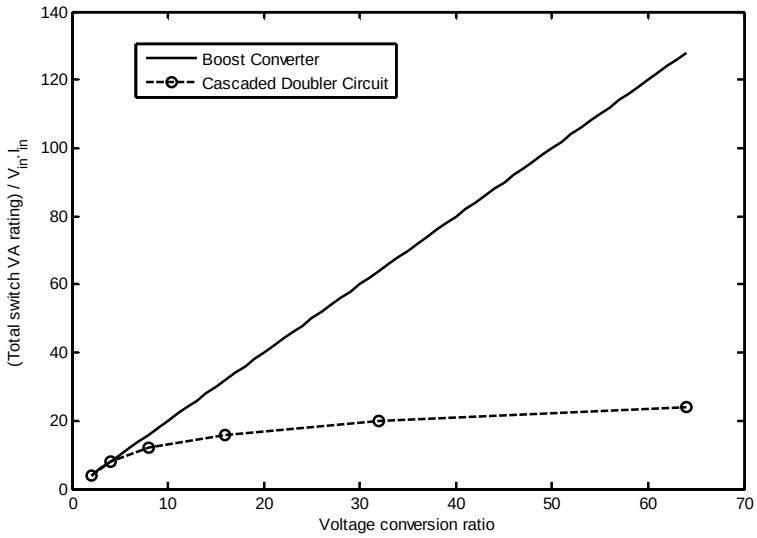


Figure 2-12. Normalised total VA rating of switches for Boost converter and cascaded Doubler circuit

In practice, there are much more suitable circuits for high voltage-conversion ratios than the Boost and Cascaded Doubler circuit used in this example, as will be discussed in the next section. However, the same conclusion remains: Direct conversion is better than Indirect conversion for high-power, high-voltage and high voltage-conversion ratio applications because for step-up conversion,

- **Indirect method**: without a transformer, *all* the switches for an Indirect converter are exposed to both the peak *high* voltage of the output and peak *high* current of the input.
- **Direct method**: a number of capacitors supports the voltage difference between the input and output of the converter. In certain topologies the switches are only exposed to the *low* voltage of the input and the *low* current of the output. The same conclusion can be made for Direct wound transformer based converters.

2.4 Discussion and Overview of Existing Indirect DC-DC Converter Topologies

This section considers only voltage-to-voltage DC-DC converters rather than for example current-to-current, since voltage-to-voltage conversion is needed for the wind-turbine and remote-load feeding applications that were discussed in Chapter 1.

Switch-mode DC-DC converters have been widely used in different applications. Different topologies have been proposed for this family of converters. However, as discussed in the previous section all of these topologies can be divided in to either Indirect or Direct categories, based on the way the input energy is transferred to the load. Most of the topologies use an Indirect

method in order to buck/boost the input voltage as discussed in section 2.2 and some of them can be modified to utilise a high-frequency transformer to reduce the component voltage and current stress between the high voltage and the low voltage sides.

In the following sections different types of existing DC-DC converters will be reviewed in more detail and their suitability for high-power and high-voltage applications will be investigated.

2.4.1 Classical PWM DC-DC Converters

Classical inductor based DC-DC converters are the most commonly used topologies to step up/down an input DC voltage in low power applications. These topologies use the Indirect method in order to buck/boost the input voltage in which the input DC voltage source is converted to a current source using an intermediate inductor and is converted back again to voltage at the output of the converter. This conversion mechanism is essential in order to change the voltage level between input and output in these types of converter. The Buck and Boost converters are the basic classical DC-DC converters, whereas other topologies such as Buck-Boost and Cuk converters are the combination or a derivation of these basic circuits. The Buck and Boost converters mostly use one controlled switch and one uncontrolled switch and due to their simple structure they have been widely used in various low-power applications. In the simple Buck and Boost converters, the inductor acts as a current source drawing power at one voltage level and releasing the power at another voltage level. Depending on the topology and the location of the inductor the output DC voltage can be higher or lower than the input DC voltage. The output voltage in these types of converters can be controlled continuously by adjusting the duty cycle of the active switch.

Figure 2-13 shows the circuit diagram of the Boost converter. In this converter the output voltage is always greater than the input voltage. In theory any voltage gain can be achieved based on the theoretical voltage conversion ratio of the converter given in equation (2-7) below. However due to the high losses in the components with high conversion ratios, and since the switches are exposed to the high current at the input and high voltage at the output, practical conversion ratios are limited to typically less than 10.

$$\frac{V_o}{V_{in}} = \frac{1}{1-D} \tag{2-7}$$

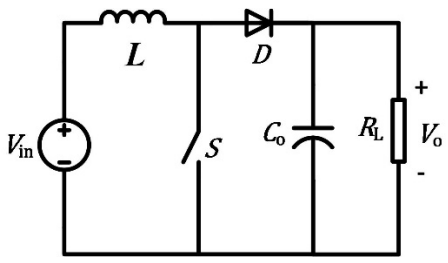


Figure 2-13. Conventional Boost converter

There are also some classical converters which use both an inductor and capacitor as the intermediate energy transferring devices. For example, the Cuk and SEPIC converters, as shown in Figure 2-14, consist of four gyrator stages - voltage-to-current, current-to-voltage, voltage-to-current and current-to-voltage. However the operation mechanism is the same as the basic inductor based circuits.

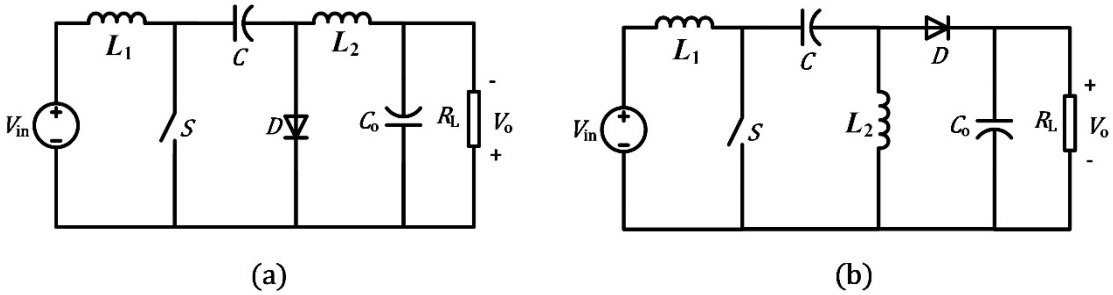


Figure 2-14.Classical inductor based DC-DC converters with intermediate capacitor (a) Cuk converter (b) SEPIC converter

DC-DC topologies such as the Boost converter have a poor efficiency when operating at extreme duty cycle in order to achieve high voltage gain. This is because components such as the inductor and the switch need to be rated at the high voltage side and high current side as discussed in the previous section. This causes excessive losses in the parasitic resistance of the inductor and the switch and excessive reverse recovery losses of the diode. Some techniques have been developed with the aim of increasing the efficiency of the conventional Boost converter to achieve a high voltage conversion ratio without using an extreme duty cycle [51, 52]. For example cascading two converter stages may be considered to increase the conversion ratio. However this increases the complexity and synchronisation of the controllers in the two stages and the stability is a concern. Furthermore, the diode on the high-voltage side has severe reverse recovery losses which degrades the efficiency and generates high EMI noises.

Since the voltage rating of these switches in these types of converter needs to be rated to the high voltage side and the current rating to the high current side, a series and parallel connection of the active switches is required for high-power and high-voltage applications. However, the series connection of active switches such as IGBTs and MOSFETs is very difficult to implement as it requires a complex active gate control system and perfectly matched switch characteristics are needed to ensure equal voltage sharing during both switching and the steady state.

In summary, classical converters have been established and are well developed in low to medium power and voltage applications. However, the extension of their applications to high-power, high-voltage and high voltage-conversion ratios is not practical.

2.4.2 Transformer Based DC-DC Converters

Different topologies of DC-DC converters based on transformers have been proposed. This section provides a brief review of basic transformer based DC-DC converters.

2.4.2.1 Galvanic Isolated Classical DC-DC Converters

A high-frequency transformer can be incorporated into a switch-mode converter to achieve high conversion ratios and provide galvanic isolation. High voltage or current gains can be achieved by adjusting the turns-ratio of the transformer. An example for this type of converter is the Forward DC-DC converter shown in Figure 2-15(a) which is derived from the classical Buck converter. A third demagnetizing winding is required in this configuration in order to reduce the transformer core flux to zero and ensure volt-second balance in each cycle. The energy stored in the core when the switch is on is restored to the input source through the third magnetising winding N_3 when the switch is turned off.

Unlike the Forward converter, the Flyback converter shown in Figure 2-15(b) interrupts the magnetising current when the switch turns-off. The flow of magnetising current then transfers to the secondary winding and the energy stored in the core is transferred to the load.

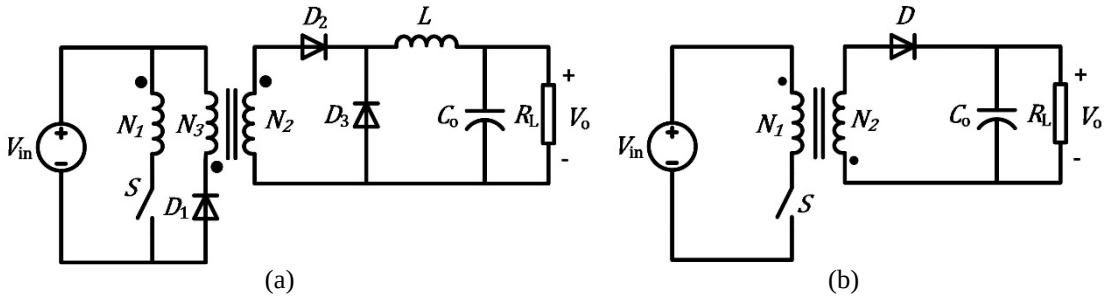


Figure 2-15. Forward DC-DC converter derived from Buck converter

The Forward and Flyback topologies are commonly used in low power DC-DC applications and have unidirectional power transfer capability [53].

Some major issues regarding these topologies for high-power, high-voltage and high voltage-conversion ratio applications are:

- The active switch suffers high switching loss due to the leakage inductance of the transformer.
- A high frequency transformer with high conversion ratio is required which is not commercially available at present.

2.4.2.2 Phase-Shifted Full-Bridge DC-DC Converter

The circuit diagram for the phase-shifted full bridge DC-DC converter is shown in Figure 2-16. The high frequency AC voltage V_{AB} generated by the full-bridge is passed through a high frequency transformer and rectified and then smoothed by a LC filter to produce the output DC voltage. Capacitors are connected in parallel with the switches which are required to achieve soft switching in conjunction with the inductor. The stray inductance of the transformer, shown by inductor L_s in the figure, plays an important role in the operation of the converter. The high frequency quasi square AC voltage, V_{AB}, is produced by phase shifting between leg A and leg B of the full-bridge shown in Figure 2-16. Switches in each leg operate in antiphase mode with duty cycle of 50 % and the voltage generated at the mid-point of each leg V_A and V_B have rectangular waveform as shown in Figure 2-16. Switches in leg B are delayed behind that in leg A by the phase variable β. When $\beta = 0$, V_{AB} and the transferred power is zero, and with $\beta = \pi$, V_{AB} becomes square wave and maximum power is transferred to the output. The frequency of V_{AB} is fixed and is equal to the switching frequency of the converter. The presence of L_s has a significant effect on the operation of the converter, which prevents the instantaneously reversal of inverter output current i_p. During the period α, when the current reversal occur, all diodes in output rectifier are conducting and therefore the phenomenon is known as overlap. The output voltage can be derived by taking the average of the output voltage of the rectifier, V_{DD}, as follow

$$V_o = \frac{nV_{in}}{\pi}(\beta - \alpha) \tag{2-8}$$

where n is the voltage-conversion ratio of the transformer and α can be calculated as

$$\alpha = \frac{nI_oL_s}{\pi f_s V_{in}} \tag{2-9}$$

where f_s is the switching frequency and I_o is the average output current.

The minimum load restriction for soft switching operation of the converter can be calculated as follows,

$$I_O \geq \frac{V_{in}}{nZ} \tag{2-10}$$

where $Z = \sqrt{L_s/2C_A}$. Therefore during light loads the converter may not operate in soft switching.

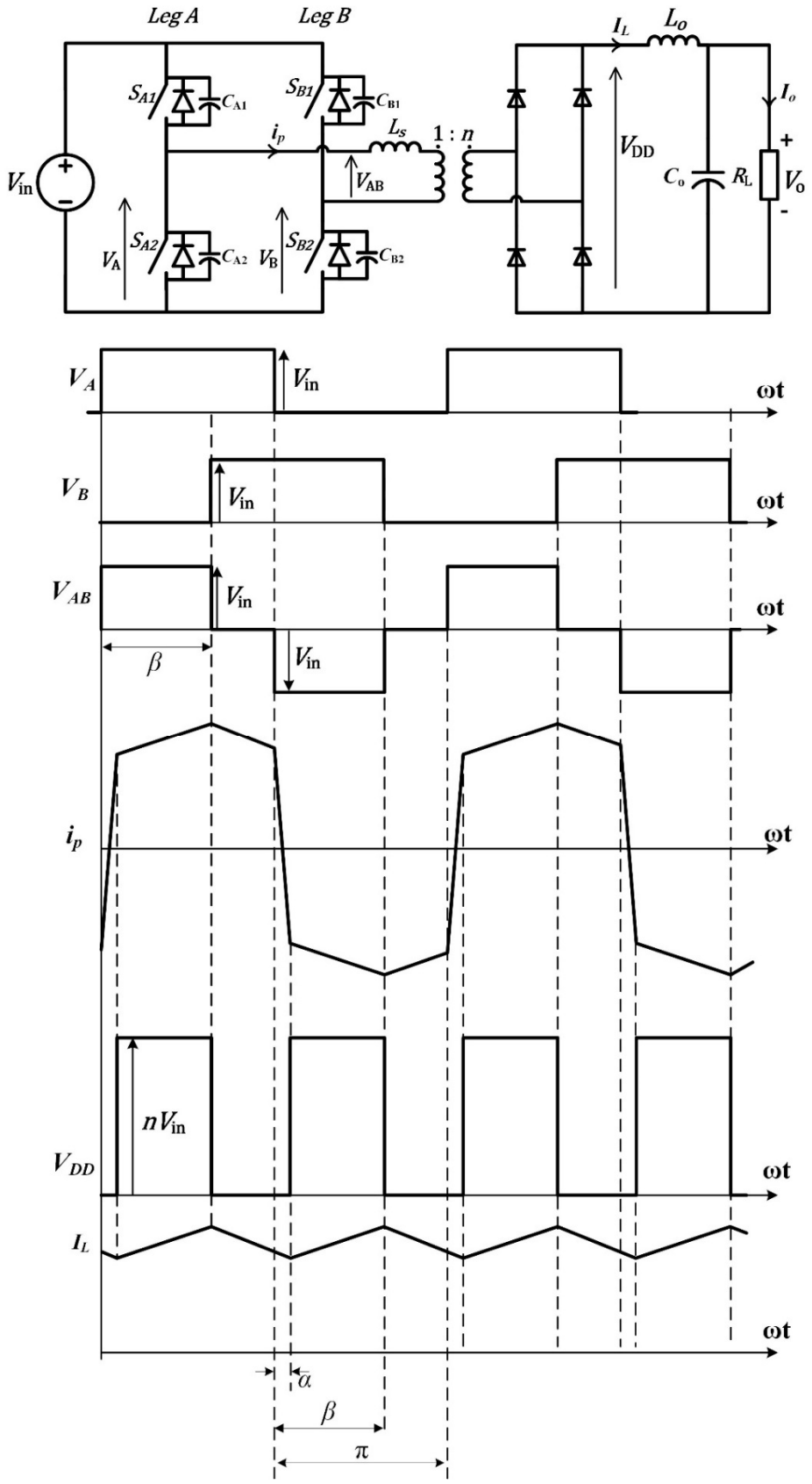


Figure 2-16. Circuit diagram and idealised circuit waveforms for phase-shifted full bridge DC-DC converter

2.4.2.3 Single Active Bridge (SAB) Converter

Transferring the output filter inductor of the phase-shifted, full-bridge converter to the AC side of the rectifier changes the operation characteristics [36], and this converter is known as a Single Active Bridge (SAB). Figure 2-17 shows the circuit topology of the SAB converter. Similar to the phase-shifted, full-bridge converter the input DC voltage is inverted to a quasi-square AC voltage. This voltage drives the high-frequency transformer which steps up/down the voltage to the desired value. An energy-storage inductor is connected on the primary side of the transformer, which may utilise the leakage inductance of the transformer. The voltage at the secondary side of the transformer is converted back to DC using a diode rectifier and further filtering is provided by the capacitor. The idealised operating waveforms for this converter are shown in Figure 2-17. Soft switching is achieved by ensuring that the device antiparallel diode is conducting when the device turns on. The DC voltage conversion ratio of the converter is given by,

$$\frac{V_o'}{V_{in}} = \frac{\beta - 2\varphi}{\pi} \tag{2-11}$$

In (2-11) V_o' is the output DC voltage of the converter referred to the primary side of the transformer where n is the turns-ratio of the transformer and φ is rectifier overlap angle defined in Figure 2-17.

Soft switching operation is achieved when,

$$\beta - d\pi \geq 0 \tag{2-12}$$

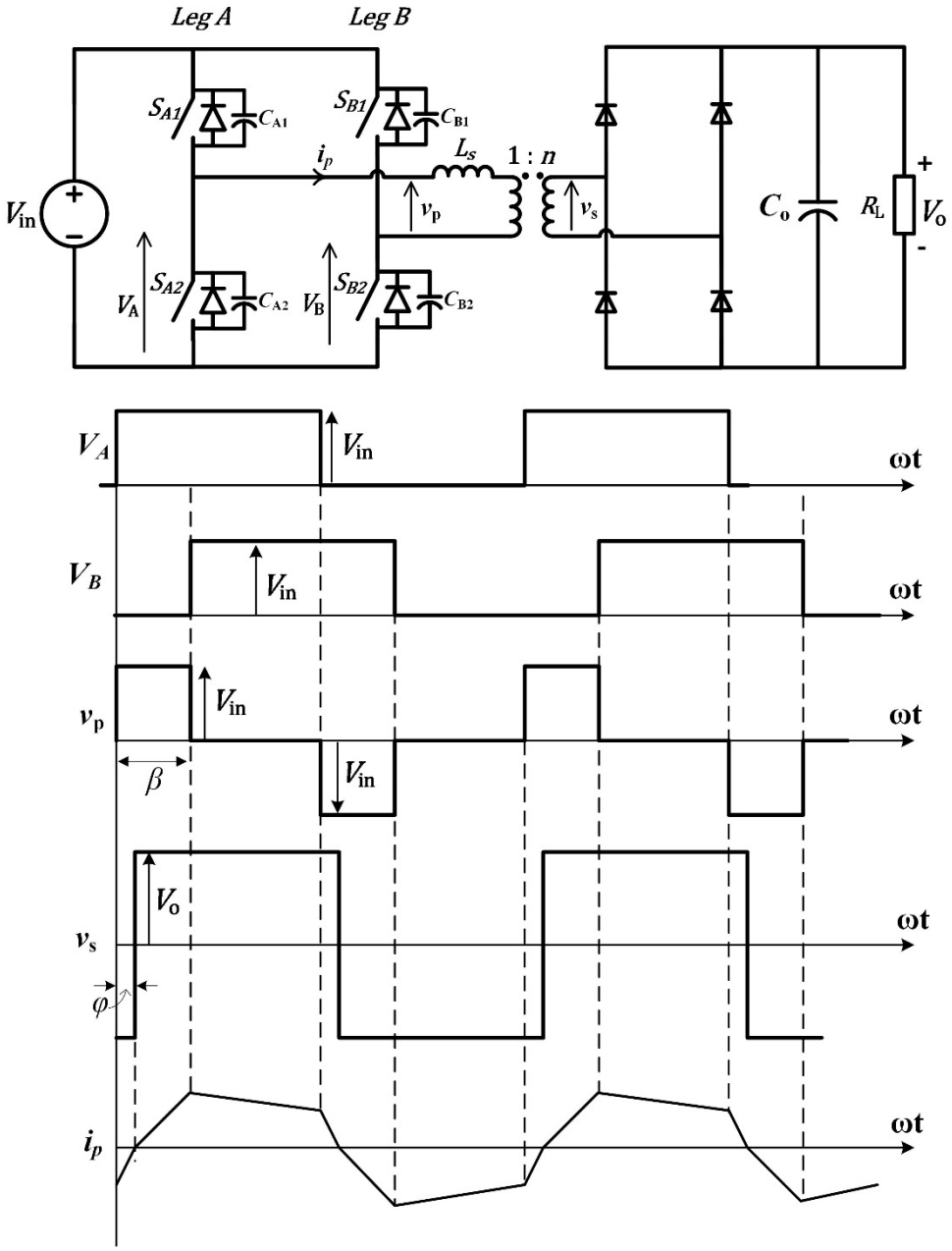


Figure 2-17. Circuit topology of single active bridge converter

2.4.3 Dual Active Bridge Converter

The circuit topology of a Dual Active Bridge (DAB) converter is shown in Figure 2-18. The output diode rectifier that appears in the SAB is replaced by an active bridge in this converter. This gives several advantages over the SAB converter. A phase-shift φ between the switching waveforms of the input and output bridges on the primary and secondary sides of the transformer as shown in Figure 2-18, is used to control the converter power flow and output voltage regulation. Furthermore this converter does not suffer from the diode reverse recovery losses as

occurs in the output rectifier of the SAB converter. The output power equation P_o for the DAB converter is given by,

$$P_o = \frac{nV_{in}V_o}{\omega L_s}\varphi\left[1 - \frac{\varphi}{\pi}\right] \tag{2-13}$$

From which an expression for the converter output can be obtained,

$$V_o = \frac{nV_{in}R_L}{\omega L_s}\varphi\left[1 - \frac{\varphi}{\pi}\right] \tag{2-14}$$

A plot of the output power of the converter P_o, which has been normalised by $V_{in}^2/L_s\omega$ and is denoted by $P_o(p.u.)$, as a function of phase shift φ is shown in Figure 2-19.

The DAB converter utilises the inductance L_s and the parasitic output capacitance of the switches [29, 36, 54, 55] for soft-switching. Again, as with the SAB, one of the major disadvantages of the DAB is that soft switching operation is not achievable for the entire control range as shown in Figure 2-19, which is restricted by the voltage conversion ratio [56]. The soft-switching region is constrained by the following equations,

$$\begin{aligned} \varphi &\geq \frac{\pi}{2}\left(1 - \frac{1}{d}\right) \quad Input\ bridge\ constraints \\ \varphi &\geq \frac{\pi}{2}(1 - d) \quad Output\ bridge\ constraints \end{aligned} \tag{2-15}$$

Different PWM control techniques have been proposed to extend the soft-switching control region of the converter [57-59]. However these techniques are complex and need an optimisation procedure to define duty cycles and the phase-shift between the bridges.

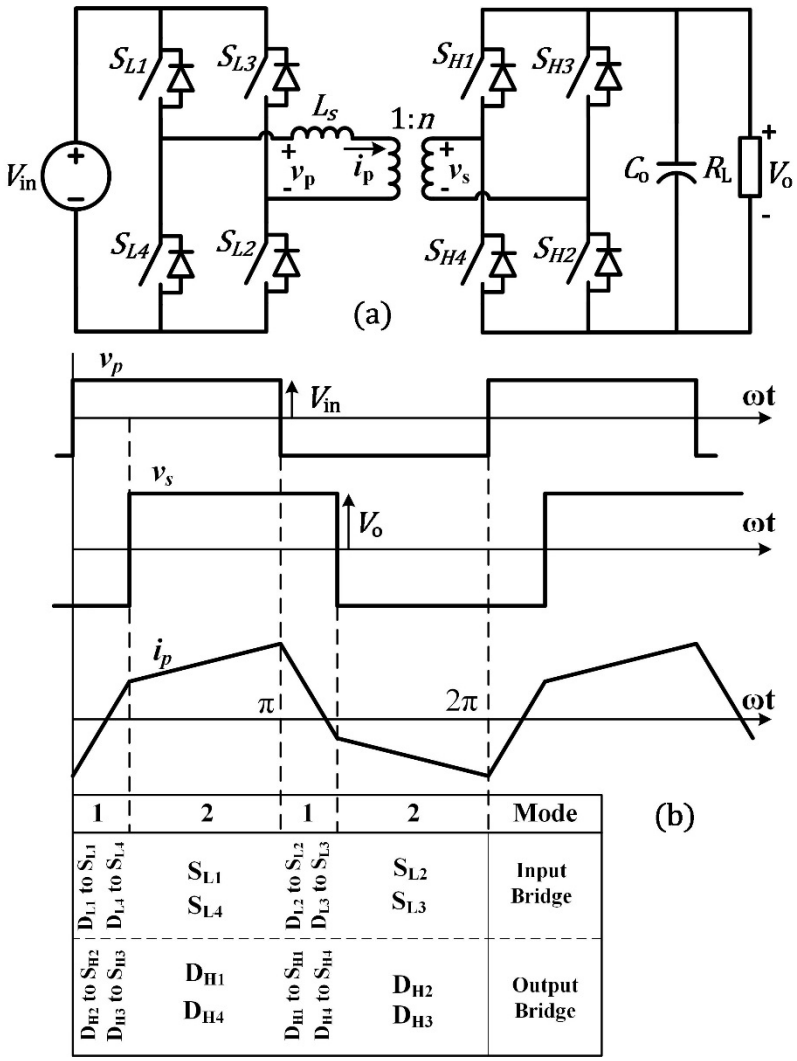


Figure 2-18. Circuit diagram for Dual Active Bridge Converter and waveforms

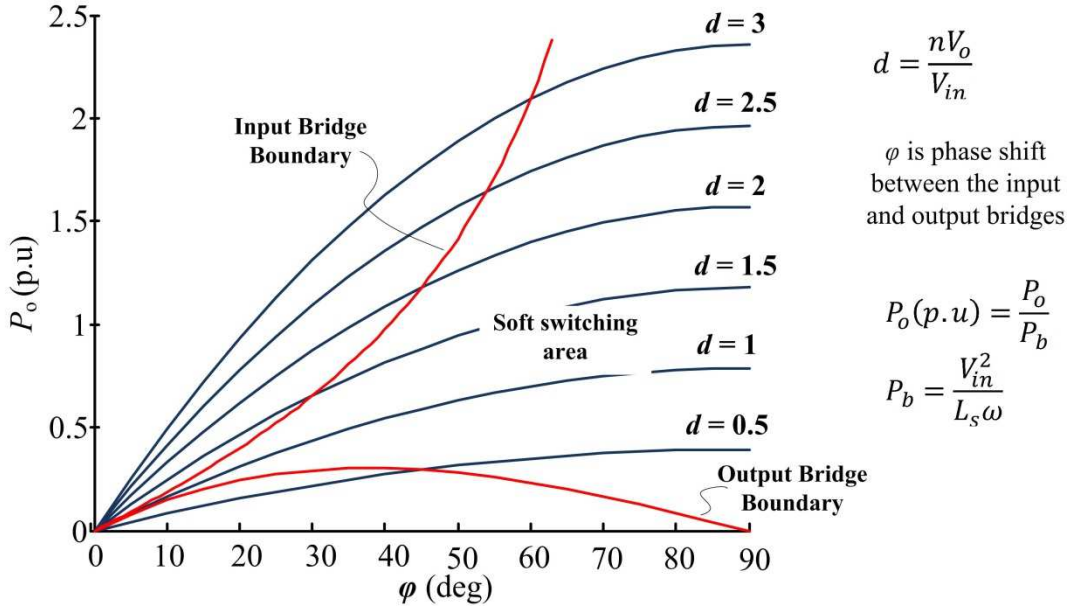


Figure 2-19. Soft switching operation area of Dual Active Bridge Converter

2.4.4 Discussion of Phase-Shifted, Full-Bridge, SAB and DAB Converters

In terms of the wind-turbine and remote load feeding applications that are the main objectives this project, then the phase-shifted, full-bridge, SAB and DAB converters suffer from the characteristic that soft-switching is not achieved over the complete range from zero to full-load. In particular the SAB and DAB have very narrow soft-switching ranges, making them unsuitable for the wind-turbine applications. This is a serious disadvantage for high power converters operating at medium to high switching frequencies. In addition, the phase-shifted, full-bridge and SAB require a medium to high-frequency transformer to step-up the voltage and these types of transformers are not commercially available at present. Whilst in theory the DAB doesn't require a transformer for voltage step-up, at high voltage-conversion ratios, for example $d > 10$, the operating range for soft-switching of the input bridge approaches zero. Furthermore, since the DAB is an Indirect converter, the input and output switches are exposed to both the peak *high* voltage of the output and peak *high* current of the input.

2.4.5 Resonant DC-DC Converters

Resonant converters can operate at high switching frequencies due to the inherent soft-switching operation of the circuit. In these converters a bipolar, square-wave voltage is produced by a half bridge or full bridge converter, and this waveform is then applied to a low-pass filter resonant LC network, known as a tank circuit, and a sinusoidal current is then drawn from the bridge. A high-frequency transformer can be inserted after the LC tank to step up/down the voltage level and provide galvanic isolation. Soft-switching allows the converter to operate at very high frequency so that the size of the transformer and other reactive components can be reduced considerably. Output voltage control is achieved by varying the converter switching frequency.

Resonant converters are generally classified into three types based on the resonant tank network: the Series Resonant Converters (SRC), Parallel Resonant Converters (PRC) and the Series Parallel Resonant Converters (SPRC).

A resonant converter topology is very similar to the SAB converter. However there is a resonant capacitor connected either in series or parallel with the high-frequency link transformer. The switching frequency of the converter is set close to the resonant frequency of the LC tank. This results in a sinusoidal current waveform flowing through the switches and the transformer. The advantages of using a sinusoidal current when compared to other converters is that the losses in the transformer are reduced since high frequency current harmonics are eliminated, which can cause additional copper and core losses. More importantly, by operating the converter above resonance, a phase angle is established between the switch voltage and current waveforms, which ensures natural soft-turn-on of the transistor and soft turn-off the opposing anti-parallel diode. However, the switch turns-off with a large current causing losses and unconstrained di/dt and

dv/dt. This can be overcome by placing a simple capacitor snubber across the transistor, where the energy stored in this capacitor is recovered in a natural, lossless manner just prior to when the device turns on again.

2.4.5.1 Series Resonant Converter

With the SRC converter shown in Figure. 2-20, the current in the power devices decreases as the load decreases. The output DC voltage is obtained by rectifying and smoothing the resonant voltage using a filter capacitor. A transformer is needed to step-up the voltage as the maximum voltage-conversion ratio without a transformer is 0.5. With the SRC the stray inductance of the transformer can form part of the resonant tank and unlike the SAB and DAB converters, the maximum power transfer capability is limited by the current rating of the devices only. The SRC converter is more suitable for high voltage applications than the parallel resonant converter, since the rectifier off-state voltages are clamped to the output voltage, V_o. One of the major disadvantages of the SRC converter for high power application is that a large filter capacitor is required in order to filter the high current ripple. Another disadvantage is that the output voltage cannot be controlled at light to zero load, making it a possible disadvantage for wind turbine applications. However, the main problem with this converter, which discounts it from further study is the need for a high-frequency, high-power transformer, which is not commercially available at present.

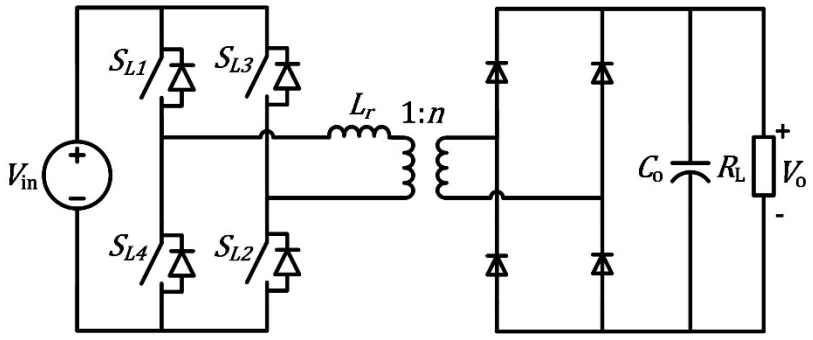


Figure. 2-20. Series resonant converter

2.4.5.2 Parallel Resonant Converter

The circuit topology for the Parallel Load Resonant (PRC) converter is shown in Figure 2-21. The main disadvantage of this converter is that the current through the power devices is approximately independent from the load and thus the efficiency of the converter is poor for light loads. The output DC voltage is obtained by rectifying the sinusoidal capacitor voltage and smoothing by a LC filter. This converter is suitable for high output current since the current is smoothed by the filter inductor which limits the ripple current in the filter capacitor.

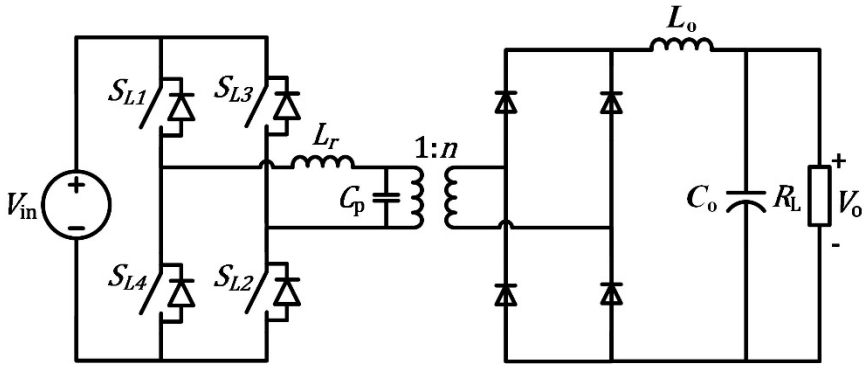


Figure 2-21. Parallel resonant converter.

The maximum voltage-conversion ratio of the converter at resonance is equal to the half the quality factor *Q*, of the LC tank. However for the voltage-conversion ratios required for the applications considered in this thesis, typically > 10, this leads to impractically high values of $Q > 20$ and a medium to high-frequency transformer is needed to achieve voltage step-up. Furthermore, since the PRC is an Indirect converter, without a transformer the input and output switches would be exposed to both the *high* voltage of the output and *high* current of the input. Furthermore, this converter is not suitable for high voltage applications, since the rectifier off-state voltages can exceed the output voltage due to presence of the transformer stray inductance. The PRC is therefore neglected from further investigation.

2.4.5.3 Series Parallel Resonant Converter

The Series-parallel resonant converter is the combination of series and parallel resonant converters which takes the advantages of both circuits [60-62]. By appropriate selection of the resonant components it is possible to control the output voltage at no-load as with the parallel load resonant converter. In addition, the current carried by power components will be reduced at low-load as with series resonant converter. These converters are generally classified into LLC and LCC converters based on the number of resonant components and circuit configuration. Figure 2-22(a) shows the structure of an LCC resonant converter.

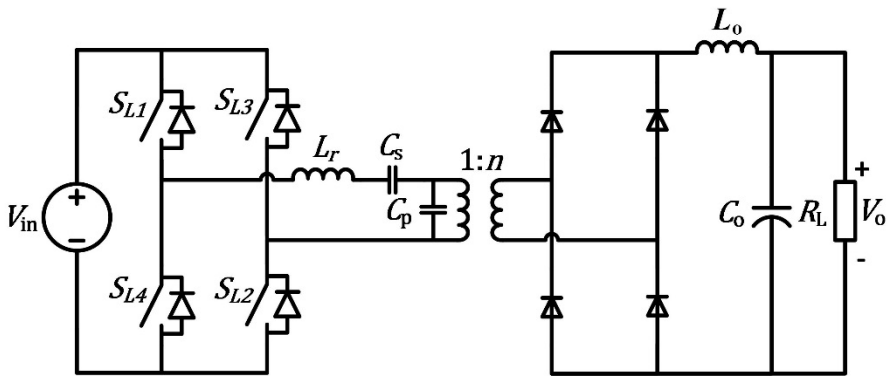


Figure 2-22. . LCC Series-Parallel resonant converter

Whilst the series-parallel converter overcomes many of the problems associated with the series and parallel resonant converters, this is not enough to overcome the problems associated with the need for a medium to high-frequency, high-power transformer.

2.4.6 Isolated Series-Parallel DC-DC Converters

In order to achieve high-power, high-voltage and high conversion-ratio DC-DC conversion, it is possible to connect the converters discussed in the previous sections in parallel on the low voltage side and in series in high voltage side as shown in Figure 2-23.

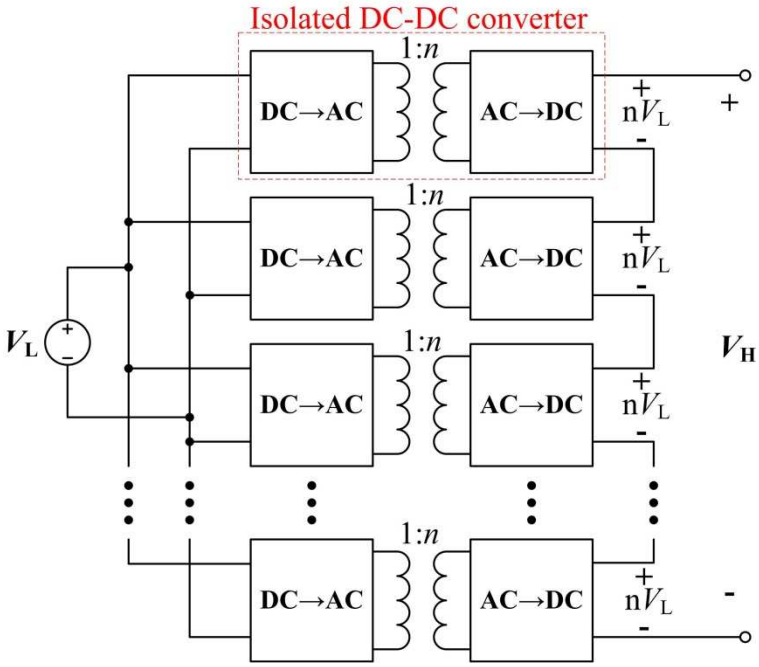


Figure 2-23. Input-parallel output-series DC-DC configuration

This arrangement reduces the voltage and current stress on the switches and offers several other advantages over a single converter structure. In general, low-voltage and low-power modules can be connected in any series or parallel combination in order to achieve the required input and output voltage and current ratings. Furthermore, redundancy can be added to improve the reliability of the converter. However the main drawback of this configuration is that it requires galvanically isolated DC-DC converter modules. Whilst for a converter with n sub-converters the power rating of each sub-converter transformer is just $1/n$ of the overall rating, the voltage isolation between the primary and secondary windings must be rated at the high-voltage side of the converter. Such a high-frequency, high-voltage transformer does not exist at the moment for HVDC voltage range applications. The converter arrangement shown in Figure 2-23 has been proposed in [29, 32] and a single module was designed and experimentally tested using a 20 kHz and 166 kW isolating transformer. However the transformer isolation voltage requirement was not included in the design.

2.5 Direct Conversion DC-DC Topologies

The family of converters that use a Direct conversion method for DC to DC voltage transformation are known as Switched Capacitor (SC) converters. These converters do not rely on intermediate voltage to current gyrator stages to change the voltage level. For voltage-to-voltage conversion this means that an intermediate inductor is not needed to increase or reduce the input DC voltage. However, inductors may be included in the structure of these converters for soft switching operation which are known as resonant switched capacitor converters. Unlike Indirect conversion where the inductor is used to store the energy in one switching cycle and release that energy to the load at a different voltage level, in resonant SC converters there is no stored energy in the inductor at the beginning and the end of each switching cycle.

2.5.1 LCL DC-DC Converter

Recently a new DC-DC converter topology was proposed for megawatt range power applications [63, 64], using a so-called rotating capacitor method for voltage step-up. The converter uses thyristors as active switches as shown in Figure 2-24, which has the advantage that they can be directly connected in series to form a single high-voltage valve. Also all the switches operate under zero current switching, so the switching losses of this converter are low. The energy is transferred to an intermediate capacitor C_r using the resonant circuit formed with inductor L_r, switches T_1 and T_2 are then used to reverse the polarity of the capacitor to receive the next resonant charge. Rectifier diodes D_1 and D_2 are used to rectify the capacitor voltage, which is filtered by capacitor C_o, which supplies a load R_{Load}.

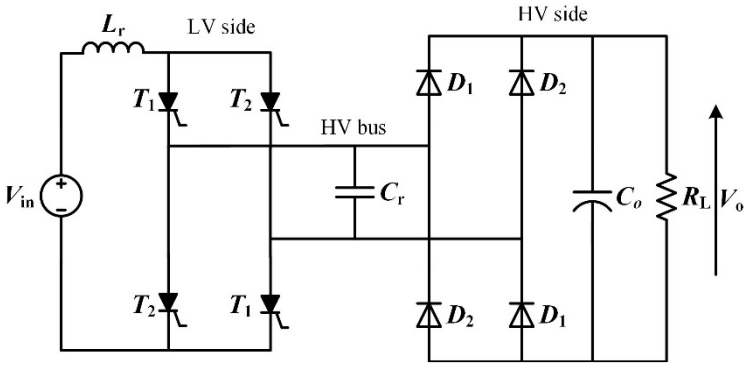


Figure 2-24. Unidirectional hybrid resonant step-up converter proposed in [63] (V_1<V_2).

Figure. 2-25(a) shows the equivalent circuit of this converter in each switching cycle. The equivalent circuit is a simple LC resonant circuit with negative initial voltage for the capacitor V_{cr_0}. Current and voltage waveforms for the circuit current i_{in} and the capacitor voltage v_{cr} are shown in Figure. 2-25(b). At $\omega t = \pi$ the inductor current become zero and the thyristor blocks

the current to flow in the reverse direction and the capacitor voltage is increased by $2V_{in}$ regardless of its polarity.

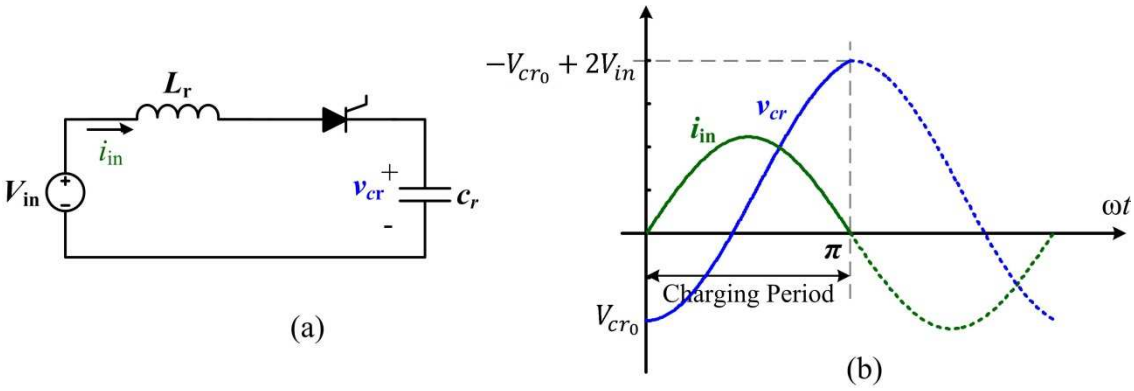


Figure. 2-25. (a) Equivalent circuit for each switching cycle of LCL converter (b) Current and voltage waveforms

By rotating the capacitor using a bridge the same process can be repeated and the voltage can be increased again by $2V_{in}$ and by continuous rotation of the capacitor very large step-up voltages can be achieved.

For accurate operation of this circuit, the switches should have a reverse blocking capability, however a turn-off capability is not required and thus thyristors can be used. The capacitor C_r is rotated by sequentially firing the T_1 and T_2 pair with a 50% duty cycle.

For no-load operation, the voltage on the capacitor C_r and the output voltage are increased by $2V_{in}$ in each switching period. However by connecting a load the main design equation of this converter in steady-state which can be derived from the transferred energy through the converter and assuming lossless converter is,

$$\frac{I_o(V_o - V_{in})}{V_{in}V_o} = 2C_r f_s \tag{2-16}$$

Where I_{out} is the high voltage side average current, V_{in} and V_o are the DC voltages at the low voltage and the high voltage sides respectively and f_s is the switching frequency. This equation also shows the controllability of the converter through the switching frequency f_s.

The voltage gain of the converter for high conversion ratio ($V_{in} \ll V_o$) can be obtained as follow:

$$\frac{V_o}{V_{in}} = 2R_L C_r f_s \tag{2-17}$$

One of the most significant disadvantages of this topology is that the thyristors in the low voltage side, which carry a high current ($I_{in} = nI_{out}$, where n is DC conversion ratio), should have a capability to withstand the resonant capacitor's peak voltage, which is approximately equal to

the high voltage side DC level. Therefore high conversion ratios cannot be realised with this converter because of the very high conduction losses in the low voltage side switches.

A bidirectional variation of this converter is also proposed in [64]. Two hybrid resonant circuits with bidirectional switches sharing a common capacitor are connected back-to-back to form the circuit shown in Figure 2-26, where V_1 is the primary side DC voltage, V_2 is the secondary side DC voltage, L_f and C_f are filter inductor and capacitor respectively and L_r and C_r are the resonant components. However, again the bidirectional configuration suffers from high switch conduction losses on the low voltage side and as the conversion ratio increases, the converter efficiency decreases significantly.

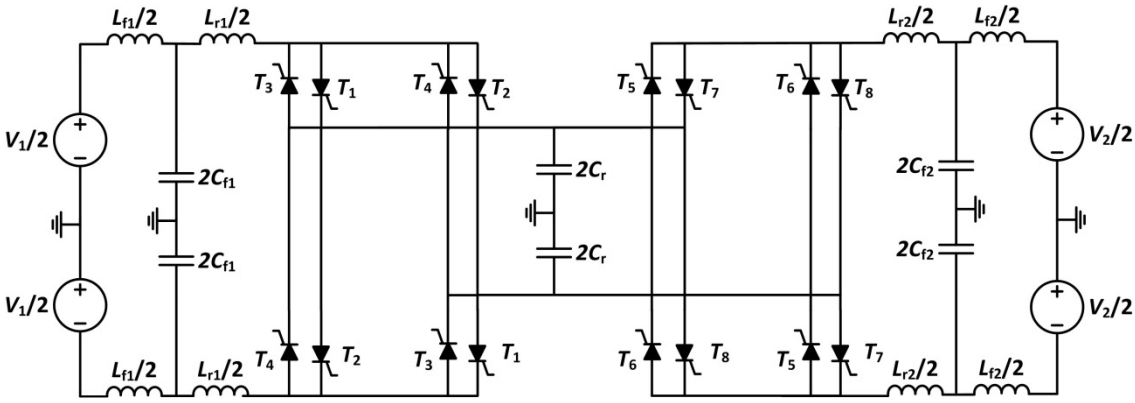


Figure 2-26. Bidirectional step up/down LCL resonant DC-DC converter proposed in [64]

2.6 Summary of Suitability of Existing Circuits for High Voltage Conversion Ratio, High-Voltage and High-Power Applications

In summary, none of the Indirect topologies discussed in 2.4 are suitable for high voltage-conversion ratio, high-voltage and high-power applications for the following reasons:

- Non-isolated Indirect based topologies require high-voltage and high-power switches on the low and high voltage sides of the converter which leads to poor switch utilisation and poor conversion efficiency for high voltage-conversion ratios.
- The practical implementation of a single high-voltage, high-power switch through the series connection of lower voltage devices is very challenging especially for IGBTs, and leads to increased switching losses.
- Many of the circuits require a medium to high-frequency transformers to either step up/down the voltage or improve the switch utilisation. However, the practical design of these transformers in megawatt range applications is a challenging issue and no such components are available commercially or have been successfully demonstrated in the literature.

Whilst the so-called Direct, rotating capacitor topology described in the previous section has a number of drawbacks for HVDC applications, nevertheless it does offer several significant advantages compared with the Indirect circuits. However, Alstom Grid has already been in discussion with Dr. Dragan Jovcic at Aberdeen University, UK, who was responsible for developing this circuit, and further investigation is outside the scope of this thesis.

Switched Capacitor (SC) converters, which will be discussed in the remainder of this thesis, promise to overcome the problems around Indirect converters and the Direct rotating capacitor converter. The voltage stress between the low and high voltage sides of a SC converter is achieved using a network of low-power and low-voltage switches and capacitors, which inherently share the voltage between individual components. This is a significant advantage for high voltage-conversion ratio, high-voltage and high-power applications.

2.7 Switched Capacitor Converters

2.7.1 Introduction

Switched capacitor converters have been widely used in integrated circuits to change voltage levels without using an intermediate inductor or transformer [65, 66]. These converters use the Direct conversion method to step-up/down the input DC voltage. As discussed in section 2.2.2 voltage conversion in the Direct method is achieved in a different manner compared to the Indirect method and there is no need for voltage to current conversion in order to boost the voltage. Unlike inductors, capacitors can be integrated in silicon, which is the reason most on-chip, low-power DC-DC conversion in integrated circuit applications uses SC converters. The energy density of a capacitor is higher than an inductor which makes SC converters an attractive alternative to inductor based converters where the size and the weight of the converter is the limiting factor. They therefore offer a more power dense solution and compact design than inductor based circuits, which is highly-desirable for low-weight EVs or off-shore HVDC collector platforms [43, 47, 67].

The operation of an SC converter is best explained using a simple example: the SC switching period is split into two phases, in the first phase a number of capacitors *n*, are connected in parallel and charged from an input voltage source V_{in}. In the second phase the capacitors are re-connected in series by means of a switched network so that the voltage that appears across them is nV_{in}. Since this voltage conversion can be achieved with a network of low-power and low-voltage switches instead of a number of single, high-power and high-voltage switches, this makes them very desirable in high-power, high voltage-conversion ratio applications.

The switching period of an SC converter is split into two phases. Switches are grouped into two switch banks, which are operated in anti-phase as shown by the gate signals in Figure 2-27, with

a small dead-band to prevent shoot-through between the switches in each bank. Capacitors can be reconfigured in any desired series/parallel combination to produce the required output voltage, which is therefore quantised as an integer multiple or divisor of the input voltage.

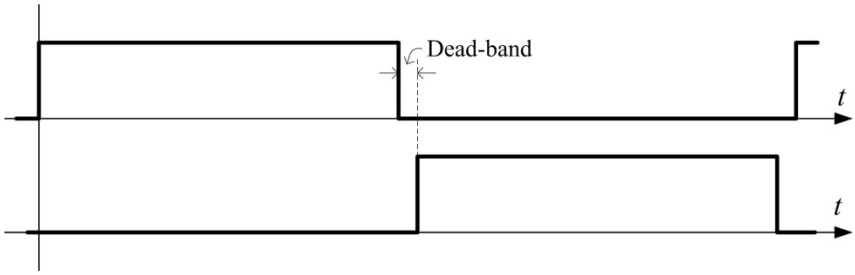


Figure 2-27. Gate signals for switch banks in SC converters

Different topologies have been proposed so far for SC DC-DC converters. It will be shown that all SC topologies can be built from the same basic cell [68], which will be presented in the next section.

2.7.2 Basic Cell, Well Known SC Topologies and Suitability for Medium/High Power Applications

2.7.2.1 Basic Switched Capacitor Cell

It is proposed that all SC topologies can be derived from the basic cell shown in Figure 2-28. The cell is a network of four switches two of which are controlled independently and the remaining two are controlled as a pair. The switches are denoted $S_1 - S_3$. The cell also contains one capacitor and has six terminals $T_1 - T_6$.

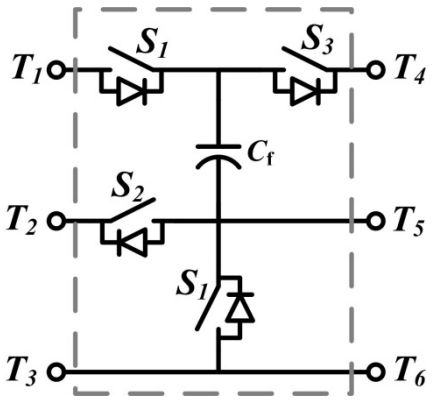


Figure 2-28. Switched Capacitor basic cell

With appropriate interconnections of a number of these basic cells a desired step up/down conversion ratio can be achieved. For example Figure 2-29 shows how simple basic operations such as addition, subtraction, isolation and inverting presented in [68], can be achieved with the basic cell shown in Figure 2-28. The red switches numbered 1 operate in anti-phase with the green switches denoted by 2, and all have a 50% duty cycle. The internal cell capacitor is denoted

C_f and the output filter capacitor C_o has an output voltage V_o. The voltage addition circuit shown in Figure 2-29(a) can be found in the structure of most of the well known SC topologies, and produces an output voltage which is the sum of the input voltage sources V_1 and V_2. In this circuit when the switches numbered 1 are on, the internal capacitor C_f is charged by the supply voltage to V_1. When switches bank 2 are on, the input voltage V_2 and capacitor C_f are connected in series across the output capacitor C_o so that $V_o = V_1 + V_2$.

The voltage doubler circuit shown in Figure 2-29(b) is a derivative of the addition circuit, where the second input terminal is connected directly to the first terminal so the output voltage will be $V_o = V_{in} + V_{in} = 2V_{in}$.

The in-phase isolator circuit shown in Figure 2-29(c) where the output voltage is equal to the input voltage, provides isolation between the input and output. In the first cycle when the switches bank 1 are on, the internal capacitor C_f is charged by the input DC supply to V_{in}. In second cycle, the internal capacitor C_f is connected in parallel with the output capacitor and transfers the charge to this capacitor so that $V_o = V_{in}$.

The inverse-phase cell shown in Figure 2-29(d) allows the polarity of the input voltage to be reversed at the output so that $V_o = -V_{in}$.

Subtraction can be achieved by exchanging the output capacitor and the input voltage V_1 in Figure 2-29(a) as shown in Figure 2-29(e), where the output voltage is $V_o = V_1 - V_2$.

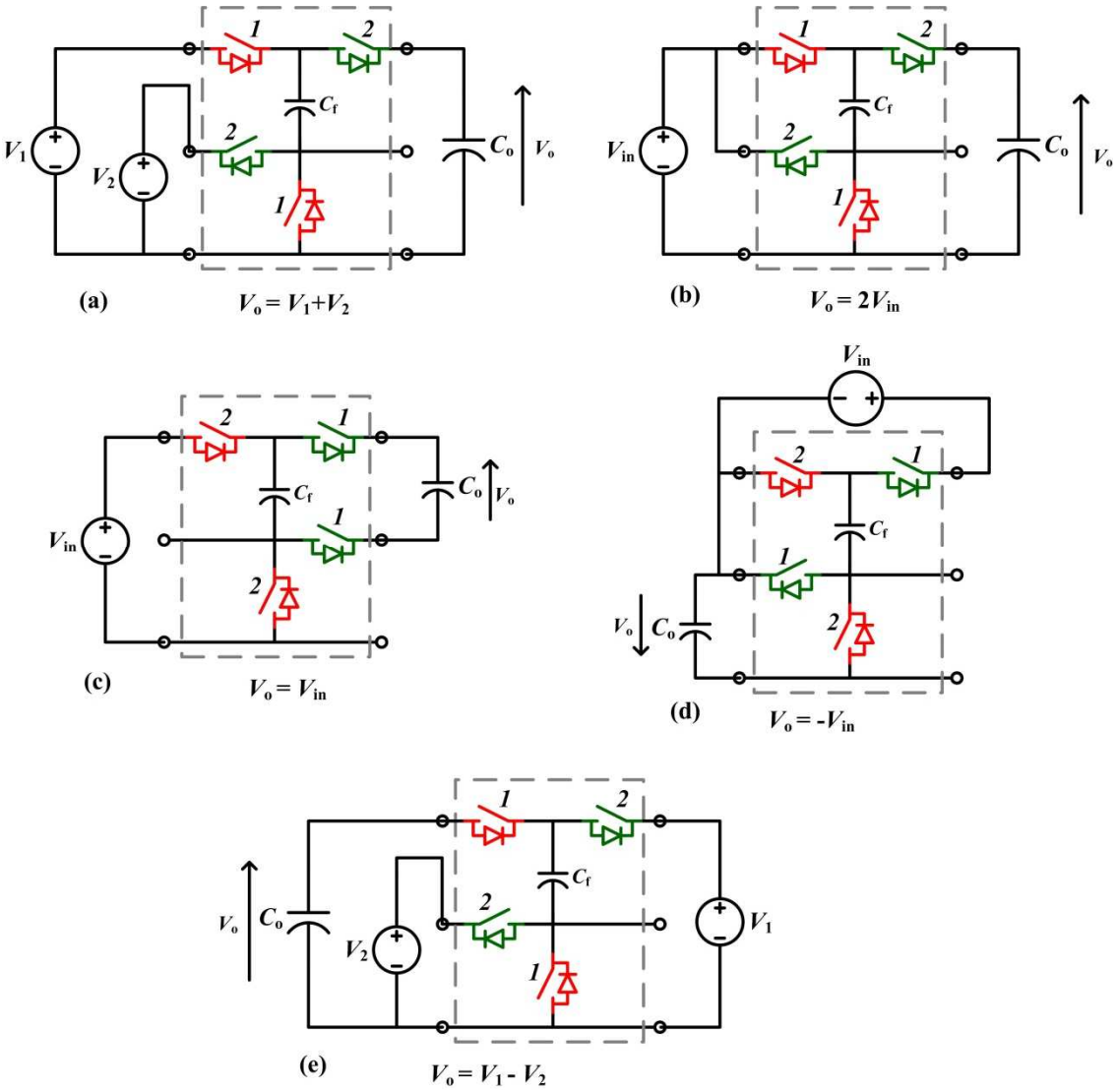


Figure 2-29. Simple SC circuits derived from a single basic SC cell (a) voltage addition cell (b) voltage doubler (c) in-phase isolator (d) inverse phase (e) voltage subtraction

2.7.2.2 Traditional Switched Capacitor Converters

This section reviews the traditional SC converters. It will be shown how these topologies are synthesised from some of the basic functions shown in Figure 2-29 of the previous section. These topologies will be compared in terms of their suitability for high voltage-conversion ratio, high-voltage, high-power applications. Only the step-up versions of the topologies are considered, but the topologies can operate equally well in step-down as long as bi-directional switches are used. The first topology is considered the so-called Fibonacci circuit.

- **Fibonacci SC converter**

A 3-stage Fibonacci SC converter is shown in Figure 2-30. The output of each cell is the summation of the voltage of the previous two cells; hence the voltage on each capacitor follows a Fibonacci series. Therefore this converter can be realised by voltage addition cells. The first

input terminal of cell k is connected to the output of cell $k-1$ and the second input terminal is connected to the output terminal of cell $k-2$ as shown in Figure 2-30, therefore $V_c(k) = V_c(k-1) + V_c(k-2)$. If the converter consists of n_c cells then the input to output voltage conversion ratio is given in terms of binomial coefficients as,

$$\frac{V_o}{V_{in}} = \sum_{k=0}^{\frac{n_c}{2}} \binom{n-k}{k} \tag{2-18}$$

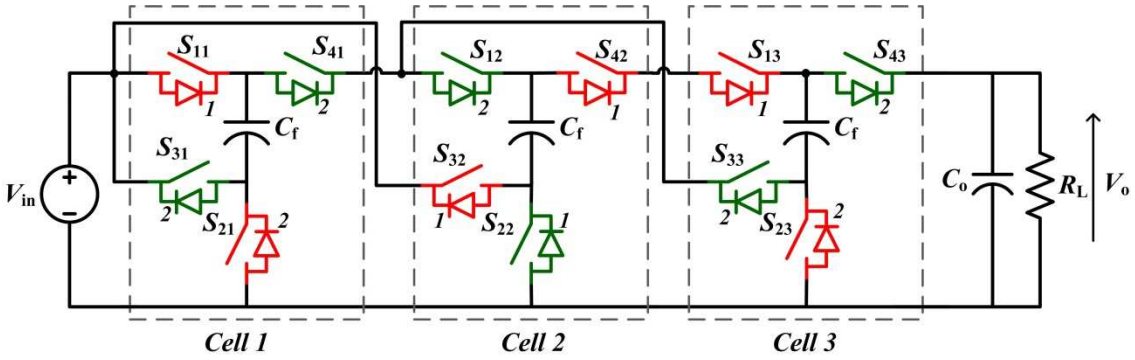


Figure 2-30. Voltage addition cells arrangement in Fibonacci circuit

Since the output switch of each cell S_{4x}, is connected to the input switch of the next cell S_{1y}, and these two switches operate simultaneously, then the connection of switch S_{3z} to the node between S_{4x} and S_{1y} can be disconnected and moved forward inside the cell and reconnected to the internal capacitor node as shown in Figure 2-31.

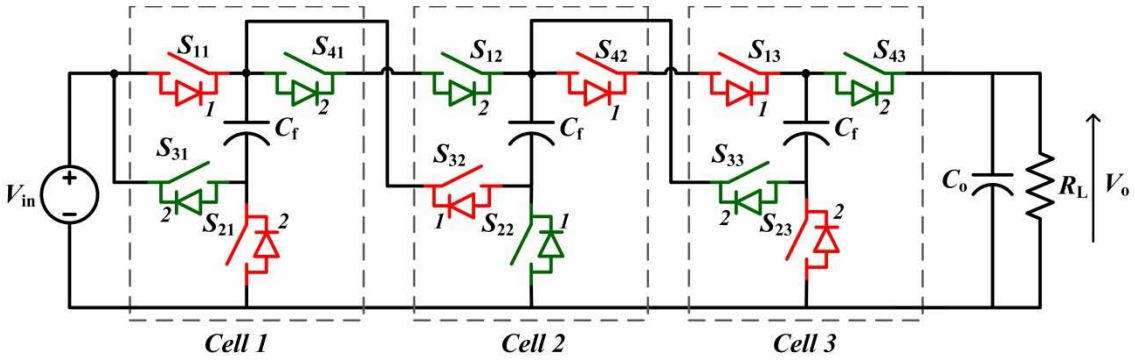


Figure 2-31. Fibonacci circuit re-configuration

Therefore one of the switches S_{4x} and S_{1y} are redundant and can be removed and the circuit can be simplified further as shown in Figure 2-32.

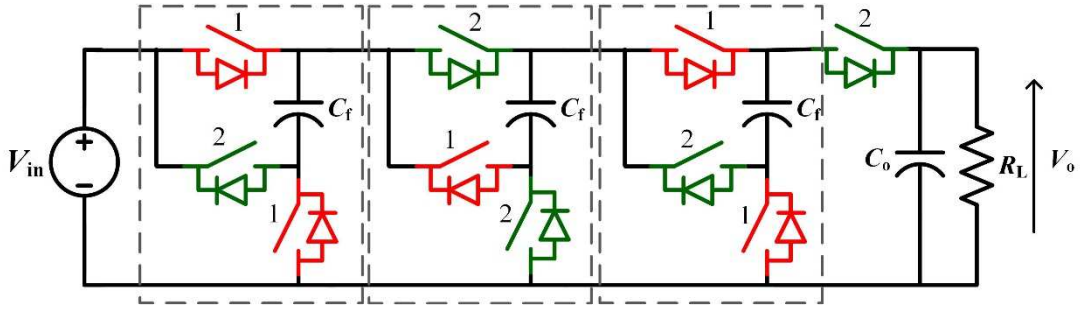


Figure 2-32. Simplified Fibonacci SC converter

Since the voltage rating of the switches in each cell of this topology depends on the capacitor voltage of that cell, the switch voltage rating will become prohibitively large for converters having a high number of cells. For example, for a 1 kV to 30 kV offshore grid application, the voltage rating of the first switch will be 1 kV and the last switch will be 30 kV. The majority of switches would therefore have to be implemented as a series connection of devices, which is very difficult to implement in practise when using high-frequency IGBT/MOSFET semiconductors.

- **Series-Parallel SC converter**

A 3-stage Series-Parallel converter is shown in Figure 2-33. This topology is also constructed from voltage addition cells. In the capacitor charging phase all the capacitors are connected in parallel to the input source and in the discharging phase cells are connected in series to achieve a high-voltage output. Unlike the Fibonacci circuit, all the capacitors in the cells are charged and discharged simultaneously. Again this topology suffers from switches that are rated at the output voltage of the converter and is therefore not suitable for high voltage applications.

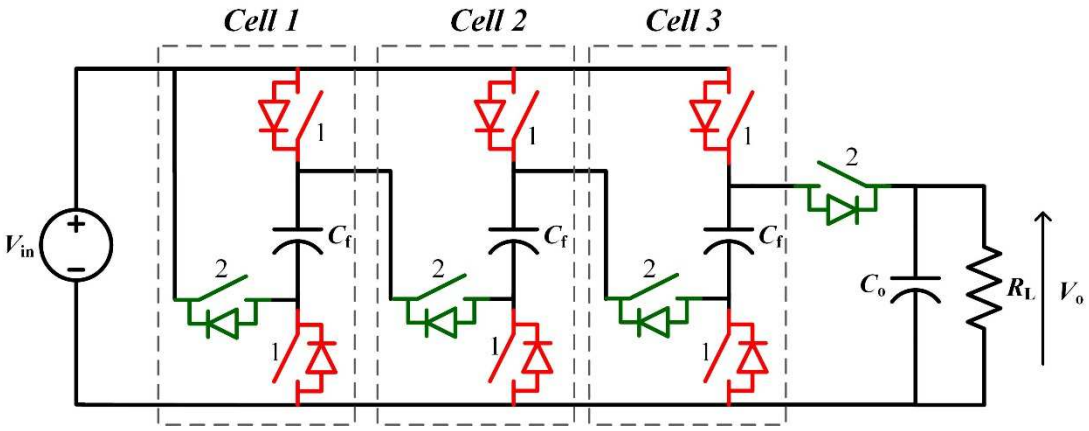


Figure 2-33. Series-Parallel SC converter

If the converter consists of n_c cells then the input to output voltage conversion ratio is given by,

$$\frac{V_o}{V_{in}} = n_c \tag{2-19}$$

- **Cascaded doubler SC converter**

A 3-stage cascaded doubler SC topology is shown in Figure 2-34 and this is a cascade connection of voltage doubler cells where the voltage on the capacitor in each cell is twice the voltage of the capacitor in the previous cell. This topology requires high voltage switches to be implemented and each switch in the cell has the voltage rating equal to the capacitor voltage of the cell.

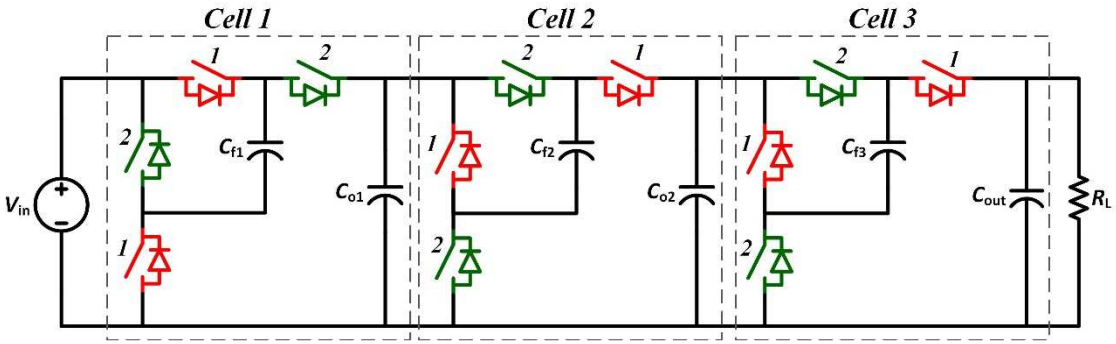


Figure 2-34. Binary SC converter

If the converter consists of n_c cells then the input to output voltage conversion ratio is given by,

$$\frac{V_o}{V_{in}} = 2^{n_c} \tag{2-20}$$

- **Ladder SC converter**

The circuit topology of a 4-stage Ladder topology is shown in Figure 2-35. This converter is synthesised from the basic cell shown in Figure 2-28, where other than in the last cell, switch S_4 is permanently on. The input to each cell is connected across the capacitor of the previous cell so that the output of each cell is raised by the input voltage V_{in} with respect to the preceding cell. If the converter consists of n_c cells then the input to output voltage conversion ratio is given by,

$$\frac{V_o}{V_{in}} = \left\lfloor \frac{\mathrm{n_c} + 1}{2} \right\rfloor + 1 \tag{2-21}$$

Since the voltage of each cell of the Ladder circuit "stands" on top of the previous cell – hence the name Ladder. The voltage rating of all the components other than the output capacitor C_{out} is equal to the converter input voltage V_{in}, which is highly desirable for high-voltage, high voltage-conversion ratio applications.

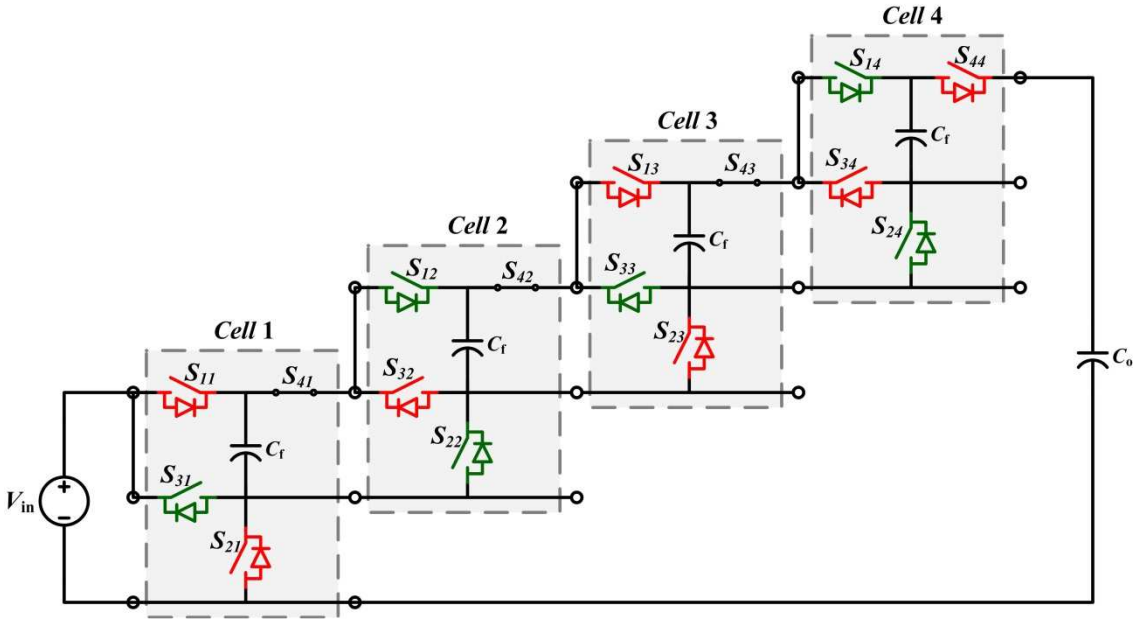


Figure 2-35. Connection arrangements of basic cells to form the Ladder topology

This circuit can be simplified as shown in Figure 2-36. Firstly, all of the permanently closed switches S_{4x} can be removed and replaced by a wire.

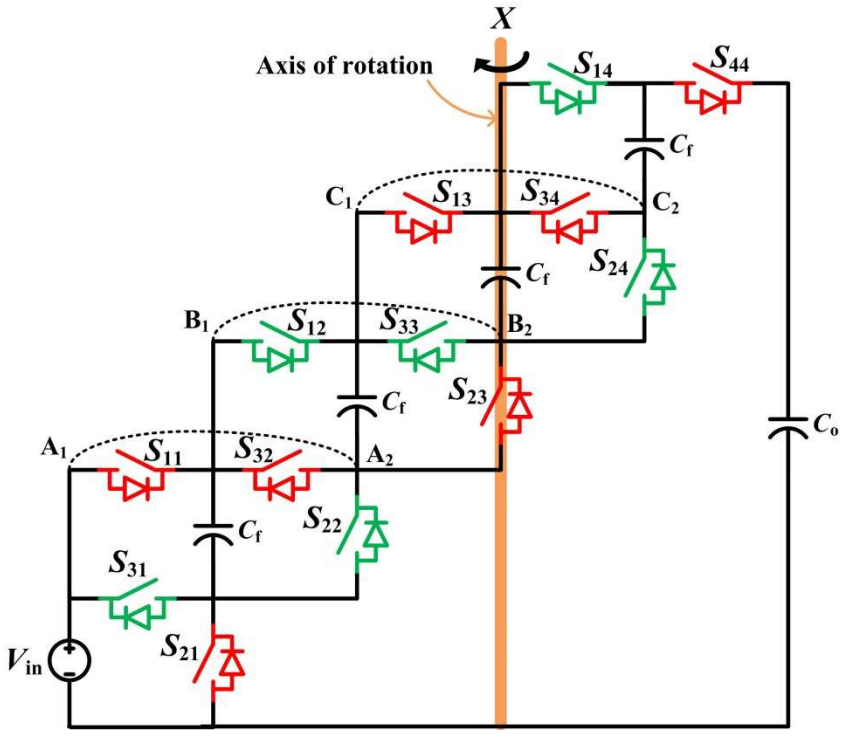


Figure 2-36. Simplified connection arrangements of basic cells for the Ladder topology

Secondly, since switch pairs S_{11}/S_{32} and S_{31}/S_{22} are switched in anti-phase, nodes A_1 and A_2 are effectively connected permanently together, shown by the dotted line in Figure 2-36. Similarly, nodes B_1/B_2 and C_1/C_2 are also connected. If these connections are made permanent

using a wire, then a number of switches become redundant. For example if node C_1 is connected to C_2, switch S_{34} can be removed. By then folding the circuit diagram around the axis shown in Figure 2-36 the circuit becomes as shown in Figure 2-37.

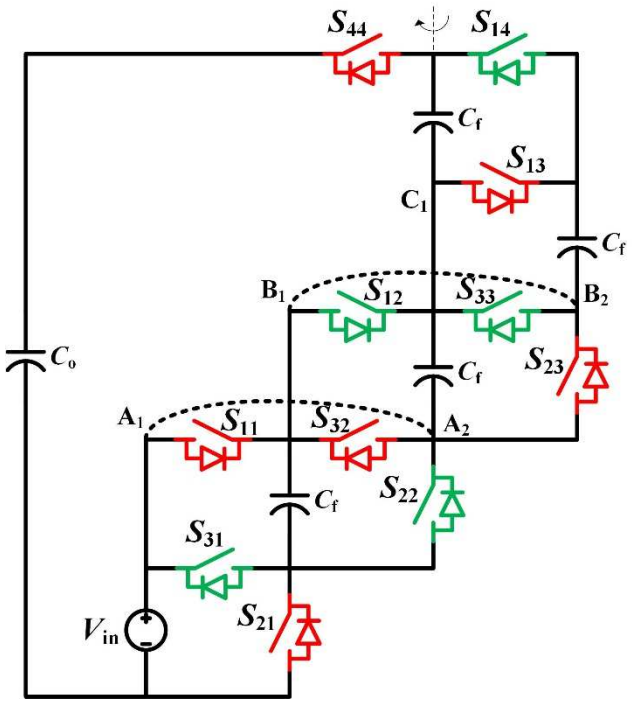


Figure 2-37. Simplified circuit configuration after first folding of circuit in Figure 2-36

If the switch removal and folding is repeated for the remaining paired nodes, nodes A_1/A_2 and B_1/B_2, then this results in the more traditional form of the Ladder circuit shown in Figure 2-38.

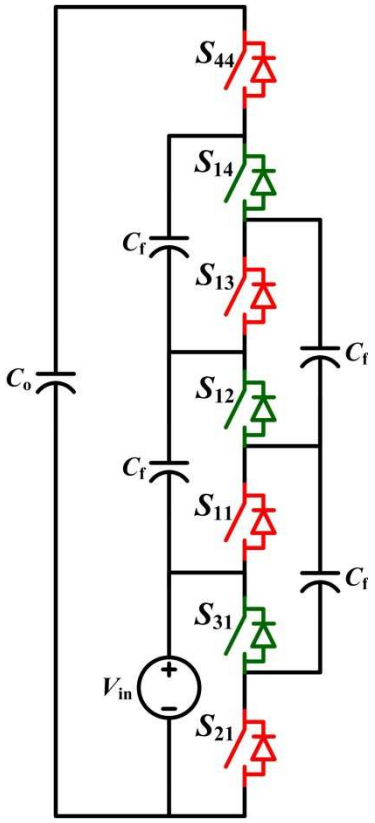


Figure 2-38. Simplified Ladder SC converter

- **Dixon Charge Pump SC converter**

Another attractive topology for high voltage applications is the Dixon Charge Pump (DCP) structure - a four-cell circuit is shown in Figure 2-39. The DCP circuit is a variation of so-called AC/DC voltage multiplier circuits [69, 70].

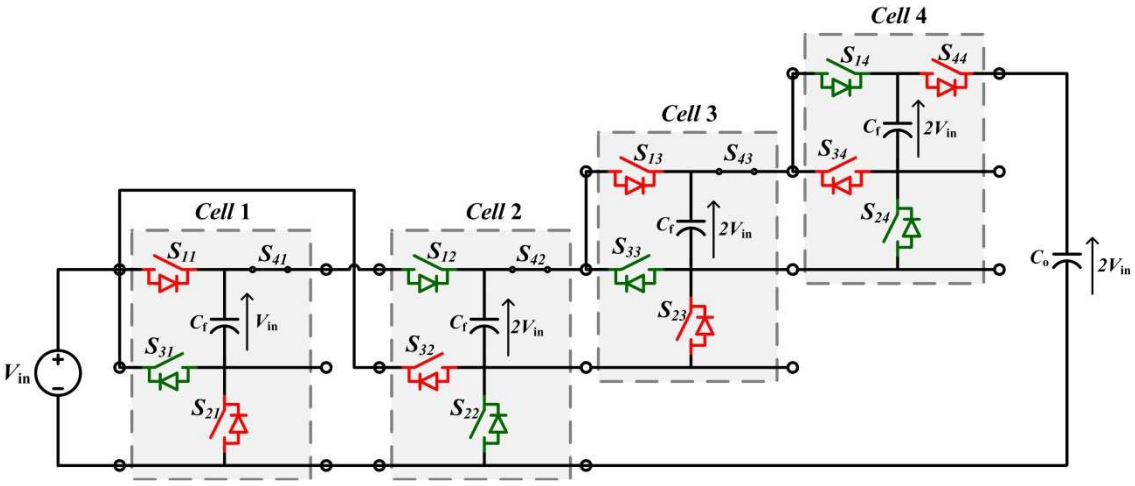


Figure 2-39. Connection arrangements of basic cells to form Dixon Charge Pump SC converter

It can be seen from Figure 2-39 that the DCP circuit consists of an initial voltage Doubler followed by a Ladder topology. The DCP circuit is very popular in hard-switched DC-DC

conversion for integrated circuit applications because of its higher efficiency when compared to the Ladder circuit. However, unlike the Ladder topology where all the switches have the same voltage rating of V_{in}, in this topology all the switches need to be rated to $2V_{in}$, other than in the first cell where they are rated at V_{in}. If the converter consists of n_c cells then the input to output voltage conversion ratio is given by,

$$\frac{V_o}{V_{in}} = \mathrm{n_c} + 1 \tag{2-22}$$

Similar to the Ladder circuit, the DCP circuit can also be simplified and this results in the circuit shown in Figure 2-40.

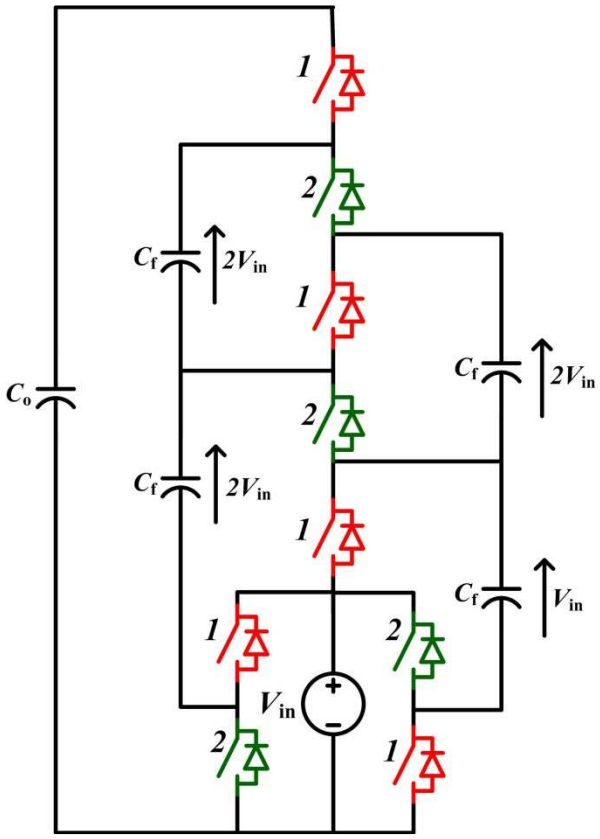


Figure 2-40. Dixon Charge Pump SC converter

2.7.3 Recently Proposed Topologies

New SC topologies have recently been proposed, which are suitable for high power applications [71-73]. Figure 2-41 shows the Multilevel Modular SC Converter (MMSCC) proposed in [72]. The topology has a modular structure in that the power ratings of the switches are the same in each cell. This modularity has the advantage of offering more cost-effective manufacturing as well as the potential to bypass faulty modules during operation. The maximum voltage rating for the horizontal switches shown in Figure 2-41 in this topology is equal to $2V_{in}$ and the vertical switches are rated at V_{in}. Again this topology is constructed from the basic cell shown in

Figure 2-28, where other than in the last cell switch S_4 is permanently closed. The circuit consist of the cascade connection of voltage addition cells shown in Figure 2-29(a), where one of the input terminals to the cell is connected directly to the input source and the other terminal is connected to the output of the previous cell.

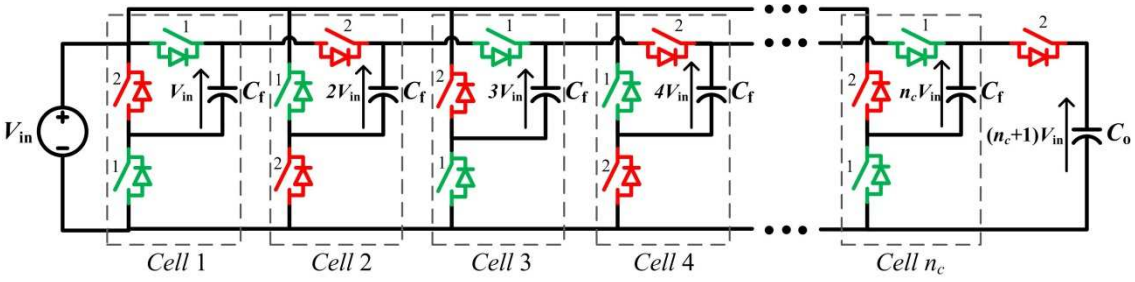


Figure 2-41. Multilevel Modular SC Converter (MMSCC)

If the converter consists of n_c cells then the input to output voltage conversion ratio is given by,

$$\frac{V_o}{V_{in}} = n_c + 1 \tag{2-23}$$

The converter can operate with the sign of the input source inverted. This is shown in Figure 2-42, where the circuit is shown flipped over from top to bottom but the source has remained the same. In addition if the operation of the switches is made complementary to those in Figure 2-41 then the two circuits can be fed from the same source as a so-called Bi-pole arrangement as shown in Figure 2-43.

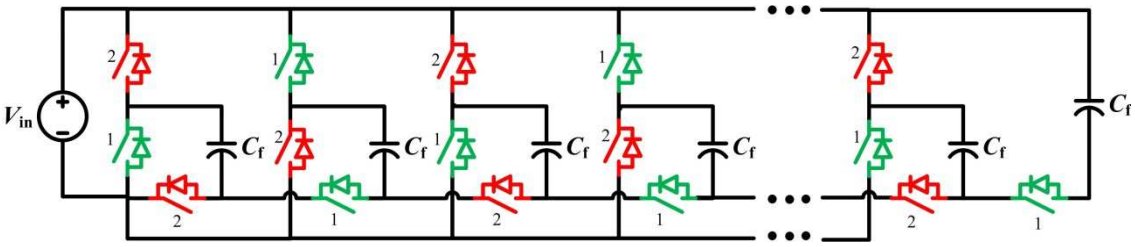


Figure 2-42. Complementary circuit arrangement for Multilevel Modular SC Converter (MMSCC)

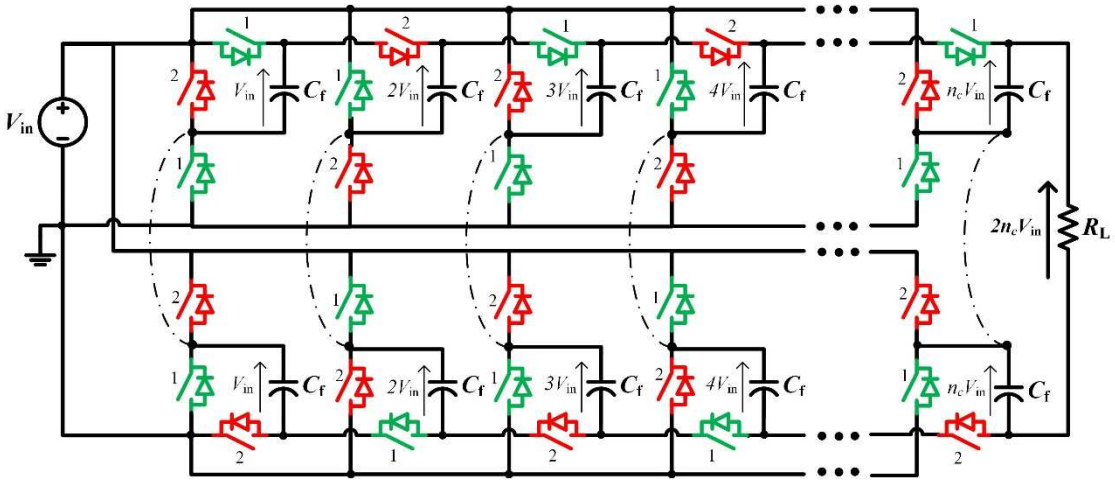


Figure 2-43. Bi-pole arrangement of two Multilevel Modular SC Converters (MMSCC)

In the Bi-pole arrangement, each parallel upper and lower converter produces an output voltage of $\pm n_c V_{in}$ respectively across the output capacitors in Figure 2-43. The converter output voltage is then taken between these two outputs giving a voltage of $2n_c V_{in}$. The Bi-pole method significantly reduces the number of capacitors needed to achieve a given step-up voltage ratio when compared with the MMSCC.

A simplification to this circuit can be made by noting that the mid-point nodes of all the vertical pairs of switches are at the same potential and therefore these nodes can be connected together as shown by the dotted lines in the above figure. If this connection is made, then the two red and green switches to the right of the line become redundant and can be removed from the circuit giving the simplified topology shown in Figure 2-44.

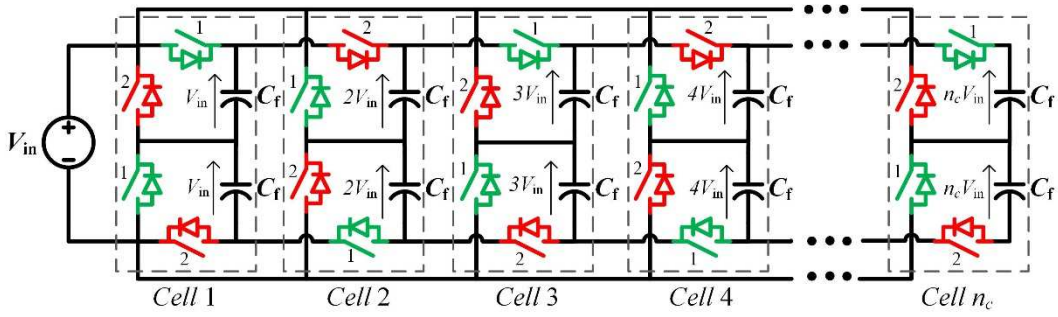


Figure 2-44. Symmetrical Multilevel Modular SC Converter (SMMSCC)

The removal of the redundant switches does not reduce the overall VA rating of the switches, since the current rating of the remaining vertical switches needs to be doubled. However, it does produce a simpler topology. One disadvantage of removing the switches is that unlike the MMSCC circuit this new topology now becomes coupled, where individual cells interact with each other in a problematic manner. Coupling is discussed in more detail in the next chapter. This converter has been proposed in [74] and it is termed a Symmetrical Modular Multilevel

Switched Capacitor Converter (SMMSCC). If the converter consists of n_c cells then the input to output voltage conversion ratio is given by,

$$\frac{V_o}{V_{in}} = 2\mathrm{n_c} \tag{2-24}$$

The voltage rating of the switches for the SMSCC is the same as those for the MMSCC converter.

Due to the Bi-pole arrangement, the number of capacitors for an SMMSCC is much less than that for the MMSCC to achieve same conversion ratio. This is because,

- By comparing the voltage conversion ratio equations (2-23) and (2-24) the number of cells required for the SMMSCC is approximately half that for the MMSCC.
- With half the number of cells, each cell of the SMMSCC is equivalent to the even numbered cells of the MMSCC. On these cells, the capacitor voltages for the MMSCC converter are twice that of the SMMCC; however the SMMCC has twice the number of capacitors. These results in 2:1 cell capacitance requirement for the MMSCC compared with the SMMCC.

This means the capacitance requirement is four times less for SMMSCC converter compared to MMSCC to achieve the same conversion ratio and same efficiency.

Another advantage of the SMMSCC over MMSCC is a lower output voltage ripple. Two capacitors of each cell in SMMSCC converter are charged/discharged in complementary phase so that when one of the capacitors is charged from the previous cell, the other capacitor is discharged to the next capacitor or load. This cancel out the ripple in the output of each cell and provides an almost ripple free output voltage and therefore there is no need for a large output filter capacitor.

However, a significant problem with the SMMSCC is that there is no common ground connection between the input and output voltages and there is no easy way to provide input/output isolation. This can be a serious issue in power networks where both the source and load need to be referenced to earth. Furthermore, if a fault occurs in one pole in the output terminal of the converter, the voltage of the other pole can jump up to twice the nominal voltage due to absence of ground in the mid-point of the output terminal which require high insulation requirement.

2.8 Summary

This chapter has given an overview of DC-DC converters. Based on the conversion mechanism the DC-DC converters are categorised as either Direct or Indirect. Indirect converters consist of a number of gyrator stages, for example the Buck and Boost converters, whereas Direct

converters use Direct transformation with no intermediate stages, such as switched capacitor converters.

Indirect converters are found to be unsuitable for high voltage-conversion ratios because of their poor switch utilisation and the need for high-power and high-voltage switches. In addition, the switches are exposed to both the high-voltage side voltage and the high-current side current. A wound transformer can be used to ameliorate these problems; however to reduce the size and weight of the converter for off-shore wind platforms, the transformer needs to operate at medium to high frequencies and no such technology currently exists for megawatt applications.

A Direct LCL, rotating-capacitor topology has been examined for high-power, high voltage applications. Unfortunately, the LCL converter suffers from the same issue as the Indirect conversion method since the switch utilisation is very poor for high voltage gain applications.

Switched capacitor converters which use the Direct conversion method, have promising features for the wind-turbine and remote-load feeding applications. A high voltage-conversion ratio and high-voltage output can be achieved using a simple network of low voltage and low power switches. Common SC topologies have been investigated in terms of their suitability for HVDC applications. The Ladder, Dixon Charge Pump, MMSCC and SMMSCC topologies have been identified as possible candidate topologies for such applications. The Ladder topology is the only topology where all the switches and capacitors are rated at the low-voltage side of the converter. A Bi-pole MMSCC converter can be used to form the simplified Symmetrical MMSCC. However the symmetrical configuration presented in this chapter is not suitable for the HVDC applications that need common ground between the input and the output of converter.

The next chapter will describe analysis and the modelling techniques for SC converters, which will then be used to compare the candidate topologies in terms of component requirements and converter efficiency.

3. Modelling and Analysis of Switched Capacitor Converters

Switched capacitor converters can be generally classified into hard-switched and resonant SC converters. Hard switched SC converters are only composed of capacitors and switches whereas resonant SC circuits include a small inductor. Due to their inductor less-structure, hard switched SC circuits are commonly used for power conversion within integrated circuits where the capacitors and switches can be directly fabricated in silicon.

The switching period of a SC converter is divided into two phases and each capacitor within the converter will be charging in one phase and discharging in another. The converter topology can be divided into a number of simple circuits for each of these phases, which includes either,

- A capacitor connected to another capacitor
- A capacitor connected to the supply voltage source
- A capacitor connected to the load

For example, for capacitor-to-capacitor energy exchange - if the first two capacitors C_1 and C_2 of an SC converter are linked by a switch *S*, and the capacitors have initial voltages V_1 and V_2, where $V_1 > V_2$, the equivalent circuit for the discharging phase of C_1, which also represents the the charging phase of C_2, will be as shown in Figure 3-1(a).

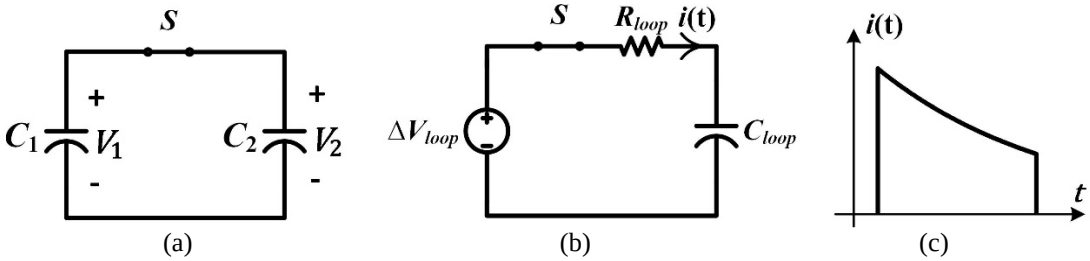


Figure 3-1. (a) Charge transfer circuit (a) charge transfer equivalent circuit (b) typical hard switched current waveform

In the next phase of the switching cycle for this example, both $C_1$and C_2 will be individually connected to different capacitors within the SC converter and the charging and discharging action of C_1 and C_2 will reverse.

Such equivalent circuits can only be derived for circuits where the circuit loop formed between each capacitor pair does not share any common circuit impedances with other pairs of capacitors. The circuit equations for these loops are then completely independent and these equivalent circuits have been termed Decoupled sub-circuits in this thesis. Coupled sub-circuits are discussed in more detail in the next chapter.

With the switch *S* closed in Figure 3-1(a), an equivalent circuit can be derived as shown in Figure 3-1(b), where $\Delta V_{loop} = V_1 - V_2$, C_{loop} is the series equivalent capacitance of C_1 and C_2, and the resistor R_{loop} represents the equivalent on-state resistance of the switch plus the equivalent series resistance (ESR) of the capacitors and any parasitic resistance of circuit wires and/or connectors. A typical exponential decay waveform for the circuit current $i(t)$ in Figure 3-1(b) for the hard-switched SC converter is shown in Figure 3-1(c).

In order to reduce the switching losses associated with the hard-switched converter, the resonant SC converter was introduced [75]. By adding inductors into the SC circuits some attractive features such as soft switching can be achieved. Furthermore the inductor can limit the current and which occurs in hard switched SC converters when the ESR of the capacitors are very small. The charge transfer path in resonant SC converters is via the equivalent series RLC circuit as shown in Figure 3-2(a), where *L* is a small external inductor added in series with charge transfer path. However, in some cases the stray inductance of the circuit may be sufficient to operate the converter in a resonant mode [71, 74]. The switching frequency of the resonant SC converter is commonly set to the damped resonant frequency of the equivalent RLC circuit so that the switch turns on at zero current and switches off when the current re-crosses zero one half-period later. This results in a soft turn-on and turn-off switching operation as shown by the switch current waveform in Figure 3-2(b).

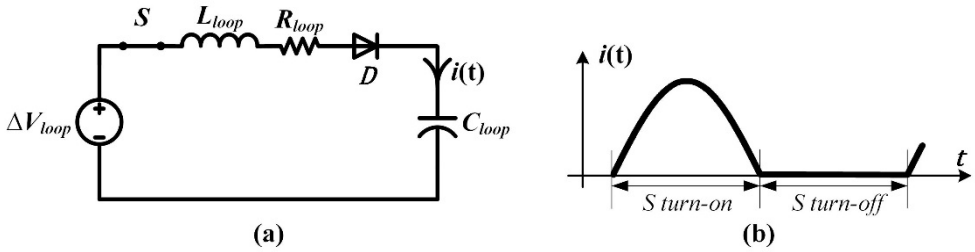


Figure 3-2. Charge transfer equivalent circuit and current waveform for resonant SC converters (a) equivalent circuit (b) typical switch current waveform

Circuit averaging of SC converters results in a model that consists of an ideal DC transformer with turns-ratio 1:*n*, followed by an output equivalent resistance R_{eq} as shown in Figure 3-3 [50, 66, 76], the circuit is fed from a DC source V_{in} and supplies a resistive load R_L. The equivalent resistance R_{eq} aggregates all the losses in the converter and is the most important parameter for SC converters as it fully determines its steady-state performance such as efficiency and output voltage drop with load.

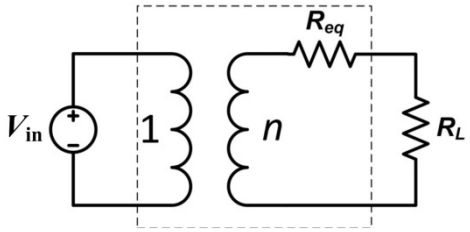


Figure 3-3. Equivalent circuit for SC converters

The objective of the analysis of SC circuits is to derive an expression for R_{eq} in terms of other circuit parameters, in particular switch on-state resistance and capacitor ESR. In recent years, there has been an increasing amount of literature on the analysis of SC converters, which has looked at developing methods to determine the output equivalent resistance [50, 66, 76-79]. In particular the two seminal papers Seeman et al [50]. and Ben-Yaakov et al. [79], provide extensive work in this area. However, whilst the analysis technique developed by Seeman applies to both Coupled and Decoupled converters, it is restricted to the use of the converter at either the so-called Slow or the Fast Switching Limits (SSL, SFL), which correspond to either low or high switching frequencies when compared to the RC time-constant of the switching cells. Ben-Yaakov's analysis is less restrictive in terms of the operation of the converter; on the other hand the analysis does not apply to Coupled topologies, for example the Ladder circuit. A more general approach has been developed in this thesis, which does not suffer from the limitations of the aforementioned techniques and is described as follows.

The fundamental approach is to equate the steady-state loss in the output equivalent resistance R_{eq}, with the sum of the losses in each component of the SC converter during each switching phase, averaged over a switching period so that,

$$\sum_{k=1}^{2}\sum_{i=1}^{m}\frac{E_{i,k}}{T_s} = R_{eq}\cdot I_o^2 \tag{3-1}$$

where I_o is the average output current of the converter over a switching period T_s, $E_{i,k}$ is the energy dissipated by the i^{th} component during the k^{th} switching phase. The average current is used because the model is based on averaging the circuit during two switching periods [80]. There are two switching phases per switching period, $k = 1$ and $k = 2$, corresponding to the two states of the red and green converter switches. These two states also correspond to the charging and discharging phases of individual capacitors. Here a component will typically be a capacitor, switch, or the parasitic resistance of a connecting wire or connector. The number of components in the converter is denoted by m.

The energy dissipated by conduction loss for the i^{th} component during the k^{th} switching phase $E_{i,k}$, can also be expressed as,

$$E_{i,k} = T_s R_{i,k} I_{rms,i,k}^2 \tag{3-2}$$

where $R_{i,k}$ is the parasitic resistance of the i^{th} component and $I_{rms,i,k}$ is the RMS current flowing through the component during phase k. The RMS current can be found by integration,

$$I_{rms,i,k} = \sqrt{\frac{1}{T_s}\left(\int_0^{T_k} i_{i,k}^2(t)\cdot dt + \int_{T_k}^{T_s} 0 \cdot dt\right)} = \sqrt{\frac{1}{T_s}\int_0^{T_k} i_{i,k}^2(t)\cdot dt} \tag{3-3}$$

where T_k is the duration of the k^{th} phase. Note the current though the component is set to zero for the remainder of the switching period $T_k \rightarrow T_s$ since the loss for this component during this period is calculated using the second k^{th} term. The effective instantaneous current waveform through a component will therefore be as shown in Figure 3-4 along with typical values for $I_{rms,i,k}$ and $I_{avg,i,k}$ – the average current $I_{avg,i,k}$, which is also shown in the figure is discussed below.

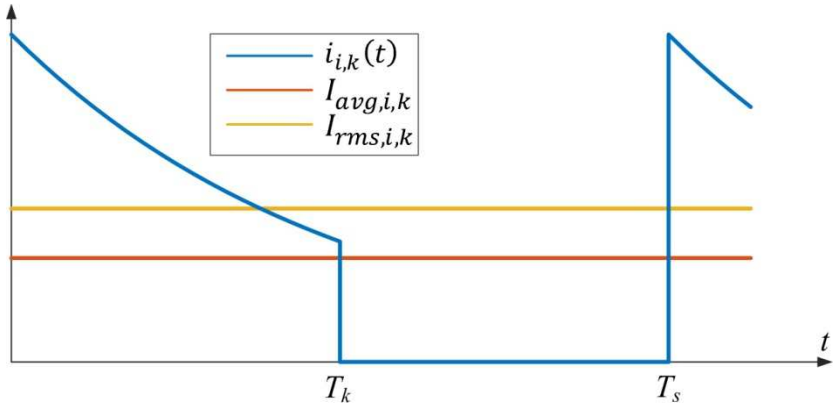


Figure 3-4. Typical instantaneous, RMS and average current waveform for component i during phase k, with the remainder of the switching period represented by zero current

From (3-1) and (3-2) the output equivalent resistance can now be expressed as,

$$R_{eq} = \sum_{k=1}^{2}\sum_{i=1}^{m} R_{i,k}\left(\frac{I_{rms,i,k}}{I_o}\right)^2 \tag{3-4}$$

The average converter output current I_o, can be eliminated from this equation by substituting in the expression for the average current through the i^{th} component during phase k, denoted $I_{avg,i,k}$, where,

$$I_{avg,i,k} = \frac{1}{T_s}\left(\int_0^{T_k} i_{i,k}(t)\cdot dt + \int_0^{T_k} 0 \cdot dt\right) = \frac{1}{T_s}\int_0^{T_k} i_{i,k}(t)\cdot dt \tag{3-5}$$

Again as with the expression for the RMS current the period of integration is taken as the whole switching period, so that the current waveform during this interval is as shown in Figure 3-4.

From fundamental circuit theory, the average current $I_{avg,i,k}$ is proportional to the average converter output current I_o, so that,

$$I_{avg,i,k} = a_{i,k} \cdot I_o \tag{3-6}$$

where $a_{i,k}$ is a constant of proportionality the value of which depends purely on the circuit topology [66, 81]. Note that in Seeman's analysis [50], circuit charge is used rather than current and the coefficient $a_{i,k}$ was known as a charge multiplier. Seeman uses a number of simplifying assumptions regarding the shape of the current waveform during the charging and discharging periods where the use of *charge* in his analysis is more convenient. However, the analysis proposed here makes no such assumptions and is more general. In this analysis the branch *currents* of the circuit are solved using nodal analysis as described in Appendix A, – rather than Seeman's accumulated *charge* – as this is more convenient. The Appendix A includes an example of how nodal analysis is used to find the values of the coefficients $a_{i,k}$ for the 3-stage Ladder circuit shown in Figure 3-5.

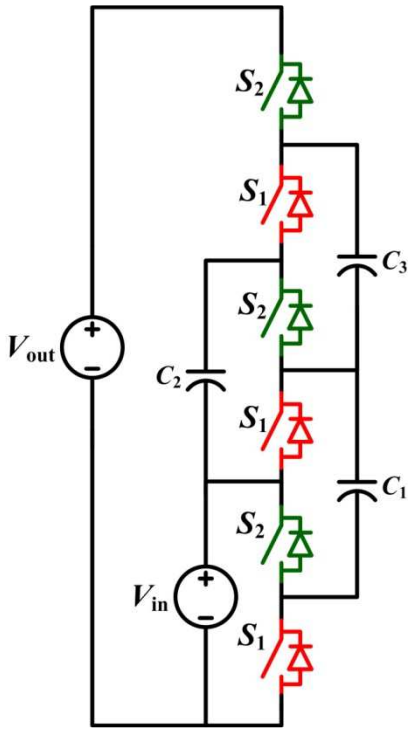


Figure 3-5. 3-Stage Ladder circuit used as an example to calculate coefficients $a_{i,k}$

Neglecting the parasitic resistance of wires, then the 3-Stage Ladder contains 9 components with conduction loss: 3 capacitors and 6 switches, so that $m = 9$. The nine coefficients $a_{i,k}$, from Appendix A, are shown in Table 3-1, where the order of the coefficients corresponds to the arrangement of the components from the bottom to the top of the circuit schematic:

Table 3-1. Charge multipliers for 3-stage Ladder circuit shown in Figure 3-5

Switching phase k	Capacitor coefficients $a_{1-3,k}$	Switch coefficients $a_{4-9,k}$
1	$2, \quad -1, \quad 1$	$0 \quad 2 \quad 0 \quad -1 \quad 0 \quad -1$
2	$-2, \quad 1, \quad -1$	$2 \quad 0 \quad -1 \quad 0 \quad -1 \quad 0$

The coefficients $a_{i,k}$ from equation (3-6) can be used to eliminate I_o from (3-4) to give,

$$R_{eq} = \sum_{k=1}^{2} \sum_{i=1}^{m} a_{i,k}^2 \cdot R_{i,k} \left(\frac{I_{rms,i,k}}{I_{avg,i,k}} \right)^2 \tag{3-7}$$

For most components such as capacitors and the parasitic resistance of wires and connectors the resistance $R_{i,k}$ is constant over the two phases and so the k subscript can be removed and $R_{i,k}$ can be replaced by R_i in (3-7). This is not the case for the resistance of switches which changes over the two phases as the switch changes state. However, when the switch turns-off the coefficient $a_{i,k}$ becomes zero so it does not matter if $R_{i,k}$ is also replaced by R_i for switches. In addition, the last term in (3-7) can be identified as the form-factor $k_{i,k}$, of the current flowing through the i^{th} component, during phase k, so that (3-7) becomes,

$$R_{eq} = \sum_{k=1}^{2} \sum_{i=1}^{m} a_{i,k}^2 \cdot R_i \cdot k_{i,k}^2 \tag{3-8}$$

The output equivalent resistance R_{eq} can be seen to be the sum of a number of partial equivalent resistances $R_{eq,i,k}$ where,

$$R_{eq} = \sum_{k=1}^{2} \sum_{i=1}^{m} R_{eq,i,k} \tag{3-9}$$

$$R_{eq,i,k} = a_{i,k}^2 \cdot R_i \cdot k_{i,k}^2 \tag{3-10}$$

These partial resistances contribute to the I^2R power loss of component i during phase k. Therefore, each component has two contributions to the total output equivalent resistance of the converter, which correspond to the two $k = 1$ and $k = 2$ conduction phases. The equivalent circuit shown in Figure 3-3, then becomes as shown in Figure 3-6(a).

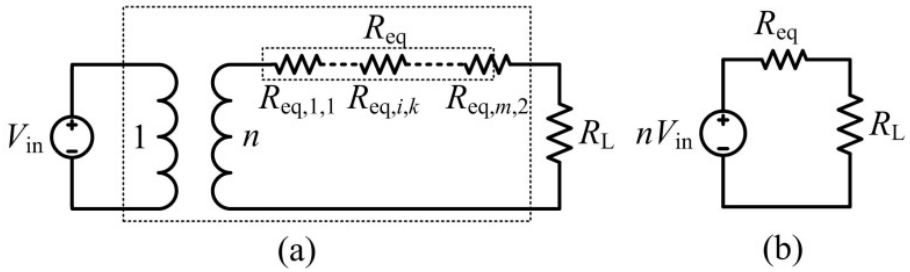


Figure 3-6. Equivalent circuits of SC converters (a) detailed equivalent circuit and (b) simplified equivalent circuit

Summing the partial equivalent resistances and transferring the supply voltage V_{in} to the secondary of the DC transformer yields the final equivalent circuit shown in Figure 3-6(b). The switching losses of the converter can also be integrated into this equivalent resistance [82], in which case the resistor can also be used to calculate both the conduction losses and the switching losses of the converter.

By inspecting equation (3-8), it can be seen that the partial output equivalent resistances $R_{eq,i,k}$, are composed of three parameters as shown in Figure 3-7:

- the coefficient $a_{i,k}$ which is purely defined by the circuit topology.
- R_i which is the equivalent or parasitic resistance of the component i and can be found from device datasheets or by measurement.
- $k_{i,k}$ which is the form-factor of the current flowing through the component i during phase k and defined as the ratio of RMS to average current. This term will be discussed in the next section.

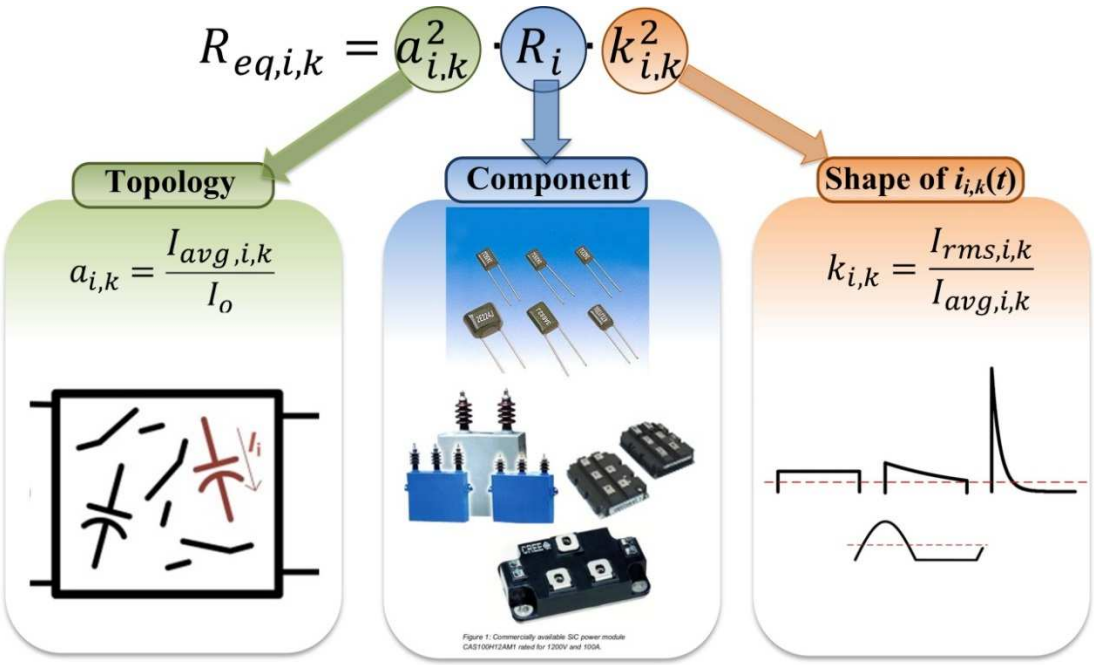


Figure 3-7. Dependency of $R_{eq,i,k}$ to the circuit parameters

With the coefficients $a_{i,k}$ obtained from the circuit topology and the values of R_i obtained from datasheets/measurement, the final step of the analysis is to find an expression for the form-factor terms $k_{i,k}$. In this case expressions for the instantaneous current waveforms need to be calculated explicitly. In some SC topologies the sub-circuit loops formed during charging/discharging do not share any common impedances and these sub-circuits consist of simple RC circuits for hard switch case circuits as shown in Figure 3-1 or an RLC circuit for resonant SC converter as shown in Figure 3-2. In either of these two cases the expressions for the current waveforms are easily derived. However, in other topologies, two or more charging/discharging sub-circuits can be coupled through a common impedance, in which case obtaining expressions for the current waveforms is not simple. In particular, the Ladder, SMMSCC and Dixon Charge Pump topologies are examples of topologies where the derivation of full expressions for the current waveforms is intractable when the number of levels is greater than two. As an example, Figure 3-8(a) shows a 3-Stage Ladder topology and its equivalent circuit Figure 3-8(b), where the odd-numbered, red switch bank is assumed to be turned on.

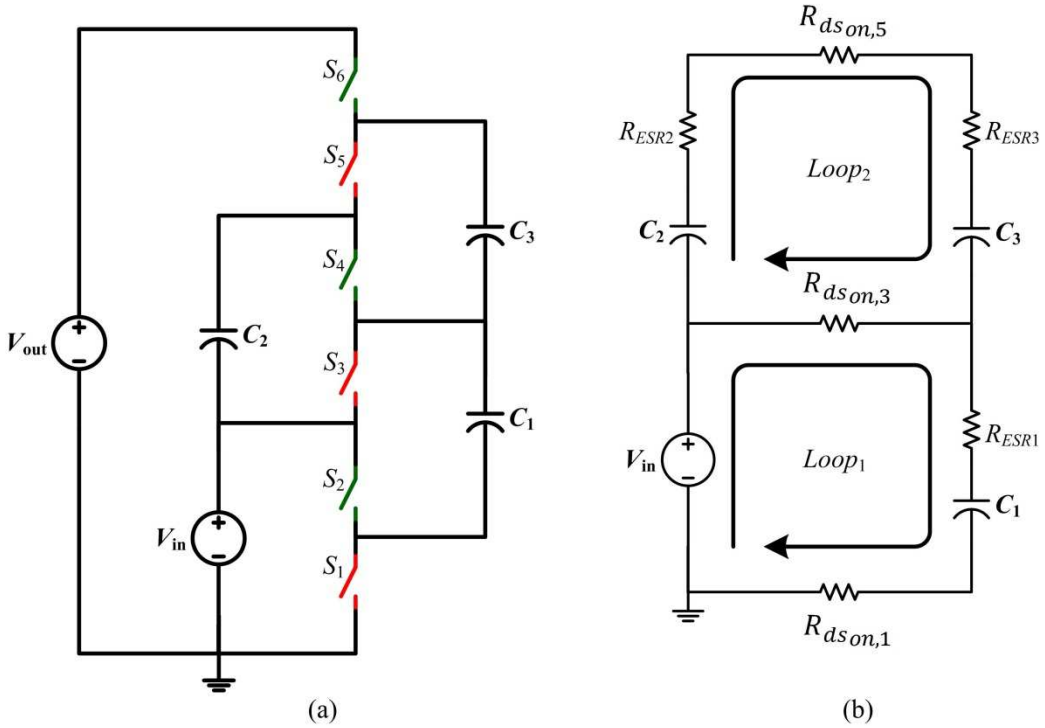


Figure 3-8. 3-Stage Ladder SC converter and the equivalent circuit when the odd-numbered red switches are on (a) circuit diagram (b) equivalent circuit during first switching phase

It can be seen that the on-state resistance $R_{ds_{on,3}}$, which represents switch S_3, is located in the common branch of two sub-circuit loops and therefore the loop-voltage equations are not independent.

The analysis technique proposed by Ben Yaakov [79] does not consider the effects of common branches on the output equivalent resistance. Therefore his method cannot be directly applied to Coupled SC converters. However, whilst Seeman's analysis can be used for Coupled circuits, it is restricted to so called Slow and Fast Switching limits as discussed in the next section.

3.1 Form-Factor and the Analysis of Hard-Switched SC converters

Hard switched SC converters rely on circuit resistances such as switch on-state resistance to limit the charging/discharging current of the capacitors. Three different operational modes based on the ratio of the switching period and the RC time constant of the sub-circuits can be defined in hard switched SC converters. Figure 3-2 shows the current waveforms for different modes during the charging phase of a capacitor:

- **Fast Switching Limit (FSL):** When the switching period is much shorter than the time constant of the sub-circuit loop, the current waveform can be considered approximately constant during this period as shown in Figure 3-9(a). This operation mode was defined as "no charging mode" in [79] and the Fast Switching Limit (FSL) mode in [50].

- **Partial Charging:** As the switching period is increased with respect to the time constant of the sub-circuit, the shape of the current waveform becomes more like an exponential decay as shown in Figure 3-9(b) and is known as partial charging mode.
- **Slow Switching Limit (SSL):** When the switching period is much longer than the time constant of the charge transfer path, the capacitor is completely discharged as shown in Figure 3-9(c). This mode is known as "complete charging mode" in [79] and the Slow Switching Limit (SSL) mode in [50].

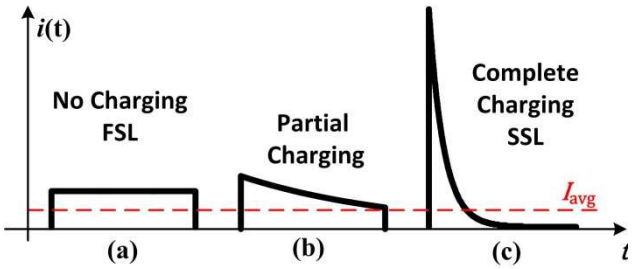


Figure 3-9. Current waveforms for a Hard Switch SC converter (a) no charging [79] or FSL mode [50], (b) partial charging [79]and (c) complete charging [79](corresponding to SSL mode [50])

The form-factor $k_{i,k}$ for the hard switched current waveform can be derived through circuit analysis. For example, for Uncoupled circuits, where the sub-circuit loop can be represented by the simple RC circuit shown in Figure 3-1(b), the instantaneous current for the i^{th} component during phase k is given by,

$$i_{i,k}(t) = \frac{\Delta V_{loop,i,k}}{R_{loop,i,k}} e^{-\frac{t}{R_{loop,i,k}C_{loop,i,k}}} \tag{3-11}$$

where the subscripts i and k have been added to the terms in Figure 3-1(b).

The average and the RMS current can then be derived using (3-3) and (3-5) and (3-11), for phase period T_k,

$$I_{avg,i,k} = f_s C_{loop,i,k} \Delta V_{loop,i,k} \left(1 - e^{-\frac{T_k}{\tau_{loop,i,k}}}\right) \tag{3-12}$$

$$I_{rms,i,k} = \Delta V_{loop,i,k} \sqrt{\frac{f_s C_{loop,i,k}}{2R_{loop,i,k}} \left(1 - e^{-\frac{2T_k}{\tau_{loop,i,k}}}\right)} \tag{3-13}$$

where the loop time constant are defined as $\tau_{loop,i,k} = R_{loop,i,k} C_{loop,i,k}$. Therefore the form-factor squared is,

$$k_{i,k}^2 = \left(\frac{I_{rms,i,k}}{I_{avg,i,k}}\right)^2 = \frac{1}{2f_s\tau_{loop,i,k}} \cdot \frac{\left(1 + e^{-\frac{T_k}{\tau_{loop,i,k}}}\right)}{\left(1 - e^{-\frac{T_k}{\tau_{loop,i,k}}}\right)} \tag{3-14}$$

In practice a dead-time is needed between the switching of the transistors of the first and second banks of switches. However, assuming this dead-time is small compared with the converter switching period then a duty cycle for the sub-circuit switch can be defined arbitrarily for say switching phase $k = 1$ so that,

$$D = T_1/T_s \tag{3-15}$$

where D is the converter duty cycle. Substituting into (3-14) gives,

$$k_{i,1}^2 = \left(\frac{I_{rms,i,1}}{I_{avg,i,1}}\right)^2 = \frac{1}{2f_s\tau_{loop,i,1}} \cdot \frac{\left(1 + e^{-\frac{DT_s}{\tau_{loop,i,1}}}\right)}{\left(1 - e^{-\frac{DT_s}{\tau_{loop,i,1}}}\right)} \tag{3-16}$$

For switching phase $k = 2$ the equivalent duty cycle would simply be replaced by $1 - D$ in (3-16). Equation (3-16) can be further simplified using a hyperbolic substitution and defining the constant $\beta_{i,k}$,

$$\beta_{i,k} = \frac{T_k}{\tau_{loop,i,k}} \tag{3-17}$$

The equations for the form-factor for switching phase 1 and 2 respectively then becomes,

$$\begin{aligned} k_{i,1}^2 &= \frac{1}{\mathrm{D}} \cdot \beta_{i,1} \cdot \coth\left(\frac{\beta_{i,1}}{2}\right) \\ k_{i,2}^2 &= \frac{1}{1-\mathrm{D}} \cdot \beta_{i,2} \cdot \coth\left(\frac{\beta_{i,2}}{2}\right) \end{aligned} \tag{3-18}$$

Substituting (3-18) into (3-10) and normalising the resulting equation by $R_i \cdot a_{i,k}^2$ gives the normalised partial equivalent resistance, $R_{eq,i,k}^*$,

$$R_{eq,i,k}^* = \frac{R_{eq,i,k}}{R_i \cdot a_{i,k}^2} = k_{i,k}^2 \tag{3-19}$$

which can be seen to be equal to the form-factor squared. The normalised partial equivalent resistance (3-19) for phase $k = 1$, can be plotted against the parameter $\beta_{i,k}$ for various values of duty cycle D as shown in Figure 3-10,

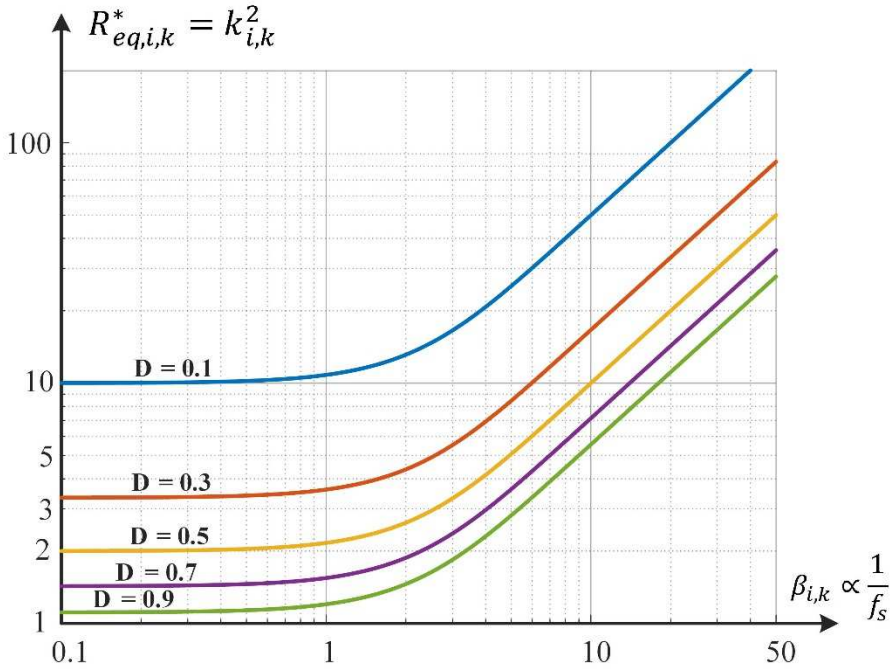


Figure 3-10. Normalised partial equivalent resistance $R^*_{eq,i,k}$ against $\beta_{i,1}$ for various values of duty cycle D a hard-switched SC converter

Note that Figure 3-10 also represents the second phase $k = 2$ relationship when the values for duty cycle D are substituted by $1 - D$. It appears from Figure 3-10 that operating the converter with a duty cycle approaching unity, $D \to 1$, minimises the equivalent resistance of a component. However, during the remaining phase where the duty cycle is equal to $1 - D$, the equivalent resistance approaches infinity. If the charging and discharging sub-circuit loop for the i^{th} component has equal resistance and capacitance $R_{loop,i,k}$ and $C_{loop,i,k}$, so that $\beta_{i,1} = \beta_{i,2}$, then it is Straightforward to show from (3-18) that the total equivalent resistance averaged over the two switching phases is a minimum when $D = 1/2$. For the majority of SC converters this is true because of the natural symmetry of the topology and therefore they operate with $D = 1/2$. Figure 3-10 has therefore been re-drawn to show just the $D = 1/2$ curve and is presented in Figure 3-11.

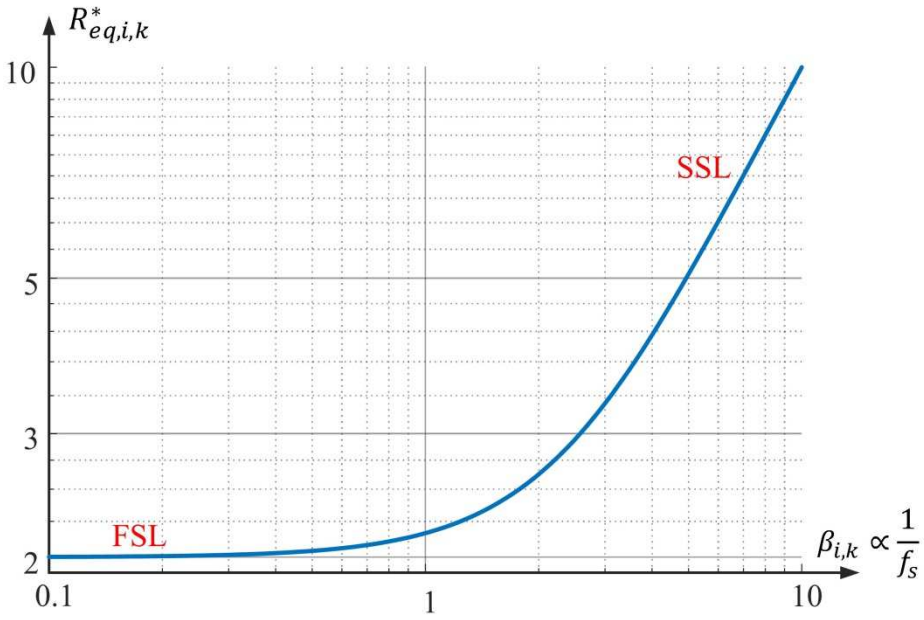


Figure 3-11. Dependency of normalised partial equivalent resistance $R^*_{eq_i}$ versus $\beta_{i,k}$ and duty cycle $D = 1/2$ for hard-switched SC converters

Note that for $D = 1/2$ then since dead-time is neglected then T_k can be approximated as half the switching period, $T_k = T_s/2$ so that (3-17) becomes,

$$\beta_{i,k} \approx \frac{T_s}{2\tau_{loop,i,k}} \tag{3-20}$$

So the physical representation by the parameter beta is of the ratio of half the switching period to the loop time constants.

The small values of the x-axis parameter $\beta_{i,k}$ in Figure 3-11 correspond to the converter switching period being much smaller than the time constant of the RC sub-circuit – see Figure 3-9(a). Whereas large values of the parameter $\beta_{i,k}$ correspond to the converter switching period being much larger than the time constant of the RC sub-circuit – see Figure 3-9(c). It can therefore be seen that the converter has a desirable characteristic of a low value of output resistance for low values of $\beta_{i,k}$, which corresponds to the converter switching frequency approaching the fast-switching limit FSL. Conversely the converter output resistance increases as the switching frequency is reduced toward slow-switching limit SSL, or as $\beta_{i,k}$ increases. Hard-switched SC converters are therefore used at high switching frequencies in order to maximise converter efficiency; however switching losses can then be a problem at high-powers and the soft-switched, resonant SC converter, which is discussed in the next section, becomes the preferred option.

It should be noted that a moderate control of the converter output voltage can be achieved by varying the output equivalent resistance of the converter. This can be done by either altering the

duty cycle as shown in Figure 3-10 or the switching frequency in the for SSL region as shown in Figure 3-11. However this is not an efficient method of varying the output voltage as the average equivalent output resistance no longer has its minimum value and the converter losses will increase.

The above analysis ignores the effect of the dead-time. In practice, the dead-time will reduce the effective duty-cycle D, which results in an increase in the partial equivalent resistance as expected and also predicted by equation (3-18).

The analysis carried out above was for Decoupled topologies. For Coupled topologies the expression for the instantaneous current through the i^{th} component during phase k, $i_{i,k}(t)$, can become very complicated. Unlike for decoupled circuits, where the current waveform is a simple exponential as shown in (3-11), coupled circuit waveforms consist of the sum of a number of exponential terms, the number of which depends on the topology and the number of SC cells. These exponential terms will not have equal time constants, so that the expressions for the average and RMS currents and hence the form-factor does not reduce to the compact hyperbolic form with the single parameter $\beta_{i,k}$ as shown by (3-18). For example, the equations for the loop currents for the coupled, 3-Stage Ladder topology shown in Figure 3-8, which are derived in Chapter 4 and contain two exponential terms with differing time constants. The normalised output resistance is then no longer solely a function of $\beta_{i,k}$, and will also be dependent on an additional parameter, for example the ratio of the loop resistance to the common resistance $R_{ds_{on,1}}$ and $R_{ds_{on,3}}$ in Figure 3-8(b). The normalised output resistance is then represented by a 2-D surface and it can be therefore appreciated that this method of visualising the behaviour of the normalised output resistance becomes unrealistic for higher levels of coupling. In addition, as the number of exponential terms increases for topologies with a large number of stages, the solution has to be solved using numerical methods or symbolically using software such as Mathematica.

3.2 Analysis of Decoupled Resonant SC converters

The method of analysis used for the hard-switched converter can also be applied to the resonant switched capacitor converter. The equivalent circuit of the charging and discharging of each capacitor in a Decoupled resonant SC converter is a series RLC circuit as shown in Figure 3-2. The only difference with hard-switch case is the additional inductance, which can be an external inductance or the stray inductance of the circuit layout. Typical current waveforms for an under-damped resonant SC converter are shown in Figure 3-12. Unlike the hard-switched converter the dead-time can have a significant influence on the shape of the current waveform and hence the form-factor. In the following analysis only converters operating with a 50 % duty cycle are

considered. Therefore each switching phase has a duration of half the switching period $T_s/2$, which is divided up into,

- A conduction period of non-zero current. This has duration T_k for the $k = 1$ and $k = 2$ switching phases for the i^{th} component.
- A dead-time period equal to $T_s/2 - T_k$. The current flowing through the component for waveform (a) and (b2) is assumed zero during this period as will be explained below.

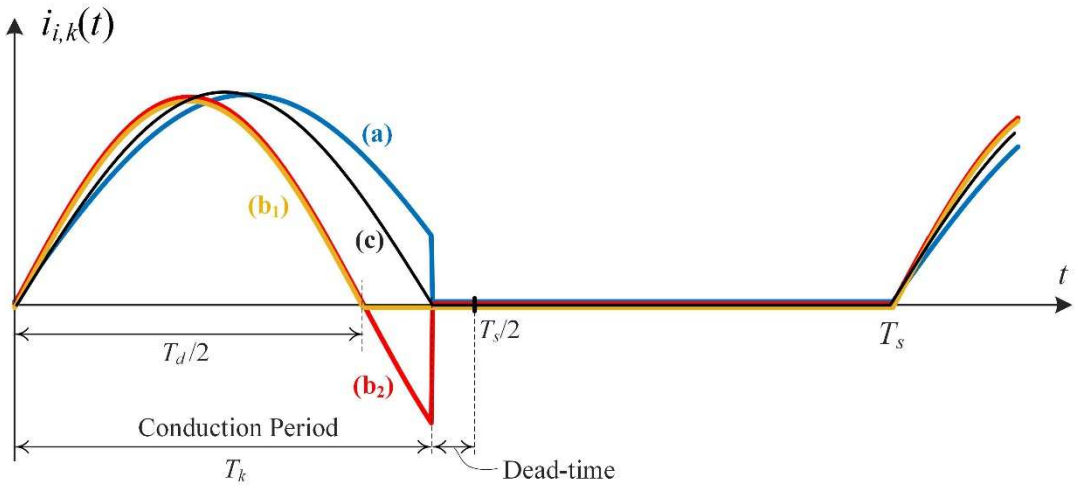


Figure 3-12. Typical current waveforms in a resonant SC converter

The four different current waveforms (a), (b1), (b2) and (c) arise depending on the relative magnitudes of the switching frequency f_s, compared with the natural damped resonance frequency of the RLC equivalent circuit f_d, and also the duration of the dead-time. The waveforms also depend on whether the converter is bi-direction or unidirectional. A bi-directional and unidirectional Doubler circuit is shown as an example in Figure 3-13(a) and Figure 3-13(b) respectively. The four waveforms shown in Figure 3-12 correspond to three different operating modes of the converter:

Mode 1 – waveform (a)

- Half of the damped resonant period is greater than the conduction period $T_d/2 > T_k$.
    - This mode applies to both the bi-directional and unidirectional converters.

Mode 2 – waveform (b)

- Half of the damped resonant period is less than the conduction period $T_d/2 < T_k$:
    - Waveform (b1): unidirectional converter.
    - Waveform (b2): bi-directional converter.

Mode 3 – waveform (c)

- Half of the damped resonant period is equal to the conduction period $T_d/2 = T_k$.
    - This mode is boundary case and applies to both the bi-directional and unidirectional converters.

Considering the Doubler circuit shown in Figure 3-13, for unidirectional step-up operation, switches S_{12} and S_{22} in Figure 3-13(a) are replaced by diodes as shown in Figure 3-13(b), which in this case prevents the current from reversing and the current waveform (b1) results rather than (b2).

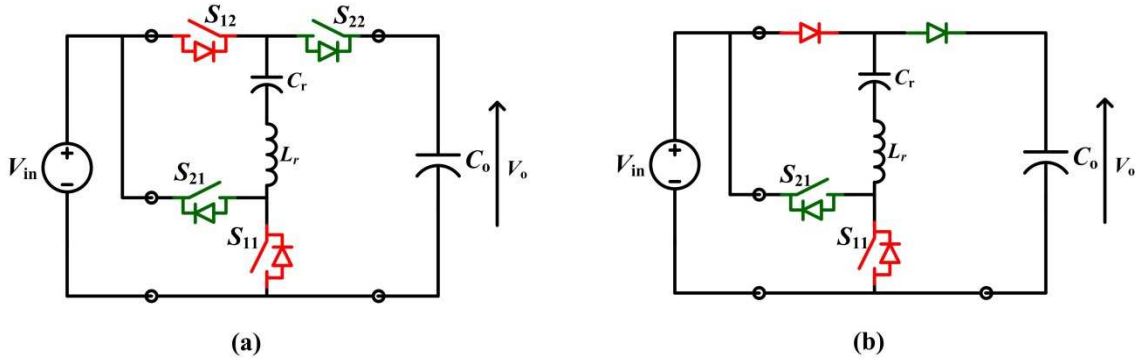


Figure 3-13. SC doubler circuit (a) bi-directional (b) unidirectional

If the inductor current of the resonant SC converter has not already returned to zero prior to the dead-time period as shown in waveforms (a) and (b2), it is rapidly forced to zero by the circuit and this transition is assumed to happen instantaneously as shown by the step-changes in Figure 3-13. This rapid transition can be explained by referring to the diagram of the Doubler circuit in Figure 3-13(a). During the conduction period the inductor voltage is equal to the small difference between the supply voltage and the capacitor voltage and this produces the near half-period sinusoidal current shown in Figure 3-12. However, during the dead-time, with the red-switches turned off any residual current in the inductor will force the diode in S_{21} to turn-on and the current freewheels through S_{21} and S_{12}. The voltage across the inductor is now equal to the capacitor voltage, which is approximately equal to V_{in}, and this rapidly drives the current to zero. This effect becomes more complex for the Ladder and Dixon Charge-Pump circuits where the rate-of-fall of residual current depends on the number of converter stages. In this case the assumption of zero current during the dead-time only applies for small step-up ratios. However, for the remaining converters that are considered in this thesis this approximation holds true.

An analysis for the Decoupled resonant SC converters is described in [79]; however the paper only considers Mode 2, unidirectional operation - waveform (b1), and Mode 3 – waveform (c).

The analysis presented here covers all operation modes for both unidirectional and bidirectional converters. The analysis of Coupled resonant converters is discussed in the following chapter.

3.2.1 Analysis of under-damped resonant SC converters

3.2.1.1 Bi-directional converter – waveforms (a), (b2) and (c)

The expression for the current $i_{i,k}(t)$, flowing through the i^{th} component during switching phase $k = 1,2$, for the Decoupled resonant SC converter is given by,

$$i_{i,k}(t) = \frac{\Delta V_{loop,i,k}}{\omega_{0,i,k} L_{loop,i,k}} e^{-\omega_{0,i,k} t/2Q_{i,k}} \sin(\omega_{d,i,k} t) \tag{3-21}$$

where, $\omega_{0,i,k}$ is the resonant frequency of the equivalent RLC circuit in rads/s, $\omega_{d,i,k}$ is the damped resonant frequency rads/s and $Q_{i,k}$ is the RLC circuit quality factor,

$$\omega_{0,i,k} = \frac{1}{\sqrt{L_{i,k} C_{i,k}}}, \quad Q_{i,k} = \frac{1}{R_{i,k} C_{i,k} \omega_{0,i,k}} \; and \; \omega_{d,i,k} = \omega_{0,i,k} \sqrt{1 - 1/4Q_{i,k}^2} \tag{3-22}$$

The square-root term in $\omega_{d,i,k}$ applies the usual constraint that for an RLC circuit operating in under-damped conditions then,

$$Q_{i,k} > \frac{1}{2} \tag{3-23}$$

Expressions for the RMS and average currents during a switching period $I_{rms,i,k}$ and $I_{avg,i,k}$, can be found by straightforward integration,

$$I_{rms,i,k} = \frac{\Delta V_{loop,i,k}}{2\sqrt{T_s}} \sqrt{\frac{C_{i,k}}{L_{i,k}}} e^{-\frac{T_k \omega_{0,i,k}}{2Q_{i,k}}} \sqrt{\frac{\left(2Q_{i,k} - \frac{1}{2Q_{i,k}}\right) e^{\frac{T_k \omega_{0,i,k}}{Q_{i,k}}} - sin(2T_k \omega_{d,i,k} - \emptyset_{i,k}) - 2Q_{i,k}}{\omega_{0,i,k}}} \tag{3-24}$$

$$I_{avg,i,k} = \frac{\Delta V_{loop,i,k}}{T_s} \sqrt{\frac{C_{i,k}}{L_{i,k}}} e^{-\frac{T_k \omega_{0,i,k}}{2Q_{i,k}}} \frac{\sqrt{1 - 1/4Q_{i,k}^2} e^{\frac{T_k \omega_{0,i,k}}{2Q_{i,k}}} - \cos(T_k \omega_{d,i,k} - \emptyset_{i,k})}{\omega_{0,i,k}} \tag{3-25}$$

Where $\emptyset_{i,k} = tan^{-1}\left(1/\sqrt{4Q_{i,k}^2 - 1}\right)$.

As with the hard-switched case, the normalised partial equivalent resistance $R^*_{eq,i,k}$ is again equal to the current form-factor squared, so that using (3-24) and (3-25),

$$R^*_{eq,i,k} = \left(\frac{\omega_{0,i,k}T_s}{4}\right)\frac{\left(2Q_{i,k} - \frac{1}{2Q_{i,k}}\right)\mathrm{e}^{\frac{T_k\omega_{0,i,k}}{Q_{i,k}}} - sin\left(2T_k\omega_{d,i,k} - \emptyset_{i,k}\right) - 2Q_{i,k}}{\left[\sqrt{1 - 1/4Q^2_{i,k}}e^{\frac{T_k\omega_{0,i,k}}{2Q_{i,k}}} - \cos\left(T_k\omega_{d,i,k} - \emptyset_{i,k}\right)\right]^2} \tag{3-26}$$

Substituting in the same definition of $\beta_{i,k}$ as for the hard-switched case - equation (3-17), and defining the ratio of the conducting period to the switching period,

$$dT_k = \frac{T_k}{T_s} \tag{3-27}$$

where $dT_k = 0 \rightarrow 1/2$, gives,

$$R^*_{eq,i,k} = \left(\frac{\beta_{i,k}}{4Q_{i,k}dT_k}\right)\frac{\left(2Q_{i,k} - \frac{1}{2Q_{i,k}}\right)\mathrm{e}^{\frac{\beta_{i,k}}{Q^2_{i,k}}} - \sin\left(\frac{2\beta_{i,k}}{Q_{i,k}}\sqrt{1 - \frac{1}{4Q^2_{i,k}}} - \emptyset_{i,k}\right) - 2Q_{i,k}}{\left[\sqrt{1 - \frac{1}{4Q^2_{i,k}}}\mathrm{e}^{\frac{\beta_{i,k}}{2Q^2_{i,k}}} - \cos\left(\frac{\beta_{i,k}}{Q_{i,k}}\sqrt{1 - \frac{1}{4Q^2_{i,k}}} - \emptyset_{i,k}\right)\right]^2} \tag{3-28}$$

This equation is a function of the three parameters $Q_{i,k}$, $\beta_{i,k}$ and dT_k and it can be plotted for the three operating modes Mode 1, 2 and 3 for the bi-directional case.

Mode 3 – waveform (c)

This is the boundary operation mode which results zero-crossing for the current. This mode of operation was considered in [79], and the expression for the normalised partial equivalent resistance $R^*_{eq,i,k}$ equation (3-28) reduces to a much more compact form. Since the waveform consists of a half-sinewave, the conduction period must be equal to π radians so that $T_k = \pi/\omega_{d,i,k}$. Under these conditions from (3-17) and (3-22),

$$\beta_{i,k} = \pi\frac{Q_{i,k}}{\sqrt{1 - 1/(4Q^2_{i,k})}} \tag{3-29}$$

Substituting into (3-28) and simplifying gives the compact expression,

$$R^*_{eq,i,k} = \frac{\pi Q^2_{i,k}}{dT_k\sqrt{4Q^2_{i,k} - 1}}\tanh\left(\frac{\pi}{2\sqrt{4Q^2_{i,k} - 1}}\right) \tag{3-30}$$

which was presented in [79]. A plot of equation (3-30) is shown in Figure 3-14 against the quality factor $Q_{i,k}$ for various values of dT_k.

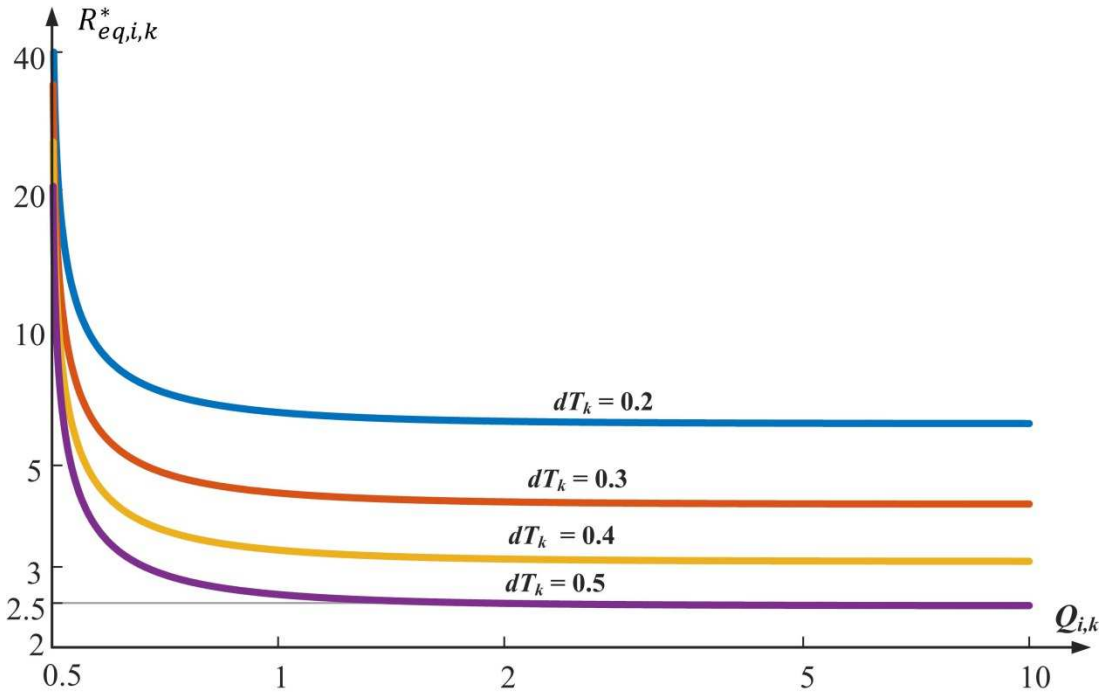


Figure 3-14. Normalised equivalent resistance $R^*_{eq,i,k}$ plotted against quality factor $Q_{i,k}$ for different values of parameter dT_k, for a unidirectional converter operating in Mode 2,

It can be seen from Figure 3-14 that $R^*_{eq,i,k}$ and hence conduction losses are minimised when the switching frequency is equal to the damped resonant frequency, $dT_k = 0.5$. This means that the half-sinusoidal current conducts over half a switching period; however this can only occur if the dead-time is zero. As dead-time increases, dT_k reduces and the normalised equivalent resistance rises.

The figure also shows that normalised equivalent resistance reduces with increasing quality factor $Q_{i,k}$ and asymptotically approaches a minimum value. This value is approximately 2.5 when $dT_k = 0.5$. The reason for this is that at low values of quality factor, the exponential decay term in equation (3-21) becomes significant and the current no longer resembles a half-sinusoid so that the form-factor increases.

3.2.1.2 Unidirectional converter – waveforms (b1)

Since the switches turn-on and off with zero current, this mode of operation produces zero switching loss similar to operation Mode 3, waveform (c). The expression for current $i_{i,k}(t)$, flowing through the i^{th} component during switching phase k=1,2, is similar to that for the Bidirectional converter as given in (3-21). However the current only flows during $t = 0 \rightarrow T_d$ as shown in Figure 3-12. A simple approach to derive the partial normalised output equivalent resistance in this case is to replace dT_k with dT_d in (3-30), which is for boundary operation Mode 3, since the current waveforms (c) and (b1) have identical shapes and where dT_d is defined as follows,

$$dT_d = \frac{T_d/2}{T_S} \tag{3-31}$$

Therefore the partial normalised equivalent resistance $R^*_{eq,i,k}$ can be directly obtained from (3-30) as,

$$R^*_{eq,i,k} = \frac{\pi Q^2_{i,k}}{dT_d\sqrt{4Q^2_{i,k}-1}}\tanh\left(\frac{\pi}{2\sqrt{4Q^2_{i,k}-1}}\right) \tag{3-32}$$

Figure 3-15 shows a plot of $R^*_{eq,i,k}$ against $\beta_{i,k}$ for various values of $Q_{i,k}$ and the parameter dT_k is fixed at the value of 1/2, which minimises the normalised equivalent resistance for all three operation modes of the converter. Since $R^*_{eq,i,k}$ is inversely proportional to dT_k, it is easy to appreciate that the curves move upwards with decreasing dT_k. Figure 3-15 also shows the curve for the hard-switched case for comparison.

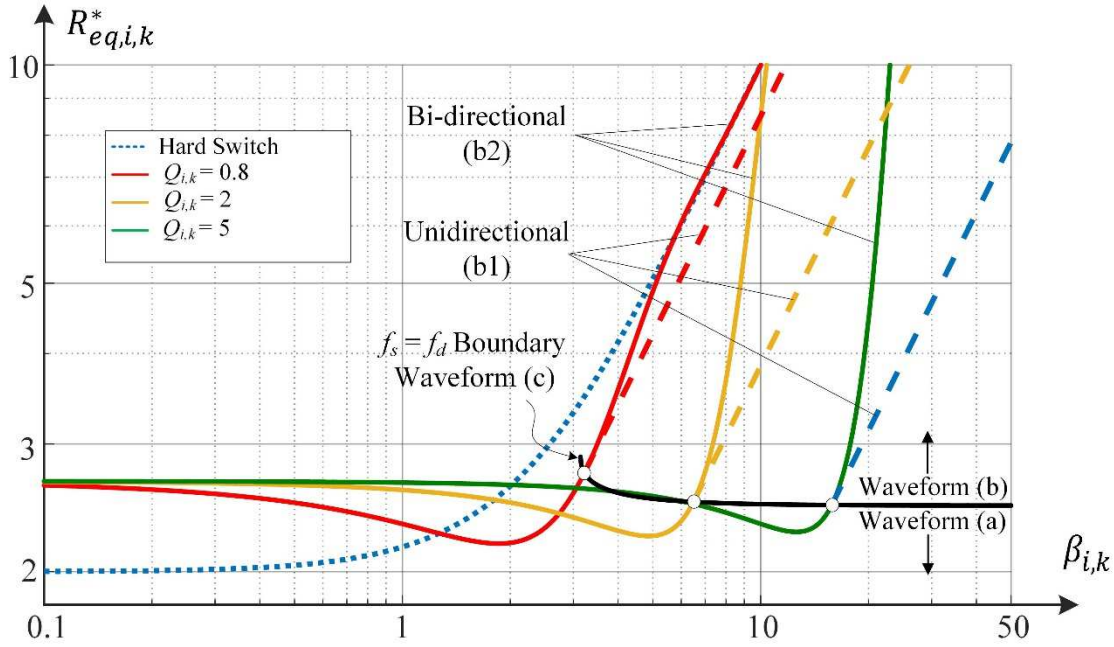


Figure 3-15. Normalised output equivalent resistance for Hard-Switch and resonant SC converters in terms of $\beta_{i,k}$

Figure 3-15 includes an indication of the boundary condition between operating between waveform (a) and (b). This boundary therefore corresponds to the current waveform just reaching zero at turn-off when switching frequency is equal to damped resonant frequency, which is the waveform (c) condition. Switching frequencies lower than damped resonant frequency corresponds to operation Mode 2, which are the waveforms (b1) and (b2).

A number of features are revealed by Figure 3-15:

- At low values of $\beta_{i,k}$ - high switching frequency - which gives the minimum normalised equivalent resistance for the hard-switched case, the resonant SCC has a value which is almost 25 % higher. This is because at high-switching frequencies the current waveform for the hard-switched converter approaches DC during a half-period, which has a form-factor of $\sqrt{2}$, whereas the resonant current waveform is a half-sinusoid which has a form-factor of $\pi/2$. The ratio squared of these two form factors is therefore $\pi^2/8 \approx 1.23$, which explains the poorer efficiency of the resonant converter due to the higher conduction loss. However, it should be remembered that the hard-switched converter will have significantly higher switching losses when operating under these conditions.
- It can be seen that the curves for the resonant converter have minima, which occur for current waveforms of type (a), which are below and to the left of the boundary. It can be seen from Figure 3-12 that this type of waveform has a lower form factor than the other two as its shape is more like an ideal square-wave. Whilst this reduces the normalised equivalent resistance and hence conduction losses, operating in the Mode 1 region means that switching losses now occur.
- Furthermore it can be seen that in operating region around the minima, the normalised equivalent resistance of the resonant SCC is much lower than for the hard-switched case and this occurs at a much lower switching frequency, $\beta_{i,k}$, which minimises switching losses.
- Operating above and to the right of the boundary produces waveform (b1) and (b2). For the bi-directional converter, which is waveform (b2), the normalised equivalent resistance rises sharply in this region and this mode of operation should be avoided. In addition, this mode of operation also produces switching losses. The sharp increase in normalised equivalent resistance arises because the current waveform now has a negative portion so that its average approaches zero. This leads to an increase in form-factor and losses due to the inefficient movement of energy backward and forward between capacitors. For a unidirectional converter, waveform (b1), the equivalent resistance increases linearly as the switching frequency decreases and is shown by the dashed lines in Figure 3-12. In addition, this operation mode benefits from soft switching at turn-on and turn-off. The lowest equivalent resistance in this case achieved when the switching frequency, f_s, approaches the damped resonant frequency, f_d, which is the boundary operation mode.

3.3 Impact of Transistor and Diode On-state Voltage on the Equivalent Circuit of SC Converters

The output equivalent resistance of SC converters has so-far neglected the losses due to the on-state junction voltage of diodes and transistors such as IGBTs. However these effects can easily be incorporated into the model using a constant DC voltage source to represent the on-state voltage as shown in Figure 3-16.

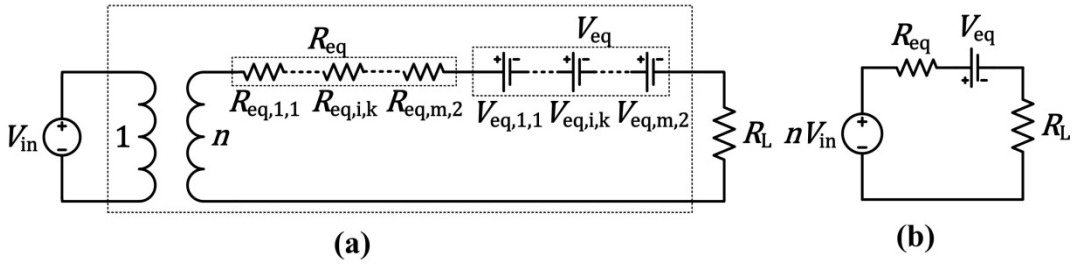


Figure 3-16. Equivalent circuit of SC converters including on-state junction voltages of diodes and IGBTs (a) detailed model and (b) simplified model

The partial output equivalent voltage for the i^{th} semiconductor component during switching phase k, is denoted $V_{eq,i,k}$, and can be calculated by equating the actual losses in the forward voltage of the component against the losses in the equivalent voltage source. For example, for diodes with an on-state voltage $V_{D,i,k}$ then,

$$V_{D,i,k} \cdot I_{avg,i,k} = V_{eq,i,k} \cdot I_o \tag{3-33}$$

Re-arranging for $V_{eq,i,k}$, and introducing the coefficients $a_{i,k}$ from (3-6),

$$V_{eq,i,k} = \left(\frac{I_{avg,i,k}}{I_o}\right) V_{D,i,k} = a_{i,k} V_{D,i,k} \tag{3-34}$$

And the overall output equivalent voltage V_{eq} is the sum of $V_{eq,i,k}$,

3.4 Summary

Switched capacitor converter performance can be assessed using their equivalent output resistance. For hard-switched SC converters, the lowest output resistance is achieved when the switching frequency is high, so that the energy transfer period between capacitors is very short compared to the RC time-constant of the path. The resistance asymptotically reaches this minimum which is known as the Fast Switching Limit (FSL) limit. However, switching losses will then dominate. As the switching frequency is reduced, the output resistance increases significantly and the rate-of change of resistance reaches another asymptotic limit known as the Slow Switching Limit (SSL). Therefore hard-switched converters would not be suitable for high-voltage, high-power applications due to the need for very high switching frequencies, which is difficult to achieve with current semiconductor technology.

It is been shown that resonant SC converters can achieve almost the same conduction loss as hard switched SC converters but at much lower switching frequencies. This is realised by adding small inductors in series with the capacitors. As an additional advantage, resonant SC converters can operate in a soft switching mode where the switches turn on and off with zero current. This occurs when the switch conduction period is equal to the damped resonant period. However this would be difficult to achieve in practice due to the effects of parasitic inductance on the tuning of individual cells.

The resonant SC analysis was extended beyond that presented in current literature by including the operating modes where the switches turn off with non-zero current. This mode reduces the equivalent output resistance losses further when the conduction period is shorter than the damped resonant period. However, the resistance increases significantly when the conduction period is longer than the damped resonant period, and this mode of operation should be avoided.

The analysis given in this chapter was for Decoupled SC converters. The common branches associated with Coupled SC converters will affect the assumptions that were made in this chapter and it is therefore no longer valid. This will be discussed in the next chapter.

4. Coupled SC Converters

4.1 Introduction

Decoupled SC converters have circuit loops that are not coupled by common impedances with other loops. Therefore deriving the output equivalent resistance is straightforward for these topologies. However, for Coupled SC circuits, deriving the circuit equations is more complex and as the number of stages increases the analysis become intractable. This chapter discusses the effects of coupling on the analysis and performance of SC circuits for both hard switched and resonant SC converters.

The 3-stage Ladder circuit shown in Figure 3-8, which is reproduced for convenience here in Figure 4-1(a), is one of the simplest coupled circuits and has only two circuit loops during its first switching phase. It is considered in this chapter in order to demonstrate the effects of coupling on the output equivalent resistance. Only the analysis of the first switching phase is presented here in order to show the coupling effects. However, the analysis for the second phase can be obtained in a similar way.

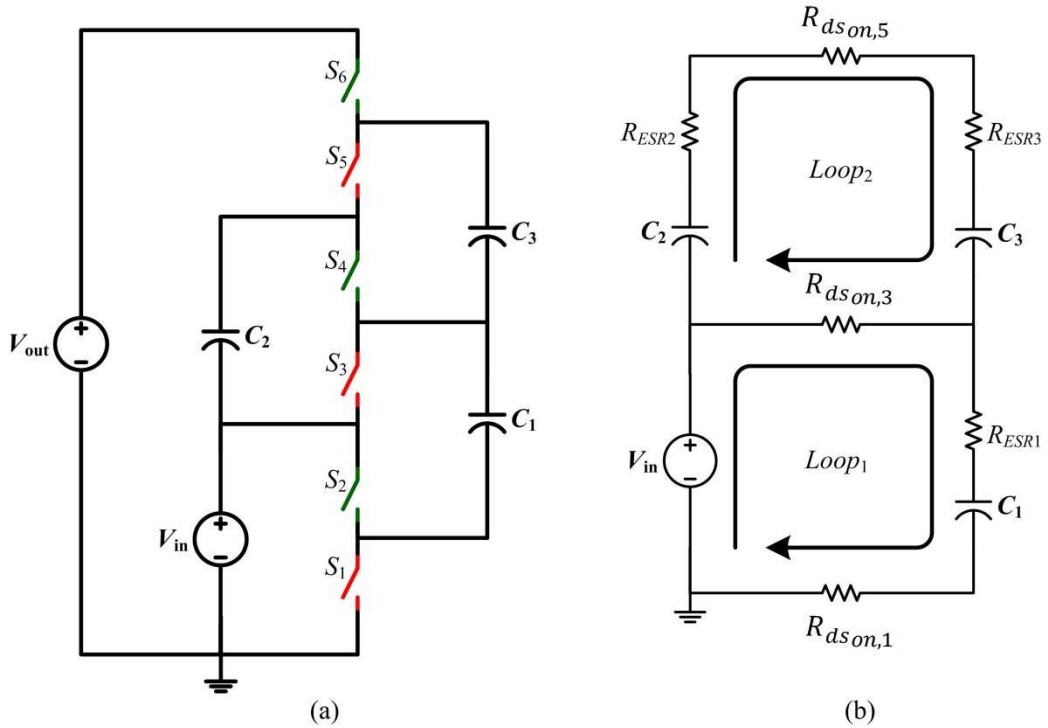


Figure 4-1. 3-Stage Ladder SC converter and the equivalent circuit when the odd-numbered red switches are on (a) circuit diagram (b) equivalent circuit during first switching phase

4.2 Analysis of hard switch 3-stage Ladder circuit in first switching phase

The equivalent circuit of the first switching phase of the 3-stage Ladder circuit is shown in Figure 4-1(b), where the capacitor ESR and switch on-state resistance are denoted R_{ESR} and R_{SW} respectively. The two circuit loops are coupled through the common on-state resistance of switch S_3. For the sake of simplicity, the following assumptions are made:

- All of the switch resistances are equal to R_{SW}.
- All of the capacitors have the same capacitance C and the same R_{ESR}.
- The circuit operates with a duty cycle *D=0.5*.

Considering these assumptions, the equivalent circuit for 3-stage ladder circuit then becomes as shown in Figure 4-2. The initial voltage on each capacitor is shown in the figure. The change in capacitor C_2 and C_3 voltages during the switching phase is denoted $2\Delta V$, so that their initial voltages are $V_{in} \mp \Delta V$ and final voltages $V_{in} \pm \Delta V$ respectively. Since the average current through capacitor C_1 is twice the average current through capacitor C_2 and C_3, the change in voltage for this capacitor is two times higher and is equal to $4\Delta V$. Therefore its initial voltage is $V_{in} - 2\Delta V$.

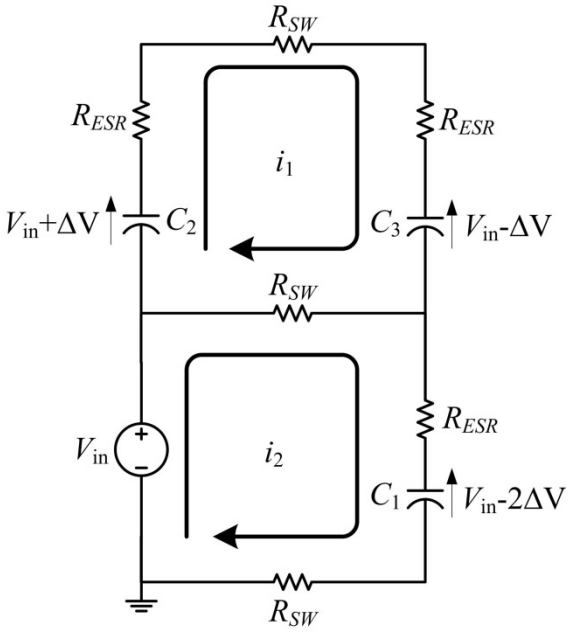


Figure 4-2. Equivalent circuit for 3 stage Ladder circuit during first switching phase showing initial capacitor voltages and assumed loop current directions

In order to calculate the output equivalent resistance, the equations for the circuit branch currents need to be derived. The upper and lower loop currents are denoted i_1 and i_2 resepctively and are assumed to flow in a clockwise direction. The middle branch current i_3 is simply $i_2 - i_1$. In the Laplace domain the upper and lower loop equations for current are:

$$(R_{SW} + 2R_{ESR})i_1 + \frac{2i_1}{sC} + (i_1 - i_2)R_{SW} - \frac{2\Delta V}{s} = 0$$
$$(R_{ESR} + R_{SW})i_2 + \frac{i_2}{sC} + (i_2 - i_1)R_{SW} - \frac{2\Delta V}{s} = 0 \quad (4\text{-}1)$$

The currents $i_1(t)$ and $i_2(t)$ can be obtained in the time domain as:

$$i_1(t) = \frac{\Delta V}{\sqrt{3}R_{SW}}\left(\frac{(3+\sqrt{3})R_{SW}}{2R_{ESR} + (3-\sqrt{3})R_{SW}}\mathrm{e}^{s_1 t} + \frac{(-3+\sqrt{3})R_{SW}}{2R_{ESR} + (3+\sqrt{3})R_{SW}}\mathrm{e}^{s_2 t}\right)$$
$$i_2(t) = \frac{\Delta V}{\sqrt{3}R_{SW}}\left(\frac{2\sqrt{3}R_{SW}}{2R_{ESR} + (3-\sqrt{3})R_{SW}}\mathrm{e}^{s_1 t} + \frac{2\sqrt{3}R_{SW}}{2R_C + (3+\sqrt{3})R_{SW}}\mathrm{e}^{s_2 t}\right) \quad (4\text{-}2)$$

Where s_1 and s_2 are the roots of characteristic equation,

$$s_1 = -\frac{1}{C\left(R_{ESR} + \left(\frac{3-\sqrt{3}}{2}\right)R_{SW}\right)}$$
$$s_2 = -\frac{1}{C\left(R_{ESR} + \left(\frac{3+\sqrt{3}}{2}\right)R_{SW}\right)} \quad (4\text{-}3)$$

The form factor and hence the normalised output equivalent resistance can be calculated from these expressions for each branch current. However, since the current waveforms consist of the sum of two exponential terms with different time constants $1/s_1$ and $1/s_2$, the parameter $\beta_{i,k}$ cannot be defined in the same way as for Decoupled topologies. A new definition for beta is required, for example $\beta_{avg,i,k}$ which is the value of beta arising from the average of the two time constants:

$$\beta_{avg,i,k} = \frac{T_k}{\frac{1}{2}\left(\frac{1}{s_1} + \frac{1}{s_2}\right)} \quad (4\text{-}4)$$

In addition, the coupling introduces an additional independent variable into the equations and a further parameter needs to be defined, for example the ratio of switch on-state resistance R_{SW} to the capacitor ESR, R_{ESR}denoted by K_r,

$$K_r = R_{SW}/R_{ESR} \quad (4\text{-}5)$$

Using these equations, expressions for the normalised output equivalent resistance $R^*_{eq,i,1}$, were computed using Mathematica software and are shown in Appendix B, in equations (B-2) to (B-3). These equations were used to plot the normalised output equivalent resistance $R^*_{eq,i,k}$ against $\beta_{avg,i,k}$, for different values of K_r where it was found that all the curves have the same shape, and this shape is the same as that for the decoupled converter shown in Figure 3-11. For example, the normalised output equivalent resistance during switching phase $k = 1$, $R^*_{eq,i,1}$, for the upper switch 5 and capacitors C_2 and C_3 is shown in Figure 4-3 for a typical value of $K_r = 10$.

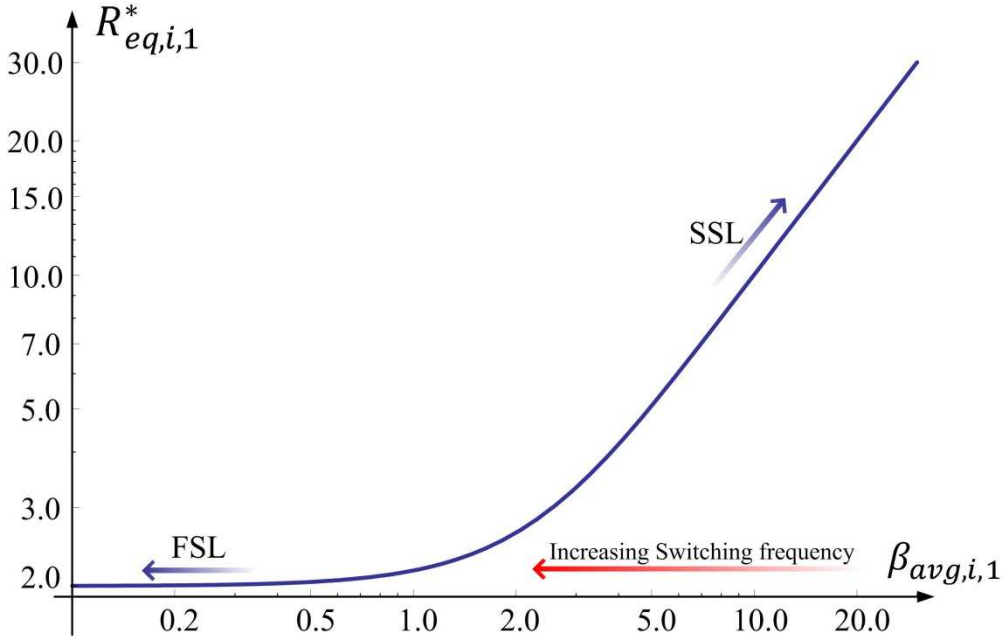


Figure 4-3. Switching phase 1, normalised output equivalent resistance $R^*_{eq,i,1}$ for the upper loop components against $\beta_{avg,i,k}$ with $K_r = 10$

The reason for the same curve shapes for coupled and decoupled cases is that as discussed in Chapter 3, in the fast switching limit (FSL) region the current waveform tends toward a DC value over the switching phase so that form-factor becomes unity and is independent of beta. Whereas in the slow switching limit region (SSL), the conduction loss is independent of circuit resistance and is purely a function of capacitance and the initial and final voltages on the capacitors – see equation (2-4). In this case, re-tracing the steps starting from equation (3-1) it can be shown that:

$$R^*_{eq,i,k} = \frac{T_S}{2C_{Ti,k}R_{i,k}} \tag{4-6}$$

Where $C_{Ti,k}$ is the combined series capacitance of the i^{th} capacitor charging/discharging pair. It can be seen from this equation that the normalised output equivalent resistance is equal to half the ratio of the switching period to the time-constant, which is the definition of beta for example see the uncoupled case (3-20), so that in the SSL region $R^*_{eq,i,1}$ is equal to beta.

At the corner frequency between the FSL and SSL regions, the curve shape will differ depending on the amount of coupling K_r.

Note that if the switch resistance $R_{SW} = 0$, the coupling between the two loops is broken and the roots s_1 and s_2 are then equal and the equations reduce to those presented in Chapter 3 for Decoupled circuits.

4.3 Analysis of resonant 3-stage Ladder circuit

This section investigates the effects of coupling on the operation of resonant SC converters. Similar to the hard switched case, a 3-stage Ladder circuit is considered here as shown in Figure 4-4(a), in order to analyse the effects of coupling, where the resonant capacitor and inductor components are denoted C and L_r. In this example, the parasitic inductance of the switch branches L_s, act as common impedances between the circuit loops. Coupling in resonant SC converters affects the resonant frequency of the individual loops and therefore degrades the overall performance of the converter. In a decoupled resonant SC circuits, each circuit loop is an independent series RLC circuit; therefore deriving the current equations and the associated output equivalent resistance is quite straightforward. However, in coupled resonant circuits, the current equations for individual loops consist of a sum of damped sinusoidal waveforms, the number of which depends on the topology and the quantity of SC cells. The equivalent circuit for a 3-stage resonant circuit during first switching phase is shown in Figure 4-4(b), where for the sake of simplicity all resistive elements have been neglected. This simplification is justified since the series resonant circuits are lightly damped by design.

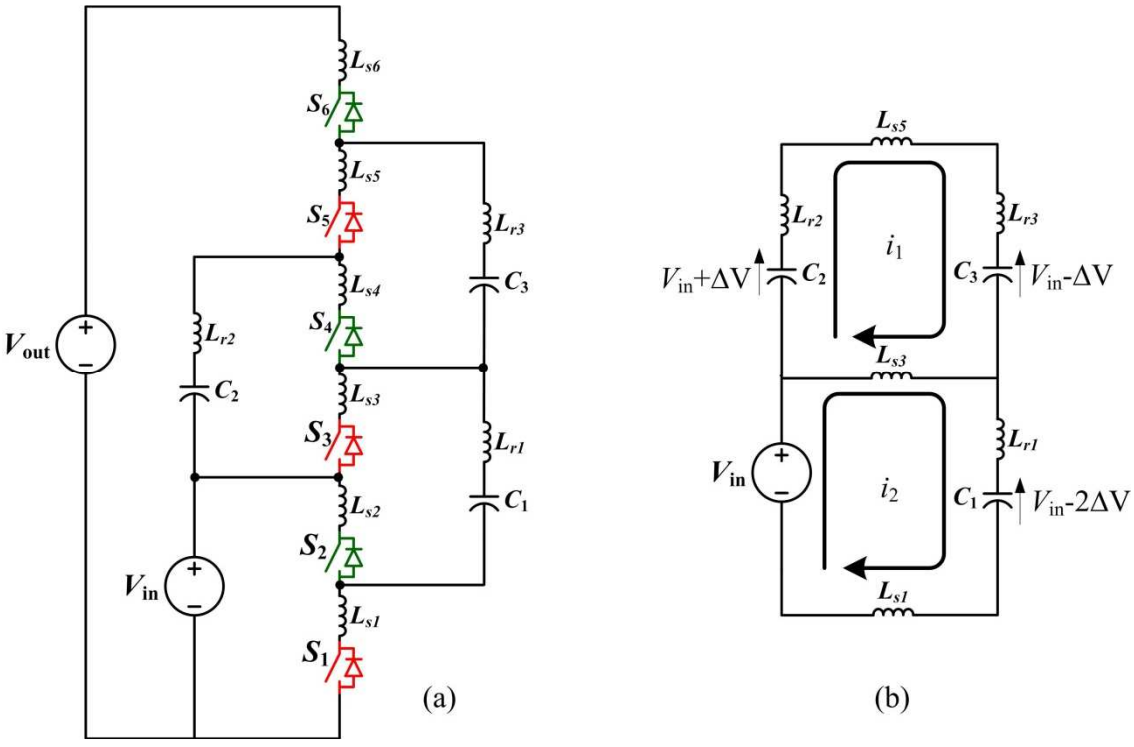


Figure 4-4. 3-stage Ladder circuit (a) circuit diagram (b) equivalent circuit during first switching phase

Assuming all of the switches have the same stray inductances equal to L_s and the resonant inductors are equal to L_r, the equations for the upper and lower loop currents i_1 and i_2 in the Laplace domain are,

$$i_1 = \frac{I_0}{(\omega_1^2 - \omega_2^2)}\left(\frac{C\omega_1^2(3L_s + L_r) - 1}{(s^2 + \omega_1^2)} - \frac{C\omega_2^2(3L_s + L_r) - 1}{(s^2 + \omega_2^2)}\right)$$
$$i_2 = \frac{I_0}{(\omega_1^2 - \omega_2^2)}\left(\frac{C\omega_1^2(3cL_s + 2cL_r) - 2}{(s^2 + \omega_1^2)} - \frac{C\omega_2^2(3L_s + 2L_r) - 2}{(s^2 + \omega_2^2)}\right) \quad (4\text{-}7)$$

where

$$\omega_1 = \sqrt{\frac{2}{C\left(\left(3+\sqrt{3}\right)L_s + 2L_r\right)}}$$
$$\omega_2 = \sqrt{\frac{2}{C\left(\left(3-\sqrt{3}\right)L_s + 2L_r\right)}} \quad (4\text{-}8)$$

$$I_0 = \frac{2\Delta V}{C(2L_r^2 + 6L_rL_s + 3L_s^2)} \quad (4\text{-}9)$$

Converting these equations to the time domain, the three branch currents $i_1(t), i_2(t)$ and $i_3(t)$, where the middle branch current $i_3(t)$ is simply $i_3(t) = i_2(t) - i_1(t)$, are,

$$i_1(t) = \frac{1}{2}C\Delta V\left(\left(1-\sqrt{3}\right)\omega_1 \sin(\omega_1 t) + \left(1+\sqrt{3}\right)\omega_2 \sin(\omega_2 t)\right)$$
$$i_2(t) = C\Delta V(\omega_1 \sin(\omega_1 t) + \omega_2 \sin(\omega_2 t)) \quad (4\text{-}10)$$
$$i_3(t) = \frac{1}{2}C\Delta V\left(\left(1+\sqrt{3}\right)\omega_1 \sin(\omega_1 t) + \left(1-\sqrt{3}\right)\omega_2 \sin(\omega_2 t)\right)$$

From (4-10), each branch current consists of the sum of two sinusoidal waveforms with different frequencies. Since the zero crossings of the current are important in ensuring efficient operation of the converter and because these two frequencies are a function of an uncontrolled switch parasitic inductance, it becomes difficult to ensure correct operation of the circuit. Furthermore, as the number of converter stages increases, so does the number of resonant frequency components within the current waveform so that the problem becomes significantly worse. The zero crossing problem can be highlighted by defining a nominal resonant frequency $\omega_0 = 1/\sqrt{L_rC}$ and the parameter $K_l = L_s/L_r$, ω_1 and ω_2 can be reformulated as a function of ω_0 and K_l as follow,

$$\omega_1 = \omega_0\sqrt{\frac{2}{\left(\left(3+\sqrt{3}\right)K_l + 2\right)}}$$
$$\omega_2 = \omega_0\sqrt{\frac{2}{\left(\left(3-\sqrt{3}\right)K_l + 2\right)}} \quad (4\text{-}11)$$

A Micro-Cap Spice simulation using the parameters listed in Table 4-1 was carried out in order to validate the equations derived in this Chapter, and the results are shown in Figure 4-5., which shows the simulated current waveforms $i_1(t)$, $i_2(t)$ and $i_3(t)$ for $K_l = 0.1$ along with the predicted currents waveforms using (4-10). Note that the simulated waveforms include typical

values for circuit resistance, whereas the predicted waveforms, which have been calculated using the analytic equations, assume zero resistance.

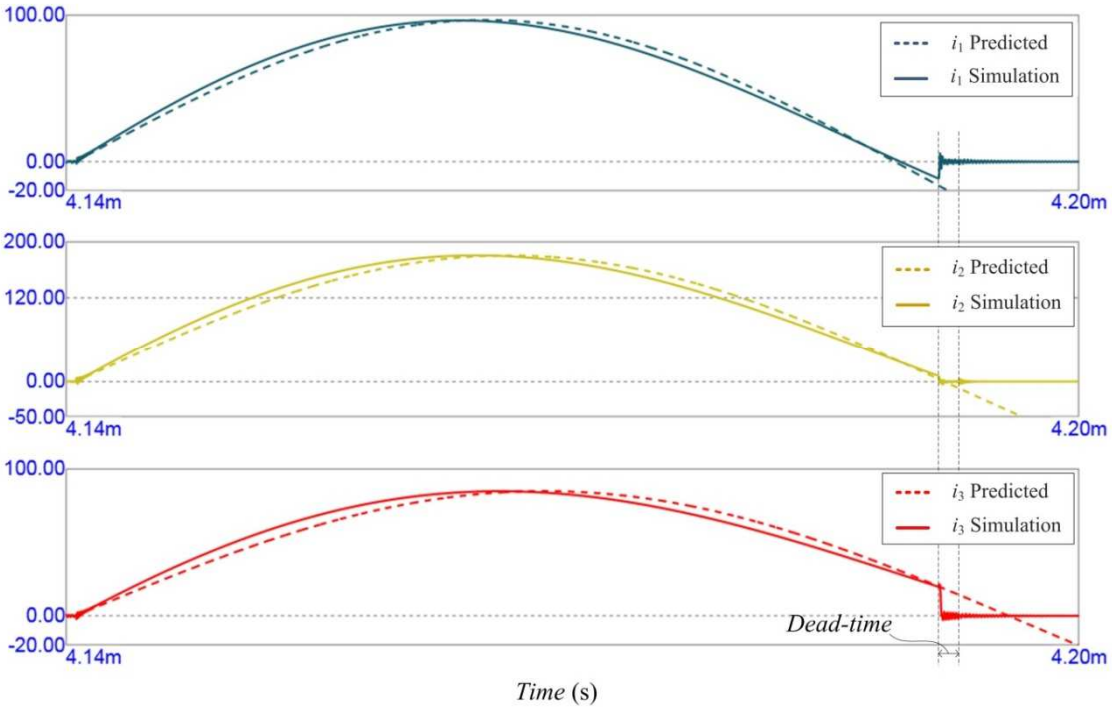


Figure 4-5. Simulation and predicted current waveforms in (A) for $i_1(t)$ (upper), $i_2(t)$ (middle) and $i_3(t)$ (lower) against time (s) for a 3-stage coupled Ladder circuit using the parameters listed in Table 4-1

Table 4-1. Parameters used for the Micro-Cap simulation of 3-stage coupled Ladder circuit shown in Figure 4-5

Component /Parameter	Values
Conversion ratio	3
L_s	0.1 µH
L_r	1 µH
C	200 µF
R_{ESR}	15 mΩ
R_{SW}	5 mΩ
Load	10 Ω resistive
Input voltage V_{in}	100 V

The simulated and predicted current waveforms show good agreement. Any errors are due to the assumption of zero resistance for the predicted waveforms. The different zero crossings of the waveforms due to coupling are clearly discernible form the plots. Current $i_2(t)$ is the closest to the ideal desired waveshape, reaching zero just as the switches turn off. However, current waveform $i_1(t)$ and $i_3(t)$ turn off with a finite current and their form factors deviate from the ideal half sinusoid. It should be noted that when the simulation is carried out for the ideal circuit

with zero resistance for the components, the predicted waveforms matches with the simulation results.

The results of numerically solving for the angular frequencies ω_0 for which the currents $i_1(t), i_2(t)$ and $i_3(t)$ cross zero and plotting against K_l are shown in Figure 4-6.

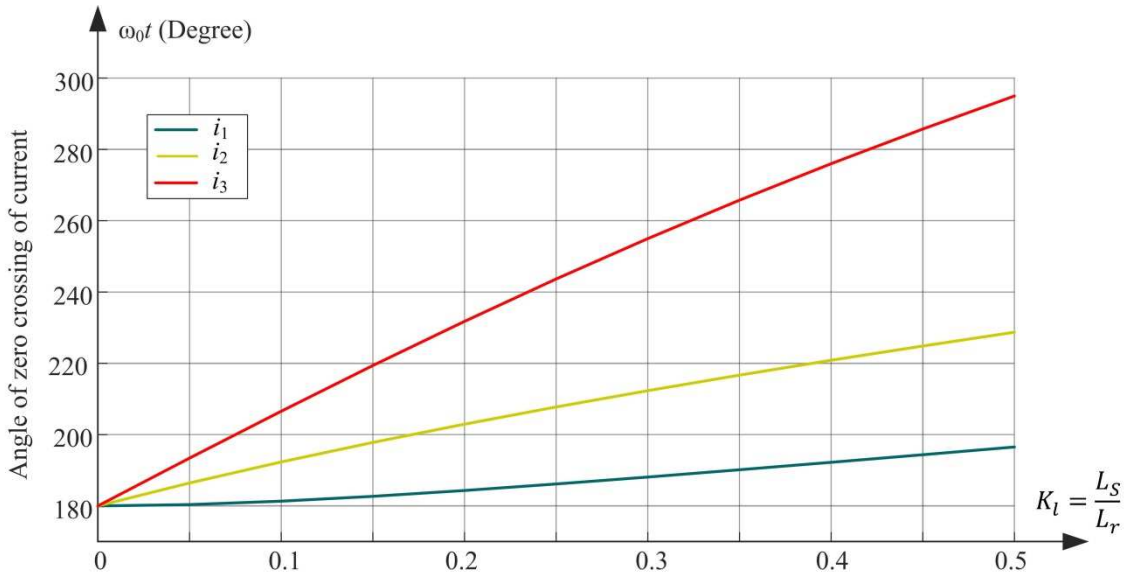


Figure 4-6. Angle of zero crossing of currents $i_1(t)$, $i_2(t)$ and $i_3(t)$ (degrees) against. K_l

It can be seen from the figure that as the coefficient K_l increases above zero, the zero crossings of the currents start to diverge. Looking at the example waveforms in Figure 4-5 for $K_l = 0.1$, where it is seen that $i_2(t)$ crosses zero at the right instant for zero switching loss, then from Figure 4-6 currents $i_1(t)$ and $i_3(t)$ cross zero at approximately ±12° with respect to $i_2(t)$. They will therefore switch with a current of $\sin(12°) = 0.21$, or 20 % of the peak sinusoidal current. This corresponds to a significant switching loss in these branches and it can be concluded that the effect of coupling has a detrimental effect on the performance of the resonant SC converters.

5. Measuring the Parasitic in Resonant SC Converters

5.1 Introduction

An ideal resonant SC converter would consist of components having zero parasitics: for example switches would have negligible resistance and inductance, whereas the resonant LC components would be completely defined by their design inductance and capacitance. However, in practice the parasitic inductance of connecting wires, which may be different in each cell, will affect the resonant frequency. In addition, whilst circuit parasitic resistance has a negligible effect on the damping resonant frequency, it can significantly reduce the converter efficiency through circuit conduction loss. It is therefore important to obtain values of the circuit parasitic inductance and resistance in order to assess the overall efficiency and output voltage regulation for a particular converter layout [79] and make any adjustments to the design where necessary. This chapter proposes a method by which SC circuit parasitics can be estimated in order to assist in the design of such a converter. The results are validated against simulation and measurements from a hardware prototype.

5.2 Doubler SC converter

The Doubler SC converter is considered here because of its simple structure. The ideal circuit is shown in Figure 5-1(a).

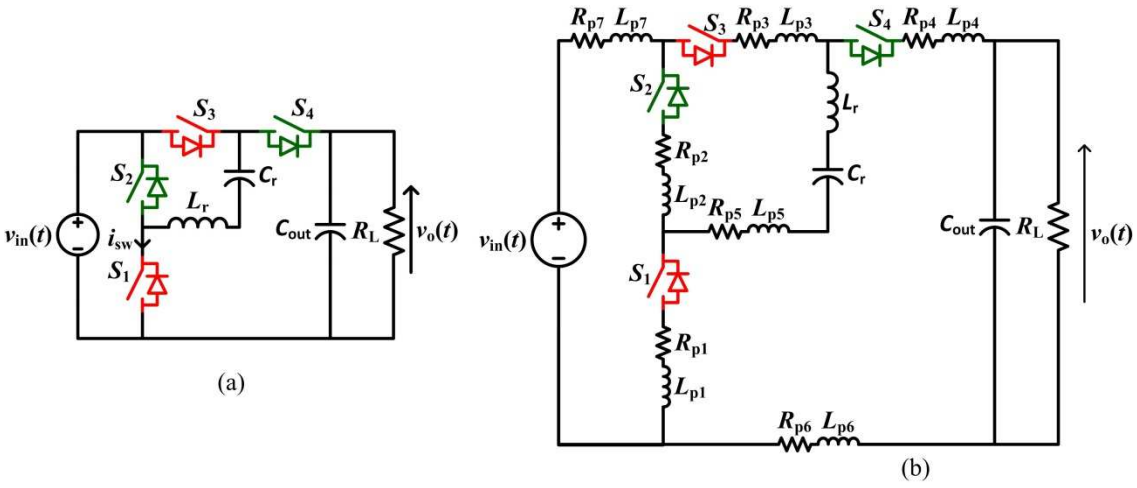


Figure 5-1. Voltage double switched capacitor converter (a) ideal circuit (b) circuit including parasitic

The converter has an instantaneous input and output voltage v_{in} and v_o respectively and switch pairs S_1/S_3 and $S_2/\ S_4$ operate in anti-phase with a 50% duty-cycle. The resonant circuit consists of capacitor C_r and inductor L_r and the converter feeds a load R_L through a filter capacitor C_{out}.

For a non-ideal converter each branch of the circuit will have parasitic inductance and resistance as represented by the lumped components L_{p1}, R_{p1}…., L_{p7}…R_{p7} in Figure 5-1(b). There will also be parasitic capacitance, which is not shown in the figure but which has been included in the measurement technique outlined in this chapter. Whilst the Doubler circuit is a decoupled topology, the resonant frequency of the circuit be different between the two phases of the switching period of the converter due to the different impedances of the branches – see Figure 5-2, where the resonant frequency for the circuit shown in Figure 5-2(a), is $1/((L_{p1} + L_{p3} + L_{p5} + L_{p7} + L_r)C_r)$ and for Figure 5-2(b) is $1/((L_{p2} + L_{p4} + L_{p5} + L_{p6} + L_{p7} + L_r)C_r)$. Hence, additional inductance/capacitance may need to be added to the circuit in order to re-tune the resonant frequency of each cell to be equal to the converter switching frequency.

Furthermore, the parasitic resistance will damp the circuit, which leads to a further reduction in converter efficiency. Again, this damping will be different between the two switching phases, and the assessment of circuit parasitic resistance is important in order to identify cells that have high resistance so that corrective measures can be applied.

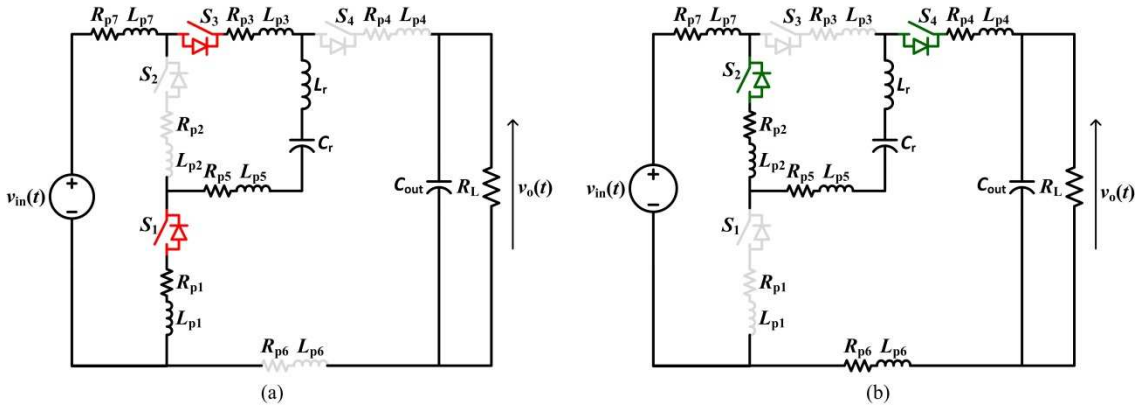
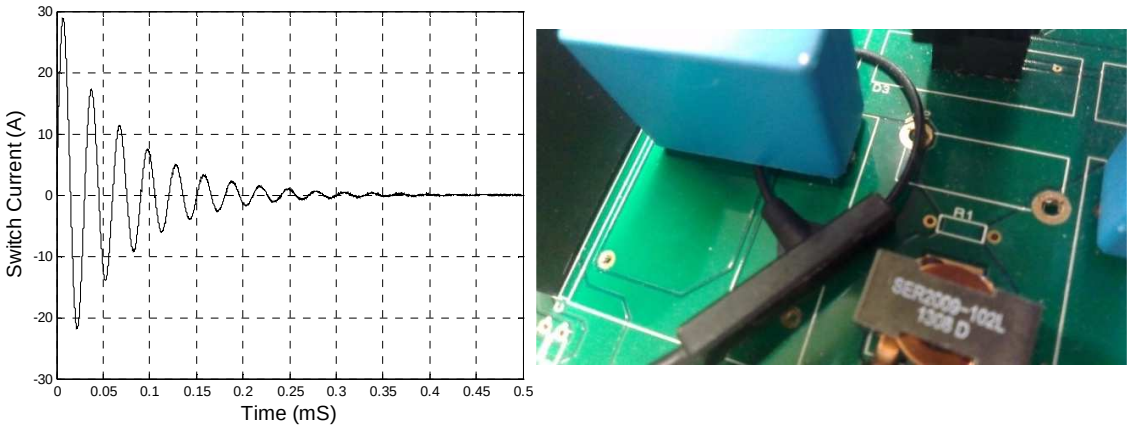


Figure 5-2. Equivalent circuit during the (a) first and (b) second phases of the converter switching period

5.3 Determination of Parasitic Components

The method proposed in this chapter for estimating the circuit parasitic is based on system identification of the equivalent series RLC circuits formed during the two switching phases of the converter. In this method the converter switching frequency is significantly reduced below its normal operating value so that the switch current-waveform consists of a number of resonant cycles rather than a single, half-sinusoid. The circuit damping will now be apparent as the sinusoid current will decay over a number of cycles as shown by a typical measurement from a hardware prototype circuit in Figure 5-3(a). The reduction in switching frequency is chosen such that the current transient falls to approximately 1 % of its initial peak value over the measurement period.



(a) (b)

Figure 5-3. (a) Measured resonant switch current with a reduced converter switching frequency (b) close-up photo of the PEM probe connected around the capacitor leg

Note that whilst the converter input voltage v_{in} should ideally be DC, in practice the input voltage source will have its own internal parasitic impedances so that the voltage seen by the resonant circuit will be time varying during the transient. The average of this input voltage must be reduced during these tests otherwise the peak resonant current will exceed the rating of the converter components. The equivalent RLC circuits for each switching phase have as their inputs the voltage v_{in} and the voltage $v_{in} - v_o$ for the first and second switching phases respectively. The circuit equation for the two switching phases is,

$$v = R_T i + L_T \frac{di}{dt} + \frac{1}{C_r}\int_0^T i\,dt \tag{5-1}$$

where i is the current flowing through the resonant components L_r and C_r, and T is the period over which the waveform has been measured. Furthermore L_T and R_T are the total inductance and resistance of the resonant circuit respectively, which include the parasitics for that particular switching phase. For the first phase of the switching period,

$$\begin{aligned} v &= v_{in} - V_{Cr0} \\ L_T &= L_r + L_{p1}+L_{p3}+L_{p5}+L_{p7} \\ R_T &= R_{p1}+R_{p3}+R_{p5}+R_{p7} \end{aligned} \tag{5-2}$$

where, V_{Cr0} is the measured initial voltage on the capacitor C_r at $t = 0$, and for the second phase,

$$\begin{aligned} v &= v_{in} - v_o + V_{Cr0} \\ L_T &= L_r + L_{p2}+L_{p4}+L_{p5}+L_{p7} \\ R_T &= R_{p2}+R_{p4}+R_{p5}+R_{p7} \end{aligned} \tag{5-3}$$

A current probe is the most convenient and accurate method for measuring the current i. However the probe must be small enough so that it can be directly placed in the circuit with minimum

disturbance to the existing circuit, otherwise the measurement itself can add additional parasitics to the circuit. For example, the addition of a small loop of wire to an existing conductor to accommodate a split-core type, clip-on probe will significantly alter the inductance of the circuit. The current measurements presented in this paper were carried out using a PEM Ultra-Mini, Rogowski probe [83]. This probe is small enough to allow access to the resonant capacitor leg by lifting the capacitor approximately 1 mm off the PCB – as shown in Figure 5-3(b). The disadvantage of using a Rogowski coil is that the measurement is AC coupled and the DC component in the waveform shown in Figure 5-3 is lost. However, equation (5-1) can be extended to include the orthogonal missing DC offset denoted i_{DC}, from the probe measurement i_{probe}, since $i = i_{DC} + i_{probe}$ then (5-1) becomes,

$$v = R_T i_{probe} + L_T \frac{di_{probe}}{dt} + \frac{1}{C_r}\int_0^T i_{probe}\, dt + \frac{i_{DC}}{C_r} t + R_T i_{DC} \tag{5-4}$$

The last term in (5-4) is an unknown DC voltage. However it can be neglected in practice since it is very small when compared with the DC voltage on the capacitor $V_{Cr0} >> R_T i_{DC}$, so that equation (5-4) becomes in matrix form,

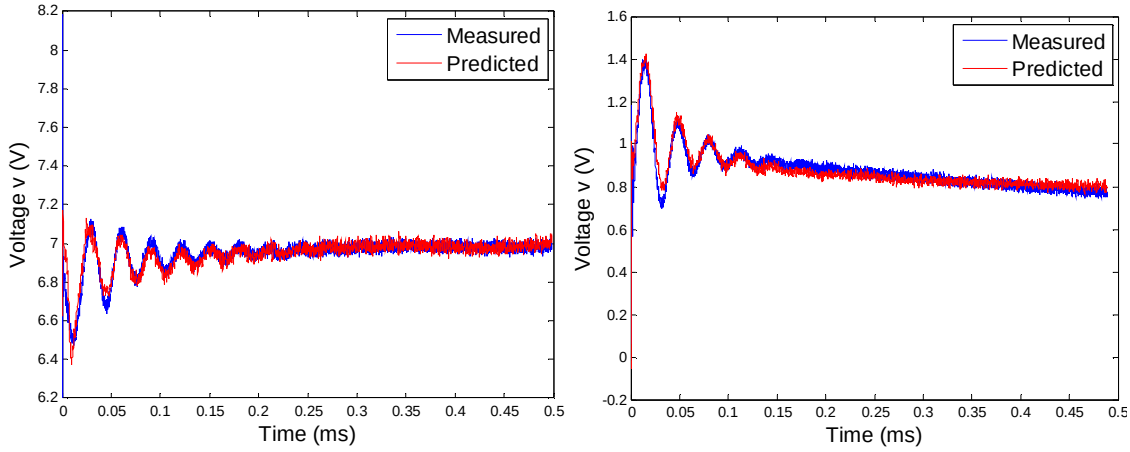
$$v \approx \begin{bmatrix} i_{probe} & \frac{di_{probe}}{dt} & \int_0^T i_{probe}\, dt & t \end{bmatrix} \begin{bmatrix} R_T \\ L_T \\ 1/C_r \\ i_{DC}/C_r \end{bmatrix} \tag{5-5}$$

Equations (5-5) is linear with unknown constant coefficients R_T, L_T , $1/C_r$ and i_{DC}/C_r. This equation can be solved by using a least-squares fit to the measured data v and i_{probe}. However, initial processing of the measured current i_{probe}, is needed in order to calculate the integral and differential terms in (5-5). In particular the differential term di_{probe}/dt is susceptible to quantisation noise from the oscilloscope, which can introduce unacceptable errors. Therefore a 4^{th} order Savitzky-Golay (SG) filter [84], with 1.05 filter length was implemented to calculate this differential term. Reflection of the measured waveform around $t = 0$ and $t = T$ was used to pad out the beginning and end of the data respectively for the SG filter.

5.4 Measurement Results

The voltage and current waveforms for the two switching phases were measured from a 1 kW, 100 V hardware prototype – the development of this hardware is discussed in more detail in Chapter 7. MATLAB code was used to calculate the integrals and SG filtered differentials of the measured current and solve the system of equations (5-5), using a least-squares fit algorithm. The measured voltage and current waveforms were sampled at 20 MHz, over a period of 0.5 ms. The

measured and predicted voltage waveforms *v*, for each of the switching phases is shown in Figure 5-4.



(a) (b)

Figure 5-4. Measured and predicted resonant voltage v (V) waveforms (a) phase 1 of the switching period and (b) phase 2 of the switching period

It can be seen that there is a good agreement between the measured and predicted voltage waveforms so that the parameters L_T, R_T and C_r that were calculated from the least-squares-fit give an accurate model of the circuit. The values of L_T, R_T and C_r for each of these two phases of the switching period are shown in Table 5-1,

Table 5-1 Estimated circuit parameters using least-squares fit

	L_T (µH)	R_T (mΩ)	C_r (µF)
Phase 1	1.12	31.4	22.5
Phase 2	1.29	64.3	21.4

The values of the resonant inductor L_r and capacitor C_r used in the prototype had nominal data sheet values of 1 µH and 22 µF respectively. One effect of parasitics manifests itself as the difference in circuit parameters between the two switching phases. For example, it can be seen that the difference between the estimated capacitance for the two phases is quite low as the PCB layout and switches do not have any significant parasitic capacitance. However, the difference in parasitic inductance and resistance between each switching phase is quite significant: the resistance of the phase 2 circuit is almost twice that of phase 1, which means conduction losses are doubled. Also, the parasitic inductance of the phase 1 circuit is lower than phase 2, which means that its resonant frequency will be around 10 % higher. A small additional inductor can be used to re-tune the cell so that the resonant frequencies are the same. However, whilst this would acceptable for a simpler Doubler circuit, it would be a very difficult task to carry out on a converter with a large number of cells. The measured voltage and current waveforms for switch S_1 of the converter hardware are shown in Figure 5-5(a) for the first charging phase of the

switching cycle and the corresponding switch currents for both the first and second phases - charging and discharging - of the switching cycle are shown in Figure 5-5(b).

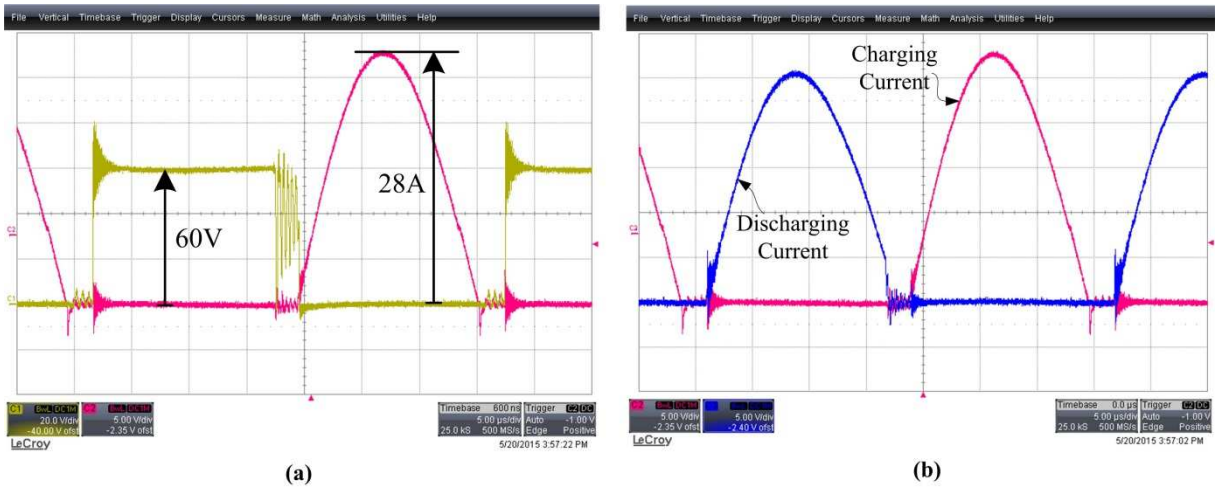


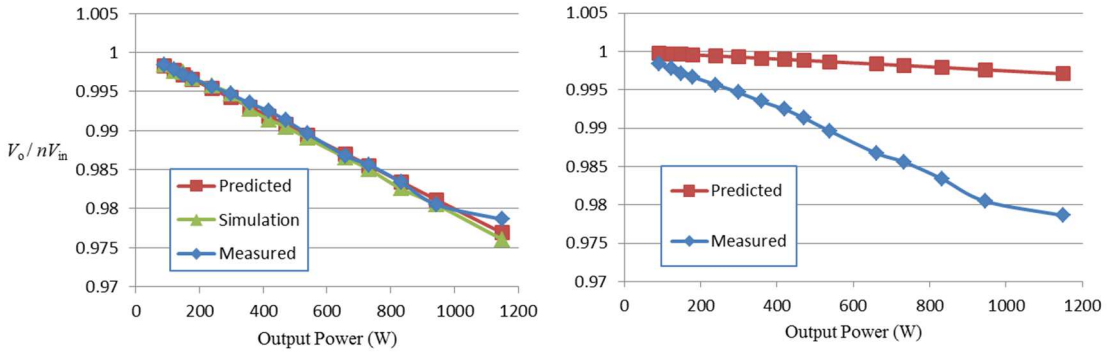
Figure 5-5. Experimental results (a) Switch S_1 current (5A/div) and voltage waveform (20 V/div) for charging phase and (b) current waveform for charging and discharging phases (5 A/div), time axis (5 µs/div)

The effect of the differences in circuit impedances between the two phases is quite apparent from Figure 5-5(b), where it can be seen that the current waveforms have different magnitudes and periods during the two switching phases. In particular the discharging current is non-zero at turn-off for the discharging current. Note that the waveforms in the above figure include a 2 µs dead-time for each switch.

The calculated equivalent resistance R_{eq} for the 2-cell hardware prototype based on the parameters given in Table 5-1 and the analysis presented in chapter 3 from equations (3-9) and (3-30) is R_{eq}=277.5 $m\Omega$, where $n = 2$. The predicted output voltage using this resistance as a voltage- behind-resistance equivalent circuit model is shown in Figure 5-6(a), where the voltage has been normalised by nV_{in}. Also included in Figure 5-6(a) are the results from a detailed, Micro-Cap Spice simulation of the circuit presented in Figure 5-1(b) using ideal switches and measurements from the hardware prototype.

It can be seen from Figure 5-6(a) that there is very close agreement between the predicted, measured and simulated values. The voltage regulation is approximately 2.5 % at full-load. However the sensitivity of the converter voltage regulation to circuit parasitics can be seen in Figure 5-6(b) where the predicted output voltage using the equivalent circuit model does not include circuit parasitics, and is compared against the measured values. The calculated equivalent resistance in this case is 34.8 $m\Omega$ and is based on the datasheet values for the MOSFET (IRFP4468PbF from International Rectifier) with $R_{ds,on} = 3$ mΩ, EPCOS 22 µF film capacitors with an ESR of 2 $m\Omega$ and Coilcraft SER1590 1 μH inductors with a parasitic resistance of 0.9

$m\Omega$. It can be seen that without the inclusion of circuit parasitics the equivalent circuit dramatically underestimates the voltage regulation by around 8 times.



(a) (b)

Figure 5-6. Predicted and measured normalised converter output voltage (a) including detailed simulation results and (b) predicted without the inclusion of circuit parasitics

5.5 Summary

This chapter has described a method of calculating values of inductance, resistance and capacitance for each of the cells of a switch-capacitor converter. The measurement of these parameters is important in order to estimate the overall voltage regulation and efficiency of the converter and hence carry out any necessary corrections to the design. The method was demonstrated using measurements from a hardware prototype, and the results showed that the calculated parameters gave an accurate equivalent circuit model of the converter. In addition if parasitics are not included in the analysis, the error in predicting the prototype converter output voltage was underestimated by approximately 8 times, which is unacceptable. This highlights the importance of determining parasitics in a SC design, especially when there are a large number of SC cells having different circuit arrangements such as non-modular converter topologies. The next chapter considers new SC topologies where features such as a modular design, which helps the management of parasitics, is seen as a significant benefit when appraising a new circuit.

6. Proposed New SC Topologies for HVDC Applications

The suitability of existing SC topologies for HVDC applications was examined in Chapter 2. The Ladder, Dixon Charge Pump, MMSCC and SMMSCC were identified as candidate circuits for HVDC applications. Amongst these topologies, the Ladder is the only circuit which has desirable features where all of the switches have the same voltage rating, and this rating is equal to low-voltage input of the converter. In other candidate topologies, some switches need to be rated to twice the low-voltage input. Although the Ladder is a better topology in terms of switch voltage rating, it has lower efficiency compared to other candidate circuits for the same overall amount of electrical capacitance. In this chapter new topologies will be proposed for HVDC applications using new synthesis techniques. These techniques consist of:

- Parallel converters with common voltage nodes.
- Stacking and Splitting capacitors.
- Modularisation.
- Bi-pole arrangements.

Each of these techniques will now be described along with the presentation of a number of new circuit topologies that emerge from applying these methods. In the following sections, circuits are drawn for hard-switched converters but the synthesis also applies to the resonant SC implementation where an inductor is connected in series with each capacitor.

6.1 Parallel converters with common voltage nodes

Two conventional ladder circuits can be connected in parallel to feed a common load. As an example of this a pair of two-stage Ladder circuits is shown in this configuration in Figure 6-1.

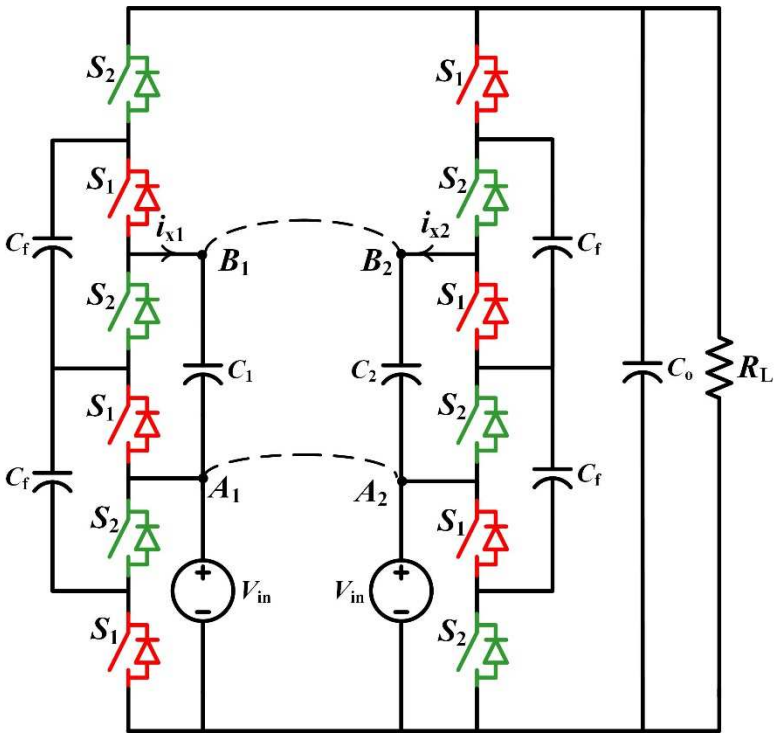


Figure 6-1. Parallel connection of two antiphase Ladder SC converters

The nodes of the right and left-hand capacitor strings of the two converters respectively are at approximately the same potential so that nodes A_1 can be connected to A_2 and B_1 to B_2. Furthermore if the two parallel connected Ladder circuits are operating in anti-phase, then one of the capacitors in the pair C_1 and C_2 shown in Figure 6-1, will be charging whilst the other is discharging. Therefore if the two converters circuits are identical then the currents i_{x1} and i_{x2} shown in Figure 6-1 will have the relationship,

$$i_{x1} = -i_{x2} \tag{6-1}$$

Hence the connection of the nodes $A_1 \rightarrow A_2$ and $B_1 \rightarrow B_2$ means that the current flowing into the capacitors C_1 and C_2 will be zero and they can be removed from the circuit. This results in the new topology shown in Figure 6-2, which has been termed a 2-Leg Ladder circuit.

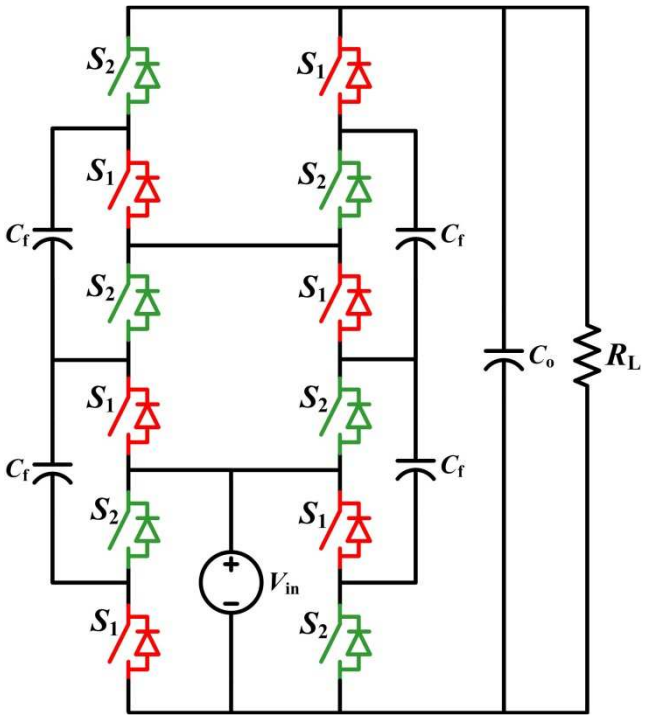


Figure 6-2. New Two-Leg Ladder circuit

For a given voltage step-up ratio and load, this new topology has the same total switch VA rating as a traditional Ladder circuit. The 2-Leg Ladder has one more capacitor compared to the Ladder, on the other hand this disadvantage becomes insignificant for large step-up ratios and the number of capacitors is approximately the same. However, importantly the current through each of these capacitors for the Two-Leg circuit is half of that for the Ladder topology since its output current was divided equally between original the parallel converters. Therefore the capacitor ESR conduction losses for the 2-Leg Ladder converter are four times lower that the Ladder circuit, which is a significant advantage. Alternatively, for the same converter efficiency the 2-Leg Ladder converter has a quarter of the capacitance of the Ladder circuit. For a size/weight critical application such as an off-shore, wind-farm collector platform again this is a considerable benefit.

Another advantage of this topology compared with the Ladder circuit is that the due to the anti-phase operation of the two legs, the output ripple current is reduced, which significantly reduces the size of the output filter capacitor C_o. This is discussed in more detail in Chapter 7.

To summarise this synthesis technique:

- Existing converter topologies are connected in parallel to feed a common load.
- Each converter is operated in anti-phase.
- Nodes having the same voltage are identified and connected together.

- Where this connection combines the same capacitors from the two legs, the net capacitor current must be zero and these capacitors can be removed.

6.2 Capacitor Stacking and Splitting

In many of the SC converter topologies low-voltage capacitors are connected in a series string in order to obtain a high voltage output. This can be seen in the Ladder, Dixon Charge-Pump and 2-Leg Ladder circuits. In the circuit diagrams for these topologies the capacitors appear to be vertically arranged on top of each other. Hence, this arrangement is here defined as capacitor Stacking and in general these converters have the following characteristics.

- Each capacitor has the same voltage rating, which is of the order of the low-voltage input to the converter. For example the capacitor voltage rating for the Ladder is V_{in}.
- Each switch has the same voltage rating, which is of the order of the low-voltage input to the converter. For example the switch voltage rating for the Ladder is V_{in} and for the Dixon Charge Pump it is a mixture of V_{in} and $2V_{in}$.
- For a step-up converter the current rating of the capacitors increases as the vertical capacitor string is descended from the output at the top to the input at the bottom.
- The average current through the bottom switches, which are connected in parallel with the low voltage terminal, are equal to the high input-current of the low voltage terminal in the Ladder and Dixon circuit and half of the high input-current of the low voltage terminal in the 2-Leg Ladder circuit.

Alternatively the capacitors in these converters can be connected directly to the input supply via their own individual switch pair. This is shown for the 2-Leg Ladder circuit in Figure 6-3, which can be compared against the original circuit shown in Figure 6-2.

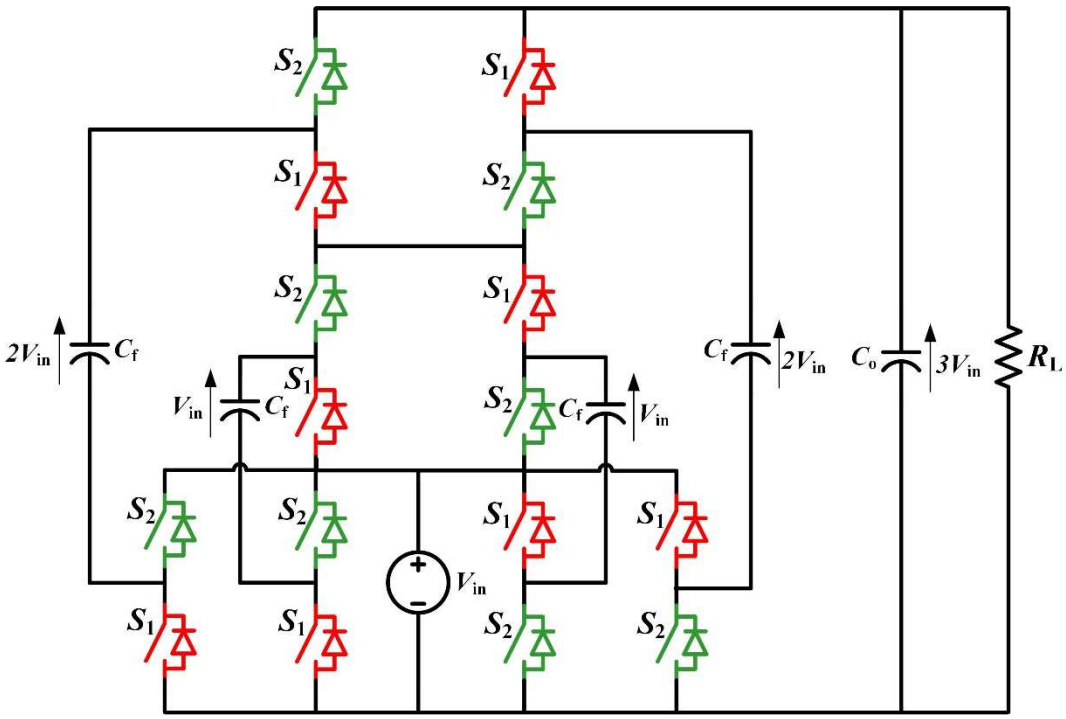


Figure 6-3. Circuit resulting from Splitting the 2-Leg Ladder topology

This synthesis technique is known here defined as capacitor Splitting and these types of converters have characteristics that in some cases are complementary to the Stacked circuits:

- For a step-up converter the voltage rating of the capacitors decreases as the vertical string of switches is descended from the output at the top to the input at the bottom.
- Each switch has the same voltage rating, which is of the order of the low-voltage input to the converter. For example the switch voltage rating for the Ladder is V_{in} and for the Dixon Charge Pump it is a mixture of V_{in} and $2V_{in}$
- Each capacitor has the same current rating, which is equal to the low-current output of the converter.
- Each switch has the same current rating, which is equal to the low-current output of the converter.

The new circuit has identical total component VA rating to the original Stacked version. However, this Split arrangement has a significant advantage in that it changes the circuit from Coupled to a Decoupled. This means the problematic effects of circuit parasitics, which were discussed in Chapter 4 for resonant SC converters are significantly reduced. For high-voltage, high-power applications where parasitics are much higher due to the distributed nature of the circuit layout, then Splitting maybe the only option to overcome parasitic effects.

Interestingly, this technique can be applied to the Dixon Charge Pump circuit from which the MMSCC emerges. The MMSCC is simply a split version of the Dixon Charge Pump.

6.3 Modularisation

Switched capacitor converters are characterised by having a large number of identical sub-topologies. The circuits therefore offer the opportunity to be constructed from the same base sub-module, which provides a significant benefit in terms of manufacturing, spares and the ability to bypass faulty modules during converter operation.

The MMSCC and SMMSCC converters presented in the literature [72] and shown in Figure 2-41 and Figure 2-44 are claimed to be modular by the authors, for example the MMSCC module is shown in Figure 6-4,

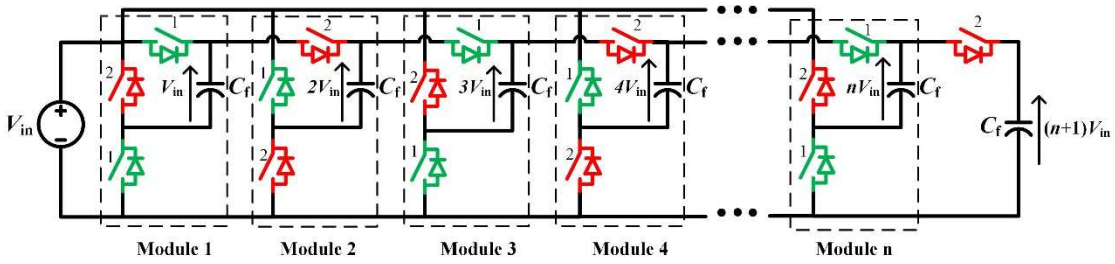


Figure 6-4. The modular MMSCC converter presented in [72]

However, due to its Split arrangement the capacitor voltages within each module increase toward the high-voltage output of the converter as shown in Figure 6-4. Therefore each module should not include the capacitor as part of its structure, as they will be different for each module. To be truly modular, the capacitor would need to be separated from the switches and their associated interconnections and re-connected to the module through a set of terminals as shown in Figure 6-5.

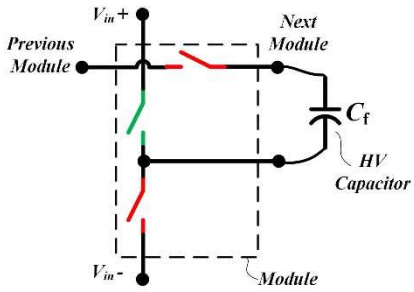


Figure 6-5. Module structure in MMSCC converter with high voltage capacitor transferred to the outside of module

Even in this case the converter is not truly modular as the voltage clearance for the capacitor terminals shown in Figure 6-5 would be different for each module. This is especially true for high-voltage applications where the terminals would include specialist insulator components. For much lower voltage applications, where voltage clearance is not an issue, then the claim of modularity would be more justified.

The Split 2-Leg Ladder converter topology of Figure 6-2 can be re-drawn to show how a genuine modular converter can be realised and this is shown in Figure 6-6.

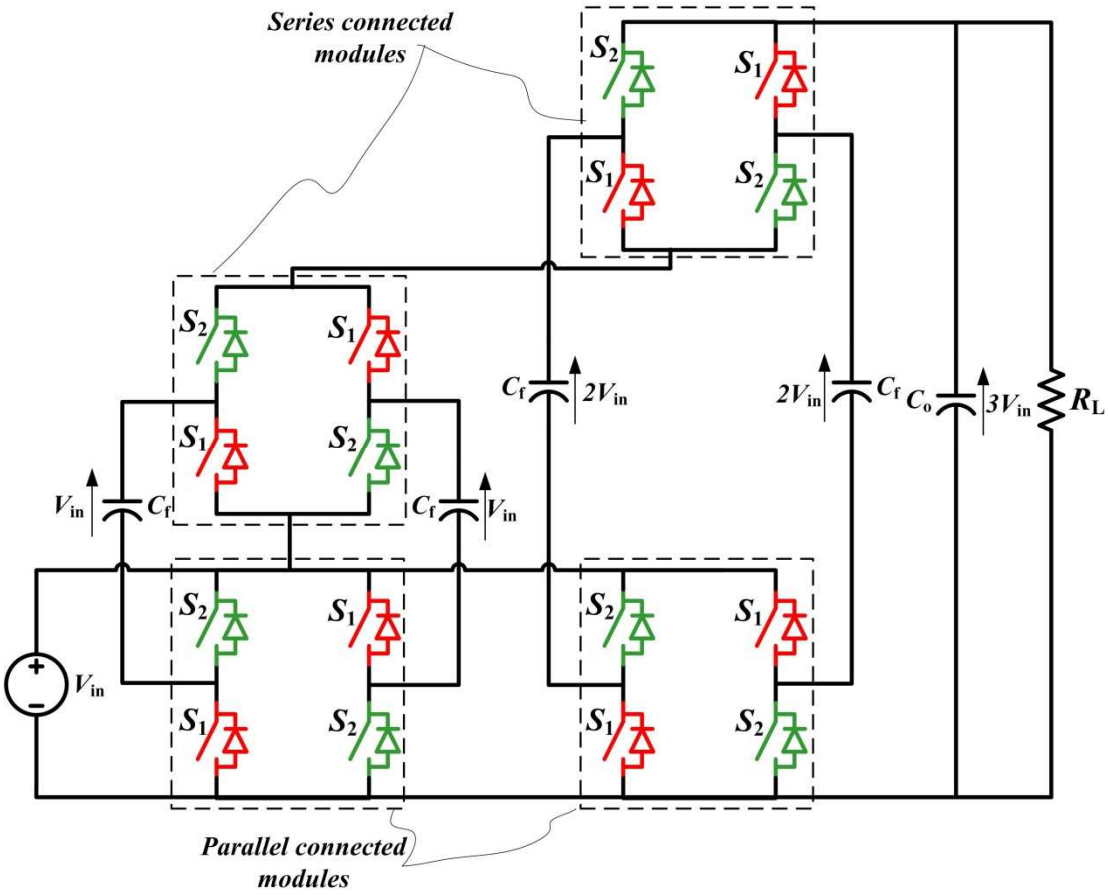


Figure 6-6. Modular reconfiguration of the proposed circuit for high-voltage applications – Series modules are connected to parallel modules via external high voltage capacitors which take the voltage stress

In this arrangement, which is termed here a Modular 2-Leg Switched Capacitor Converter (M2LSCC), each stage of the converter is composed of two H-Bridge modules which are connected together via high voltage capacitors. All H-Bridge modules have identical voltage and current ratings and the capacitors are connected externally to these modules.

6.4 The Bi-pole Arrangement

This technique was presented in Chapter 3 to explain the synthesis of the SMMSCC from the MMSCC. The same technique can also be applied to the M2LSCC converter as follows – the M2LSCC converter can operate with the sign of the input source inverted. This is shown in Figure 6-7, where the circuit is shown flipped over from top to bottom.

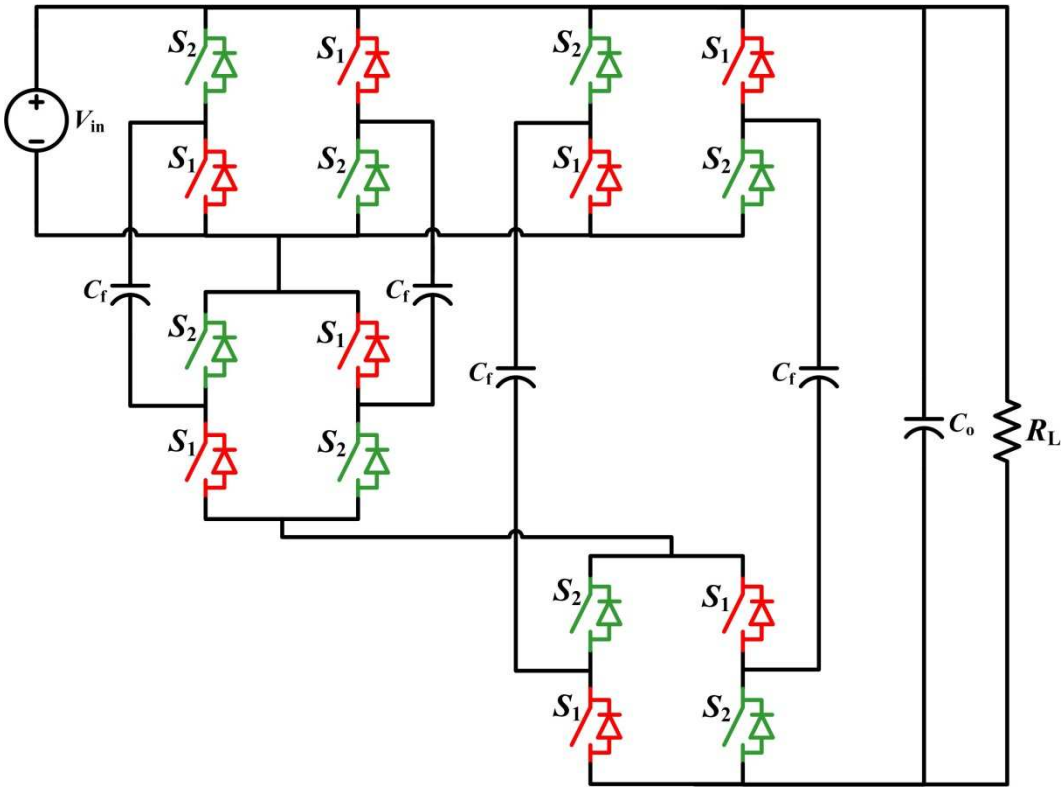


Figure 6-7. Complementary circuit arrangement for M2LSCC converter

A Bi-pole arrangement can be achieved by feeding the inverted and non-inverted topologies from a single input DC source as shown in Figure 6-8. Unlike the SMMSCC converter a common ground exists between midpoints of the input and the output terminals, which makes it suitable for DC networks. However, it should be noted that the technique of switch splitting can also be applied to the SMMSCC converter to make it decoupled and to provide a common ground.

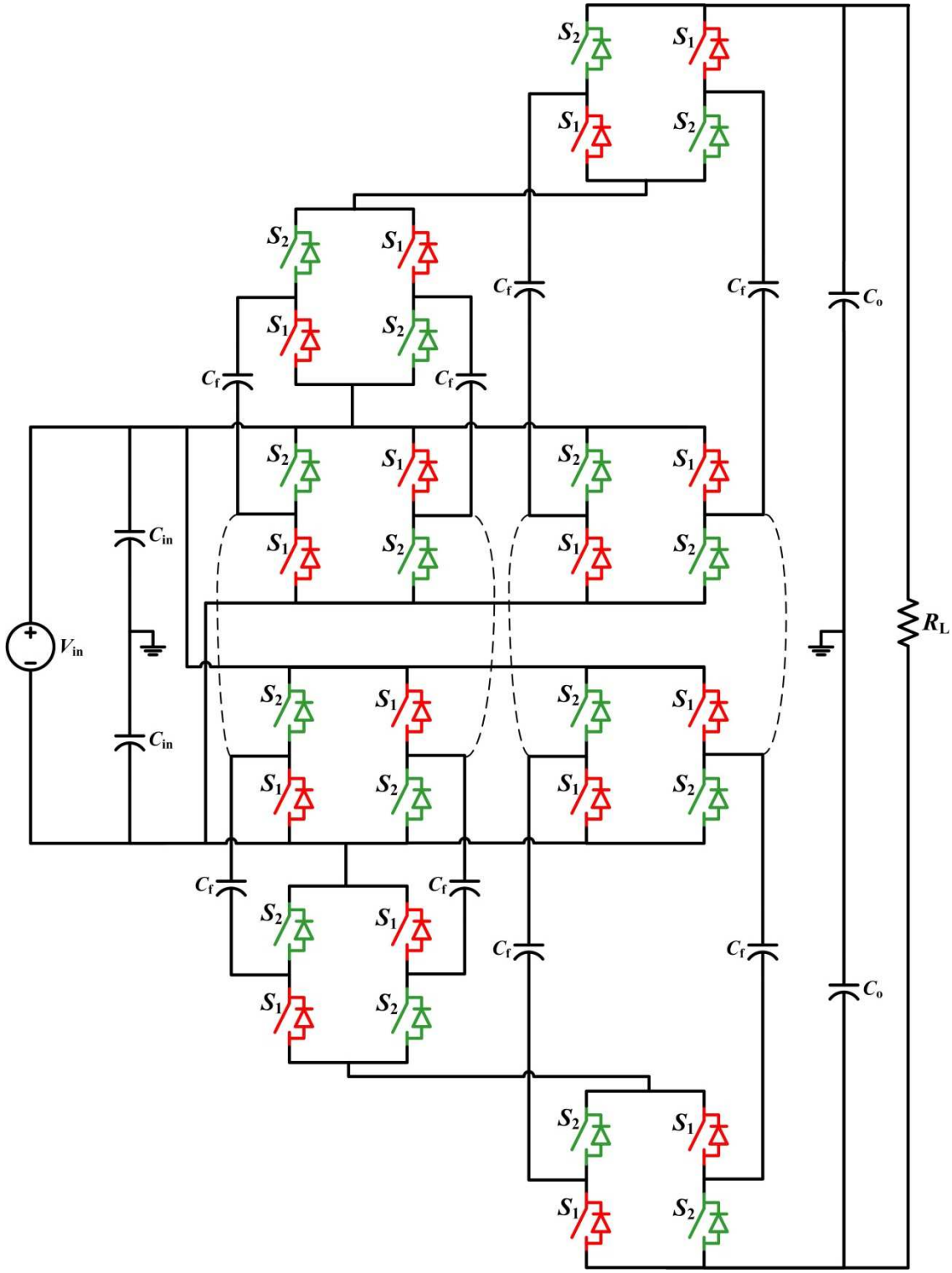


Figure 6-8. Bi-pole arrangement of the proposed Split Two-Leg Ladder converter

This new topology shown in Figure 6-8 has been termed a Symmetric, Modular, 2-Leg Switched Capacitor Converter (SM2LSCC). The Bi-pole arrangement reduces the number of capacitors by a factor of 16 when compared with the original Ladder circuit.

Nodes having the same potential in the inverted and non-inverted parts of the circuit can be connected permanently together as shown by the dashed lines in Figure 6-8. A number of switches then become redundant and the circuit reduces to that shown in Figure 6-9. However this reduction makes the converter into a Coupled circuit without offering any advantages in terms of switch VA reduction. Whereas this combination may be useful in low voltage/power applications in order to reduce the number of switches, the Decoupled variant is more suitable for high-voltage, high-power applications.

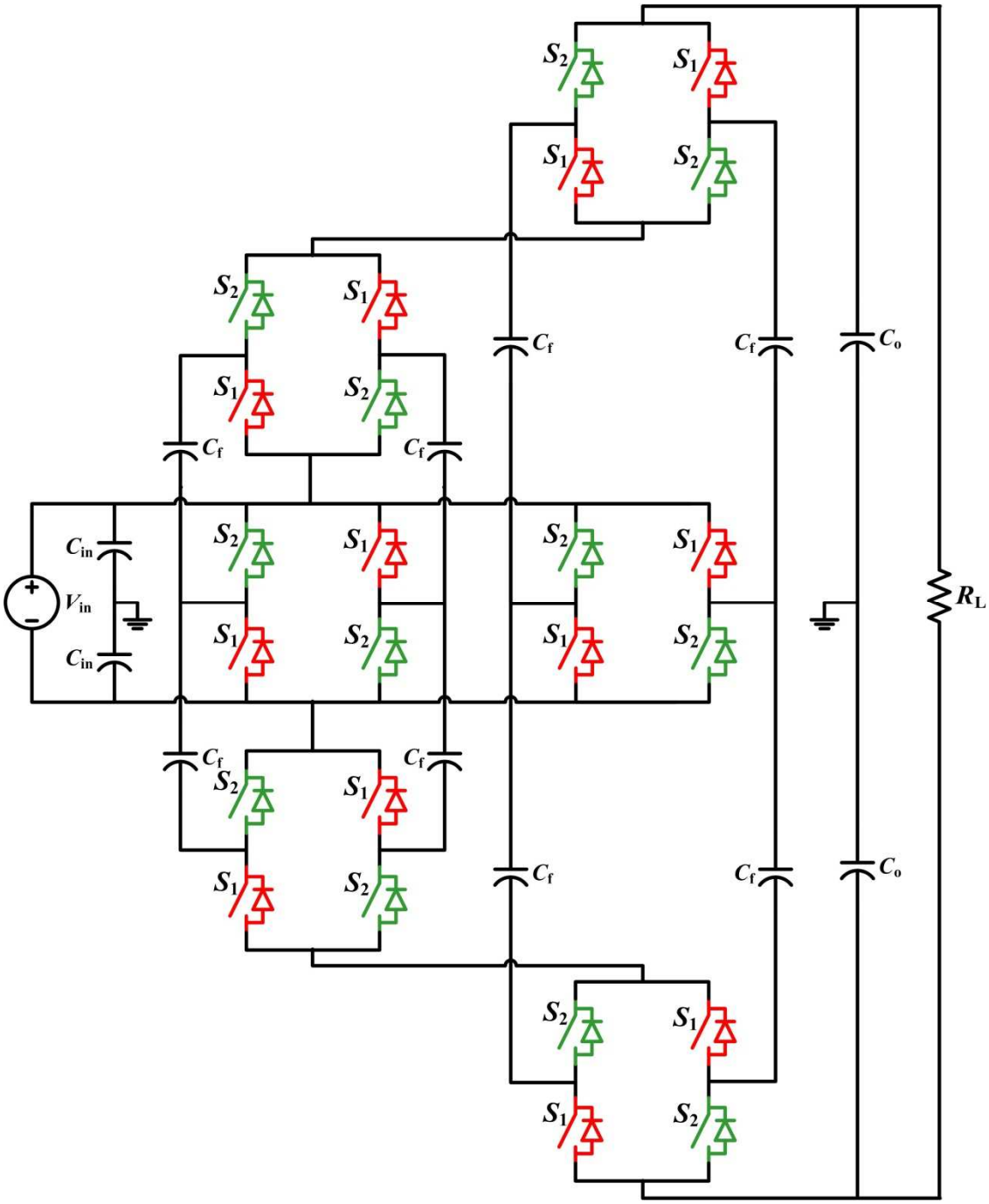


Figure 6-9. Simplified Bi-pole arrangement of the new modular SC converter showing switch reduction but introducing Coupling

6.5 Comparison of the Proposed SC Converters with Existing Topologies in Resonant Mode

This section compares the candidate topologies in terms of capacitor and switch requirements, normalised output equivalent resistance, modularity, and whether they are Coupled or Decoupled for the resonant implementation of the converters. Step-up operation is assumed and the input voltage is considered as 1 p.u. along with the output current. Switches and capacitors are assumed to be assembled from base components having 1 p.u. voltage and current ratings so that components are connected in series to obtain higher voltage ratings and in parallel to achieve higher current ratings. Switches having a voltage rating of more than 2 p.u. are not considered as this implies a series connection of transistors, which is not practical.

The on-state resistance of switches is denoted by R_{sw} and the ESR of capacitors is denoted by R_c in these comparisons, both being equal to 1 p.u.

Table 6-1 shows the comparison of the different candidate topologies including an estimate of converter efficiency calculated using equation (3-30), for waveform b(1) shown in Figure 3-12, assuming $Q_{i,k} \gg 1$ and assuming dead time is negligible. In this case equation (3-30) becomes,

$$\lim_{Q_{i,k}\to\infty} R^*_{eq,i,k} = \frac{\pi^2}{4} \approx 2.5 \tag{6-2}$$

Table 6-1. Comparison of the candidate topologies in terms of component requirement and output equivalent resistance for resonant mode

	Require 2 p.u. voltage Switches?	Decoupled Circuit?	Number of 1 p.u. capacitor	Number of 1 p.u. switches	Output Equivalent resistance	Output Equivalent resistance, $n \gg 1$
Ladder	No✓	No ×	$(n-1)^2$	4(n-1)	$\approx 2.5((n-1)^2 R_c + (4n-4)R_{sw})$	$\approx 2.5(n^2 R_c + 4nR_{sw})$
2-Leg Ladder	No✓	No×	$\frac{1}{2}n(n-1)$	4(n-1)	$\approx 2.5\left(\frac{1}{2}n(n-1)R_c + (4n-4)R_{sw}\right)$	$\approx 2.5\left(\frac{1}{2}n^2 R_c + 4nR_{sw}\right)$
Dixon	Yes×	No×	$\frac{1}{2}n(n-1)$	4n-3	$\approx 2.5\left(\frac{1}{2}n(n-1)R_c + (4n-3)R_{sw}\right)$	$\approx 2.5\left(\frac{1}{2}n^2 R_c + 4nR_{sw}\right)$
MMSCC	Yes×	Yes✓	$\frac{1}{2}n(n-1)$	4n-3	$\approx 2.5\left(\frac{1}{2}n(n-1)R_c + (4n-3)R_{sw}\right)$	$\approx 2.5\left(\frac{1}{2}n^2 R_c + 4nR_{sw}\right)$
M2LSCC	No✓	Yes✓	$\frac{1}{2}n(n-1)$	4(n-1)	$\approx 2.5\left(\frac{1}{2}n(n-1)R_c + (4n-4)R_{sw}\right)$	$\approx 2.5\left(\frac{1}{2}n^2 R_c + 4nR_{sw}\right)$
SMMSCC	Yes×	No×	$\frac{n^2}{4}$	2(2n-1)	$\approx 2.5\left(\frac{n^2}{4}R_c + (4n-2)R_{sw}\right)$	$\approx 2.5\left(\frac{n^2}{4}R_c + 4nR_{sw}\right)$
SM2LSCC	No✓	Yes✓	$\frac{n^2}{4}$	4(n-1)	$\approx 2.5\left(\frac{n^2}{4}R_c + (4n-4)R_{sw}\right)$	$\approx 2.5\left(\frac{n^2}{4}R_c + 4nR_{sw}\right)$

For high step-up voltage ratios $n \gg 1$, it can be seen that the number of 1 p.u. switches is the same for all the converters and is given by $4n$. The table then becomes simplified as shown in Table 6-2.

Table 6-2. Comparison of the candidate topologies assuming high voltage step-up ratios, $n \gg 1$

	Require 2 p.u. voltage Switches?	Decoupled Circuit?	Number of 1 p.u. capacitor	Output Equivalent resistance, $n \gg 1$
Ladder	No✓	No ×	n^2	$\approx 2.5(n^2 R_c + 4nR_{sw})$
2-Leg Ladder	No✓	No×	$\frac{1}{2}n^2$	$\approx 2.5\left(\frac{1}{2}n^2 R_c + 4nR_{sw}\right)$
Dixon	Yes×	No×	$\frac{1}{2}n^2$	$\approx 2.5\left(\frac{1}{2}n^2 R_c + 4nR_{sw}\right)$
MMSCC	Yes×	Yes✓	$\frac{1}{2}n^2$	$\approx 2.5\left(\frac{1}{2}n^2 R_c + 4nR_{sw}\right)$
M2LSCC	No✓	Yes✓	$\frac{1}{2}n^2$	$\approx 2.5\left(\frac{1}{2}n^2 R_c + 4nR_{sw}\right)$
SMMSCC	Yes×	No×	$\frac{1}{4}n^2$	$\approx 2.5\left(\frac{n^2}{4}R_c + 4nR_{sw}\right)$
SM2LSCC	No✓	Yes✓	$\frac{1}{4}n^2$	$\approx 2.5\left(\frac{n^2}{4}R_c + 4nR_{sw}\right)$

It can be seen from Table 6-2 that the Ladder circuit requires the highest number of 1 p.u. capacitors and has the highest normalised output equivalent resistance. The 2-Leg Ladder, Dixon Charge Pump MMSCC and M2LSCC, have half the number of capacitors of the Ladder circuit and consequently have only half the contribution to the normalised equivalent resistance. The SMMSCC and SM2LSCC have the lowest capacitor requirement and lowest contribution to output equivalent resistance.

In order for the converters to have the same output equivalent resistance, additional capacitors would need to be added in parallel to the existing components in order to reduce capacitor ESR. For example, each capacitor of the Ladder circuit would need to be replaced by four 1 p.u. parallel connected capacitors. Since the Ladder already has four times more capacitors than say the SM2LSCC circuits, then by replacing each capacitor with four parallel connected capacitors the capacitance requirement would be 16 times that of the SM2LSCC circuit to achieve the same efficiency. Similarly the 2-Leg Ladder, Dixon Charge Pump, MMSCC and M2LSCC converters would require almost four times more capacitance than the SM2LSCC to achieve the same efficiency.

Overall the SM2LSCC would be the most suitable topology for high voltage step-up ratio, high-power applications as it has the lowest capacitor requirement, uses 1 p.u. voltage rating switches, is decoupled and is modular.

6.5.1 Comparison and validation of analysis using detailed simulations

A Micro-Cap Spice simulation was carried out in order to validate the analysis and compare the proposed topologies against existing circuits. Resonant versions of the topologies with a conversion ratio of 11 were considered during the simulation studies. Parameters used in the simulations are listed in Table 6-3.

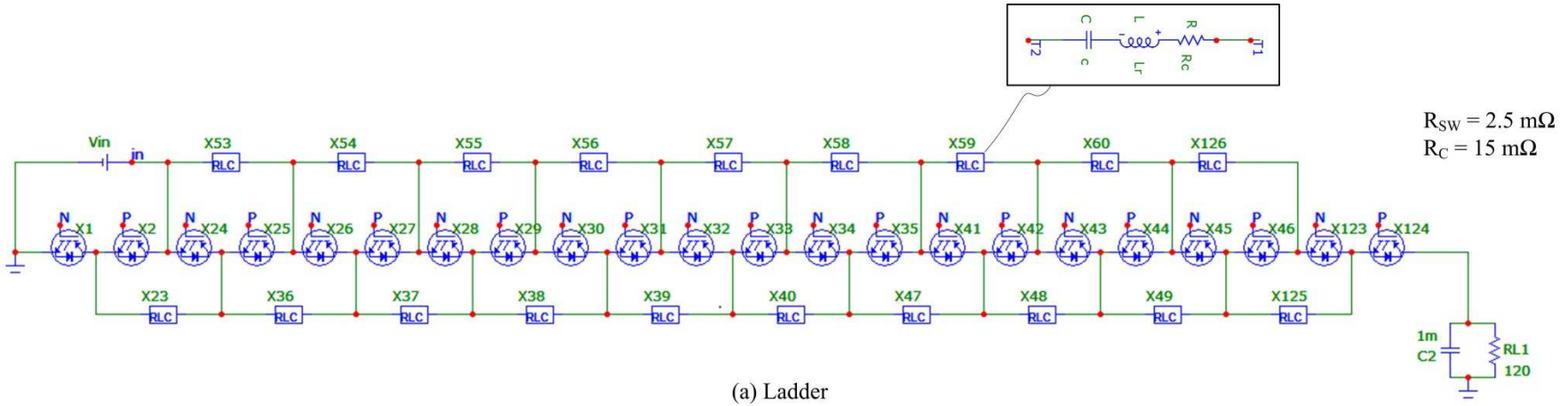
Table 6-3. Parameters used in simulation

Conversion ratio	$R_{ds,on}$ of switches	ESR of capacitors	Input voltage	C_i	L_r	Switching frequency	Dead-time
11	5 mΩ	15 mΩ	1 kV	200 µF	1 µH	10.8 kHz	1 µs

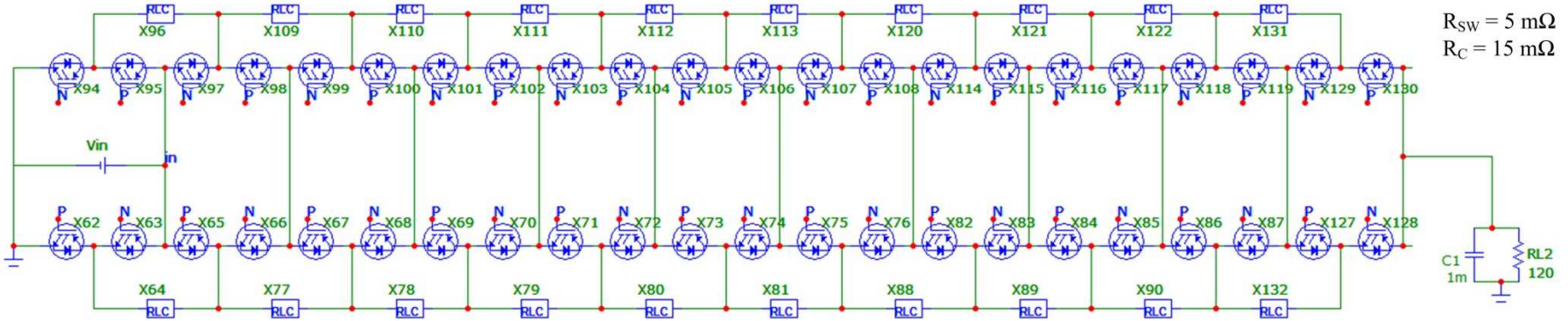
Since the switching losses of the converter are negligible for resonant case, switches having zero turn on/ off times were considered in the simulations for the sake of simplicity. The on-state resistance of the switches was $R_{SW} = 5\ m\Omega$, which is a typical value for new Silicon Carbide (SiC) MOSFET modules [85], and the ESR for the capacitors was $R_C = 15\ m\Omega$ [86]. The switching frequency was set to the resonant frequency of the LC circuit with values given in Table 6-3.

6.5.1.1 Comparison of Ladder and new 2-Leg Ladder circuit

The simulation schematic for the 2-Leg Ladder and Ladder topologies is shown in Figure 6-10. In order to make a meaningful comparison of the two converters the simulation parameters were modified for the Ladder circuit so that both circuits effectively utilised the same number of identical switches, capacitors and inductors. In this way the converters would in practice have the same component cost, mass and volume, so a comparison can then be made in terms of converter efficiency. In order to do this, the on-state resistance of the Ladder circuit used in the simulation was half that used for 2-Leg Ladder, since the Ladder circuit requires half the number of switches but each switch has a current rating that is twice that of the 2-Leg Ladder circuit. It should also be noted that for a conversion ratio of 11 the Ladder circuit requires 21 resonant capacitors, while the 2-Leg Ladder requires 22 resonant capacitors. Whilst the number of capacitors is therefore not identical, the error in this approximation is small and can be neglected.



(a) Ladder



(b) 2L-Ladder

Figure 6-10. Micro-Cap simulation schematic for Ladder and 2-Leg Ladder topologies

Based on the analysis and using the parameters given in Table 6-3, the output equivalent resistance calculated for the Ladder circuit using equation (3-30) is 41.31 Ω compared to 12.66 Ω for the 2-Leg Ladder circuit. A 1 μs dead-time was considered in simulation which is also applied in the analysis results as a constant factor based on equation (3-30).

A comparison of the corresponding output voltage and converter efficiency with a 120 Ω resistive load, which corresponds to a nominal power of 1 MW for an ideal converter, using both the analytic equation and steady-state results from the Micro-Cap simulations are summarised in Table 6-4. Note that the efficiency η of any DC-voltage-behind-resistance equivalent circuit, such as used to represent a SC converters can be calculated from the ratio of the output DC voltage on load to the open-circuit voltage,

$$\eta = \frac{V_o}{nV_{in}} \tag{6-3}$$

Table 6-4. Comparison of Ladder and 2-Leg Ladder circuits in terms of efficiency and output voltage based on the parameters given in Table 6-3 and a 120 Ω resistive load.

	Analysis		Simulation	
	Ladder	**2-Leg Ladder**	**Ladder**	**2-Leg Ladder**
Output voltage	7.62 kV	9.68 kV	7.5 kV	9.69 kV
Efficiency	69.27%	88.02%	68.18%	88.09%

From Table 6-4, it can be seen that there is very good agreement between the analysis and simulated results with a worst-case error of approximately 1% in the calculation of efficiency. This small error can be explained by the fact that both the Ladder and 2-Leg ladder circuits are coupled, whereas the analysis assumes uncoupled circuits.

The proposed 2-Leg Ladder topology has approximately 20% higher efficiency when compared to the Ladder circuit with both converters having the same number and type of switches, capacitors and resonant inductors.

The simulation output voltage start-up transient waveforms for the Ladder and 2-Leg Ladder circuits are shown in Figure 6-11. As it can be seen from Figure 6-11, the transient simulation is run to steady state with steady state output average voltage values of 9.69 kV for 2-Leg Ladder and 7.5 kV for Ladder circuit.

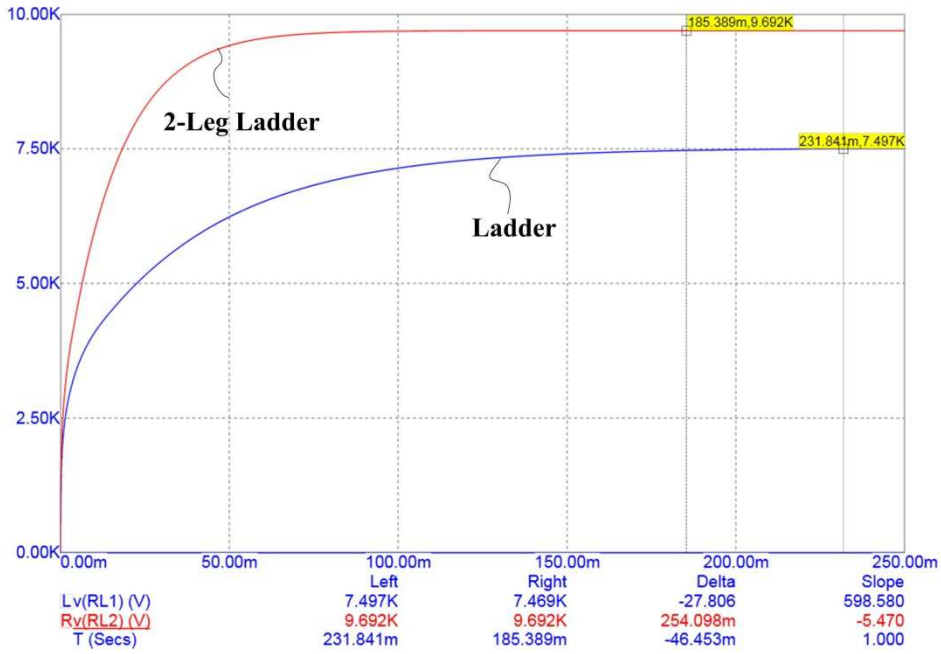


Figure 6-11. Output voltage waveforms (kV) against time (ms) for the Ladder and 2-Leg Ladder circuits, input voltage = 1kV, conversion ratio = 11

The current through each capacitor in the Ladder is twice that of the 2-Leg Ladder circuit. Since the number of capacitors is almost the same for both topologies, for example 21 and 22 for the Ladder and 2-Leg Ladder respectively, then the efficiencies of the two converters can be equalised by reducing the individual capacitor ESR by a factor of four for the Ladder circuit. In practice this can be achieved by replacing each capacitor in the Ladder circuit with 4 parallel connected capacitors, and this was incorporated in the simulation by simply reducing R_C by factor of four. The analysis and steady-state simulation results for this case are summarised in Table 6-5. The switching frequency in this case is increased to 11.2 kHz since the damped resonant frequency of the Ladder is slightly increased due to the decrease in resistance of the charge transfer path.

Table 6-5. Comparison of Ladder and 2-Leg Ladder circuits in terms of efficiency and output voltage based on the parameters given in Table 6-3 and a 120 Ω resistive load when the number of capacitors is increased in Ladder circuit by the factor of 4

	Analysis		Simulation	
	Ladder	**2-Leg Ladder**	**Ladder**	**2-Leg Ladder**
Output voltage	9.84 kV	9.71 kV	9.85 kV	9.72 kV
Efficiency	89.53%	88.28%	89.55%	88.36%

As it can be seen from Table 6-5 the efficiency of Ladder and the proposed 2-Leg Ladder circuits are almost same when resistance of capacitors are decreased by a quarter for the Ladder circuit.

However, this has been achieved at the expense of increasing the volume and mass of the electrical capacitance for the Ladder circuit by a factor of 4. Since the capacitors are the dominant component in terms of size in an SC cell, the whole converter will be much larger and heavier than the 2-Leg converter, which is a critical factor in terms of off-shore platform applications.

6.5.1.2 Comparison of MMSCC and the new M2LSCC topology

In this section the modular version of the new 2-Leg Ladder circuit converter (M2LSCC) is compared against the equivalent existing MMSCC topology. The Micro-Cap simulation schematic is shown in Figure 6-12. As in the previous section, in order to make a direct comparison between the two converters, the MMSCC consists of two identical parallel converters so that the overall cost, size and weight of the M2LSCC and MMSCC converters were the same.

The analysis and steady-state simulation results for converter output voltage and efficiency for the MMSCC and M2LSCC converters is given in Table 6-6 for conversion ratio 11, the circuit parameters given in Table 6-3 and a resistive load of 120 Ω.

Table 6-6. Comparison of MMSCC and DW-MMSCC circuits for conversion ratio 11,the circuit parameters given in Table 6-3 and a 120 Ω resistive load

	Analysis		Simulation	
	MMSCC	**M2LSCC**	**MMSCC**	**M2LSCC**
Output voltage	10.94 kV	10.94 kV	10.95 kV	10.95 kV
Efficiency	99.45%	99.45%	99.55%	99.55%

Again there is good agreement between the analytic and simulated results with an error in efficiency of approximately 0.1%. This error is much smaller than that for the comparison of the Ladder and 2-Leg Ladder comparison, which can be explained by the fact that the circuits investigated in this section are de-coupled. As expected from Table 6-1, the output voltage and efficiency are identical for both the MMSCC and M2LSCC converters for the same cost, size and weight of converter. However, the minimum voltage rating of the switches for the new M2LSCC circuit is half that of the existing MMSCC topology, which makes it more suitable for HV applications.

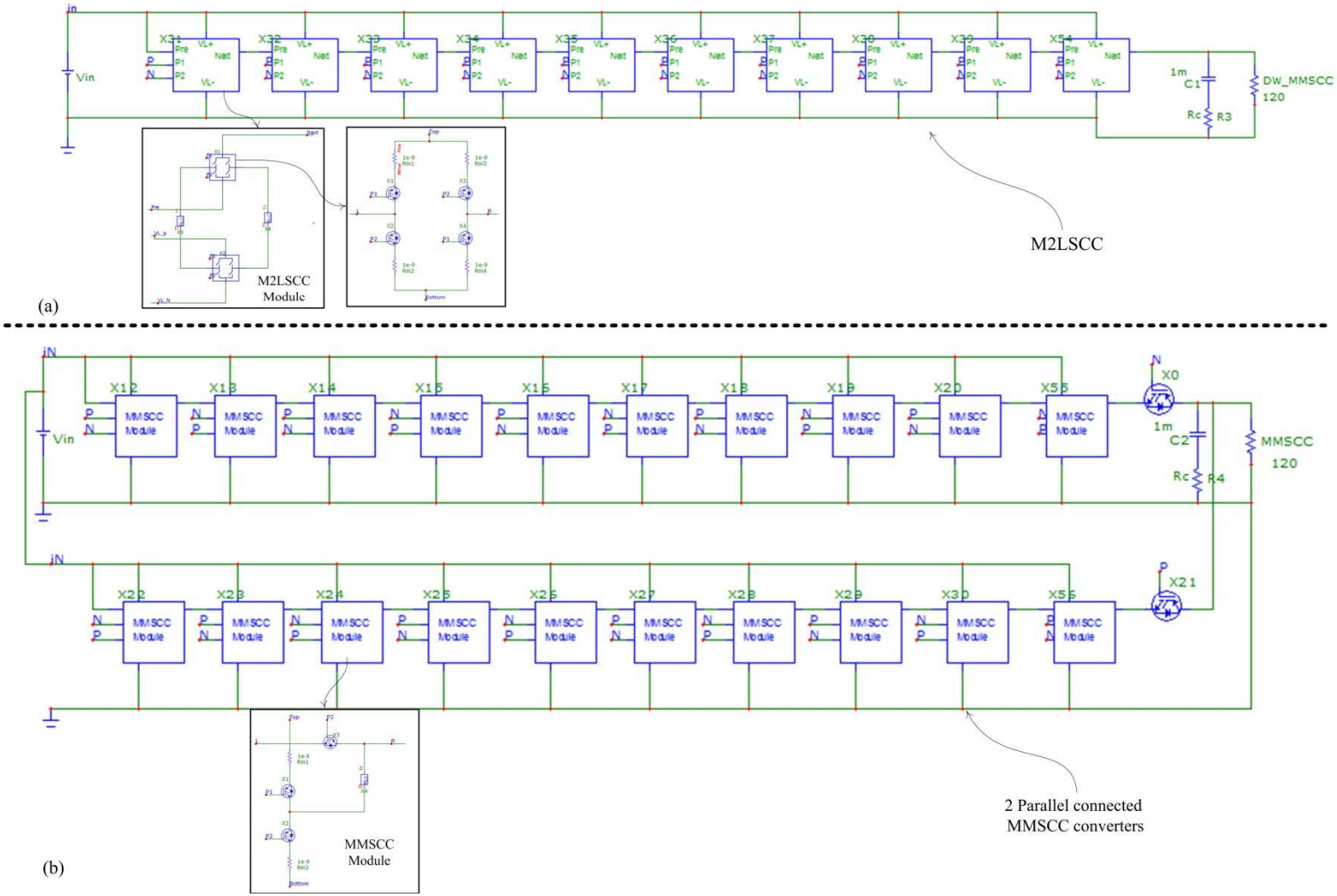


Figure 6-12. Simulation schematic in Micro-Cap for (a) M2LSCC and (b) two parallel connected MMSCC converters

6.5.1.3 Comparison of SMMSCC and the new SM2LSCC topologies

It is difficult to make a direct comparison of the existing Symmetric, Multi-Module SC circuit (SMMSCC), and the new Symmetric, Multi-Module, 2-Leg Ladder SC converter (SM2LSCC), which are both based on the Bi-pole arrangement described in section 6.4. This is because the SMMSCC only provides even voltage conversion ratios, whereas the SM2LSCC topology provides only odd conversion ratios. In addition the SMMSCC is a coupled topology. Therefore to allow some form of comparison between the two topologies, the decoupled variant of the SMSMCC converter was used and was further modified by adding an additional conversion stage in the form of two additional switches connected to the high voltage side of the converter as shown in Figure 6-13. The latter modification then allows the SMMSCC to have an odd conversion ratio. It is interesting to note that this additional stage also provides common ground between the input and the output sides, which is missing from the traditional topology and is therefore a significant improvement to the circuit. However, this circuit is not discussed in more detail in this thesis and has been left for future work.

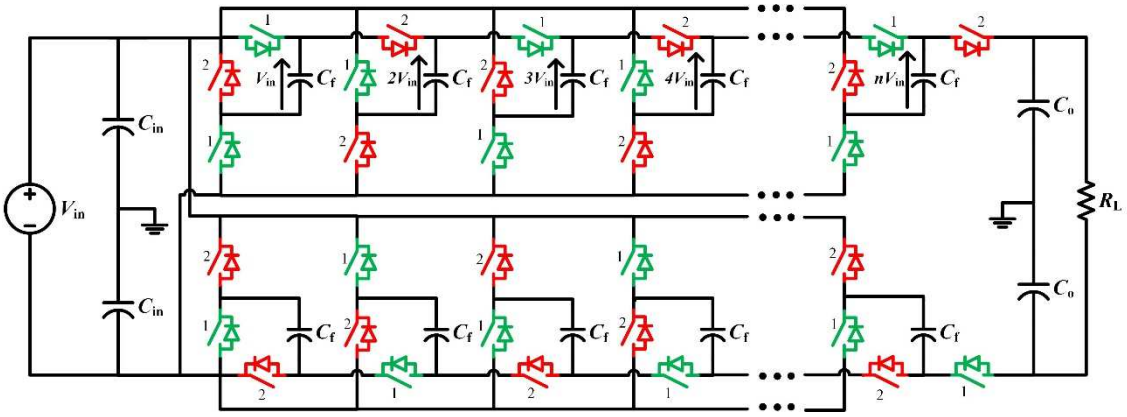


Figure 6-13. Decoupled SMMSCC converter with additional conversion stage to give an odd number conversion ratio

The Micro-Cap simulation schematic for the comparison of the two converters is shown in *Figure 6-14*.

The steady-state simulation results for converter output voltage and efficiency for the SMMSCC and SMM2LSCC converters is given in Table 6-7 for a conversion ratio of 11, the circuit parameters given in Table 6-3 and a resistive load of 120 Ω.

Table 6-7. Comparison of modified, Decoupled SMMSCC and SM2LSCC circuits for conversion ratio 11, the circuit parameters given in Table 6-3 and a 120 Ω resistive load

	Bi-pole SMMSCC	SM2LSCC
Output voltage	10.95 kV	10.95 kV
Efficiency	99.55%	99.55%

As expected from Table 6-1, the output voltage and efficiency are identical for both the SMMSCC and SM2LSCC converters for the same cost, size and weight of converter. However, the minimum voltage rating of the switches for the new SM2LSCC circuit is half that of the existing SMMSCC topology, which makes it more suitable for HV applications.

Comparing the results for the non-symmetrical and symmetrical converters from Table 6-6 and Table 6-7, it can be seen that the efficiency is approximately the same for converter types. However the symmetrical arrangements were implemented with four times less capacitance, which is a significant saving in terms of converter size and cost.

6.6 Summary

In this chapter four formal synthesis techniques have been proposed for SC converters, namely using parallel converters and eliminating common voltage nodes and redundant capacitors, stacking and splitting capacitors, modularisation and bi-pole arrangements.

These techniques were used to develop new 2-Leg SC topologies. A comparison between the proposed and existing topologies was carried out in terms of efficiency and the cost/volume/weight of the converter for resonant operation mode based on the analysis introduced in Chapter 3. These comparisons were then validated using detailed, switched simulations using Micro-Cap Spice software. The new SM2LSCC converter was found to be the most suitable topology for HVDC applications, since the capacitance size is at least four times less compared to non-symmetrical topologies. In addition it uses switches having a voltage rating equal to the input voltage of the converter.

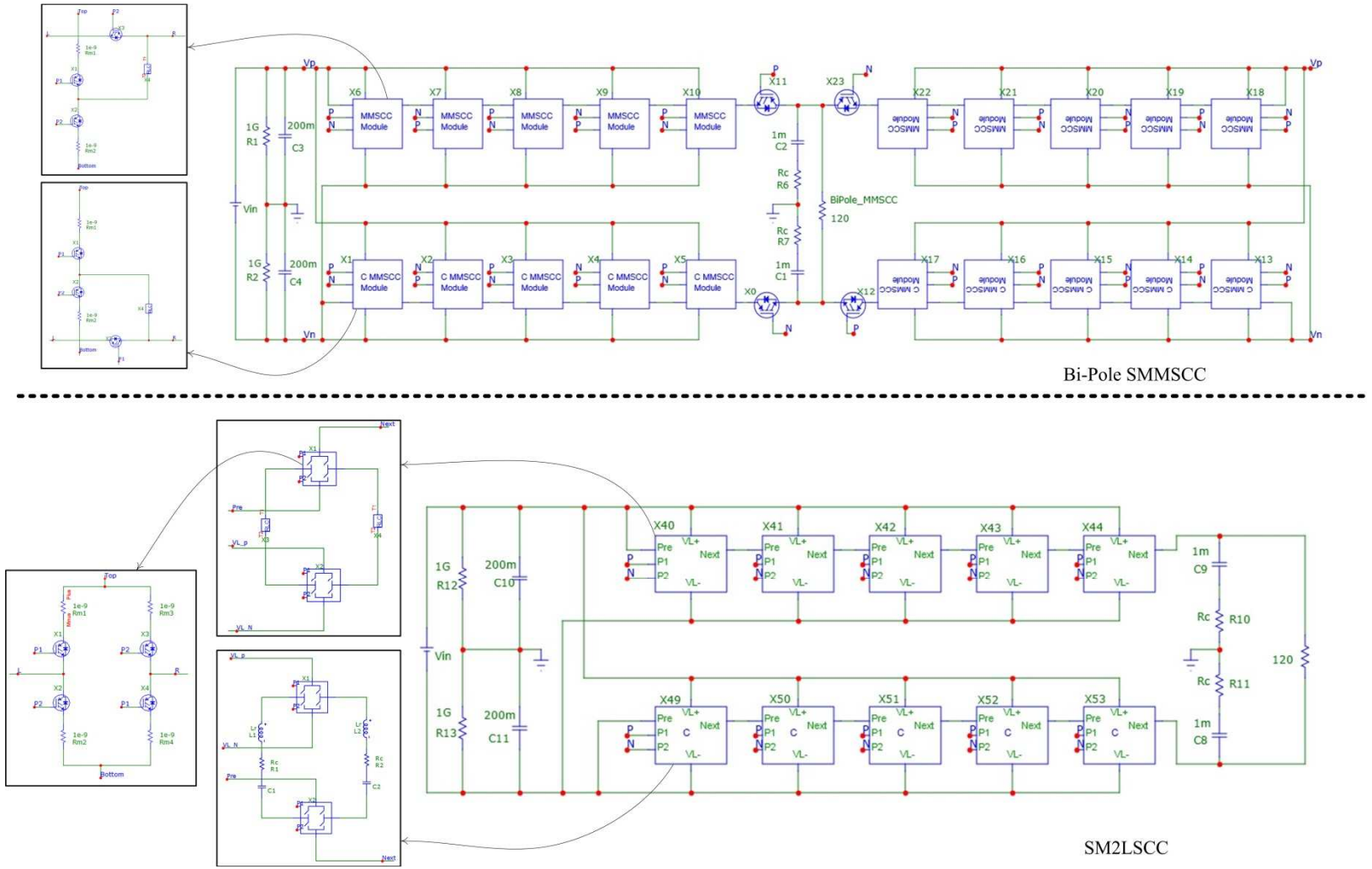


Figure 6-14. Simulation schematic in Micro-Cap for (a) modified, Decoupled SMMSCC circuit and (b) SM2LSCC topology

7. Experimental Setup and Validation

7.1 Power board design

In order to assess the operation of the 2-Leg Ladder circuit in either hard switch or resonant modes and to validate the analysis and simulation results, a 1200 W, 60 V/240 V laboratory prototype converter was designed and built as shown in Figure 7-1.

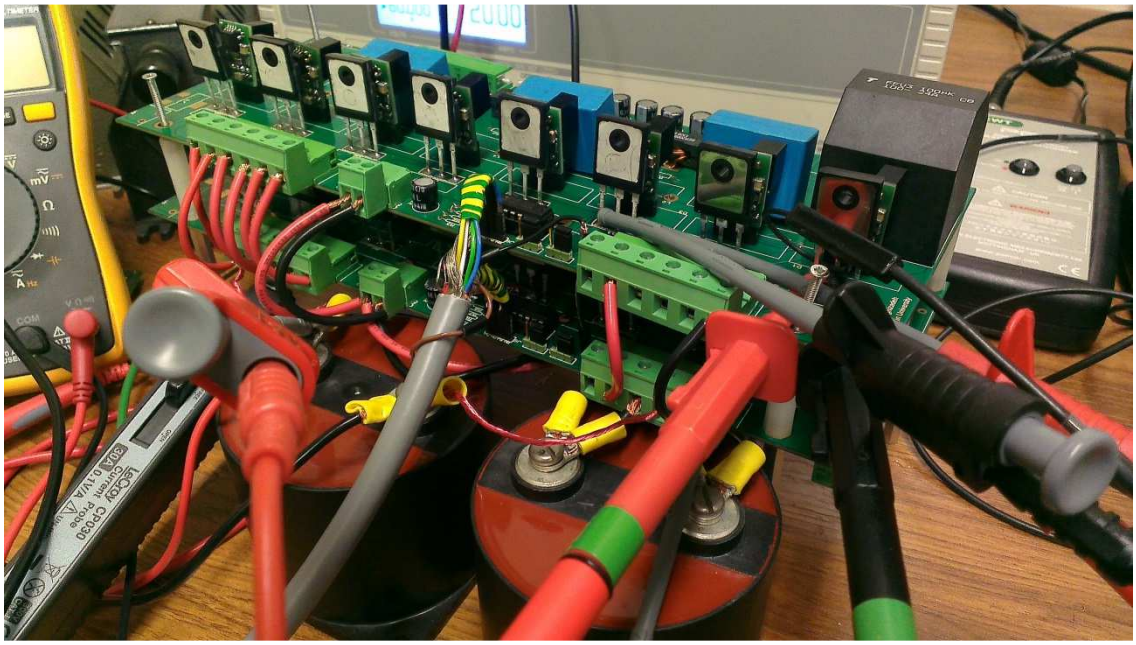


Figure 7-1. Experimental prototype 1200 W, 2-Leg Ladder topology

Each leg of the 2-Leg Ladder converter was implemented on a separate PCB board. Therefore two identical PCB boards were designed, each representing one leg of the converter and then connected together via external wires. The circuit diagram for each leg of the converter is shown in Figure 7-2. The two legs could be connected via terminal $T_1 - T_6$ to form the 2-Leg Ladder topology or each leg could be separately used as a conventional Ladder circuit by connecting two external capacitors or resonant tanks between terminals $T_2 - T_3$ and $T_3 - T_4$. This allowed both the proposed 2-Leg Ladder and the conventional Ladder circuits to be compared against each other using the experimental setup. The PCB layout for the top and bottom layers of each leg are shown in Appendix C. Special care was taken in order to ensure power tracks were traced as wide and short as possible to reduce the stray inductance and resistance.

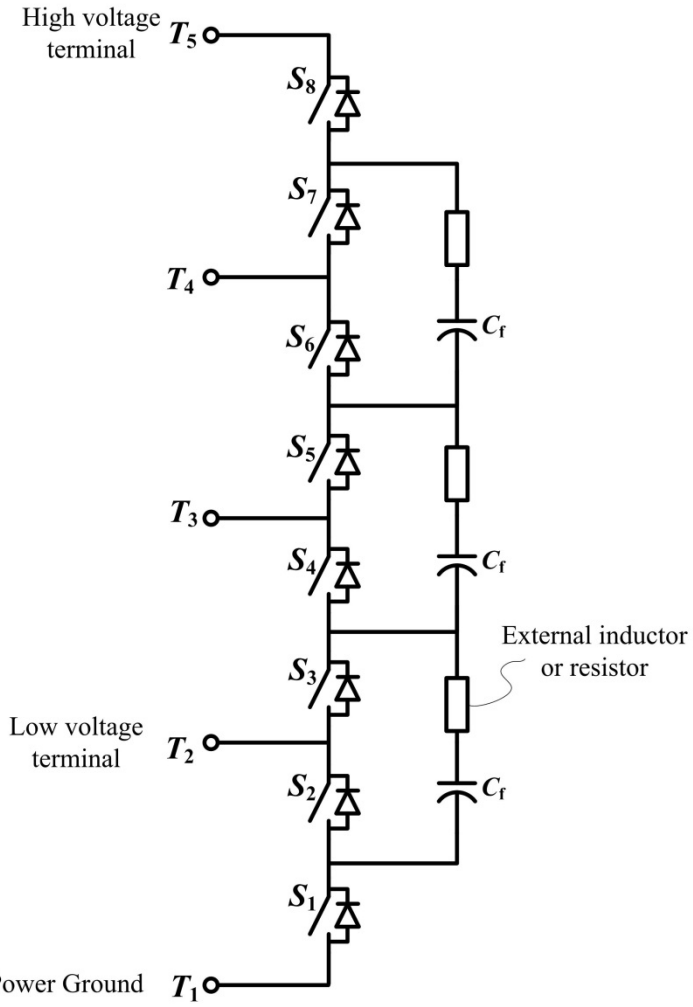


Figure 7-2. Circuit diagram for each leg of the 2-Leg Ladder circuit, implemented for the prototype converter.

The voltage rating of the switches are equal to the low voltage terminal of the converter - 60 V in this case - for both the Ladder and 2-Leg Ladder circuits, therefore the switches were implemented using 100 V MOSFETs (IRFP4468PbF from International Rectifier). These switches had very low $R_{ds,on}$ with a datasheet value of 2.5 $m\Omega$, which is needed to achieve a high quality factor for the resonant circuit.

7.2 MOSFET gate driver board

Each MOSFET gate driver was implemented as an individual PCB board, which were connected as close as possible to the MOSFETs via 5 pin headers as shown in Figure 7-3.

Figure 7-3. MOSFET gate driver board

The gate driver PCB design is shown Appendix E. An optically isolated gate-drive integrated circuit - ACPL-H342 from Avago Technologies, was used to drive the MOSFETs, which also provides a built-in active Miller clamp. Isolated, 2W, board mount, 5 V/15 V, DC/DC converter modules from XP POWER (IL0515S) were used to power the gate driver chip. A gate resistance of 10 Ω was used for MOSFET turn-on and 1 Ω for turn off, which gave switching times of 80 ns for turn on and 26 ns for turn off as shown respectively in Figure 7-4 and Figure 7-5.

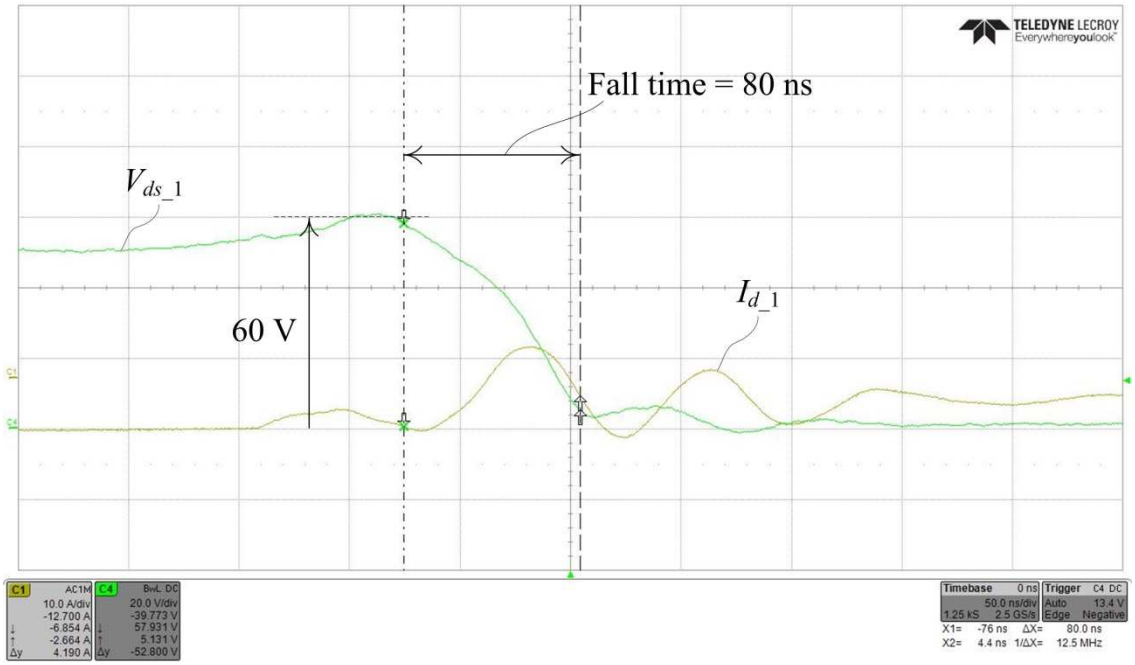


Figure 7-4. Switch S_1 turn-on transient

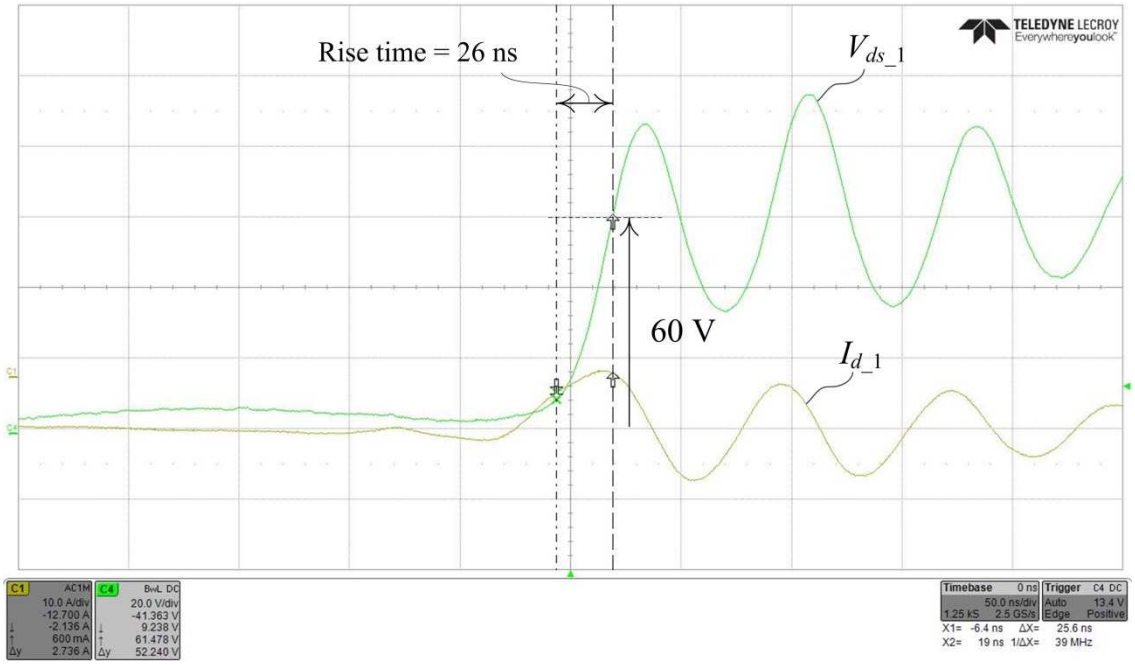


Figure 7-5. Switch S_1 turn-off transient

7.3 Generation of PWM signals using an FPGA

Two complementary signals with 50 % duty cycle and variable dead-time were generated using DE0 Development board from Terasic Technologies, which uses Altera Cyclone IV EP4CE22F17C6N FPGA. The dead-time period can have a significant effect on the efficiency of the converter in that it should be as short as possible to achieve high efficiency conversion, but not too short so that shoot-through can happen. A 1 µs maximum dead-time was found to be an appropriate duration for this design, based on the switching speed of the MOSFETs, which from the previous section were 80 ns for turn on and 26 ns for turn off.

Two push-button switches were available on the development board which were used to adjust the converter switching frequency from 500 Hz to 100 kHz. The clock cycle of the development board was 50 MHz. The schematic diagram designed to generate the gate signals in Quartus II software is shown in Appendix D along with the associated VHDL code.

Shielded cable was used to interface the FPGA development board with the power board in order to protect the control signals from induced noise.

7.4 Experimental comparison of 2-Leg Ladder and the conventional Ladder topologies

In this section the performance of the proposed 2-Leg Ladder topology is compared against the conventional Ladder circuit for both hard switched and resonant operation modes.

7.4.1 Hard switched converters

Whilst the converter FPGA design allowed the switching to be varied for experimental purposes, the nominal design was based on a switching frequency of 15 kHz, which is high enough to reduce the size of the circuit passive components whilst accommodating a 1 % dead-time period of 1 µs.

The converter was designed to operate close to the FSL region as this provided low conduction losses and avoided large peak currents. From Figure 3-11 this means that $\beta_{i,k} < 1$, so that from equation (3-20),

$$\tau_{loop,i,k} \approx \frac{0.5}{15 \times 10^3} = 33\ \mu s$$

Since the on-state resistance of the MOSFETs was 2.5 $m\Omega$, then the circuit loop resistance, which includes two series MOSFETs would be at least 5 $m\Omega$. With a loop time constant of $\tau_{loop,i,k} = 33\ \mu s$, the cell capacitor value would have to be 20 mF, which is impractically large even allowing for additional loop resistance from the capacitor ESR and wiring. Therefore it was decide to add additional 1 Ω resistors in series with each capacitor for the following reasons:

- The circuit time constant was dominated and controlled by the 1 Ω resistors rather than the capacitor and switch parasitic resistance. A 33 µs loop time constant then gave a more reasonable capacitor value of 100 µF and ensured the converter operated in the FSL region. The capacitors chosen for the experiment were 100 V film capacitors from AVX (FFV34E0107K) with datasheet ESR value of 0.55 mΩ.
- By making the capacitor series resistance much greater than the parasitics and switch resistances, the coupling, which is inherent in the Ladder and 2-Leg ladder became negligible.
- The overall losses of the converter would be dominated by the conduction losses in the 1 Ω resistors and could be used to represent the capacitor ESR losses. A direct comparison of capacitor losses between the Ladder and 2-Leg Ladder converters could then be made.
- The experimental method used to estimate converter losses was to calculate the difference between the converter input and output powers. This method becomes inaccurate as the converter efficiency approaches 100 % since any error in the individual measurement of input or output power contributes an unacceptable error in the calculation of losses. Therefore, by using the 1 Ω resistors, which gave a low converter operating efficiency, the comparison of losses for the two converters would be more accurate.

The circuit parameters used in this experiment are summarised in Table 7-1 below. The converter was operated as a unidirectional step-up converter. Therefore MOSFETs S_3 to S_8 shown in Figure 7-2, were disabled and received no gate signals so that only their anti-parallel diodes were conducting. A switching frequency of $15\ kHz$ was used, which corresponds to a value for $\beta_{i,k}$ of 1/3. The load resistor of $120\ \Omega$, corresponds to a nominal power of 480 W.

Table 7-1. Circuit parameters used in the hard-switched converter experiment

Component /Parameter	Specification
Conversion ratio	4
Switching frequency	15 kHz
MOSFETs	International rectifier IRFP4468 with $R_{ds,on} = 2.5\ m\Omega$
Capacitors	100 µF Film from AVX with ESR = 0.55 mΩ, with external 1 Ω series resistors.
Load	120 Ω resistive load
Input voltage	60 V

Experimental and analysis results based on the parameters given in Table 7-1 are listed in Table 7-2 for both the 2-Leg Ladder and Ladder circuits.

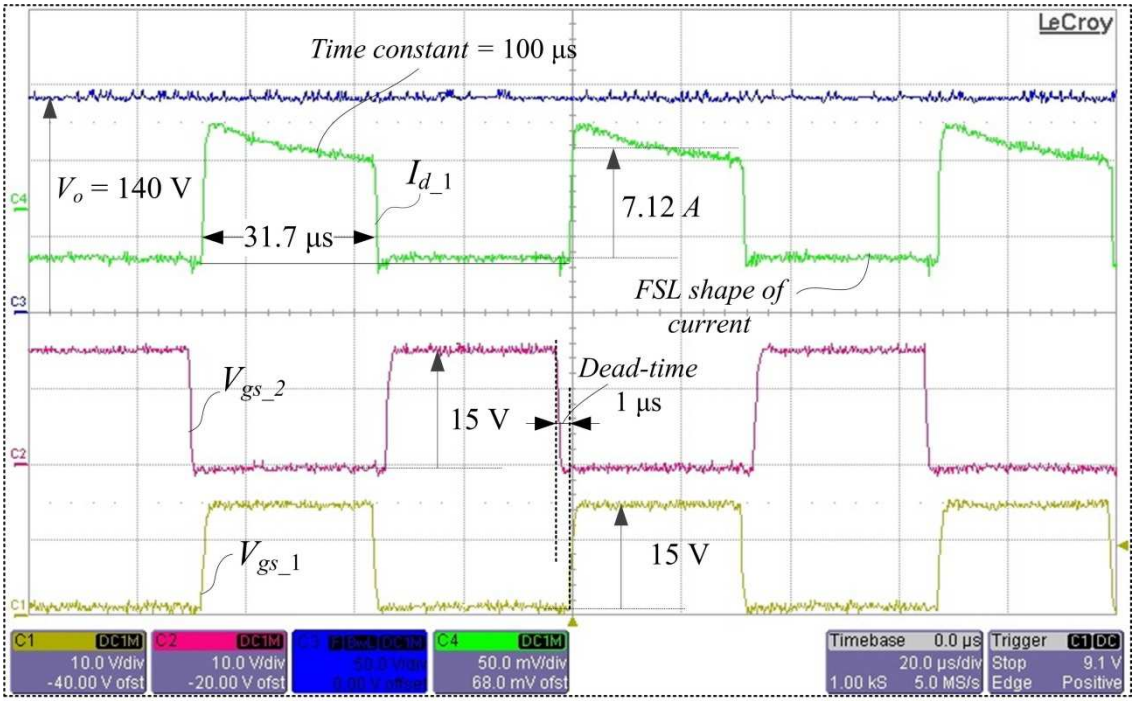
Table 7-2. Analysis and experimental results for Ladder and 2-Leg Ladder circuits with the parameters given in Table 7-1

	Analysis		Experiment	
	Ladder	**2-Leg Ladder**	**Ladder**	**2-Leg Ladder**
Output voltage (V)	141.8	189.5	140	189.4
Efficiency (%)	59.1%	79%	58.3%	78.9%
R_{eq} (Ω)	81.07	30.45	83.65	30.53

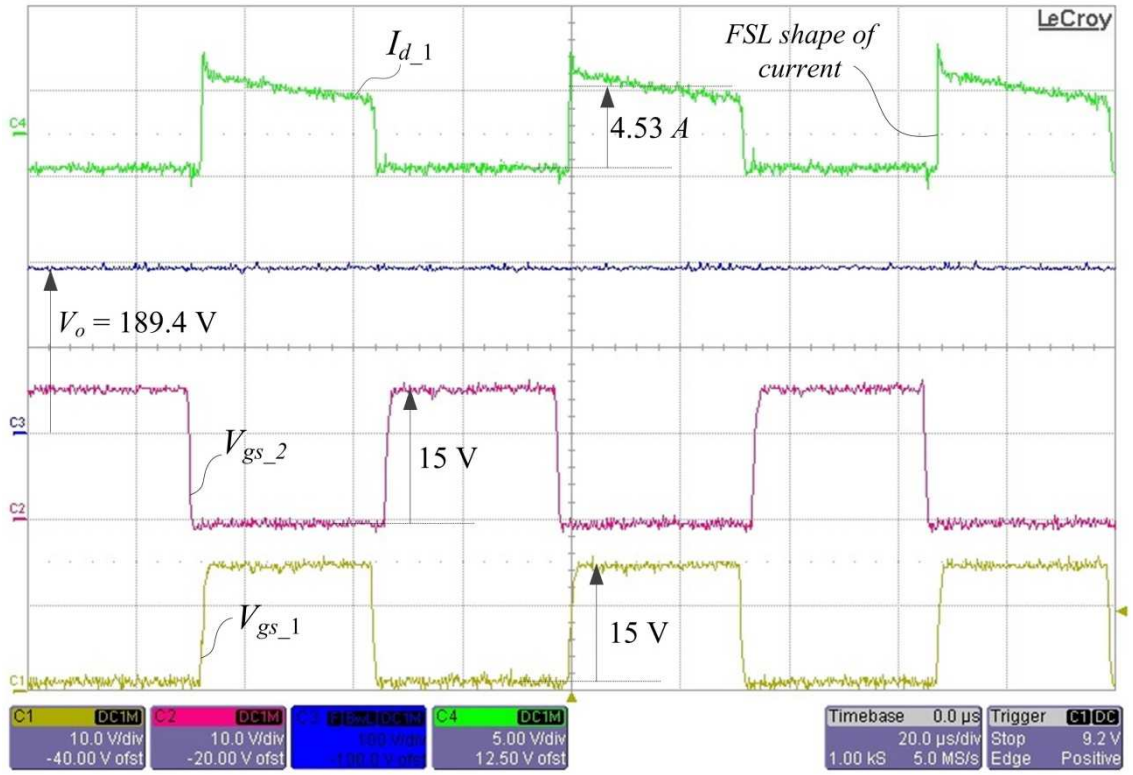
The experimental results are well matched with the predicted analytic values for the output voltage, efficiency and output equivalent resistance. Note that the anti-parallel diodes junction on-state voltage contributed an approximate 2.4 V voltage drop in the output of the converter, which has been included in the predicted results.

Comparing the two topologies it can be seen that the Ladder circuit, which had five capacitors, has approximately 270% higher capacitor losses when compared to the 2-Leg Ladder topology, which had six identical capacitors. Since the converters consisted of almost the same number of components and component types, their volume and cost is approximately the same. Therefore the higher efficiency achieved by the new 2-Leg Ladder circuit demonstrates its superior performance when compared to the Ladder topology.

The experimental output voltage waveform, the current for the bottom MOSFET (switch S_1 shown in Figure 7-2) and the complementary gate signals for Ladder and 2-Leg Ladder circuits are shown in Figure 7-6(a) and Figure 7-6(b) respectively.



(a)



(b)

Figure 7-6. Measured waveforms for the hard switched case. Output voltage (Upper), followed by MOSFET S_1 current and complementary gate signals respectively for (a) Ladder circuit (b) 2-Leg Ladder circuit

7.4.2 Resonant converters

The prototype described in the previous section was changed from a hard-switched circuit to a resonant topology by removing the 1 Ω resistors in series with the capacitors, and replacing them with 1 µH inductors. A high quality factor, 1 µH, 27 A, power inductor with a DC resistance of 0.9 mΩ from Coilcraft (SER2009-102L), was used for the resonant inductor. The switching frequency was increased from 15 kHz for the hard-switched converter to approximately 30 kHz for the resonant converter in order to exploit the inherent lower switching losses for this type of circuit. A resonant converter is designed so that the switching frequency and resonant frequency are equal, hence from equation (3-22)

$$C_{i,k} = \frac{1}{L_{i,k}\omega_{0,i,k}^2} \tag{7-1}$$

Allowing for a 1 µs deadtime, the capacitor value is therefore given by,

$$C_{i,k} = \frac{1}{1\text{x}10^{-6}}\left(\frac{1}{2\pi}\left(\frac{1}{30\text{x}10^{3}} - 2\text{ x }1\text{x}10^{-6}\right)\right)^2 = 25\ \mu\text{F} \tag{7-2}$$

A 22 µF EPCOS film components with an ESR value of 2 mΩ was used in the experiment. The switching frequency was adjusted to take account of circuit stray inductance and the change from the calculated capacitor value of 25 µF to 22 µF, until zero-current crossings at the MOSFET turn-on and off - curve (c) in Figure 3-12 was achieved. This corresponded to a switching frequency of 29.8 kHz. The circuit parameters are summarised in Table 7-3.

Table 7-3. Experimental circuit parameters for the resonant 2-Leg Ladder

Component /Parameter	Specification
Conversion ratio	4
Switching frequency	29.8 kHz
MOSFETs	International rectifier IRFP4468 with $R_{ds,on} = 2.5\ m\Omega$
Resonant Capacitors	22 µF Film Capacitors from EPCOS with ESR = 2 mΩ
Resonant Inductors	1 µH Power Inductor from CoilCraft SER2009-102ML with 0.67 mΩ DC resistance
Load	Resistive load (600 W)
Output filter capacitor	33 μF
Input voltage	60 V

Unlike the hard switched converter, where an additional 1 Ω resistor was added in series with the capacitor so that circuit parasitics and coupling effects became negligible, adding such a resistor to the resonant converter would reduce the quality factor of the resonant circuit to unacceptable

levels. Therefore, a comparison of results from the analysis equations against measurement could not be carried out due to the overriding effects of parasitics and coupling. In which case the results presented here are restricted to comparison of the measured performance of the Ladder circuit compared with the 2-Leg ladder converter only.

The first experimental tests were carried out on the resonant Ladder circuit. The measured steady-state, DC input/output voltage and current are shown in Table 7-4, along with the calculated efficiency of the converter using equation (6-3).

Table 7-4. Measured input and output voltage and current for resonant Ladder with the parameters given in Table 7-3

Parameter	Measured value
DC Output voltage	234.8 V
DC Input voltage	59.87 V
DC Input current	10.03 A
DC Output current	2.55 A
Calculated efficiency ($\boldsymbol{V_{out}/4V_{in}}$)	98.05 %

The results from the Ladder circuit measurements show that a high efficiency of approximately 98% was achieved. The ideal open-circuit output voltage for this converter is $4 \times 59.87 = 239.48$. The measured output voltage therefore indicates a drop of around 5 V at 600 W, which is due to the converter losses.

The measured drain current and drain-source voltage waveform for MOSFET S_1 is shown in Figure 7-7.

It can be seen from Figure 7-7 that the MOSFET drain current is the expected half-sinusoid, with zero crossings at approximately the start and end of the switching period. The switching and resonant current frequencies are not quite equal as the current goes slightly negative at the end of the period. The 1 µs dead-time is apparent following at the end of the period as the drain-source voltage rises toward half the converter input voltage due to the voltage divider formed by MOSFETs S_1 and S_2 in an off-state.

The Ladder circuit is coupled and the effect of the coupling and circuit parasitics can be seen in Figure 7-8, which shows measured drain current waveforms for MOSFET switches S_1 at the converter input and S_7 at the converter output.

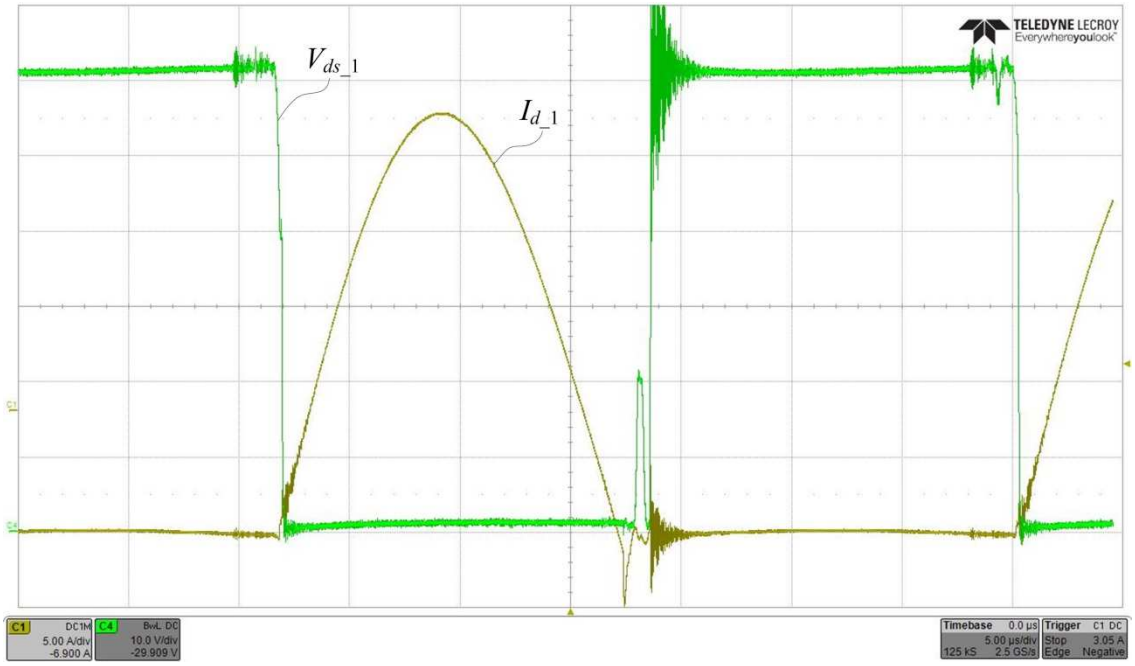


Figure 7-7. MOSFET S_1 measured drain current (I_{d_1}, 5 A/div) and drain-source voltage waveform(V_{ds_1}, 10 V/div) against time (5 µs/div)

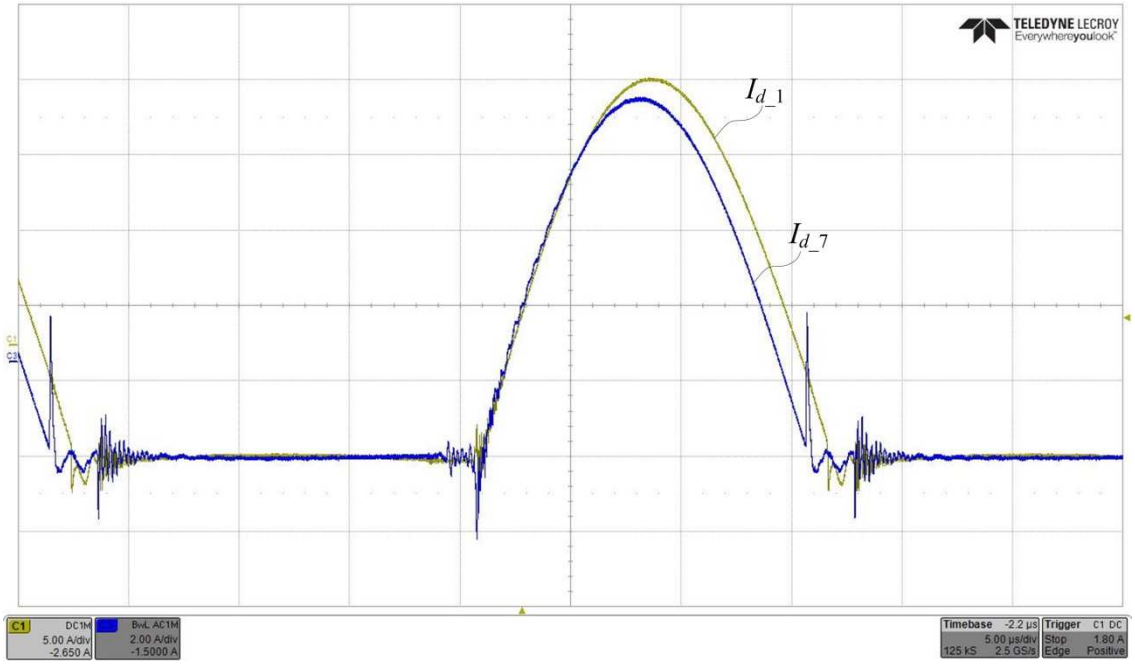


Figure 7-8. Measured drain current waveform for MOSFET switches S_1 and S_7 (I_{d_1} and I_{d_7}, 5 A/div and 2A/div) for the Ladder circuit against time (5 µs/div)

It can be seen from the above figure that the resonant frequency for the two currents are different, which is due to parasitic effects and coupling discussed in Chapters 4 and 5.

The output filter capacitor current ideally consists of a half-wave sinusoid with zero mean as shown by the measurement from the Ladder circuit in Figure 7-9.

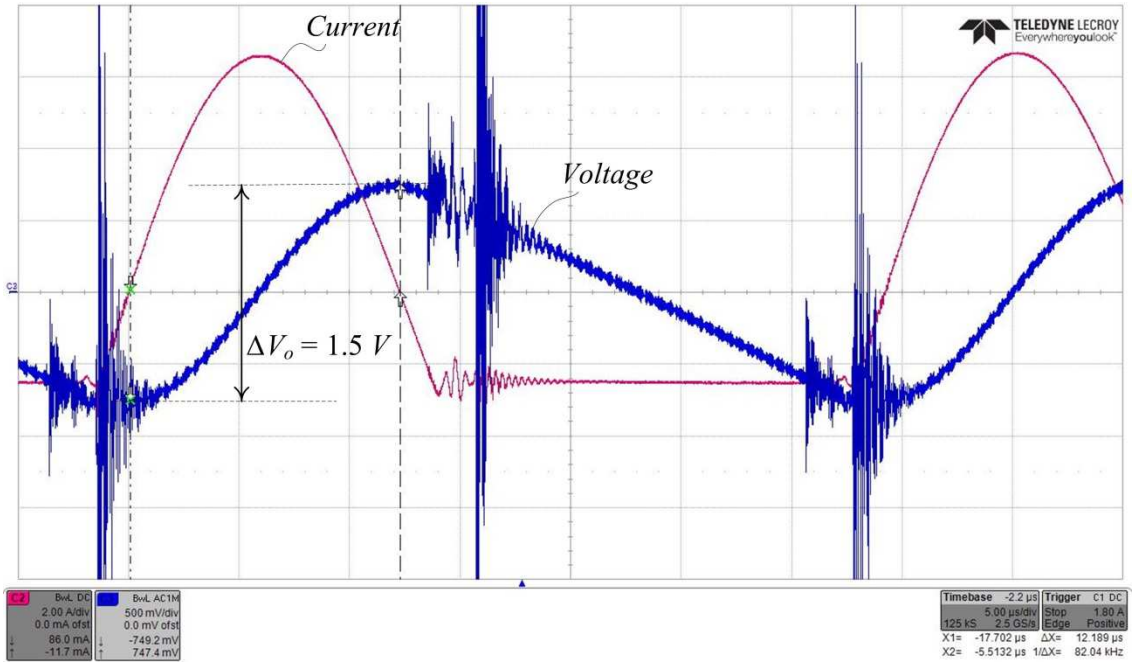


Figure 7-9. Output filter capacitor current (2 A/div) and voltage (0.5 V/div) for the Ladder circuit against time (5 µs/div)

It is straight forward to show by integration of the current waveform that the peak-peak capacitor ripple voltage ΔV_o for a half-wave sinusoid with zero mean is given by,

$$\Delta V_o = \frac{2}{\omega_s C_o}\left(\sqrt{\pi^2 - 1} - \sec^{-1}\pi\right) \mathrm{I_L} \tag{7-3}$$

where:

C_o : output filter capacitance (F)

$\mathrm{I_L}$: DC load current (A)

ω_s : switching frequency (rad/s)

The output voltage ripple based on the measured output current given in Table 7-4 and with a $C_o = 33\mu F$ output filter capacitor is calculated as 1.43 V, which compares well with the measured voltage ripple of 1.5 V shown in Figure 7-9.

Next, experimental tests were carried out on the resonant 2-Leg Ladder circuit. The measured steady-state, DC input/output voltage and current are shown in Table 7-5, along with the calculated efficiency of the converter using equation (6-3).

Table 7-5. Measured input and output voltage and current for resonant 2-Leg Ladder with the parameters given in Table 7-3

Parameter	Measured value
DC Output voltage	237.5 V
DC Input voltage	59.83 V
DC Input current	10.04 A
DC Output current	2.55 A
Calculated efficiency ($\boldsymbol{V_{out}/4V_{in}}$)	99.24 %

The results from the Two-Leg Ladder circuit measurements show that a high efficiency of approximately 99% was achieved. The ideal open-circuit output voltage for this converter is $4 \times 59.83 = 239.32\,V$. The measured output voltage therefore indicates a drop of around 1.8 V at 600 W, which is due to the converter losses.

The measured drain current and drain-source voltage waveform for MOSFET S_1 is shown in Figure 7-10.

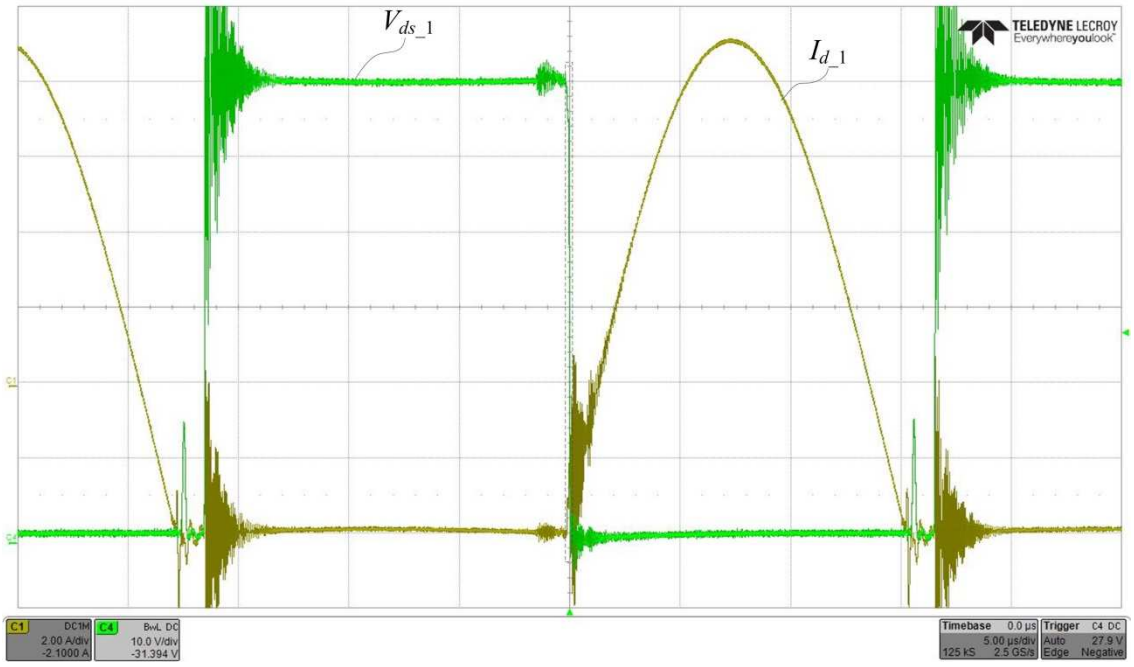


Figure 7-10. MOSFET Switch S_1 measured drain current (I_{d_1}, 2 A/div) and drain-source voltage waveform(V_{ds_1}, 10 V/div) against time (5 µs/div)

It can be seen from Figure 7-10 that the MOSFET drain current is the expected half-sinusoid, with zero crossings at approximately the start and end of the switching period. The 1 µs dead-time is apparent following at the end of the period.

The Two-Leg Ladder circuit is coupled and the effect of the coupling and circuit parasitics can be seen in Figure 7-11, which shows measured drain current waveforms for MOSFET switches

S_1 at the converter input and S_7 at the converter output and the odd-numbered MOSFET gate voltages.

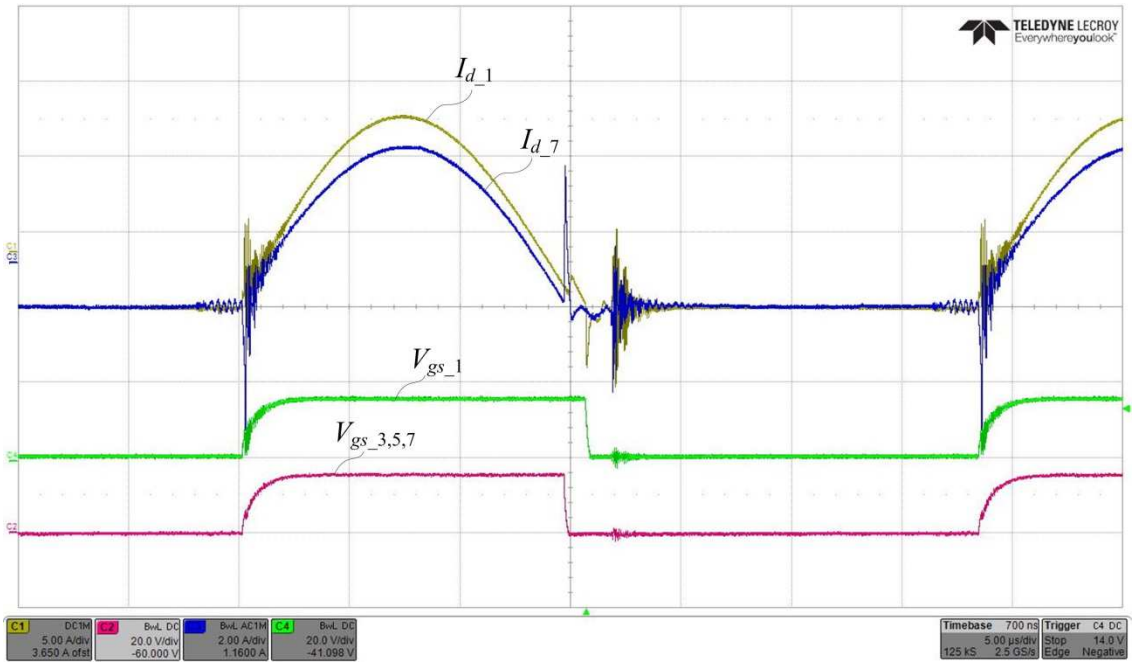


Figure 7-11. Measured drain current waveform for MOSFET switches S_1 and S_7 (I_{d_1} and I_{d_7}, 5 A/div and 2A/div) and odd-numbered MOSFET gate-signals ($V_{gs\_1,3,5,7}$ 20V/div) for the Ladder circuit against time (5 µs/div)

It can be seen from the above figure that the resonant frequency for the two currents are different, which is due to parasitic effects and coupling discussed in Chapters 4 and 5.

Note that since the converter power flow is purely unidirectional then only MOSFETs S_1 and S_2 need be active, whereas the conduction through MOSFETs S_3 to S_7 is entirely through their anti-parallel diodes so that these switches can in principal be disabled. On the other hand, the conduction losses through the anti-parallel diodes are much higher than when the MOSFET are enabled and current flows through the MOSFET channels. Therefore in this experiment, MOSFETs S_3 to S_7 where made active but the turn-off signals instants were individually adjusted to coincide with the zero current crossings, which prevents negative current flow and operation with the more inefficient b2 waveform – see Figure 3-12. This adjustment is apparent from the gate-signals in Figure 7-11, which highlights the difference in the turn-off instances of MOSFET S_1 and MOSFETs S_3, S_5 and S_7. It should also be noted that this switching technique was also used for the Ladder circuit experiments, which were discussed previously.

The output filter capacitor current ideally consists of a full-wave rectified sinusoid with zero mean as shown by the measurement from the Two-Leg Ladder circuit in Figure 7-9.

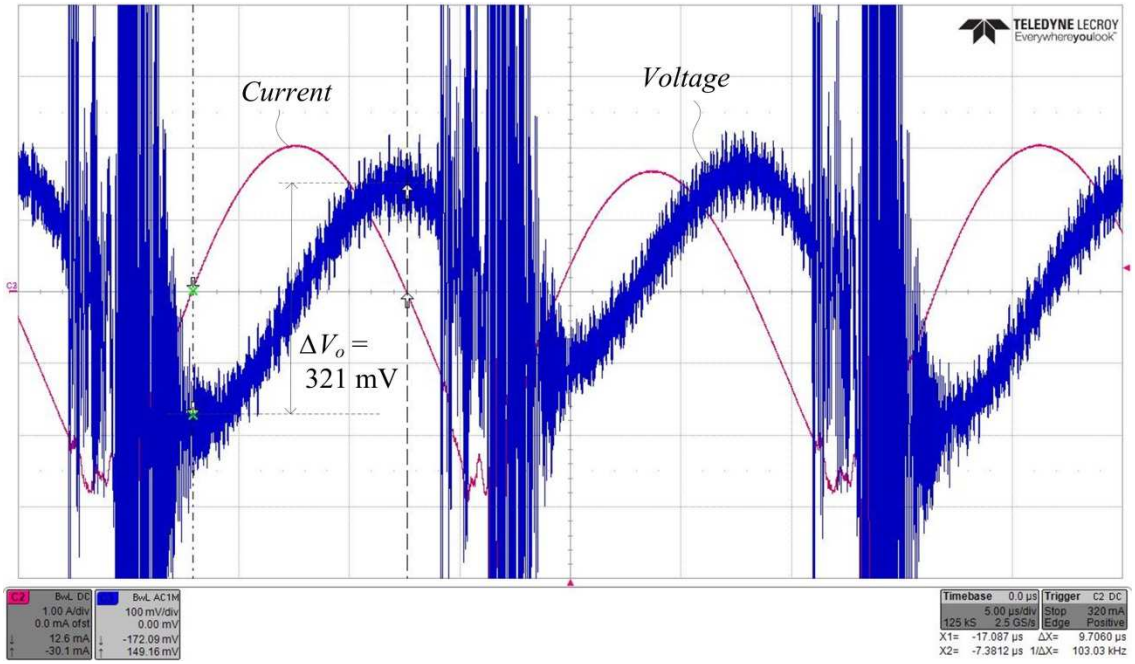


Figure 7-12. Output filter capacitor current (1 A/div) and voltage (0.1 V/div) for the Ladder circuit against time (5 µs/div)

It is straight forward to show by integration of the current waveform that the peak-peak capacitor ripple voltage ΔV_o for a rectified full-wave sinusoid with zero mean is given by,

$$\Delta V_o = \frac{1}{\omega_s C_o}\left(\sqrt{\pi^2 - 4} - 2\cos^{-1}\left(\frac{2}{\pi}\right)\right) I_L \qquad (7\text{-}4)$$

The output voltage ripple based on the measured output current given in Table 7-5 and with a $C_o = 33\mu F$ output filter capacitor is calculated as 0.27 V, which compares well with the measured voltage ripple of 0.32 V shown in Figure 7-12.

Comparison of the Ladder and 2-Leg Ladder circuits in terms of efficiency and output voltage ripple based on the experimental results for 600 W load is summarised in Table 7-6.

Table 7-6. Comparison of Ladder and 2-Leg Ladder circuits (Load is 600 W)

	Efficiency	Voltage ripple	Voltage ripple as % of output voltage
Ladder	98.05 %	1.50 V	0.64
2-Leg Ladder	99.24 %	0.32 V	0.13

The new 2-Leg Ladder circuit with almost the same converter cost, size and weight has a higher efficiency than the Ladder converter with losses being 0.76% and 1.95% respectively. This confirms the results of the analysis shown in Table 6-2. In addition, the analysis and measurement of the output voltage ripple for the two converters shows that the 2-Leg Ladder has almost four times lower ripple than the Ladder circuit for the same output filter capacitor. This can be

explained by the fact that the Ladder circuit only operates for a half a switching period and relies on the output capacitor to supply the load for the remainder of the period. Whereas, since the two legs of the 2-Leg ladder circuit operate in anti-phase, one of the legs is always supplying the load during a switching period.

A final experiment is carried out at a higher output power of 1050 W load, which highlights another advantage of the 2-Leg Ladder circuit when compared with the Ladder topology. The MOSFET S_1 drain current waveforms are shown in Figure *7-13* and Figure 7-14 for the Ladder and 2-Leg Ladder circuits respectively.

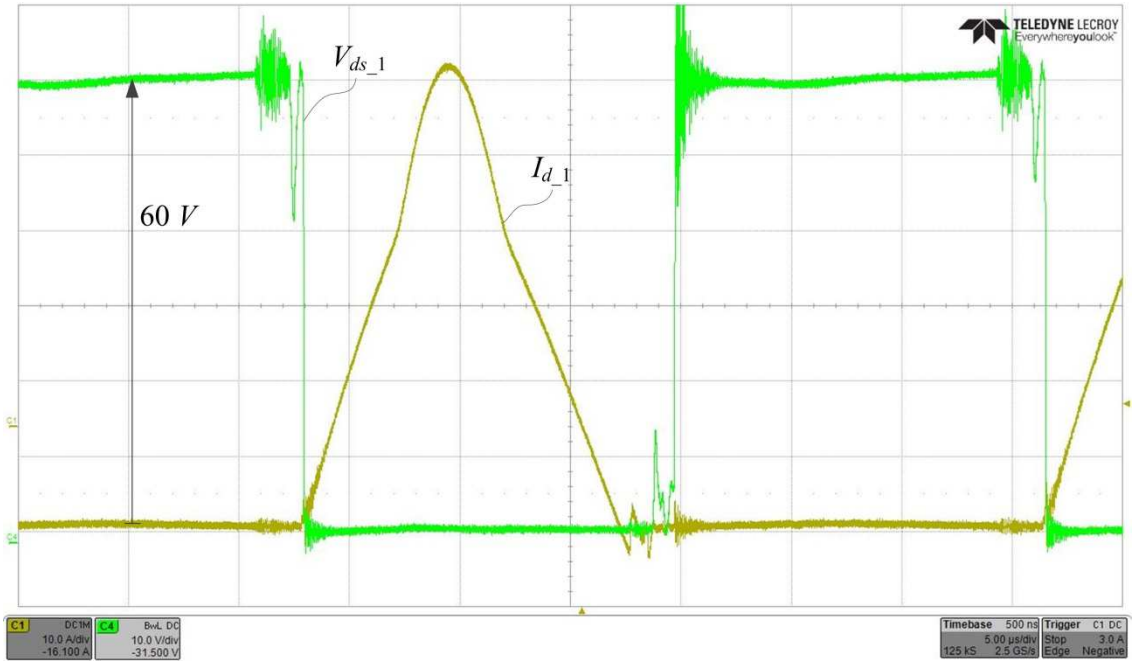


Figure 7-13. MOSFET Switch S_1 measured drain current (I_{d_1}, 10 A/div) and drain-source voltage waveform(V_{ds_1}, 10 V/div) against time (5 µs/div) for Ladder circuit.

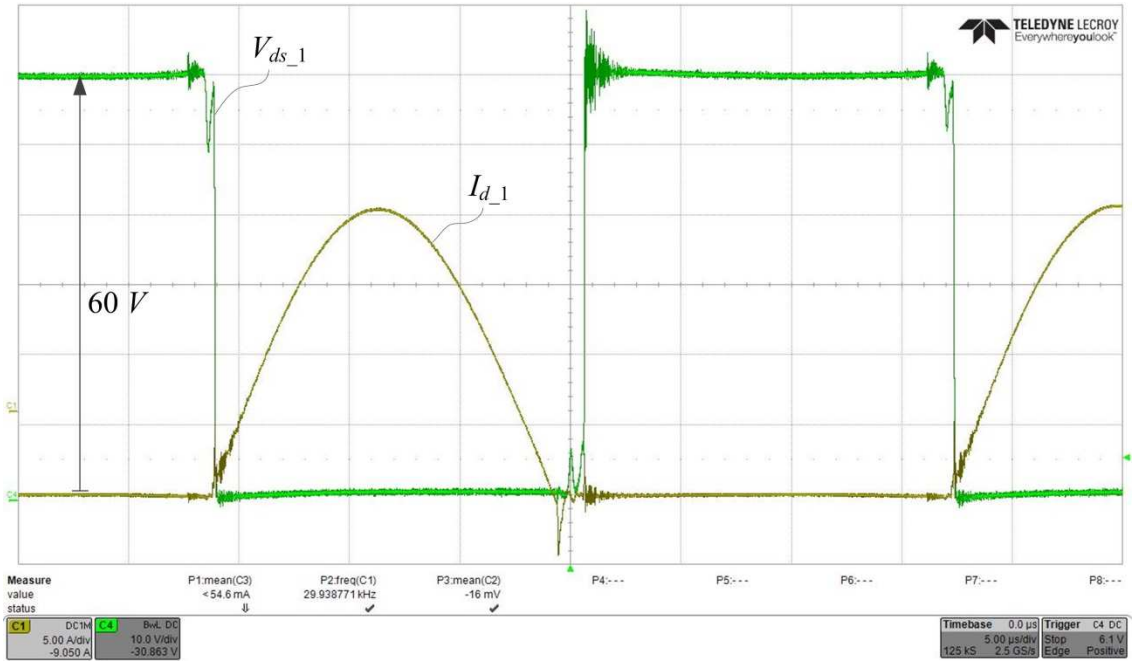


Figure 7-14. MOSFET Switch S_1 measured drain current (I_{d_1}, 5 A/div) and drain-source voltage waveform(V_{ds_1}, 10 V/div) against time (5 µs/div) for 2-Leg Ladder circuit.

The resonant current for the Ladder circuit has twice the magnitude of that for the 2-Leg Ladder. Therefore at the higher power level of 1050 W, this caused the resonant inductor in the Ladder circuit to saturate as can be seen by the distortion of the half-sine shown in Figure *7-13*. The Ladder peak resonant current is 62 A, whereas the 2-Leg Ladder has a peak resonant current of only 20 A. The datasheet saturation current of the resonant inductor was 27 A. In order to operate the Ladder circuit at 1050 W the inductors would need to be replaced with larger components, which would increase the cost, size and weight of the converter.

The measured steady-state, DC input/output voltage and current are shown in Table 7-7, along with the calculated efficiency of the converter using equation (6-3).

Table 7-7. Measured input and output voltage for resonant 2-Leg Ladder with the parameters given in Table 7-3 but with a load of 1050 W

Parameter	Measured value
DC Output voltage	236.1 V
DC Input voltage	59.88 V
DC Input current	4.46 A
DC Output current	17.65 A
Calculated efficiency ($\boldsymbol{V_{out}/4V_{in}}$)	98.57 %

The results from the Two-Leg Ladder circuit measurements show that a high efficiency of approximately 98.5% was achieved. The ideal open-circuit output voltage for this converter is

$4 \times 59.88 = 239.2$. The measured output voltage therefore indicates a drop of around 3.4 V at 1050 W, which is due to the converter losses.

7.5 Summary

The performance of the new 2-Leg Ladder circuit has been compared to a traditional Ladder circuit through tests on a laboratory prototype at 600 W. The 2-Leg Ladder has a superior performance, with approximately half the losses and four times lower output voltage ripple. In addition, the 2-Leg Ladder was shown to operate at almost twice the output power of the Ladder circuit, whereas the maximum output power of the Ladder circuit was limited by saturation of its resonant inductors.

8. Conclusion and Future Work

This thesis has investigated different DC-DC converter topologies and has assessed their suitability for high voltage, high power and high voltage-conversion ratio applications. Applications considered in this work were the connection of offshore wind farms to offshore DC grids and remote load feeding for small communities through HVDC lines. The specification requirements for the DC-DC converter were identified in Chapter 1.

The classification of converters into Direct and Indirect types was proposed in Chapter 2 along with a review of existing DC-DC converter circuits. Indirect topologies were found to be unsuitable for high voltage and high power applications due to their low efficiency and poor component utilisation when operating at high conversion-ratios. Whilst in theory a wound transformer can alleviate these problems to some extent, no such device exists in the market at present. However, Direct converters were found to be suitable for the target applications. In particular, switched capacitor (SC) converters, which have commonly been used in very low power applications, are now being considered for high power applications such as automotive and offshore DC-DC grids. The basic operation of SC converters was described in Chapter 2 where it was proposed that all SC topologies can be realised from a basic SC cell. In particular, the derivation of well-known SC topologies such as the Series-Parallel, Fibonacci, Ladder, Voltage-Doubler, Dixon Charge Pump, MMSCC and SMMSCC converters from the basic cell was also presented. For mega-watt range converters the Ladder, Dixon Charge Pump, MMSCC and SMMSCC were identified as being suitable candidate topologies.

The modelling and analysis of SC converters was investigated in Chapter 3. Switched capacitor converters were categorised into hard switched and resonant SC converters. Hard switched SC converters need to operate at very high switching frequencies to achieve high efficiency, which is not feasible in high power applications due to switching losses. However, resonant SC converters can achieve approximately the same efficiency as hard switch SC converters but at much lower switching frequencies with the added advantage of soft switching operation. Analysis techniques were developed that derive the output equivalent resistance of SC converters, and these methods were based on two important and recent publications in this area [50, 79]. Moreover the analysis techniques outlined in [79] was extended for resonant converters to include operation with non-zero current crossings. This is an important factor as circuit's parasitics and coupling can disturb the ideal half-sinewave shape causing switching losses and/or an increase in the output equivalent resistance.

The analysis techniques outlined in Chapter 3 are restricted to decoupled circuits where the circuit loops do not contain any common impedance. However, with coupled topologies such as the

Ladder and Dixon Charge Pump, SMMSCC and 2-Leg ladder the analytic expressions for the equivalent output resistance become intractable. This is because the equations contain terms with multiple time constants for the hard-switched converter and multiple frequencies for the resonant converter. In addition, this interaction between the circuit loops makes it difficult to achieve an ideal half-sinusoidal current waveform, which results in switching losses and increased conduction losses. It is proposed that decoupling is a critical feature when selecting resonant SC topologies for a particular application.

An experimental method for measuring circuit parasitics was developed using a system identification technique, which was based on a least-squares fit. The method is useful for identifying circuit impedances of uncoupled circuits. In a practical design this would then allow corrective measures to be taken to the circuit layout in order to ensure an optimum operation of the converter.

Four new SC synthesis techniques have been proposed namely using parallel converters and connecting common voltage nodes and eliminating redundant capacitors, stacking and splitting capacitors, modularisation and Bi-pole arrangements. Using these techniques a 2-Leg Ladder SC circuit was derived as well as a modular (M2LSCC) and bi-pole (SM2LSCC) variant. Based on these synthesis techniques, it was shown that some new topologies, which have been proposed in the literature, are actually derivatives of existing traditional topologies.

The resonant variants of the new M2LSCC and SM2LSCC circuits were identified as promising topologies for high power, high voltage and high voltage conversion-ratio applications. This is because unlike the existing MMSCC and SMMSCC converters, which have different capacitor and switch voltage ratings in each module, the proposed circuits have a pure modular structure where all the modules have identical voltage and power ratings and they are decoupled. Amongst these two new converters the SM2LSCC has a quarter of the number of capacitors than the M2LSCC circuit. All the topologies devised in this thesis have bidirectional capability and therefore are suitable for both the target applications introduced in chapter 1.

A scaled power 1.2 kW converter was designed and constructed in the laboratory to validate the analysis and to compare the performance of the new 2-Leg ladder circuit against a conventional Ladder circuit for both hard-switched and resonant operation. The experimental results for the hard-switched converter matched well with the analysis and the performance of the new resonant 2-Leg ladder circuit was shown to have approximately half the losses and four times lower output voltage ripple of the Ladder circuit. In addition, the 2-Leg Ladder circuit could operate at almost twice the output power of the Ladder topology, since the latter suffered from saturation of its resonant inductors.

Future work should include:

- An experimental investigation of parasitic effects and module interactions on a number of mega-watt scale M2LSCC modules.
- Assess the performance of the modified SMMSCC outlined in Chapter 6, which has a common ground point at the input and output.
- Scaled prototyping of all the topologies derived in the thesis in order to validate the operation of the circuits experimentally.
- An analysis of the operation of the proposed 2-Leg converter under fault conditions, in particular output short-circuit. This would include the development of fault protection and fault blocking techniques.
- An investigation on whether faulty modules could be bypassed during operation of the converter as used on new so-called voltage-source M^2C AC-DC HVDC converters.
- Devise methods to allow some level of output voltage control in SC converters.
- Techno-economic comparison of IGBT and SiC MOSFET transistors for use in the proposed modular SC converters.
- Interleaving operation of Bi-Pole SM2LSCC converter in order to further reduce the output voltage ripple

Two conference papers have been published and two patents are in the process of being filed by Alstom Grid as follow.

Conference papers:

- H. Taghizadeh, A. M. Cross, R. S. Whitehouse, and C. D. Barker, "Switched Capacitor DC-DC Converters for HVDC Applications," presented at the ACDC2015, Birmingham, United Kingdom, 2015.

- H. Taghizadeh and A. M. Cross, "The Effect of Circuit Parasitics on Resonant Switched Capacitor Converters," in *EPE 2015*, ed. Geneva, Switzerland: IEEE, 2015.

Patents:

- Modular 2-Leg Switched Capacitor converter (M2LSCC) (Alstom reference number RPA2540)
- Resonant Modular 2-Leg Switched Capacitor converter (Alstom reference number RPA2541)

Appendix A

Nodal Analysis to derive charge vector for 3-stage Ladder circuit

In this section, a 3-stage Ladder circuit will be used as an example, as shown in Figure A-1(a), to demonstrate how the charge vector can be derived for a properly-posed SC converter. The properties of properly-posed SC converters are discussed in detail in [81]. The graph of the circuit is also shown in Figure A-1(b). The current branch follows from node i to node j is represented by i_{ij}.

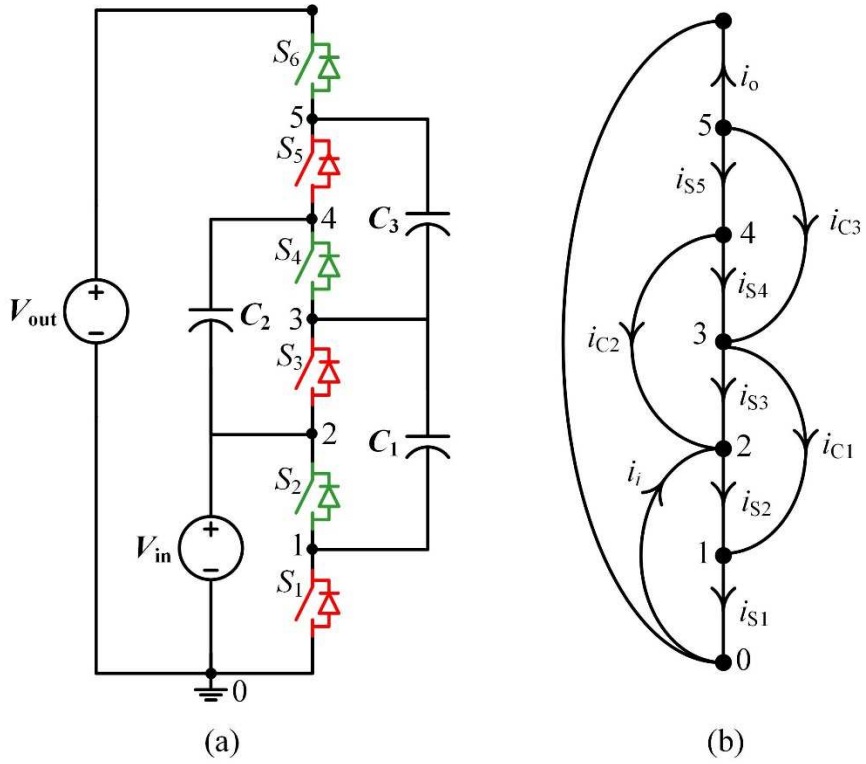


Figure A-1 (a) 3-stage Ladder circuit (b) The graph of the circuit

The following equations can be written for branch currents based on nodal analysis.

$$\begin{aligned} i_{C1} + i_{S1} - i_{S2} &= 0 \\ i_{C2} + i_{S3} - i_{S2} + i_i &= 0 \\ i_{S4} + i_{C3} - i_{C1} - i_{S3} &= 0 \\ i_{S5} - i_{C2} - i_{S4} &= 0 \\ i_{C3} + i_{S5} + i_o &= 0 \end{aligned} \tag{A-1}$$

Currents for switches S_2, S_4 and S_6 are zero during first phase and for switches S_1, S_3 and S_5 current is zero during second phase, therefor

$$\begin{aligned} i_{S2}^1 = i_{S4}^1 = i_o^1 &= 0 \\ i_{S1}^2 = i_{S3}^2 = i_{S5}^2 &= 0 \end{aligned} \tag{A-2}$$

where superscript 1 and 2 shows the switching phase in the SC converter. By substituting (A-2) in equations (A-1) and taking average during one switching period, nodal equations for average branch currents can be written as follows for switching phase one,

$$\begin{aligned} I_{C1}^{1} - I_{S1}^{1} &= 0 \\ I_{C2}^{1} + I_{S3}^{1} + I_{i}^{1} &= 0 \\ I_{C3}^{1} - I_{C1}^{1} - I_{S3}^{1} &= 0 \\ I_{S5}^{1} - I_{C2}^{1} &= 0 \\ I_{C3}^{1} + I_{S5}^{1} &= 0 \end{aligned} \tag{A-3}$$

and for the second switching phase,

$$\begin{aligned} I_{C1}^{2} + I_{S2}^{2} &= 0 \\ I_{C2}^{2} - I_{S2}^{2} + I_{i}^{2} &= 0 \\ I_{C3}^{2} - I_{C1}^{2} + I_{S4}^{2} &= 0 \\ I_{C2}^{2} + I_{S4}^{2} &= 0 \\ I_{C3}^{2} + I_{o}^{2} &= 0 \end{aligned} \tag{A-4}$$

Charge balance in capacitors implies,

$$\begin{aligned} I_{C1}^{1} + I_{C1}^{2} &= 0 \\ I_{C2}^{1} + I_{C2}^{2} &= 0 \\ I_{C3}^{1} + I_{C3}^{2} &= 0 \end{aligned} \tag{A-5}$$

The input and output average currents, I_{in} and I_{out}, can be written as follows,

$$\begin{aligned} I_{i} &= I_{i}^{1} + I_{i}^{2} \\ I_{o} &= I_{o}^{1} + I_{o}^{2} = I_{o}^{2} \end{aligned} \tag{A-6}$$

Average branch currents in terms of output average current can be obtained from equations (A-3) to (A-6) as follows for each capacitor,

$$\begin{aligned} I_{C1}^{1} &= -I_{C1}^{2} = 2I_{out} \\ I_{C2}^{1} &= -I_{C2}^{2} = -I_{out} \\ I_{C3}^{1} &= -I_{C3}^{2} = I_{out} \end{aligned} \tag{A-7}$$

and for the switches,

$$\begin{aligned} I_{S1}^{1} &= 2I_{out} \\ I_{S2}^{2} &= 2I_{out} \\ I_{S3}^{1} &= -I_{out} \\ I_{S4}^{2} &= -I_{out} \\ I_{S5}^{1} &= -I_{out} \\ I_{S6}^{2} &= -I_{out} \end{aligned} \tag{A-8}$$

For the input voltage source,

$$\begin{aligned} I_{i}^{1} &= I_{o} \\ I_{i}^{2} &= 2I_{o} \\ I_{i} &= I_{i}^{1} + I_{i}^{2} = 3I_{o} \end{aligned} \tag{A-9}$$

The charge vectors $\boldsymbol{a_c^1}$ and $\boldsymbol{a_c^2}$ for capacitors during first and second phases respectively are then defined as follows,

$$\begin{aligned} \boldsymbol{a_c^1} &= \begin{bmatrix} I_{c_1}^{1} & I_{c_2}^{1} & I_{c_3}^{1} \end{bmatrix} / I_o \\ \boldsymbol{a_c^2} &= \begin{bmatrix} I_{c_1}^{2} & I_{c_2}^{2} & I_{c_3}^{2} \end{bmatrix} / I_o \end{aligned} \tag{A-10}$$

Therefore the charge vector $\boldsymbol{a_c^1}$ and $\boldsymbol{a_c^2}$ based on (A-7) can be written as follow

$$\begin{aligned} \boldsymbol{a_c^1} &= [2 \quad -1 \quad 1] \\ \boldsymbol{a_c^2} &= [-2 \quad 1 \quad -1] \end{aligned} \tag{A-11}$$

From (A-2) and (A-8) the charge vector for switches S_1 to S_6 can be writen as follow during phase 1 and 2

$$\begin{aligned} \boldsymbol{a_{sw}^1} &= [0 \quad 2 \quad 0 \quad -1 \quad 0 \quad -1] \\ \boldsymbol{a_{sw}^2} &= [2 \quad 0 \quad -1 \quad 0 \quad -1 \quad 0] \end{aligned} \tag{A-12}$$

From (A-12), the devices S_1 and S_2 are conducting positive current while they are on, therefore these devices must be implemented by active transistors. However devices $S_3 - S_6$ are conducting negative current and blocking positive voltage therefore these devices can be implemented by diode.

Bu defining charge vector as $\boldsymbol{a^k} = \begin{bmatrix} \boldsymbol{a_c^k} & \boldsymbol{a_{sw}^k} \end{bmatrix}$, where k is the operation phase, the charge vectors form (A-11) and (A-12) for the 3 stage converter can be writes as follow

$$\begin{aligned} \boldsymbol{a^1} &= [2 \quad -1 \quad 1 \quad 0 \quad 2 \quad 0 \quad -1 \quad 0 \quad -1] \\ \boldsymbol{a^2} &= [-2 \quad 1 \quad -1 \quad 2 \quad 0 \quad -1 \quad 0 \quad -1 \quad 0] \end{aligned} \tag{A-13}$$

Each element $a_{i,k}$ in charge vector $\boldsymbol{a^k}$ corresponds to the charge multiplier for element i in switching phase k.

Appendix B

Normalised equivalent resistances for 3-stage Ladder circuit in switching phase 1

In this section normalised equivalent resistances for the 3-stage Ladder circuit, shown in Figure 4-4, is computed using Mathematica for first switching phase. Computed normalised equivalent resistance for switch S_1 and capacitor C_1 is as follows,

$$R^*_{eq,i,1} = \frac{(3+2K_r)\left(\frac{e^{-\frac{2(1.5+K_r)\beta_{\text{avg},i,1}}{0.63+K_r}}}{-3+\sqrt{3}-2K_r} - \frac{2e^{-\frac{2(1.5+K_r)^2\beta_{\text{avg},i,1}}{1.5+3K_r+K_r^2}}}{3+2K_r} - \frac{e^{-\frac{2(1.5+K_r)\beta_{\text{avg},i,1}}{2.37+K_r}}}{3+\sqrt{3}+2K_r} + \frac{15+24K_r+8K_r^2}{9+24K_r+18K_r^2+4K_r^3}\right)\beta_{\text{avg},i,1}}{\left(-2+e^{-\frac{(1.5+K_r)\beta_{\text{avg},i,1}}{0.63+K_r}}+e^{-\frac{(1.5+K_r)\beta_{\text{avg},i,1}}{2.37+1.K_r}}\right)^2} \tag{B-1}$$

The normalised equivalent resistance $R^*_{eq,i,1}$ for switch S_5 and capacitors C_2 and C_3 is computed as follow

$$R^*_{eq,i,1} = \left((3+2K_r)\left(\left(3+\sqrt{3}+2K_r\right)\left(-3+2\sqrt{3}+\left(-1+\sqrt{3}\right)K_r\right)^2 - e^{-\frac{2(1.5+K_r)\beta_{\text{avg},i,1}}{2.36+K_r}}\left(3+\sqrt{3}+2K_r\right)\left(-3+2\sqrt{3}+\left(-1+\sqrt{3}\right)K_r\right)^2 - \frac{4\left(3+6K_r+2K_r^2\right)^2}{3+2K_r} + \frac{4e^{-\frac{2(1.5+1K_r)^2\beta_{\text{avg},i,1}}{1.5+3K_r+K_r^2}}\left(3+6K_r+2K_r^2\right)^2}{3+2K_r} - \left(-3+\sqrt{3}-2K_r\right)\left(3\left(7+4\sqrt{3}\right)+2\left(9+5\sqrt{3}\right)K_r+2\left(2+\sqrt{3}\right)K_r^2\right) + e^{-\frac{2(1.5+K_r)\beta_{\text{avg},i,1}}{0.63+K_r}}\left(-3+\sqrt{3}-2K_r\right)\left(3\left(7+4\sqrt{3}\right)+2\left(9+5\sqrt{3}\right)K_r+2\left(2+\sqrt{3}\right)K_r^2\right)\beta_{\text{avg},i,1}\right) \Big/ \left(\left(2-\left(1+\sqrt{3}\right)e^{-\frac{(1.5+K_r)\beta_{\text{avg},i,1}}{0.63+K_r}}+\left(-1+\sqrt{3}\right)e^{-\frac{(1.5+K_r)\beta_{\text{avg},i,1}}{2.36+K_r}}\right)^2\left(3+6K_r+2K_r^2\right)^2\right) \tag{B-2}$$

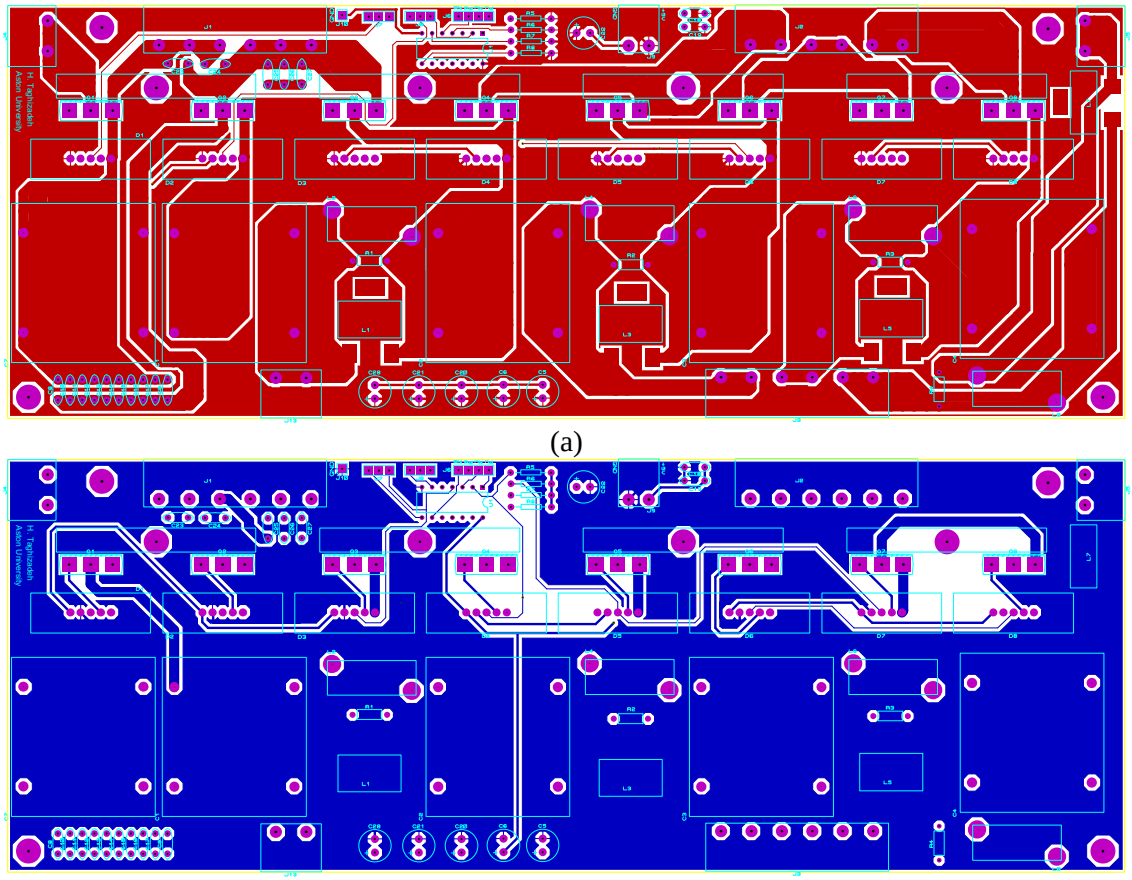
and for switch S_3 the normalised equivalent output resistance is computed as follows,

$$R^*_{eq,i,1} =$$

$$-\beta_{\mathrm{avg},i,1}(0.95e^{\frac{2(1.5+K_r)\beta_{\mathrm{avg},i,1}}{0.63+K_r}} + 0.25e^{\frac{2(1.5+K_r)\beta_{\mathrm{avg},i,1}}{2.36+K_r}} - 0.8e^{\frac{2(1.5+K_r)^2\beta_{\mathrm{avg},i,1}}{1.5+3K_r+K_r^2}} - 0.4e^{\frac{4(1.5+K_r)^2\beta_{\mathrm{avg},i,1}}{1.5+3K_r+K_r^2}} + (2.13e^{\frac{2(1.5+K_r)\beta_{\mathrm{avg},i,1}}{0.63+K_r}} + 0.27e^{\frac{2(1.5+K_r)\beta_{\mathrm{avg},i,1}}{2.36+K_r}}$$
$$- 1.6e^{\frac{2(1.5+K_r)^2\beta_{\mathrm{avg},i,1}}{1.5+3K_r+K_r^2}} - 0.8e^{\frac{4(1.5+K_r)^2\beta_{\mathrm{avg},i,1}}{1.5+3K_r+K_r^2}})K_r + (e^{\frac{2(1.5+K_r)\beta_{\mathrm{avg},i,1}}{0.63+K_r}} + 0.07e^{\frac{2(1.5+K_r)\beta_{\mathrm{avg},i,1}}{2.36+K_r}} - 0.53e^{\frac{2(1.5+K_r)^2\beta_{\mathrm{avg},i,1}}{1.5+3K_r+K_r^2}} \quad \text{(B-3)}$$
$$- 0.53e^{\frac{4(1.5+K_r)^2\beta_{\mathrm{avg},i,1}}{1.5+3K_r+K_r^2}})K_r^2)/((e^{\frac{(1.5+K_r)\beta_{\mathrm{avg},i,1}}{0.63+K_r}} - 0.26e^{\frac{(1.5+K_r)\beta_{\mathrm{avg},i,1}}{2.36+K_r}} - 0.73e^{\frac{2(1.5+K_r)^2\beta_{\mathrm{avg},i,1}}{1.5+3K_r+K_r^2}})^2(1.5 + 3K_r + K_r^2))$$

Appendix C

PCB layout of Power Board for the Top and Bottom Layers of Each Leg



(a)

(b)

Figure C-1. PCB layout for each leg, a) Top layer and b) Bottom layer

Appendix D

Schematic diagram designed to generate the gate signals in Quartus II and VHDL code.

The schematic diagram designed to generate the gate signals in Quartus II software is shown in Figure D-1. The “freq” module shown in Figure D-1, provides the switching period or accordingly switching frequency for “PWMGen” module. VHDL codes for “freq” and “PWMGen” are shown in Figure D-2 and Figure D-3 respectively. Two inputs for “freq” module are connected to two push-button keys provided on the development board. One push bottom key is assigned to reduce the switching period and another one is assigned for increasing the switching period. Since the system clock speed was too high for the purpose of “freq” module, the clock is reduced to 1 kHz using clock division module “Clock_divideN”. The VHDL code for “Clock_divideN” is shown in Figure D-4.

The “PWMGen” module generates four PWM signals with adjustable switching frequency and dead-time with a pre-defined period which can be set by the user. Two gate signals are slightly shorter which is used only in resonant converter as described in 7.4.2.

D.1. Schematic diagram

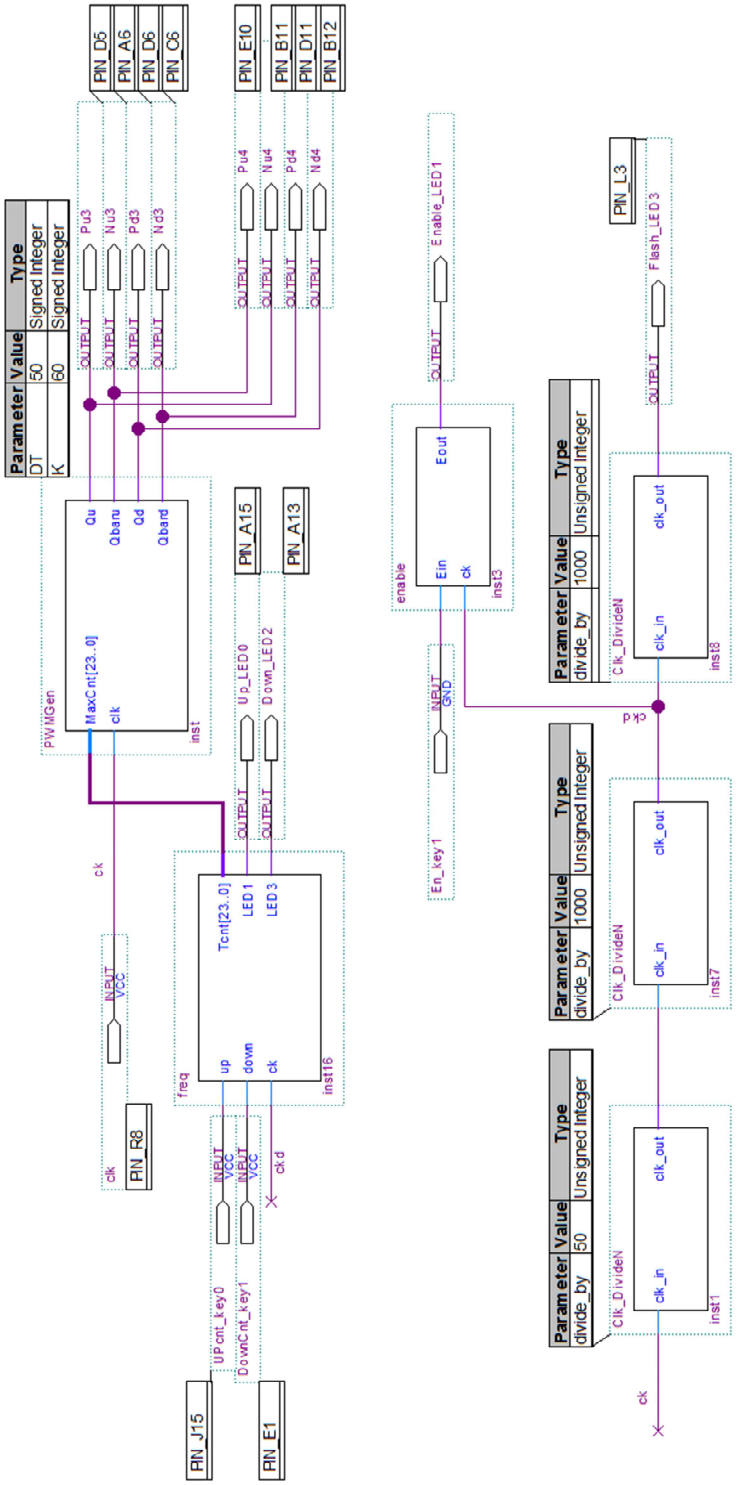


Figure D-1. Schematic diagram to generate the complementary gate signals in Quartus II

D.2. VHDL code for "freq" module

Date: November 07, 2015 freq.vhd

```
1   library ieee;
2   use ieee.std_logic_1164.all;
3
4   entity freq is
5      port(
6         up,down,ck     :  in std_logic;
7         Tcnt           :  buffer integer range 0 to 11000000;
8         LED1,LED3      :  out std_logic
9         );
10  end freq;
11  ------------------
12  architecture freq_arch of freq is
13  begin
14
15     process (ck)
16     variable cnt       :  integer range 0 to 15:=0;
17     variable Tcnt1     :  integer range 0 to 100000:=1666;
18     begin
19
20        if rising_edge(ck) then
21              if Tcnt1 < 200 then
22                 Tcnt1 := 500;
23              end if;
24
25              cnt := cnt + 1;
26              if cnt > 5 then
27                 cnt := 0;
28                 if Tcnt1 > 5000 then
29                    if up = '0' then
30                       Tcnt1 := Tcnt1 + 1;
31                       LED1 <= '1';
32                    else
33                       LED1 <= '0';
34                    end if;
35                    if down = '0' then
36                       LED3 <= '1';
37                       Tcnt1 := Tcnt1 - 1;
38                    else
39                       LED3 <= '0';
40                    end if;
41                 else
42                    if up = '0' then
43                       Tcnt1 := Tcnt1 + 1;
44                       LED1 <= '1';
45                    else
46                       LED1 <= '0';
47                    end if;
48                    if down = '0' then
49                       LED3 <= '1';
50                       if Tcnt1 > 250 then
51                          Tcnt1 := Tcnt1 - 1;
52                       end if;
53                    else
54                       LED3 <= '0';
55                    end if;
56                 end if;
57
58              end if;
59        Tcnt <= Tcnt1;
60        end if;
61     end process;
62  end freq_arch;
```

Figure D-2. VHDL code for "freq" module

D.3. VHDL code for "PWMGen" module

Date: November 07, 2015 PWMGen.vhd Project: PWM_Gen_with_enable

```
1   library ieee;
2   use ieee.std_logic_1164.all;
3
4   entity PWMGen is
5      generic (DT: integer range 0 to 511 :=50; K: integer range 0 to 500 :=150) ;
6      port(
7         MaxCnt   :  in integer range 0 to 11000000;
8         clk      :  in std_logic;
9         Qu,Qbaru :  out std_logic;
10        Qd,Qbard :  out std_logic
11        --count     :  out integer range 0 to 65535;
12        --Dcount :  out integer range 0 to 64
13        );
14  end PWMGen;
15  ------------------
16  architecture PWMGen_arch of PWMGen is
17  --signal    Q_t,Qbar_t  :  std_logic;
18  --signal  flag    :  std_logic;
19  begin
20     process (clk)
21     variable cnt                  :  integer range 0 to 11000000:=0;
22     variable Dcnt                 :  integer range 0 to 511:=0;
23     variable Denable              :  std_logic;
24     variable Q_t,Qbar_t           :  std_logic;
25     variable flag                 :  std_logic;
26        begin
27        if(rising_edge(clk)) then
28        -- count <= cnt;
29        -- Dcount <= Dcnt;
30                  if  ((cnt >= maxCnt/2 - DT - K) AND flag='0')    then
31                     Qd <= '0';
32                     Qbard <= '0';
33                     flag := not (flag);
34                  end if;
35                  if  ((cnt >= maxCnt/2 - DT) AND flag='1')    then
36                     cnt := 0;
37                     Dcnt := 0;
38                     Qu <= '0';
39                     Qbaru <= '0';
40                     Denable := '1';
41                     Qbar_t := Q_t;
42                     Q_t := not (Q_t);
43                     flag := not (flag);
44                  end if;
45           if Denable = '1' then
46              Dcnt := Dcnt + 1;
47              if Dcnt = DT  then
48                 Denable := '0';
49              end if;
50           elsif flag = '0' then
51              Qd <= Q_t;
52              Qbard <= Qbar_t;
53              Qu <= Q_t;
54              Qbaru <= Qbar_t;
55              cnt := cnt + 1;
56           else
57              cnt := cnt + 1;
58           end if;
59        end if;
60     end process ;
61  end PWMGen_arch;
```

Figure D-3. VHDL code for "PWMGen" module

D.4. VHDL code for "PWMGen" module

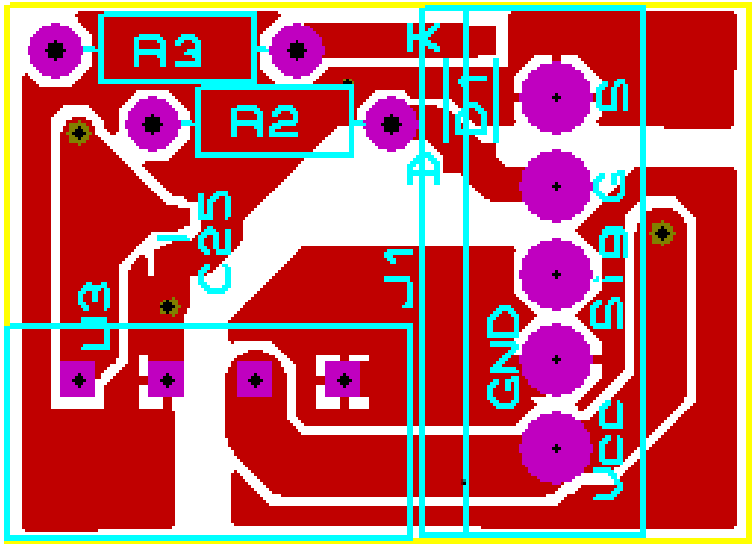
Date: November 07, 2015 Clk_DivideN.vhd

```
1   library ieee;
2   use ieee.std_logic_1164.all;
3
4   entity Clk_DivideN is
5      generic ( divide_by : integer range 0 to 1023 :=1000
6      ) ;
7      port(
8         clk_in    :  in std_logic;
9         clk_out   :  buffer std_logic
10        );
11  end Clk_DivideN;
12  ------------------
13  architecture Clk_DivideN_arch of Clk_DivideN is
14  begin
15     process (clk_in)
16     variable cnt    :  integer range 0 to 1023;
17        begin
18           if (rising_edge(clk_in)) then
19              cnt := cnt+1;
20              if cnt >= (divide_by/2) then
21                 clk_out <= not(clk_out);
22                 cnt := 0;
23              end if;
24           end if;
25     end process;
26  end Clk_DivideN_arch;
```

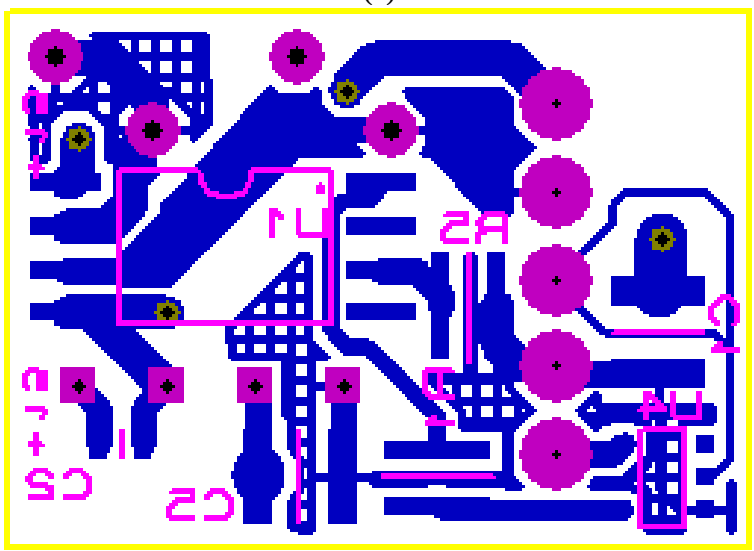
Figure D-4. VHDL code for "Clk_DivideN" module

Appendix E

PCB layout for Gate driver board



(a)



(b)

Figure E-1. PCB layout for gate driver board (b) top layer (c) bottom layer

9. References

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