Asynchronous Digital Optical Regenerator for 4×40 Gbit/s WDM to 160 Gbit/s OTDM Conversion

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Abstract: We propose and numerically analyse an asynchronous digital optical regenerator using a single-EAM loop and a novel neighbor-combine approach. It effectively re-synchronizes input signals with arbitrary phases to the local clock, and regenerates signals with high amplitude fluctuation and polarization mode dispersion. We demonstrate the application of this regenerator for 4×40 Gbit/s WDM to 160 Gbit/s OTDM conversion.

OCIS codes: (060.2330) Fiber optics communications; (060.4510) Optical communications.

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1. Introduction

In many proposed future networks, interconnection between backhaul and metro-core networks operating at different data rates is required [1]. For example, lower data rate signals from wavelength-division-multiplexed (WDM) networks would be aggregated into high data rate optical-time-division-multiplexed (OTDM) channels [2], and vice versa [3]. Whilst many papers have addressed all-optical techniques for such trans-multiplexing, few have addressed the synchronization issues associated with buffer-less (optical) multiplexing of signals from different sources. For WDM to OTDM conversion, each individual WDM channel must be time adjusted with bit level precision to a common reference clock before they can be aggregated to a single high data rate channel. Cotter and Ellis [4] suggest a novel approach to optical packet re-synchronization. Rather than performing traditional burst mode clock recovery and subsequent signal processing for bit-level synchronization of the incoming data

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at each node, these networks align an incoming signal with arbitrary phase and frequency offset to the local clock asynchronously. This is achieved by simultaneously sampling each data packet with several equally spaced clock phases, and selecting the sampling clock phase which maximises the performance. A minimum of four sampling clock phases is required for good error rate performance in the case of ideal gates [4]. Appropriate realizations have been established electronically [5] and optically [6]. The optical realisation [named Asynchronous Digital Optical Regenerator (ADORE)] uses two bi-directional electro-absorption modulator (EAM)-loops. The two EAM-loops provide timing of the necessary four clock phases needed in the regenerator, which was completed by a 4×1 selector switch [6].

In this paper, we propose and numerically analyse a simplified ADORE configuration, increasing the operating speed to 40 Gbit/s, whilst using only a single-EAM loop. By using the clockwise and anti-clockwise paths, as well as the two orthogonal polarizations in the EAM-loop, four clock sampling phases may be implemented, whilst optimisation of the overall system allows operation at high data rates without excessive bandwidth increases. We further simplify the ADORE architecture by interferometrically combining the signals from two adjacent sampling clock phases (so-called neighbor-combination). Although the single-EAM ADORE with neighbor-combination shows slight performance degradation when compared with using four separate sampling phases, the former reduces the required port count of the selector switch from four to two, which simplifies the comparator circuit and optical switch. We also propose and numerically analyse a 4×40 Gbit/s WDM to 160 Gbit/s OTDM converter constructed by using four single-EAM ADOREs, each sharing the same high quality local laser clock source and with appropriate delays between them, enabling OTDM multiplexing without further high speed wavelength conversion. Numerical analysis shows that the single-EAM ADORE effectively re-synchronizes and regenerates signals with high amplitude fluctuation and polarization mode dispersion (PMD), and reshapes and re-times pulses suitable for subsequent 160 Gbit/s OTDM multiplexing.

2. Operation Principle of ADORE with Neighbor-Combination

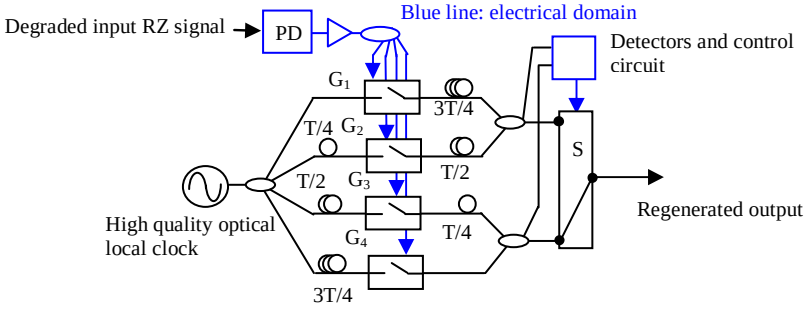

Fig. 1. Functional diagram of ADORE. PD: photodiode, G: gate, T: bit period, S: switch.

Figure 1 shows a functional diagram of an ADORE, using four gates to provide the four sampling clock phases but with the neighbor-combine approach. A high quality local optical clock (frequency = f_L) is applied to the inputs of the four gates with each input successively delayed by one-quarter of the nominal bit period T=1/ f_L. Each "one" bit of an input RZ signal at a frequency f_R, is used to simultaneously trigger all four gates opening a switching window of at least 25 % of the bit period, ensuring that the switching window of at least one gate overlaps with a single local clock pulse, irrespective of the phase difference between them. For a sufficiently small frequency difference (f_R - f_L) readily achieved in practice for 40 Gbit/s data packets of up to 4,000 bytes, the phase difference between the incoming packet and the local clock will vary by an insignificant amount [4] and so the data packet correctly modulates at least one clock phase, producing a re-timed data packet of frequency f_L. Thus, by simply selecting the optimum sampling clock phase from the output of one of the four gates, asynchronous regeneration can be achieved. By further ensuring that all possible clock phase paths are of identical total length, the relative phase of the re-timed packet is also

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known. Now for any given clock phase, whilst at least one of the two gates immediately adjacent to the optimum gate will be partially opened by the same data bit as the optimum gate, this will not necessarily be true for the other gates. In a conventional ADORE [6], all incorrectly gated data is rejected by the selector switch. However, the overall system may be simplified by interferometrically combining the two nearest neighbors (named neighbor-combine approach) which are both partially switched by the same data bit. For one of these combinations, both the contributing gates will have selected the same data bits, albeit with different amplitudes. Note that for a unipolar (optical) signal, the selector switch may be controlled by an appropriate power comparator [4] allowing a 2×1 optical switch to select the correctly regenerated packet.

3. Simulation Set-up for Single-EAM ADORE

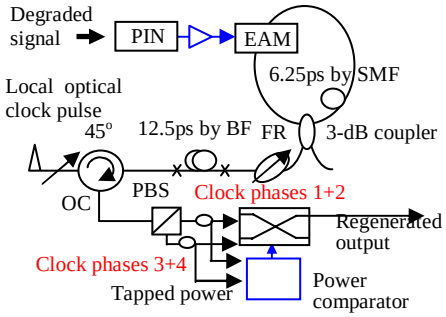

Fig. 2. Simplified ADORE using single-EAM loop with neighbor-combination. OC: optical circulator, BF: birefringent fiber, FR: Faraday rotator, SMF: single mode fiber and PBS: polarization beam splitter.

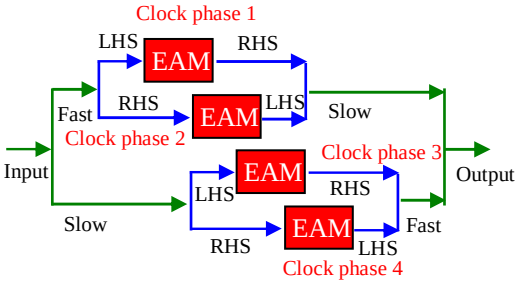

Fig. 3. Schematic diagram of the path lengths experienced by the 4 sampling clock phases in the single EAM-loop ADORE. LHS: left hand side, RHS: right hand side, Green: BF, Blue: loop.

Figure 2 shows the proposed setup of the single-EAM ADORE using a polarization diversity EAM-loop and the neighbor-combine approach. Numerical analysis was performed using VPI Transmission Maker V6.5, at 40 Gbit/s at DBBS of 2^7. A 40 Gbit/s (f_R) 33% RZ signal with variable delay (phase) is detected by a 40-GHz PIN (bandwidth optimised for optimum eye opening), which is then amplified and applied to an EAM to produce an extinction ratio of 20 dB. We use the VPI built-in EAM transmission characteristic, which is $T_{dB}(V) = T_{dB,0} + T_{dB,1}V$, where T is the transmission magnitude in dB ($T_{dB,0}$ = 0, $T_{dB,1}$ = -10) and V is the voltage. The local 40 GHz (f_L) 2 ps full width half maximum (FWHM) Gaussian clock pulses are launched into a birefringent fiber (BF) at 45° with respect to the fast/slow axes to produce two orthogonally polarized pulses with 12.5 ps delay. They are then rotated 45° by a Faraday rotator (FR) and launched into the EAM-loop in both clockwise and anti-clockwise directions via a 3-dB coupler. By offsetting the EAM from the loop centre, pulses propagating in the right hand side (RHS) of the loop are further delayed with respect to the pulses in the left hand side (LHS) by an additional 6.25 ps. After being gated by the EAM and travelling around the remainder of the loop, the pulses are reflected to the input port of the loop. Note that the equalization of the loop delays allows the co-polarised signals to be interferometrically combined, effectively implementing neighbor-combination. It is worth to notice that further rotation of the resultant signals by 45° using the FR to switch the polarization axes ensures that the total optical path for each of the four sampling phases is equalized after the second passage along the BF. The orthogonal pulses are then separated by a polarization beam splitter (PBS). Optical power is tapped out from each output of the PBS and fed to the power comparator to control the 2×1 optical selector switch. Figure 3 shows the relative path lengths traversed by the local optical pulse arriving at the EAM and at the output of the PBS for the four possible optical paths (numbered clock phase 1 to 4). As the system is limited by distortion rather than noise, we evaluate the performance in term of an eye opening factor (EOF), which is defined as $20\log_{10}[(U_{1min}-U_{0max})/(u_1-u_0)]$, where U_{1min} is the minimum value

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of ones, U_{0max} is the maximum value of zeros, and u_1, u_0 are the respective means. The EOF measurements are performed using a detector with 40 GHz 3rd-order Bessel bandwidth. Optical eye diagrams are captured without electrical filtering bandwidth.

4. Re-synchronization of the Single-EAM ADORE

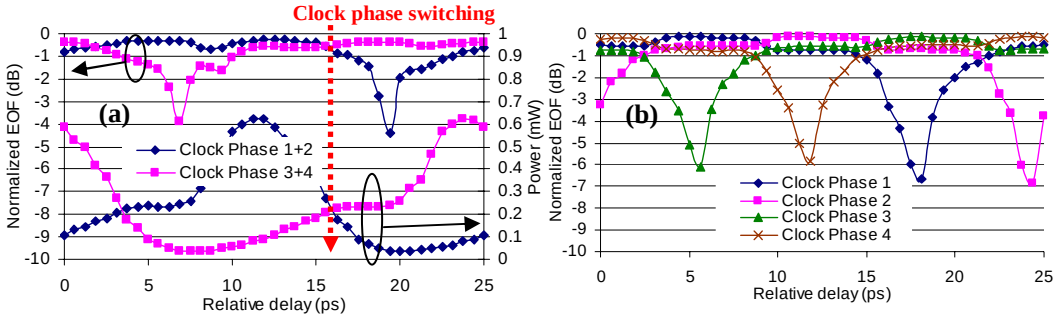

Fig. 4. (a) Optical power and EOF of single EAM ADORE with neighbor-combination, (b) conventional 4-EAM ADORE at relative delay between remote and local signals.

Firstly, we compared the re-synchronization property of the proposed single-EAM ADORE using neighbor-combination with a conventional ADORE [4] based on four separate clock phases (implemented by four independent EAMs). The EOF (normalized to the input RZ signal) and the tapped optical power of the single-EAM ADORE (Fig. 2) were measured as a function of the delay difference between the RZ input and local clock pulses, as shown in Fig. 4(a). This shows that at least one of the single-EAM ADORE output clock phases can fully re-synchronize the incoming data; and that we can effectively use the tapped optical power to control the 2×1 selector switch. At the points of output clock phase switching [at 3.75 ps and 16.25 ps relative delay in Fig. 4(a)], the tapped power levels are equal, and erroneous decisions could be made, resulting in a small eye opening penalty of 0.6 dB for both outputs. The performance of a conventional 4-EAM ADORE [Fig. 4(b)] suggested that the simple single-EAM ADORE performs as well as the 4-EAM ADORE with an additional penalty of only 0.2 dB. We also verified that for the proposed single-EAM ADORE, if non-neighbor channels are combined (i.e. Clock phases 1+3 and Clock phases 2+4), delays exist with unacceptable inter-symbol interference (ISI).

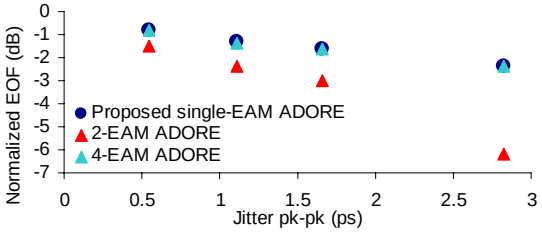

Fig. 5. EOF comparison of single EAM ADORE, conventional 4-EAM ADORE and 2-EAM ADORE at different input RZ signal with timing jitter peak-to-peak (pk-pk).

In order to verify the performance advantage of the proposed single-EAM ADORE, we compared the performance to a conventional 4-EAM ADORE and a 2-EAM ADORE (2 sampling clock phases with 12.5 ps time difference between them) as a function of timing jitter in the input RZ signal. The timing jitter may introduce an error in selecting the optimum output clock phase. For a 4-EAM ADORE, this is mitigated by the large overlap of the switching windows. The comparison was performed using the same EAM model and input RZ pulses as described in Section 3, and the random timing jitter peak-to-peak (pk-pk) of the input RZ was generated by the built-in function of VPI. Figure 5 shows the normalized EOF for the worse input phase for each simulated jitter value. The high sensitivity of the 2-EAM ADORE is apparent in this figure for a jitter above 1 ps pk-pk. However, the expected shape of the tapped power versus input phase curve of the single-EAM ADORE is modified by the interferometric addition of the two optimised neighbor switching windows. This significantly

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reduces the probability of high eye opening penalty from such switching errors, restoring the performance to the 4-EAM ADORE case.

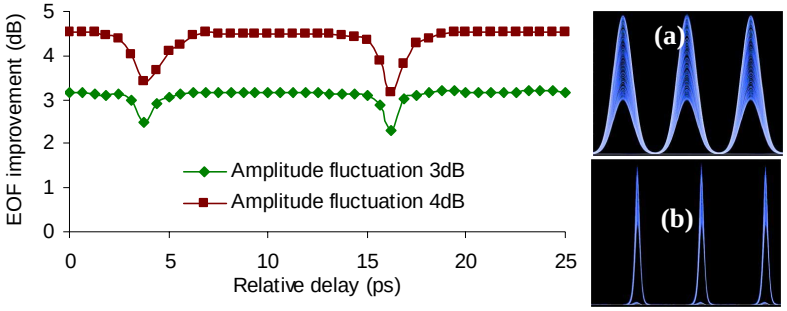

Fig. 6. EOF improvement of re-synchronized signals. Inset: 40 Gbit/s optical eye diagrams of (a) input degraded signal at amplitude fluctuation of 4 dB and (b) re-synchronized signal (worst case).

Figure 6 shows the EOF improvement of the re-synchronized signal (optimum clock phase selected using power comparator) when an amplitude fluctuation was added to the input signal by using another amplitude modulator, which was driven with a 1 GHz sinusoidal signal. The amplitude fluctuation is defined as $10\log_{10}(U_{1max}/U_{1min})$, where U_{1max} and U_{1min} are maximum and minimum value of ones respectively. This confirms that the nonlinear transfer characteristic of the EAM suppresses one level amplitude fluctuation when used in the single-EAM ADORE. We observe >3 dB EOF improvement when input signal with amplitude fluctuation of 4 dB, even at the worst relative delay.

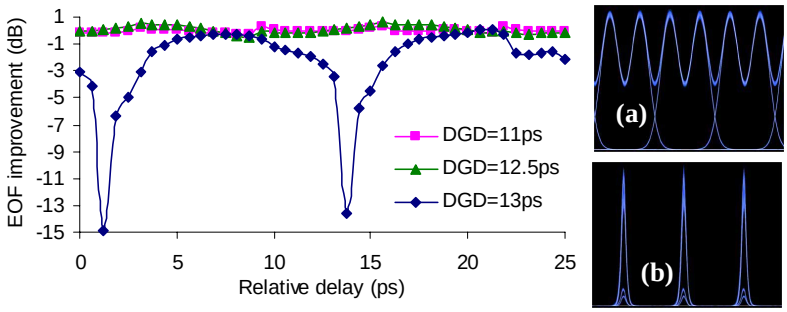

Fig. 7. EOF improvement of re-synchronized signals. Inset: 40 Gbit/s optical eye diagrams of (a) input degraded signal at DGD of 12.5 ps and (b) re-synchronized signal (worst case).

The input signal was then degraded by fiber birefringence, simulating differential group delay (DGD), to evaluate the system tolerance to first order PMD. The input RZ signal was launched at a 45° angle with respect to the principle states of fiber to produce the greatest impact in each case. Figure 7 shows that the single-EAM ADORE can re-synchronize signals at high DGD of 12.5 ps, providing a EOF improvement of 0.7 dB in the best cases, and -0.5 dB at the worst case [inset (b)]. However, when the DGD is more than about half of the bit period (at 12.5 ps), the EOF decreases rapidly due to the increase in ISI. Since the re-synchronized output signal is produced from a local laser source, any polarization fluctuation from the input signal is removed, improving the PMD tolerance of the ADORE output signal [7]. For timing jitter tolerance, we has shown that the proposed single-EAM ADORE effectively retimes signals with small level of jitter (Fig. 5), but has a reduced jitter tolerance when compared with direct detection of the signal using a conventional phase locked loop [8].

5. WDM-to-OTDM Conversion

We finally studied a WDM-to-OTDM format converter, constructed by using four single-EAM ADOREs, sharing the same high quality local laser clock source and with appropriate delays following them to time interleave the re-synchronized output signals, as shown in Fig. 8. Whilst the insertion loss of each ADORE at optimum relative delay is identical, no further

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attempt to equalize the re-synchronized power levels was made. The four independent 40 Gbit/s 33% duty cycle WDM input pulses (numbered WDM 1, 2, 3 and 4) and the 2 ps FWHM 40 GHz local laser clock source are at wavelengths of 1548.51, 1549.31, 1550.11, 1550.91 and 1554.94 nm respectively. The converted 160 Gbit/s OTDM signal is then optically time demultiplexed using two cascaded Mach-Zehnder modulators into a 40 Gbit/s signal, which are detected by 40 GHz PDs for EOF analysis. We arbitrarily select the demultiplexed WDM 1 and analysed the relative delays between its neighboring OTDM channels (WDM 2 and WDM 4) and the local clock pulses in the WDM-to-OTDM converter, and depict the EOF (normalized to the input WDM1) in Fig. 9(a) and (b) respectively, with the corresponding optical eye diagrams. The delay of WDM 3 was arbitrarily chosen. The results show that the converter effectively re-shapes (compresses) and retimes pulses suitable for 160 Gbit/s multiplexing. Note that for the worst case signal, the EOF degradation is only 2 dB [Fig. 9(d)], which is dominated by power fluctuations - clear and wide open eye can still be observed.

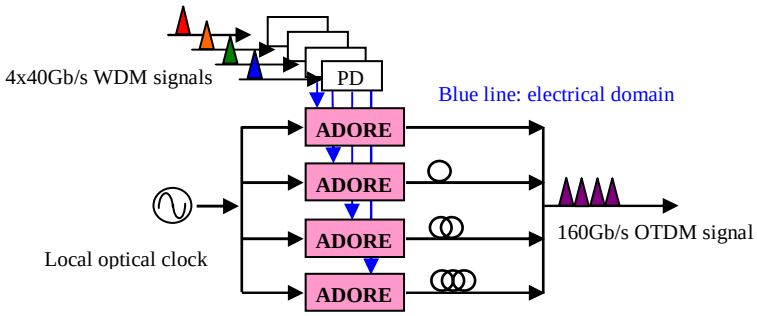

Fig. 8. WDM-to-OTDM conversion using four ADOREs.

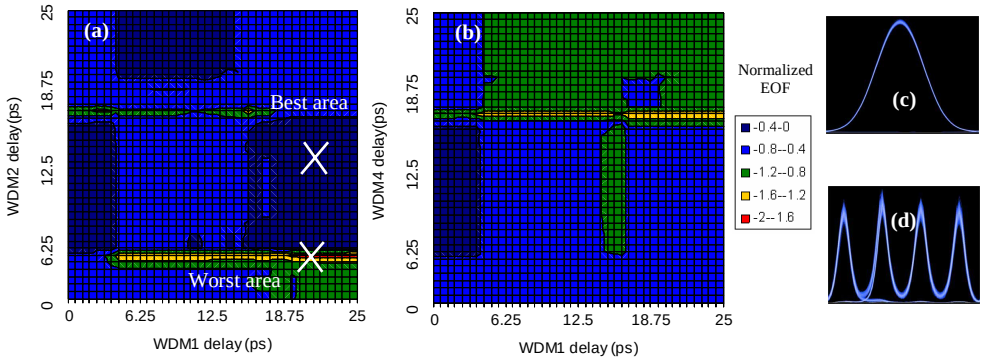

Fig. 9. (a), (b) normalized EOF of the WDM-to-OTDM converter. Optical eye diagrams of (c) 40Gbit/s input signal and (d) 160Gbit/s output at the worst case.

6. Conclusion

We propose and numerically analyse an ADORE using a single-EAM loop (using the clockwise and anti-clockwise paths, as well as the two orthogonal polarizations in the EAM-loop to implement the required four clock sampling phases) with neighbor-combine approach, showing that it effectively re-synchronizes input signals with arbitrary phases to the local clock, regenerates signals with high amplitude fluctuation and PMD, and re-shapes (compresses) pulses suitable for 4×40 Gbit/s WDM to 160 Gbit/s OTDM conversion.

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