VSC Topology Comparison For STATCOM Application Under Unbalanced Conditions

Aitor Laka[1], Andrew Cross[2], Jon Andoni Barrena[1], Javier Chivite-Zabalza[3], Miguel Ángel Rodríguez[3]

[1]UNIVERSITY OF MONDRAGON
20500, Loramendi 4
Mondragon, Spain
Tel: (+34) 943 739 461
alaka@mondragon.edu
jabarrena@mondragon.edu
www.eps.mondragon.edu

[2]ASTON UNIVERSITY
B4 7ET, Aston Triangle
Birmingham, United Kingdom,
Tel: +44 (0)121 204 3731
a.m.cross@aston.ac.uk
www1.aston.ac.uk

[3]INGETEAM TECHNOLOGY S.A.
48170, Edificio 108
Zamudio, Spain
Tel: (+34) 946 018 900
javier.chivite@ingeteam.com
miguelangel.rodriguez@ingeteam.com
www.ingeteam.com

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Keywords

« Fault Ride-Through », « Voltage Source Converter (VSC) », « Static Synchronous Compensator (STATCOM) ».

Abstract

This paper compares the performance of four different power electronic converter topologies, which have been proposed for STATCOM applications. Two of the topologies are Modular Multilevel Cascaded Converters (MMCC), whilst the remaining circuits utilize magnetic elements and an open-winding transformer configuration to combine individual power modules. It is assumed that the STATCOM has to work under unbalanced conditions, so that it delivers both positive and negative sequence currents. Simulation studies for the four topologies have been carried out using the simulation tool Saber.

Introduction

The number of grid connected power electronics devices have increased significantly over the last few decades. This has been driven for example, by an increase in the penetration of the renewable energy such as wind-farms and Flexible AC Transmission System (FACTS) devices, which are used to control the key parameters of an electrical network [1]. One of the commonly used FACTS device is the Static Synchronous Compensator (STATCOM) [2]. The STATCOM is suitable device for the control of the voltage at the Point of Common Coupling (PCC), for instance. It consists of a Voltage Source Converter (VSC) shunt connected through a series inductance to the PCC. By exchanging reactive power, the voltage amplitude at the PCC can be controlled. Subsequently, the VSC only needs a capacitor bank on its DC side, simplifying the configuration of the system. A small amount of active power is drawn from the grid by the STATCOM in order to overcome its own internal losses and keep constant the voltage of the DC bus. In some applications the STATCOM has to work under unbalanced conditions. In these cases, the STATCOM can be used to balance the voltage at the PCC by injecting positive and negative sequence currents [3-5]. In addition, the STATCOM can balance the voltage at the PCC when an unbalanced load has been connected. This case is given for example in electrified railway traction power supply applications [6], or arc furnace applications [7-9]. The selection of the most suitable VSC topology for a STATCOM application is a challenging issue. There are many VSC topologies that can be used in STATCOM applications [10]. In high power

applications, standardized power converters are inter-connected in order to increase the power rating of the overall VSC. These standardized power converters are known as Power Electronic Building Blocks (PEBB) [11]. The PEBBs can be connected in series to increase the output voltage or they can be parallelized to increase the output current. In order to increase the output voltage or current of the VSC, isolated DC buses [12], magnetic elements [13] or open-winding configurations [10,14-15] can be used. The Modular Multilevel Cascaded Converters (MMCC) are based on PEBB inter-connection using isolated DC buses [16]. A review of different MMCC topologies was carried out in [17], where they were classified into four different circuit configurations. Two of these topologies are analyzed and compared in [18] for STATCOM application under balanced conditions.

In this paper four converter topologies for STATCOM application are compared: two MMCC topologies and two open-end winding topologies with a combination of magnetic elements. It is considered that the STATCOM can work under balanced or unbalanced conditions, taking into account the influence of the working conditions on the sizing of the DC side capacitors. In Section II the individual VSC topologies are presented and described. In Section III, the comparison criteria are introduced namely the magnitude of the output voltage, the VA rating of the magnetic elements, the electrical capacitance requirement and the converter efficiency. Section IV describes the conditions in which the VSC topologies have been simulated and the simulation results are discussed in Section V.

High Power Converter Topologies

The paper studies the arrangement of 12 PEBBs for a 40 MVA STATCOM. The study is based on existing industrial 3-Level Neutral Point Clamped (3L-NPC) PEBBs, individually rated at 3.3 MVA. The nominal output current of each PEBB is 1650 A and the DC side voltage is rated at 5 KV as is shown in Figure 1.

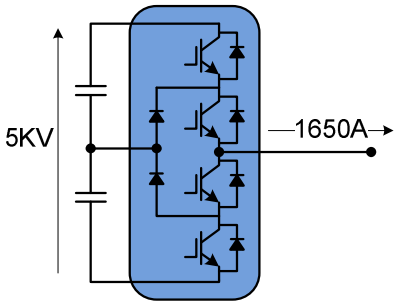

Figure 1. 3.3 MVA PEBB based on Neutral Point Clamped (NPC) topology.

In two of the compared topologies the PEBBs are inter-connected by using magnetic elements and the output transformer is connected in open-winding configuration. The other two topologies are Modular Multilevel Cascaded Converters (MMCC). The four topologies have been simulated in the simulation tool Saber applying Pulse Width Modulation (PWM) with a switching frequency of 600Hz. The carriers of the PEBBs are phase shifted to improve the harmonic content of the output voltage of the VSC. In order to increase the amplitude of the fundamental component of the output voltage, a third order harmonic (1/6 of the fundamental) is injected to the reference of the PWM. The DC side capacitors of the converters have been simulated using ideal voltage sources and the average powers of these sources were monitored to ensure that they equated to zero.

Topology I: A single common DC bus

Figure 2 shows the configuration scheme of the first VSC topology that was presented in [13]. It consists of twelve 3L-NPC PEBBs with a single common DC bus, that is, all the PEBBs are sharing the same DC bus. As the converter is a three-phase converter and a total of 12 PEBBs are used, four PEBBs are used for each phase. Each PEBB pair is parallelized using an Inter-Phase Transformer (IPT) which assures the same current sharing through the paralleled PEBBs. A total number of 6 IPTs are used. It is considered that each half of the converter is combined by feeding the opposite ends of an ideal open winding transformer. Zero Sequence Blocking Transformers (ZSBT) are then essential in order to prevent large zero sequence currents circulating around the converter. Zero sequence currents can be generated for example because of the third harmonic injection used in the PWM.

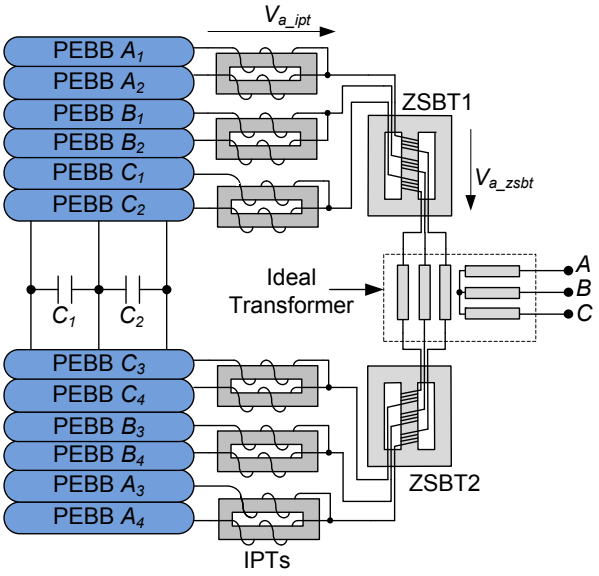

Figure 2. Converter topology with a single common DC bus.

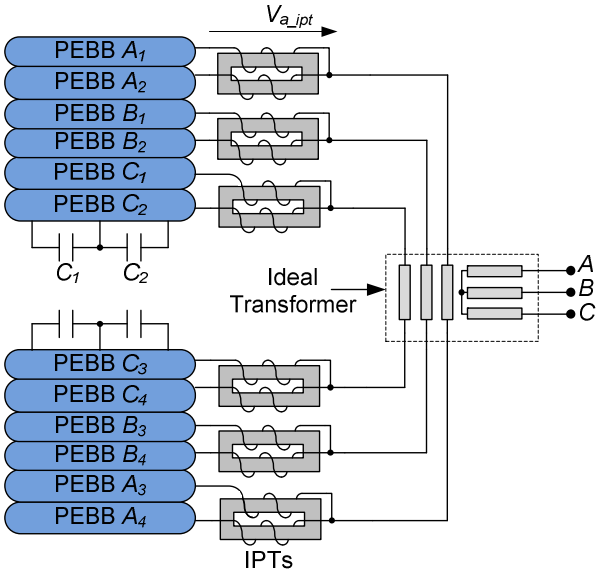

Figure 3. Converter topology with two isolated DC buses.

Topology II: Two isolated DC buses

Figure 3 shows the configuration scheme of the second VSC topology. It is similar to the Topology I, but the DC bus is divided in two parts, forming two isolated DC buses. Therefore, the use of ZSBTs is not necessary in this topology because zero sequence currents can not flow through the open winding transformer. However, two isolated DC buses are necessary.

Topology III: The Single-Star Bridge Cells (SSBC).

The third VSC topology is shown in Figure 4. It consists of 12 NPC PEBBs that are connected in a Single-Star Bridge Cells (SSBC) configuration [17]. Therefore, 6 isolated DC buses are needed, one for each H-bridge cell. Two series connected H-bridges are used per phase and hence, the current sharing through the PEBBs in each inverter leg is assured and the IPTs are not required. At the converter output terminals an ideal three-phase transformer is connected in wye configuration. Therefore, zero sequence currents cannot flow and the use of the ZSBT is not necessary.

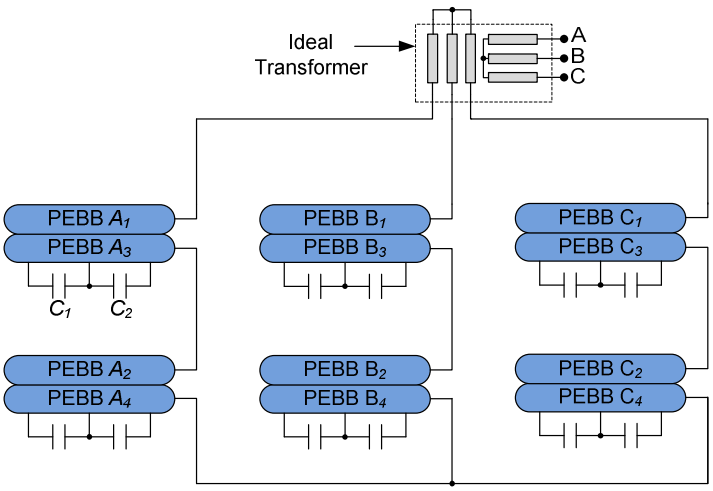

Figure 4. The Single-Star Bridge Cells (SSBC).

Topology IV: The Double-Star Chopper Cells (DSCC)

Figure 5 shows the VSC scheme of the fourth topology. It consists of twelve NPC PEBBs that are connected in Double-Star Chopper Cells (DSCC) configuration [17]. Therefore, twelve isolated DC buses are necessary, one for each chopper cell. In this topology six decoupled inductors are used to connect the upper side legs to the lower side legs and control the circulating currents between individual converter legs. The value of each inductor is defined as a percentage of the nominal power rating of the VSC (Y%mH). The current through the upper and lower side legs must be controlled independently.

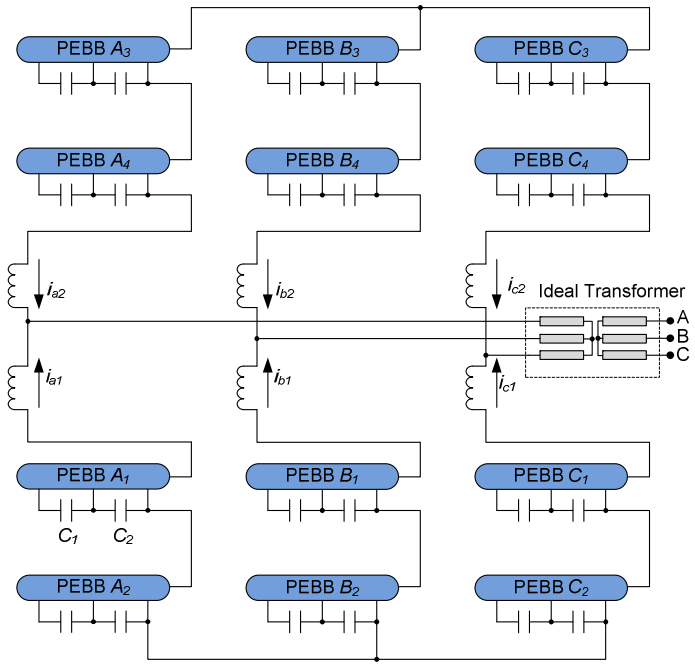

Figure 5. The Double-Star Chopper Cells (DSCC) topology.

VSC Comparison Criteria

In order to compare different converter topologies, firstly, the comparison criteria must be defined. In [19] a thorough comparison procedure for medium voltage-high power topologies is presented. This procedure is able to take into account all the range of switching and output frequencies, power factors and modulation indexes that the converter can work with. In this paper a basic comparison between converter topologies is carried out, assuming that the output current leads the converter voltage by 90 degrees, the converter is working at its maximum modulation index and the switching frequency is constant (600Hz). Four points are considered: the output voltage, the VA rating of the magnetic elements, the capacitance requirements and the efficiency.

Output Voltage

For an equal power rating, the output current decreases when the output voltage increases. So, the higher the output voltage level, the better. On the other hand, the harmonic content of the output voltage must be taken into account. The STATCOM must comply with the harmonic content legislation at the PCC [20]. Hence, the THD of the converter output voltage needs to be considered.

VA rating of the magnetic elements

As stated previously, the magnetic elements can be used to inter-connect the PEBBs. However, they usually are bulky and expensive devices. Therefore, they are an important part of the power electronics converters. The VA rating of a magnetic element is closely related to its weight, volume and cost. The VA ratings of the magnetic elements that are used in the converter are calculated as follows:

$$VA = \frac{1}{2} \cdot \sum_{k=1}^{\text{Total Number of Windings}} \frac{\hat{\Psi}_k \cdot \omega}{\sqrt{2}} \cdot I_{RMS_k} \tag{1}$$

where I_{RMS} is the RMS current flowing through the winding, Ψ is the peak value of the flux linkage and ω the angular frequency. The voltage drop across the winding of the magnetic element is measured in the simulation. Finally, the result is given as a percentage of the nominal power rating of the converter. In this point, it is not considered the series inductance that is necessary to connect the VSC to the PCC.

DC side capacitor sizing

The impact of the DC-link capacitor bank is high in terms of the cost and volume of the converter [21]. In the simulation of the converters, constant ideal voltage sources have been used to represent the PEBB DC-capacitors and the average power through each source was monitored to ensure it equated to zero. The current i_{DC} delivered by the ideal voltage sources is measured. Then, the necessary capacitance, to keep the voltage ripple between a 5% of the DC value V_{DC} is calculated as:

$$C = 100 \cdot \frac{2 \cdot \left(\int i_{DC} \cdot dt \right)_{MAX}}{V_{DC} / 2 \cdot ripple(\%)} \tag{2}$$

As the PEBBs are NPC circuits, the DC-side bus consists of two equal series connected capacitors, one in the upper side and the other at the lower side. In order to obtain the peak value of the time integral the current through the upper and lower side capacitors is measured. Then, the time integral of each current is obtained and their average is calculated.

Efficiency

In order to obtain the efficiency of the converter, the power losses P_{losses} must be calculated. The power losses are arisen from the switching devices and also from the magnetic elements. The conduction and switching losses have been considered in the switching devices. In the magnetic elements, both the core and cupper losses are considered. The efficiency of the converter η is obtained as:

$$\eta(\%) = 100 \cdot \left(1 - \frac{P_{losses}}{S_{out} + P_{losses}} \right) \tag{3}$$

where S_{out} is the apparent power of the converter.

Simulation Conditions

The four converter topologies have been simulated in Saber assuming that the converter is delivering 40 MVA. In order to obtain the harmonic content of the output voltage, the VA rating of the magnetic elements and the efficiency, the converters have been simulated under balanced conditions. However, the worst case has been found in order to determine the capacitance requirements of the VSC topologies. Under balanced conditions the oscillation of the instantaneous power in a three-phase system is zero. Hence, in a three-phase VSC with a common capacitance, the current oscillation of the DC side is only generated by the harmonics of the switching frequency. When working under unbalanced conditions, the oscillation of the instantaneous power is not zero, and the DC-side capacitance requirements increase significantly. The highest capacitance requirements are given for the highest instantaneous power oscillations. The amplitude of the oscillation of the instantaneous power in a three-phase system is derived in terms of the positive and negative sequences [22]:

$$\begin{aligned} Pc2 &= 1.5 \cdot \left(v_d^+ \cdot i_d^- + v_q^+ \cdot i_q^- + v_d^- \cdot i_d^+ + v_q^- \cdot i_q^+ \right) \\ Ps2 &= 1.5 \cdot \left(v_q^- \cdot i_d^+ - v_d^- \cdot i_q^+ - v_q^+ \cdot i_d^- + v_d^+ \cdot i_q^n \right) \end{aligned} \tag{4}$$

where v_d^+ and v_q^+ define the positive sequence voltage at the VSC output terminals; v_d^- and v_q^- define the negative sequence voltage at the VSC output terminals; i_d^+ and i_q^+ define the positive sequence current

delivered by the VSC; and, i_d^- and i_q^- define the negative sequence current delivered by the VSC. From (4) can be deduced that the highest power oscillations are produced when the converter is generating a positive sequence voltage and the output current is only a negative sequence current. Under this condition the needed capacitance is the highest in a three-phase VSC. This worst-case scenario is shown in Figure 6. The PCC has been simplified as one positive sequence voltage source (V_{th}^+), one negative sequence voltage source (V_{th}^-) and an equivalent impedance (Z_{th}). In this case, the objective of the STATCOM is to control only the negative sequence voltage at the PCC. Therefore, the VSC generates an equal positive sequence voltage as the generated one at the network (V_{th}^+), and only delivers negative sequence current (i^-).

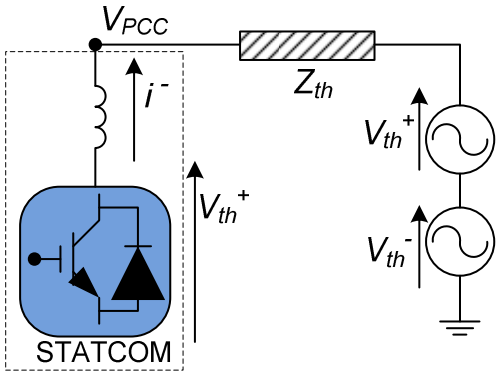

Figure 6. STATCOM application under unbalanced condition.

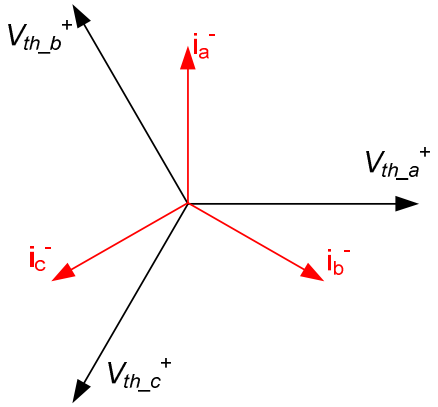

Figure 7. VSC output voltages and currents.

From the point of view of the VSC, the phase currents and voltages at its output terminals are defined as in Figure 7. As the voltages are positive sequence components and the currents are negative sequence components, the phase voltage $V_{th\_b}^+$ leads $V_{th\_a}^+$, whilst the phase current i_b^- lags i_a^-.

It can be observed that the current i_a^- leads the voltage $V_{th\_a}^+$ by 90 degrees, so, it exchange only reactive power. However; in the other two phases an active power is generated. The active power generated in the phases *b* and *c* have the same amplitude but they have the opposite sign. Hence, the overall active power of the three-phase system remains at zero. Under the defined conditions, in the topology III and IV, the capacitors of the phase *b* are charged whereas the capacitors of the phase *c* are discharged. Subsequently, this topology III is not workable under these conditions. However in the topology IV a circulating DC current is generated between the phase *b* and *c*, maintaining all the capacitors charge balanced [12].

Discussion And Evaluation Of The Compared Topologies

Output voltage

In Figure 8 the output voltage waveforms of the four topologies are shown. The output waveform is the same in the topologies I, II and IV, whereas topology III has twice the amplitude. It is considered that the output voltage of the topology IV is the average value between the upper and lower side converters.

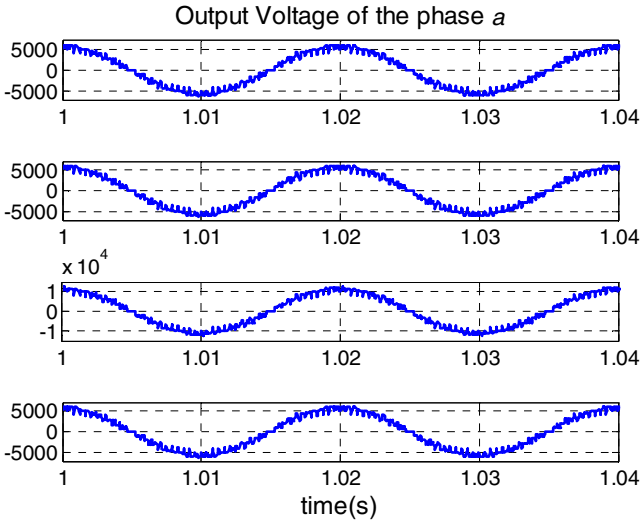

Figure 8. The output voltage waveform of the compared topologies. From up to down: Topology I, Topology II, Topology III and Topology IV.

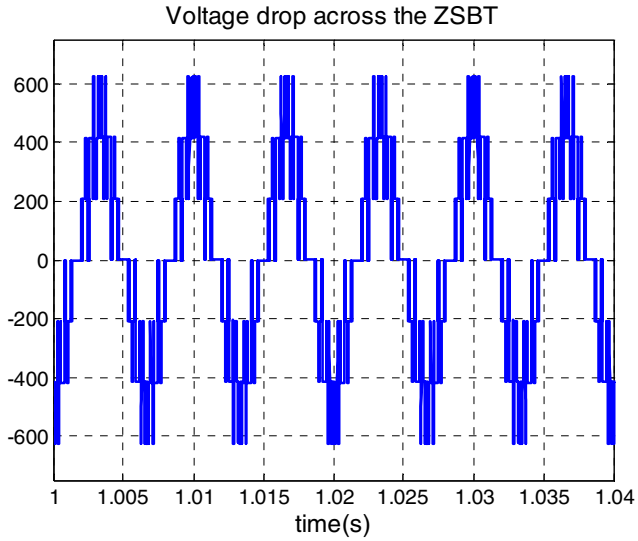

Figure 9. The voltage drop of the phase a across the ZSBT.

The amplitude of the fundamental component of the output voltage of each converter is measured by carrying out the Fast Fourier Transform (FFT) of each waveform. The amplitude of the fundamental component has been normalized respect to the DC side voltage (5KV). So, the obtained fundamental values are 1.13 p.u., 1.13 p.u., 2.26 p.u. and 1.13 p.u. for topologies I, II, III and IV, respectively. The THD of the output voltage is the same in all the topologies: 12.3%. The voltage harmonics of the VSC output are propagated through the PCC. This propagation depends on the network impedances [20].

Magnetic elements

In this Subsection the magnetic elements that are used in the topologies I and II are considered. Their VA rating is obtained and they are normalized with respect to the nominal power rating of the converter. The inductances that are necessary to connect the VSC to the PCC are not considered. Apart from the IPTs, two ZSBTs are used in the topology I. The voltage drop across the ZSBT is shown in Figure 9. It can be observed that it is composed by voltage harmonics of zero sequence. The flux linkage is obtained and according to (1), the VA rating of the ZSBTs is calculated. Considering that there are 6 IPTs and 2 ZSBTs in the topology I and there are 6 IPTs in the topology II, the total rating of the magnetic elements is obtained. Being the nominal power rate 40MVA, the VA rating of the magnetic elements are 5.2% and 2.5% for topologies I and II, respectively. Apart from the magnetic elements that are necessary to inter-connect the PEBBs, a series inductance is needed to connect the VSC to the PCC. The value of this series inductance is given as a percentage of the nominal power rating of the VSC (X%mH). In the topology III the magnetic elements are not necessary to inter-connect the PEBBs. The VSC can be connected to the PCC through the inductances (X%mH) or by using a transformer (being the leakage inductance of the transformer X%mH). In the topology IV the upper and lower side converters are connected in parallel. Hence, a minimum inductance must be imposed between them which is defined as 2Y%mH (the inductance value is given as a percentage of the nominal power rating of the VSC). This inductance can replace the series inductance needed to connect the VSC to the PCC. From the point of view of the VSC output, the equivalent series inductance is Y/2%mH. In addition, it should be noted that these inductances must support a DC current under unbalanced conditions.

Capacitor sizing

The necessary minimum capacitance for each topology to keep the DC voltage ripple under 5% is calculated according to (2) under unbalanced conditions. In Figure 10 the currents through the DC side capacitors C1 and C2 are shown for each topology.

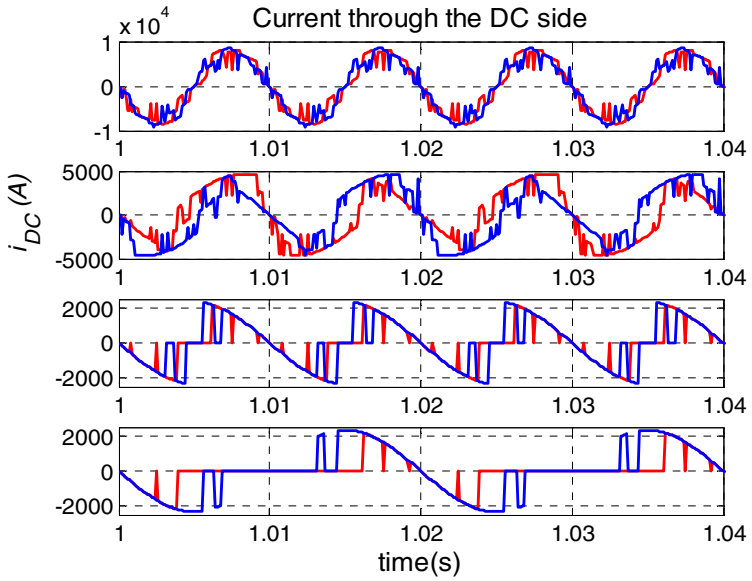

Figure 10. Currents through the DC side capacitors. From the top waveform to the bottom waveform: Topology I, Topology II, Topology III and Topology IV.

The time integral of the currents shown in Figure 10 has been obtained and the total capacitance for each topology has been calculated according to (2). So, the total capacitance for each half DC bus is 200mF, 144mF x2=288mF, 39mF x6=234mF and 57.6mF x12=691.2mF, for topologies I, II, III and IV, respectively.

Efficiency

In order to obtain the efficiency of each converter topology, the power losses in the semiconductors as well as in the magnetic elements are calculated. In the topology I, the losses at the semiconductors are 200kW, in the IPTs 100kW and in the ZSBTs 60.4kW. So, according to (3) the efficiency of this topology is therefore 99.1%. Similarly in the topology II, the losses at the semiconductors are 200kW, in the IPTs 100kW and the efficiency is 99.2%. In the topology III, the losses at the semiconductors are 193kW, and the efficiency is 99.5%. In the topology IV, the losses at the semiconductors are 177kW and in the inductors 50kW. The efficiency of this topology is 99.3%. Although the power losses in the semiconductors are low, under unbalance conditions one of the switches of the PEBBs (the IGBT 2) exceeds its thermal limit due to the DC current that flows from the leg b to c. Hence, the power delivered by this topology under unbalanced topologies is limited by the thermal limit of the semiconductors.

Comparison summarize

The most important characteristics of each converter topology are summarized in TABLE I. All the characteristics have been obtained under balanced conditions. However, the stored energy in the capacitors has been obtained under balanced and unbalanced conditions.

TABLE I

COMPARISON OF THE TOPOLOGIES

	Top I	**Top II**	**Top III**	**Top IV**
V_{out} level	1.13	1.13	2.26	1.13
V_{out} THD	12.3%	12.3%	12.3%	12.3%
VA magnetic	5.2%	2.5%	0%	Special (2Y% mH)
Series inductance	X% mH	X% mH	X% mH	(X-Y/2)% mH
Output transformer	Open winding	Open winding	None or Standard[1]	None or Standard[1]
Cap. energy balanced	62.5KJ	410KJ	1.46MJ	4.32MJ
Cap. energy unbalanced	1.25MJ	1.8MJ	-	4.32MJ
Efficiency	99.1%	99.2%	99.5%	99.3%
Support unbalances	Yes	Yes	No	Yes

[1]Only needed if voltage step up to grid required.

Regarding to the amplitude of the fundamental component of the output voltage, the topologies I, II and IV have the same voltage level. The voltage level of the topology III is two times higher than in the other topologies which is an advantage, for instance because the output currents are reduced. The harmonic content of the output voltage is the same in all the topologies, having the same THD. The topology I uses 6 IPTs and 2 ZSBTs and the VA ratings of the magnetic elements represent the 5.2%. In the topology II, this value decreases to 2.5% because only IPTs are used. In the topology III magnetic elements are not necessary to inter-connect the PEBBs. In the topology IV special inductances are used because they must support a DC current under unbalanced conditions. The detailed analysis of their VA rating goes beyond the scope of this paper. The inductance that they have to impose for differential sequence mode has been defined as a percentage (2Y% mH). In order to connect the VSC to the PCC, series inductances are necessary which their value has been defined as X% mH (in the first two topologies can be referred to the leakage inductance of the output transformer). In the topology IV the necessary series inductance is (X-Y/2)% mH. The stored energy in the DC side capacitors under balanced and under unbalanced conditions is also shown in Table I and gives an indication of the capacitor requirements for each converter, which can be a significant factor in terms of converter size and cost. Topology IV has many advantages in terms of efficiency, unbalanced capability and it does not require a line-transformer for low voltage grids. However, the electrical capacitance requirement is high for both balanced and unbalanced operation. On the other hand Topology I and II have a lower electrical capacitance but with slightly lower efficiencies. However they do suffer from the need for a line-transformer with a special winding arrangement to connect to the grid for all grid voltage levels. The main drawback of Topology III is that it is not able to work under unbalanced conditions. However for balanced operation it does not require a line-transformer and has good efficiency. In addition it has a higher capacitance requirement than topology I and II.

Conclusion

In this paper four Voltage Source Converter topologies are compared for STATCOM applications. Two of the topologies are Modular Multilevel Cascaded Converters (MMCC) and the other two are based on the use of magnetic elements with open-end winding configuration. Depending on the application, the STATCOM must work under balanced or unbalanced conditions. Subsequently, the four topologies have been simulated in the simulation tool Saber under balanced and unbalanced conditions. In order to simulate the VSC under unbalanced condition one particular case has been considered. This particular case is given when the converter output voltage is a positive sequence voltage and all the delivered current is a negative sequence current. Under this condition, the oscillation of the instantaneous power is the highest in a three phase system, increasing the required capacitance in the three-phase converters with common capacitor in the DC side. In addition, the phase *b* must absorb active power whereas the phase *c* must provide the same amount of active power. Hence, the topology III (SSBC) is not a suitable topology. In the topology IV (DSCC) a dc current is generated between the phases *b* and *c*, sharing the active power and keeping charged all the capacitors. In the other two topologies this effect is not shown because of the common DC side capacitor. Although the required total capacitance of the topology I is relatively low under balanced conditions, it is observed that the capacitance requirements increases significantly under unbalanced conditions. Finally, the capacitance requirements are high in the topology IV but it can work under any unbalanced conditions.

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