40 Gbit/s asynchronous digital optical regenerator

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Abstract: We present the first experimental demonstration of an asynchronous digital optical regenerator at 42.67 Gbit/s. The system effectively retimes incoming asynchronous data bursts to a local clock without burst mode clock recovery and converts the signal to a desired wavelength and duty cycle.

OCIS codes: (060.2330) Fiber optics communications; (060.4510) Optical communications

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1. Introduction

Transparent optical networks are known to offer many significant advantages over their opto-electronic counterparts [1]. In optical high speed communication systems the differing techo-economic requirements of various sectors of the network often result in divergent solutions, ranging from low cost passive optical access networks for low bit rate traffic [2] to ultra high capacity high performance core networks [3]. For efficient operation it is necessary to aggregate traffic from different origins onto a single wavelength high-bit rate signal. Such aggregation currently requires opto-electronic conversion and the use of buffer stores and/or timing pointers to merge bit streams of continuously varying relative phase. Ultimately, this restricts transparent networks to islands. In order to overcome this limitation a novel router has recently been proposed, where transparency is extended to networks operating at different speeds in different layers, such as metro/access networks and core network rings [4]. For

#93767 - $15.00 USD Received 12 Mar 2008; revised 12 Aug 2008; accepted 22 Aug 2008; published 3 Nov 2008

instance, the novel router of [4] allows aggregation of signals at bit rates up to 43 Gbit/s from different sources on multiple collector rings to be retimed and multiplexed into a single OTU4 based optically time division multiplexed (OTDM) signal for transmission over a high capacity core network.

While OTDM multiplexing of several lower bit-rate channels at first looks like a straight forward process, it effectively requires shortening the pulse-widths of the tributaries and introducing precise relative timing delays between the signals so that pulses from neighbouring channels do not overlap after optical multiplexing. Incoming low speed data signals from multiple sources usually have different clock frequencies and environmentally induced changes in propagation delay [5]. One potential solution to this problem is the so called Asynchronous Digital Optical REgenerator (ADORE) [6,7,9]. In the ADORE, an incoming data burst is simultaneously sampled at multiple clock phases [8], subsequently, the optimum clock phase is selected for onward processing. In this way, complex optical time division processing nodes and networks may be envisioned, using ideally at least four or more sampling pulses with different relative phases, for sampling circuits with rectangular switching windows [9]. Simplification may be achieved by interferometrically combining neighbouring clock phases which are encoded with the same bit of the input signal [6]. In this paper we present the first experimental implementation of this scheme at 42.67 Gbit/s using a single optical gate using the neighbour combination approach of [6]. Error free operation has been achieved for all possible data phases.

2. Principle of operation

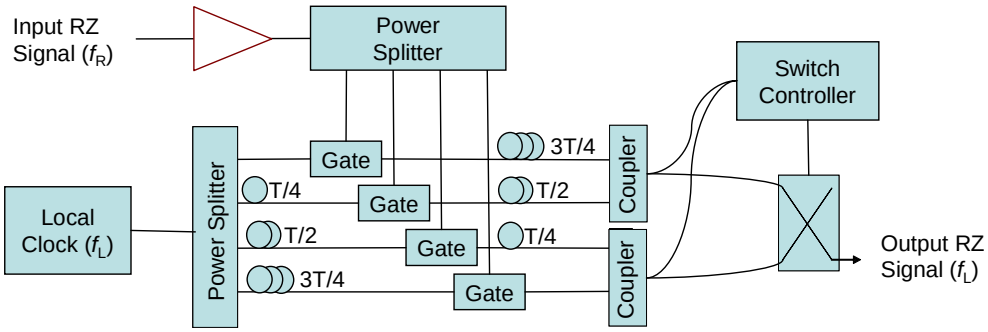

Fig. 1. Functional diagram of the ADORE using channel combination to reshape the effective gating window.

Figure 1 shows a functional diagram of an ADORE, using four optical gates to provide the four sampling clock phases, adjacent pairs of which are interferometrically combined. For optimal performance, each interferometer is set for constructive interference, ensuring that the amplitude of the signal is within 3dB of its ideal value irrespective of whether the signal is correctly modulated by one or two of the adjacent gates. A local optical clock (frequency = f_L) probes each of the four gates after successive delays of one-quarter of the nominal bit period $T = 1/ f_L$. Each bit of an input RZ signal at a frequency f_R simultaneously modulates all four gates with a switching window of at least 25 % of the bit period, such that the switching window of a minimum of one gate overlaps with one of the copies of the local clock pulse, irrespectively of the phase difference between the signal and the clock. As discussed qualitatively elsewhere [7,9] the ADORE may operate with free running clock sources within permitted limits [5]. In this case the relative phase difference would vary by an insignificant amount for bursts of up to 4,000 bytes. By selecting the optimum sampling clock phase from the output of one of the four gates, asynchronous regeneration can be achieved. If the phase delays before and after the optical gates are reversed, all possible clock phase paths are of identical total length, so that the output signal will be at a known phase, irrespective of the

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incoming phase difference between clock and data. In the basic ADORE scheme without interferometric combination [9], reduction of the number of sampling gates to two would either result in an increased sensitivity to timing jitter at the edge of the gating window (gating window with fast rise and fall times) or a performance degradation due to the incorrect simultaneous switching of probe pulses corresponding to adjacent bit slots (gating window with slow rise and fall times). These restrictions resulted in previous demonstrations employing four effective gating windows and an effective sampling gate bandwidth of 20 GHz for 10 Gbit/s operation [7].

In the neighbor combination scheme, as in Fig. 1, two adjacent sampling phases of the local clock pulses (which, in general, have different amplitudes) are combined interferometrically at the output of a 2×1 coupler offering a significant simplification of the ADORE configuration. By combining neighbouring samples into one channel interferometrically this setup effectively combines beneficial aspects of both a dual gate and a quad gate regenerator. The limiting feature of jitter to amplitude noise conversion is dominated by the correctly phased gate, where the pulses are well separated from the window edges, as in the conventional ADORE [9]. On the other hand, the use of the interferometer in the neighbour-combined ADORE [6] allows for the generation of a broader switching window without any associated increase in the rise and fall times minimising incorrect switching events. However, the potential for bit errors arising from simultaneous switching of pulses from an adjacent time slot is determined by the switching window of the combined pulses, and it is therefore expected that the performance of the neighbour-combined ADORE will be dominated by such incorrect switching events.

To complete the ADORE circuit, it is necessary to select the optimum clock phase. This may be performed either by comparing the total output powers of each of the signal paths [6, 7], or by using a simple single RF phase measurement, as in this paper, together with an appropriate pipeline delay.

3. Implementation and experiment

The experimental setup of the ADORE is shown in Fig. 2. The four probe pulses to be gated are generated as follows. An electro-absorption modulator (EAM1) was driven by a locally generated 42.67 GHz clock signal with peak to peak amplitude of 5 V in order to generate 5.2 ps probe pulses at the wavelength of a local CW laser source at 1553 nm. These local optical pulses were then launched at 45° into a polarization maintaining fibre (PMF) exciting two orthogonal linearly polarised pulses delayed by 11.7ps (i.e. one half of the bit period) at the fibre output. An incorrect launch angle would simply result in a path dependent insertion loss, readily compensated prior to the optical switch. Each orthogonal pulse was then split at the 3 dB coupler and counter-propagated around the standard single mode fibre (SSMF) loop. Thus a total of four pulses propagated around the loop, consisting of two orthogonally-polarized pulses in each direction. A second EAM (EAM2) was spliced in the loop with 6.25ps offset from the centre. Errors in these delays would increase the required phase margin for the optical gate. Polarisation controllers were also included to birefringently bias the loop mirror for transmission mode. EAM2 was pigtailed with anti-reflection coated fibres to minimise multi-path effects within the loop mirror.

A 42.6 Gbit/s 33% RZ 2^7-1 PRBS data signal at 1554.9nm was generated with an external cavity laser and two Mach-Zehnder modulators. To mimic timing wander it was passed through a variable optical delay line. It was then amplified to a total power of +3.2 dBm before entering the ADORE circuit of Fig. 2. Within the ADORE, the data signal was detected using a 50 GHz photodiode, and then amplified using a 42 GHz amplifier with 30dB small signal gain to a maximum swing of 5V peak to peak. This signal was then fed into EAM2 in order to switch the EAM (operated with an offset of -1.4V) into the transmit state for every incoming data pulse. The limited bandwidth of the opto-electronic gate results in a switching window wider than a quarter of a bit period. Within a bit period, the previously generated four

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probe pulses pass through EAM2 with incremental delays of one quarter of a bit period – thus emulating a four gate ADORE using a single modulator – with at least one of the pulses efficiently gated by the incoming data bit. Note that in contrast to a parallel multi-gate approach (Fig. 1), this configuration strictly limits the number of distinct paths to four, imposing a minimum phase margin for the optical gate of $\pi/2$ [7].

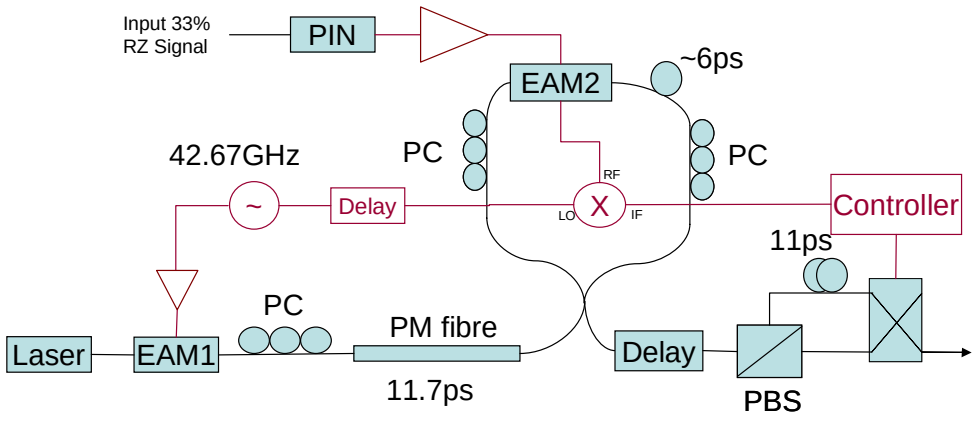

Fig. 2. Experimental setup of the ADORE using a single EAM within a loop. The birefringence in the loop is adjusted to achieve maximum transmission (constructive interference)

On exiting the loop, each pair of co-polarised pulse streams was recombined interferometrically, with the polarisation controllers adjusted to ensure constructive interference at the transmission port of the SSMF linear loop mirror. The two modulated probes generated in this way are delayed by half a bit period with respect to each other and orthogonally polarised. Depending on the relative phase delay of input and probe pulses, one of the probe pulse streams is the interferometric combination of, first, the probe pulse stream optimally switched by the incoming data and, second, its neighbour, which was switched by the same data bits. The other signal comprised the probe pulse stream incorrectly timed for efficient switching by the data signal, and its neighbour. The two orthogonally polarized signals were then separated at the polarization beam splitter and the optimum channel was selected automatically by the control circuit using the 2×1 optical switch, whilst the half bit period delay was removed by appropriately adjusting the delays between the beam splitter and the switch. The beam splitter extinction ratio was selected to minimise homodyne interference in this portion of the circuit.

In this demonstration, an RF phase detector was used to detect the optimum channel, also shown in Fig. 2. This phase detector comprised a double balanced mixer with its local oscillator port connected to the local clock, and its RF port connected to the incoming data signal after it has been detected, amplified and traversed EAM2, thus avoiding the need for an RF power splitter prior to this EAM. The mixer effectively detected the phase difference between the carrier components of the RZ data signal and the local clock, giving a voltage at the IF port of the mixer proportional to the cosine of the phase delay of the incoming signal relative to the local clock. By carefully arranging the relative delay of the probe pulses with respect to this local phase reference, it was possible to ensure that the polarity of the IF output indicated the optimum optical output channel. Optimum channel detection was completed using a control circuit including a Schmitt trigger, to induce a controlled level of hysteresis, which was necessary to avoid repeated switching events at relative phase differences of 0 and π where the mixer output would be close to zero. Finally this control signal was applied to the 2×1 switch to select the optimum channel automatically. This channel selection scheme was

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found to offer greater robustness to environmental fluctuations than the output power comparison method proposed previously [6, 9].

4. Results

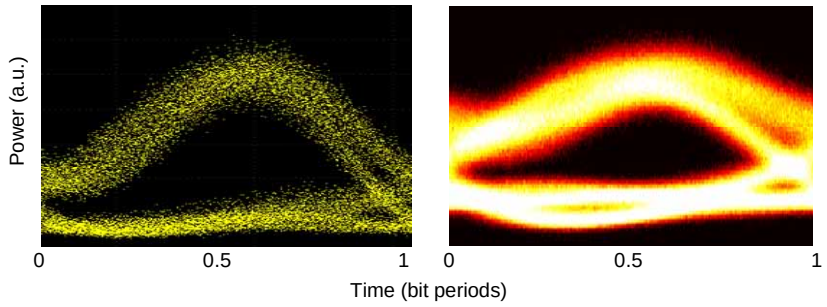

Fig. 3. Observed single polarisation switching windows for single pass through the EAM (left) and the output of the ADORE loop (right).

By omitting both EAM1 and the PMF in Fig. 2, it is possible to directly observe the switching windows generated by EAM2 alone and by EAM2 within the loop. Figure 3 shows the corresponding eye diagrams of the modulated cw probe, obtained using an optical oscilloscope with 1.5ps resolution. These results show that the addition of the loop mirror circuit broadens the peak of the switching window, as expected. In addition, the frequency response of the particular combination of electrical amplifier and EAM2 used in this demonstration results in a significant increase in the pattern dependant jitter of the rising edge of the switching window. Given that the performance is determined by restricted conversion bandwidth, similar performance will be observed for signals with shorter pulse widths.

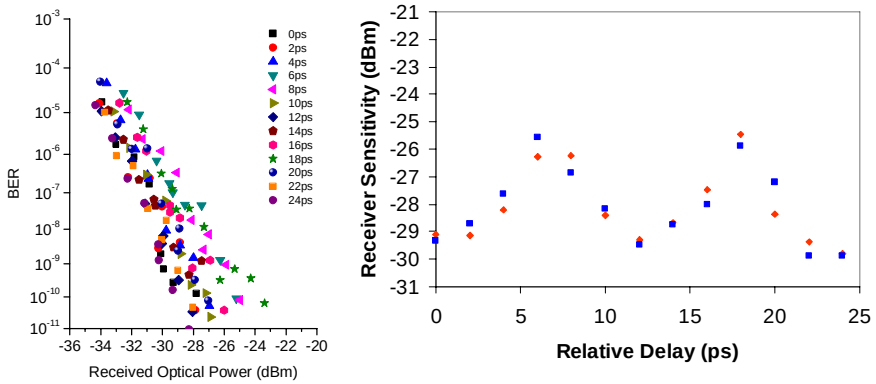

Fig. 4. Bit Error Rate Performance of ADORE with automatic channel selection for a variety of different input phase delays (left) and variation in receiver sensitivity as a function of phase delay showing two independent measurements (red and blue, right).

With the local clock frequency synchronised to the incoming data the BER performance of the full ADORE circuit was measured as a function of the delay between the local clock and the incoming data signal, with the automatic channel selection enabled. Error rate characteristics and receiver sensitivity are plotted in Fig. 4. It can be seen that the ADORE operated error free over the whole range of phase difference between incoming data signal and local clock, and that both channels offered similar performance at the optimum phase. The cyclic degradation corresponds to the clock pulse being switched at the edge of the switching window, maximising the degradation associated with the pattern dependant jitter,

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whilst the asymmetry between the two optima results from the slight misalignment of the path length differences.

Typical input and output eye diagrams are shown in Fig. 5, illustrating that the eye remained open and at a fixed output phase, even for the worst input phase delay. The apparent amplitude noise on the '1' symbols is consistent with the decrease in the receiver sensitivity and is believed to be dominated by the pattern dependent jitter induced by the drive amplifier-EAM2 combination, in addition to the expected degradation due to operation at the edge of the switching window [9]. This resulted in a maximum variation in receiver sensitivity of 4.5 dB. We do not anticipate that this variation would add linearly to penalties associated with degraded input signals because the non-linear amplitude response of EAM2 regenerates the signal to a certain extent. However, performance would clearly be improved by optimizing the frequency response of the gate or by including an additional optical regenerator at the output of the gate.

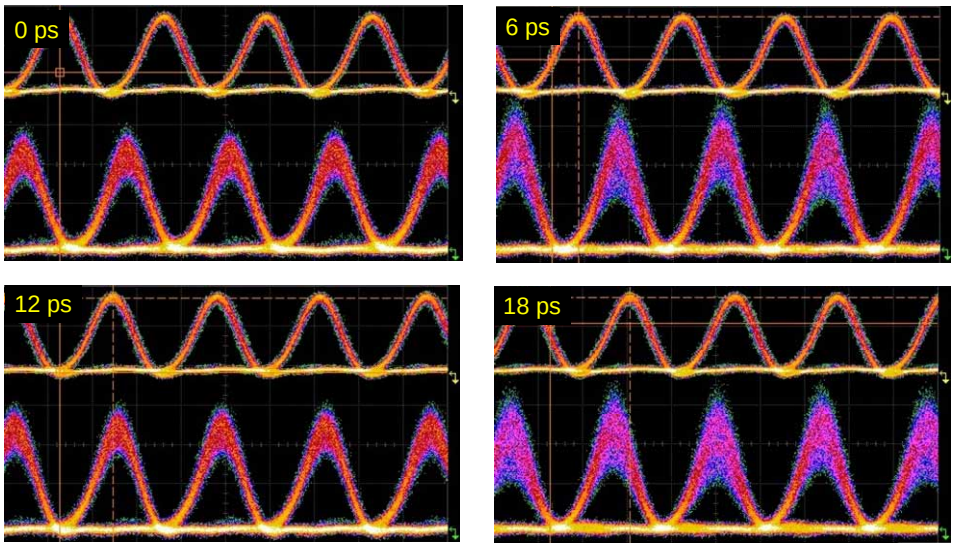

Fig. 5. Eye diagrams for the ADORE input (top) and output signals (bottom) at best and worst relative phases for each polarisation.

The minor change in the optimum performance with respect to the back to back measurements (typical receiver sensitivity of -30.5dBm) is attributed to the change in duty cycle and extinction ratio of the local clock pulses.

5. Conclusion

In this paper, we have successfully demonstrated for the first time an asynchronous digital optical regenerator operating at a bit rate of 42.67 Gbit/s. The overall receiver sensitivity variation was constrained to 4.5dB at the worst case phase with automatic selection of the optimum channel. These results experimentally confirm for the first time that the approach of neighbour combination allows the simplification of an ADORE to a single bi-directional optical gate and a 2×1 switch. We have demonstrated that the ADORE offers error free retiming of an incoming optical signal without high speed clock recovery, particularly suited to retiming burst or packet-switched data signals.

Acknowledgments

This work has been supported by the European Commission under TRIUMPH project IST-027638 STP, and by Science Foundation Ireland under grant 06/IN/I969.

#93767 - $15.00 USD Received 12 Mar 2008; revised 12 Aug 2008; accepted 22 Aug 2008; published 3 Nov 2008